General Description

The SN74HC4053 is a triple single-pole double-throw analog switch (3×SPDT) suitable for use in analog or digital 2:1 multiplexer/demultiplexer applications. Each switch features a digital select input (Sn), two independent inputs/outputs (nY0 and nY1) and a common input/output (nZ). A digital enable input (E) is common to all switches. When E is HIGH, the switches are turned off. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

Features

- Wide analog input voltage range from -5 V to +5 V
- Wide supply voltage range
  SN74HC4053: from 3V to 9V
- Low ON resistance:
  – 80 Ω (typical) at VCC - VEE = 4.5 V
  – 70 Ω (typical) at VCC - VEE = 6.0 V
  – 60 Ω (typical) at VCC - VEE = 9.0 V
- Logic level translation: to enable 5 V logic to communicate with ±5 V analog signals
- Typical “break before make” built-in
- Specified from -40℃ to +85℃
- Packaging information: DIP16/SOP16/TSSOP16

Applications:

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
XBLW SN74HC4053N	DIP-16	74HC4053N	Tube	1000Pcs/Box
XBLW SN74HC4053DTR	SOP-16	74HC4053	Tape	2500Pcs/Reel
XBLW SN74HC4053TDTR	TSSOP-16	74HC4053	Tape	5000Pcs/Reel

Block Diagram And Pin Description

Block Diagram

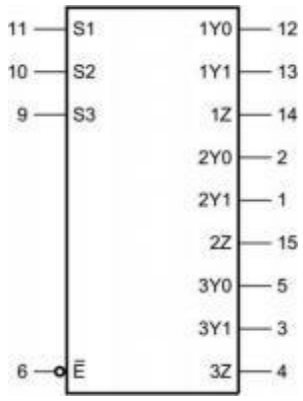


Figure 1.Logic symbol

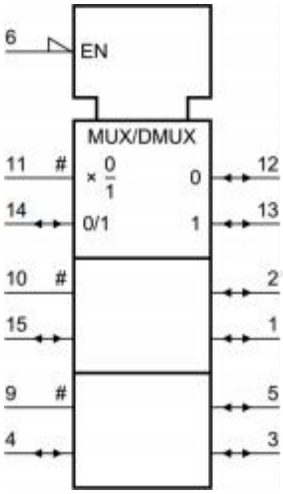


Figure 2. IEC logic symbol

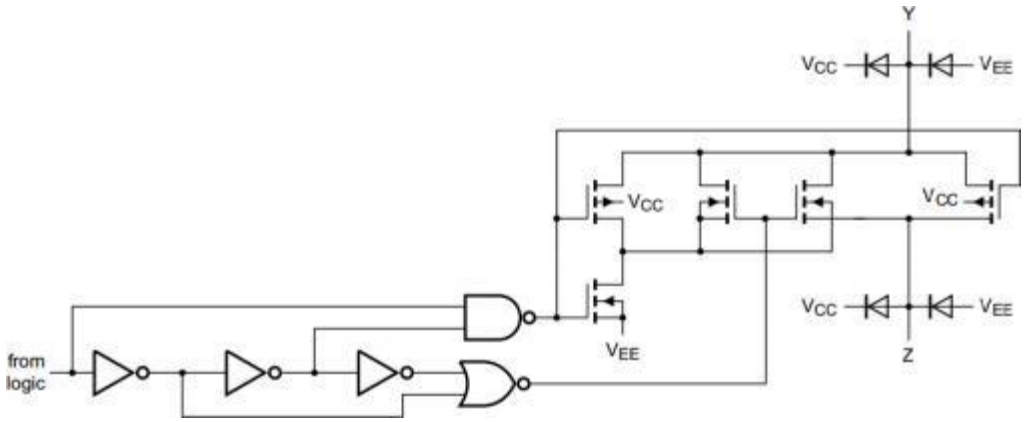


Figure 3. Schematic diagram (one switch)

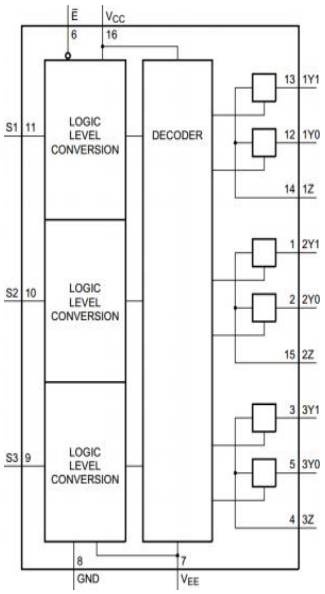
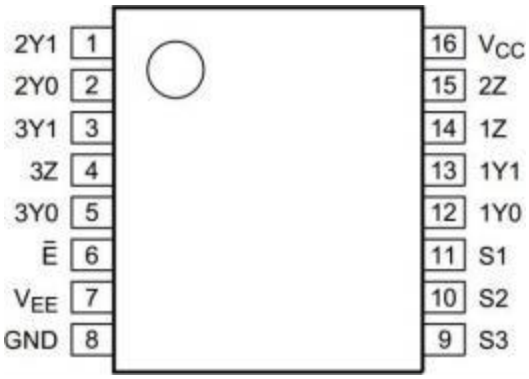


Figure 4. Functional diagram

Pin Configurations



Pin Description

Pin No.	Pin Name	Description
1	2Y1	independent input or output
2	2Y0	independent input or output
3	3Y1	independent input or output
4	3Z	common output or input
5	3Y0	independent input or output
6	$\bar{E}$	enable input (active LOW)
7	V_{EE}	supply voltage
8	GND	ground supply voltage
9	S3	select input
10	S2	select input
11	S1	select input
12	1Y0	independent input or output
13	1Y1	independent input or output
14	1Z	common output or input
15	2Z	common output or input
16	V_{CC}	supply voltage

2.4 、Function Table

Input		Channel ON
$\bar{E}$	Sn	
L	L	nY0 to nZ
L	H	nY1 to nZ
H	X	switches off

Note: H=HIGH voltage level; L=LOW voltage level; X=don’tcare

Electrical Parameter

Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{CC}	- [1]		-0.5	+11.0	V
input clamping current	I_{IK}	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V		-	±20	mA
switch clamping current	I_{SK}	$V_{SW} < -0.5$ V or $V_{SW} > V_{CC} + 0.5$ V		-	±20	mA
switch current	I_{SW}	-0.5 V $< V_{SW} < V_{CC} + 0.5$ V		-	±25	mA
supply current	I_{EE}	-		-	±20	mA
supply current	I_{CC}	-		-	50	mA
ground current	I_{GND}	-		-	-50	mA
storage temperature	T_{stg}	-		-65	+150	℃
total power dissipation	P_{tot}	- [2]		-	500	mW
power dissipation	P	per switch		-	100	mW
Soldering temperature	T_L	10s	DIP	245		℃
			SOP	250		℃

Note:

[1] To avoid drawing V_{CC} current out of terminal nZ, when switch current flows into terminals nYn, the voltage drop across the bidirectional switch must not exceed 0.4V. If the switch current flows into terminal nZ, no V_{CC} current will flow out of terminals nYn, and in this case there is no limit for the voltage drop across the switch, but the voltages at nYn and nZ may not exceed V_{CC} or V_{EE}.

[2] For DIP16 packages: above 70℃ the value of P_{tot} derates linearly with 12mW/K.

For SOP16 packages: above 70℃ the value of P_{tot} derates linearly with 8mW/K.

For TSSOP16 packages: above 60℃ the value of P_{tot} derates linearly with 5.5mW/K

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	V_{CC} - GND	3.0	5.0	9.0	V
		V_{CC} - V_{EE}	3.0	5.0	9.0	V
input voltage	V_I	-	0	-	V_{CC}	V
switch voltage	V_{SW}	-	V_{EE}	-	V_{CC}	V
ambient temperature	T_{amb}	in free air	-40	-	+85	℃
input transition rise and fall rate	Δt/ΔV	V_{CC} = 4.5 V	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	ns/V
		V_{CC} = 9.0 V	-	-	31	ns/V

Electrical Characteristics

DC Characteristics 1

(T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
ON resistance (peak)	$R_{ON(peak)}$	V_{is} = V_{CC} to V_{EE}; I_{SW} = 1000 uA	V_{CC} = 4.5 V; V_{EE} = 0 V	-	100	180	Ω
			V_{CC} = 6.0 V; V_{EE} = 0 V	-	90	160	Ω
			V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	70	130	Ω
ON resistance (rail)	$R_{ON(rail)}$	V_{is} = V_{EE}; I_{SW} = 1000 uA	V_{CC} = 4.5 V; V_{EE} = 0 V	-	80	140	Ω
			V_{CC} = 6.0 V; V_{EE} = 0 V	-	70	120	Ω
			V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	60	105	Ω
		V_{is} = V_{CC};	V_{CC} = 4.5 V; V_{EE} = 0 V	-	90	160	Ω
		I_{SW} = 1000 uA	V_{CC} = 6.0 V; V_{EE} = 0 V	-	80	140	Ω
			V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	65	120	Ω
ON resistance mismatch between channels	ΔRON	V_{is} = V_{CC} to V_{EE}	V_{CC} = 4.5 V; V_{EE} = 0 V	-	9	-	Ω
			V_{CC} = 6.0 V; V_{EE} = 0 V	-	8	-	Ω
			V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	6	-	Ω
HIGH-level input voltage	V_{IH}	V_{CC} = 4.5 V		3.15	2.4	-	V
		V_{CC} = 6.0 V		4.2	3.2	-	V
		V_{CC} = 9.0 V		6.3	4.7	-	V
LOW-level input voltage	V_{IL}	V_{CC} = 4.5 V		-	2.1	1.35	V
		V_{CC} = 6.0 V		-	2.8	1.8	V
		V_{CC} = 9.0 V		-	4.3	2.7	V
input leakage current	I_I	V_{EE} = 0 V; V_I = V_{CC} or GND	V_{CC} = 6.0 V	-	-	±0.1	uA
			V_{CC} = 9.0 V	-	-	±0.2	uA
OFF-state leakage current	$I_{S(OFF)}$	V_{CC}= 9.0 V; V_{EE}= 0 V; V_I= V_{IH} orV_{IL}; $\|V_{SW}\|$ = V_{CC} - V_{EE}; see Figure 7	per channel	-	-	±0.1	uA
			all channels	-	-	±0.1	uA
ON-state leakage current	$I_{S(ON)}$	V_I= V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{CC}-V_{EE};V_{CC}= 9.0 V; V_{EE}= 0 V; see Figure 8		-	-	±0.1	uA
supply current	I_{CC}	V_{EE} = 0 V; V_I = V_{CC} or GND; V_{is} = V_{EE} or V_{CC}; V_{os} = V_{CC} or V_{EE}	V_{CC} = 6.0 V	-	-	8.0	uA
			V_{CC} = 9.0 V	-	-	16.0	uA
input capacitance	C_I	-		-	3.5	-	pF

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
switch capacitance	C_{SW}	independent pins nYn	-	5	-	pF
		common pins nZ	-	8	-	pF

Note:

[1] $V_I = V_{IH}$ or V_{IL}; for test circuit see Figure 5.

[2] V_{is} is the input voltage at anYnor nZ terminal, whichever is assigned as an input.

[3] V_{os} is the output voltage at a nYnor nZ terminal, whichever is assigned as an output.

DC Characteristics 2

(T_{amb} = -40℃~85℃, voltages are reference to GND (ground=0V), unless otherwise specified, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
ON resistance (peak)	$R_{ON(peak)}$	V_{is} = V_{CC} to V_{EE}; I_{SW} = 1000 uA	V_{CC} = 4.5 V; V_{EE} = 0 V	-	-	225	Ω
			V_{CC} = 6.0 V; V_{EE} = 0 V	-	-	200	Ω
			V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	-	165	Ω
		V_{is} = V_{EE}; I_{SW} = 1000 uA	V_{CC} = 4.5 V; V_{EE} = 0 V	-	-	175	Ω
			V_{CC} = 6.0 V; V_{EE} = 0 V	-	-	150	Ω
ON resistance (rail)	$R_{ON(rail)}$		V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	-	130	Ω
		V_{is} = V_{CC}; I_{SW} = 1000 uA	V_{CC} = 4.5 V; V_{EE} = 0 V	-	-	200	Ω
			V_{CC} = 6.0 V; V_{EE} = 0 V	-	-	175	Ω
			V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	-	150	Ω
ON resistance mismatch between channels	ΔR_{ON}	V_{is} = V_{CC} to V_{EE}	V_{CC} = 4.5 V; V_{EE} = 0 V	-	-	-	Ω
			V_{CC} = 6.0 V; V_{EE} = 0 V	-	-	-	Ω
			V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	-	-	Ω
HIGH-level input voltage	V_{IH}	V_{CC} = 4.5 V		3.15	-	-	V
		V_{CC} = 6.0 V		4.2	-	-	V
		V_{CC} = 9.0 V		6.3	-	-	V
LOW-level input voltage	V_{IL}	V_{CC} = 4.5 V		-	-	1.35	V
		V_{CC} = 6.0 V		-	-	1.8	V
		V_{CC} = 9.0 V		-	-	2.7	V
input leakage current	I_I	V_{EE} = 0 V; V_I = V_{CC} or GND	V_{CC} = 6.0 V	-	-	±1.0	uA
			V_{CC} = 9.0 V	-	-	±2.0	uA
OFF-state leakage current	$I_{S(OFF)}$	V_{CC}= 9.0 V; V_{EE}= 0 V; V_I= V_{IH} orV_{IL}; $\|V_{SW}\|$ = V_{CC} - V_{EE}; see Figure 7	per channel	-	-	±1.0	uA
			all channels	-	-	±1.0	uA
ON-state leakage current	$I_{S(ON)}$	V_I= V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{CC}-V_{EE};V_{CC}= 9.0 V; V_{EE}= 0 V; see Figure 8		-	-	±1.0	uA
supply current	I_{CC}	V_{EE} = 0 V; V_I = V_{CC} or GND; V_{is} = V_{EE} or V_{CC}; V_{os} = V_{CC} or V_{EE}	V_{CC} = 6.0 V	-	-	80.0	uA
			V_{CC} = 9.0 V	-	-	160.0	uA
input capacitance	C_I	-		-	-	-	pF
switch capacitance	C_{SW}	independent pins nYn		-	-	-	pF
		common pins nZ		-	-	-	pF

Note:

[1] V_I= V_{IH} or V_{IL}; for test circuit see Figure 5.

[2] V_{is} is the input voltage at anYnor nZ terminal, whichever is assigned as an input.

[3] V_{os} is the output voltage at a nYnor nZ terminal, whichever is assigned as an output.

AC Characteristics 1

(T_{amb}=25℃, GND = 0 V; t_r= t_f= 6 ns; C_L= 50 pF; unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
propagation delay	t_{pd}	V_{is} to V_{os}; R_L = ∞ Ω; see Figure 9[1]	V_{CC} = 4.5 V; V_{EE} = 0 V	-	5	12	ns
			V_{CC} = 6.0 V; V_{EE} = 0 V	-	4	10	ns
			V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	4	8	ns
			V_{CC} = 4.5 V; V_{EE} = 0 V	-	20	44	ns
turn-on time	t_{on}	$\overline{E}$ to V_{os}; R_L = ∞ Ω; see Figure 10[2]	V_{CC} = 5.0 V; V_{EE} = 0 V; C_L = 15 pF	-	17	-	ns
			V_{CC} = 6.0 V; V_{EE} = 0 V	-	16	37	ns
		Sn to V_{os}; R_L = ∞ Ω; see Figure 10[2]	V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	15	31	ns
			V_{CC} = 4.5 V; V_{EE} = 0 V	-	25	44	ns
			V_{CC} = 5.0 V; V_{EE} = 0 V; C_L = 15 pF	-	21	-	ns
			V_{CC} = 6.0 V; V_{EE} = 0 V	-	20	37	ns
			V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	15	31	ns
turn-off time	t_{off}	$\overline{E}$ to V_{os}; R_L= 1 kΩ; see Figure 10[3]	V_{CC} = 4.5 V; V_{EE} = 0 V	-	21	42	ns
			V_{CC} = 5.0 V; V_{EE} = 0 V; C_L = 15 pF	-	18	-	ns
			V_{CC} = 6.0 V; V_{EE} = 0 V	-	17	36	ns
			V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	15	29	ns
		Sn to V_{os}; R_L = 1 kΩ; see Figure 10[3]	V_{CC} = 4.5 V; V_{EE} = 0 V	-	20	42	ns
			V_{CC} = 5.0 V; V_{EE} = 0 V; C_L = 15 pF	-	17	-	ns
			V_{CC} = 6.0 V; V_{EE} = 0 V	-	16	36	ns
			V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	15	29	ns
power dissipation capacitance	C_{PD}	per switch; V_I = GND to V_{CC}[4]		-	36	-	pF

Note:

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] t_{on} is the same as t_{PZH} and t_{PZL}.

[3] t_{off} is the same as t_{PHZ} and t_{PLZ}.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma\{(C_L + C_{SW}) \times V_{CC}^2 \times f_O\}$ where:

f_i = input frequency in MHz;

f_O = output frequency in MHz;

N = number of inputs switching;

$\Sigma\{(C_L + C_{SW}) \times V_{CC}^2 \times f_O\}$ = sum of outputs;

C_L = output load capacitance in pF;

C_{SW} = switch capacitance in pF;

V_{CC} = supply voltage in V.

[5] For test circuit see Figure 11.

[6] V_{is} is the input voltage at anYnor nZ terminal, whichever is assigned as an input.

[7] V_{os} is the output voltage at a nYnor nZ terminal, whichever is assigned as an output.

AC Characteristics 2

(T_{amb}= -40℃~+85℃; GND = 0 V; $t_r = t_f$= 6 ns; C_L = 50 pF; unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
propagation delay	t_{pd}	V_{is} to V_{os}; R_L= ∞ Ω; see Figure 9[1]	V_{CC} = 4.5 V; V_{EE} = 0 V	-	-	15	ns
			V_{CC} = 6.0 V; V_{EE} = 0 V	-	-	13	ns
			V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	-	10	ns
turn-on time	t_{on}	$\overline{E}$ to V_{os}; R_L= ∞ Ω; see Figure 10[2]	V_{CC} = 4.5 V; V_{EE} = 0 V	-	-	55	ns
			V_{CC} = 6.0 V; V_{EE} = 0 V	-	-	47	ns
			V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	-	39	ns
		Sn to V_{os}; R_L= ∞ Ω; see Figure 10[2]	V_{CC} = 4.5 V; V_{EE} = 0 V	-	-	55	ns
			V_{CC} = 6.0 V; V_{EE} = 0 V	-	-	47	ns
			V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	-	39	ns
turn-off time	t_{off}	$\overline{E}$ to V_{os}; R_L = 1 kΩ; see Figure 10[3]	V_{CC} = 4.5 V; V_{EE} = 0 V	-	-	53	ns
			V_{CC} = 6.0 V; V_{EE} = 0 V	-	-	45	ns
			V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	-	36	ns
			V_{CC} = 4.5 V; V_{EE} = 0 V	-	-	53	ns

		Sn to V_{os}; R_L = 1 kΩ; see Figure 10[3]	V_{CC} = 6.0 V; V_{EE} = 0 V	-	-	45	ns
			V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	-	36	ns
power dissipation capacitance	C_{PD}	per switch; V_I = GND to V_{CC}[4]		-	-	-	pF

Note:

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] t_{on} is the same as t_{PZH} and t_{PZL}.

[3] t_{off} is the same as t_{PHZ} and t_{PLZ}.

[4] C_{PD} isused to determine the dynamic power dissipation (P_D in uW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma\{(C_L + C_{SW}) \times V_{CC}^2 \times f_O\}$ where:

f_i = input frequency in MHz;

f_O = output frequency in MHz;

N = number of inputs switching;

$\Sigma\{(C_L + C_{SW}) \times V_{CC}^2 \times f_O\}$ = sum of outputs;

C_L = output load capacitance in pF;

C_{SW} = switch capacitance in pF;

V_{CC} = supply voltage in V.

[5] For test circuit see Figure 11.

[6] V_{is} is the input voltage at anYnor nZ terminal, whichever is assigned as an input.

[7] V_{os} is the output voltage at a nYnor nZ terminal, whichever is assigned as an output.

AC Characteristics 3

(T_{amb}= 25℃; GND = 0V; C_L=50pF; recommended conditions and typical values.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
sine-wave distortion	d_{sin}	f_i = 1 kHz; R_L = 10 kΩ; see Figure 12	V_{is} = 4.0 V (p-p); V_{CC} = 2.25 V; V_{EE} = -2.25 V	-	0.04	-	%
			V_{is} = 8.0 V (p-p); V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	0.02	-	%
		f_i = 10 kHz; R_L = 10 kΩ; see Figure 12	V_{is} = 4.0 V (p-p); V_{CC} = 2.25 V; V_{EE} = -2.25 V	-	0.12	-	%
			V_{is} = 8.0 V (p-p); V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	0.06	-	%
isolation (OFF-state)	u_{iso}	R_L= 600 Ω; f_i= 1 MHz; see Figure 13	V_{CC} = 2.25 V; V_{EE} = -2.25 V [1]	-	-50	-	dB
			V_{CC} = 4.5 V; V_{EE} = -4.5 V [1]	-	-50	-	dB
crosstalk	Xtalk	between two switches/multiplexers; R_L= 600 Ω;f_i= 1 MHz; see Figure 14	V_{CC} = 2.25 V; V_{EE} = -2.25 V [1]	-	-60	-	dB
			V_{CC} = 4.5 V; V_{EE} = -4.5 V [1]	-	-60	-	dB
crosstalk voltage	V_{ct}	peak-to-peak value; between control and any switch; R_L= 600 Ω; f_i= 1MHz; $\overline{E}$ or Sn square wave between V_{CC} and GND; t_r= t_f= 6 ns; see Figure 15	V_{CC} = 4.5 V; V_{EE} = 0 V	-	110	-	mV
			V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	220	-	mV
-3dB frequency response	$f_{(-3dB)}$	R_L = 50 Ω; see Figure 16	V_{CC} = 2.25 V; V_{EE} = -2.25 V [2]	-	160	-	MHz
			V_{CC} = 4.5 V; V_{EE} = -4.5 V [2]	-	170	-	MHz

Note：

[1] Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).

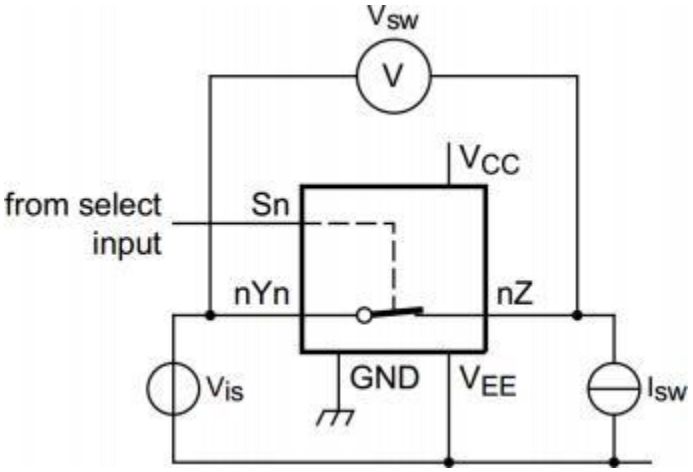
[2] Adjust input voltage V_{is} to 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

[3] V_{is} is the input voltage at anYnor nZ terminal, whichever is assigned as an input.

[4] V_{os} is the output voltage at a nYnor nZ terminal, whichever is assigned as an output.

Testing Circuit

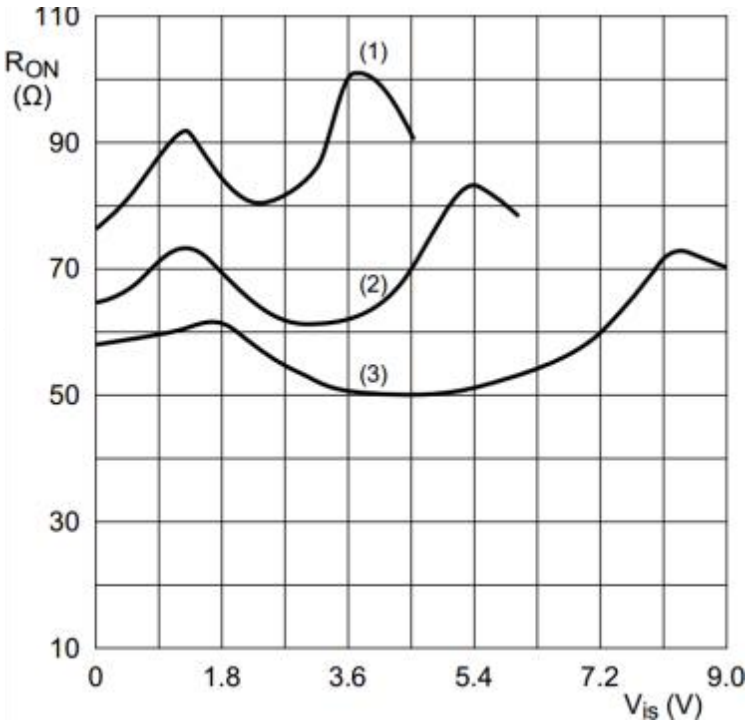
DC Testing Circuit 1



V_{is} = 0V to (V_{CC} -V_{EE})

R_{ON} = V_{SW}/I_{SW}

Figure 5. Test circuit for measuring R_{ON}



V_{is} = 0V to (V_{CC} -V_{EE})

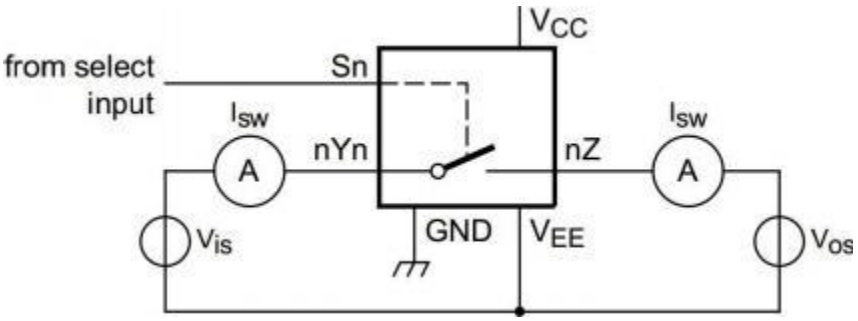
(1)V_{CC} = 4.5V

(2)V_{CC} = 6V

(3)V_{CC} = 9V

Figure 6. Typical R_{ON} as a function of input voltage V_{is}

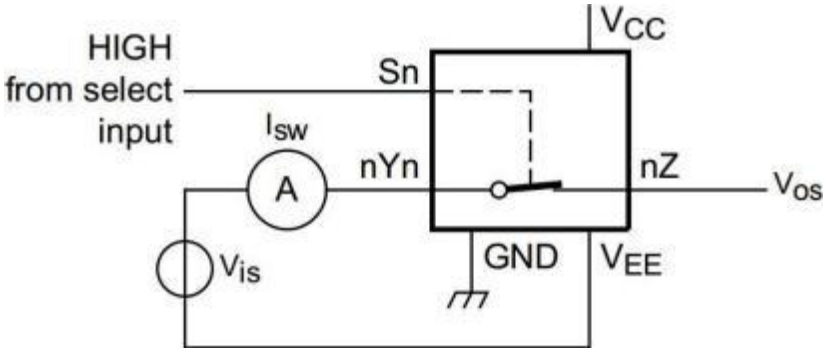
DC Testing Circuit 2



V_{is}= V_{CC} andV_{os}= V_{EE}.

V_{is}= V_{EE} and V_{os}= V_{CC}.

Figure 7. Test circuit for measuring OFF-state current



V_{is}= V_{CC} andV_{os}= open-circuit.

V_{is}= V_{EE} and V_{os}= open-circuit.

Figure 8. Test circuit for measuring ON-state current

AC Testing Waveforms

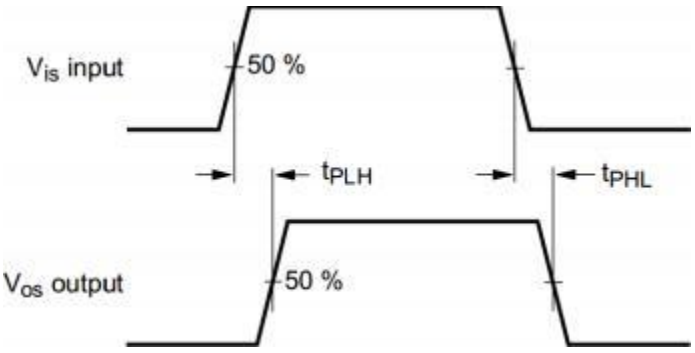
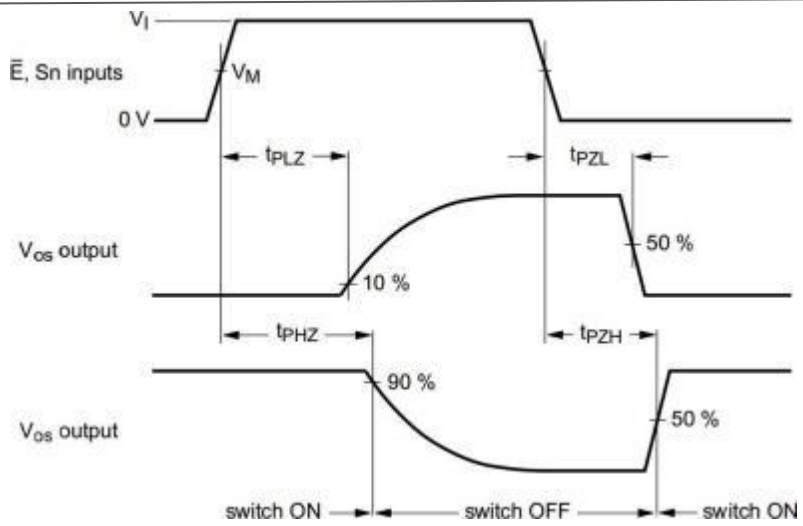


Figure 9. Input (V_{is}) to output (V_{os}) propagation delays



For SN74HC4053: $V_M = 0.5 \times V_{CC}$

Figure 10. Turn-on and turn-offtimes

AC Testing Circuit 1

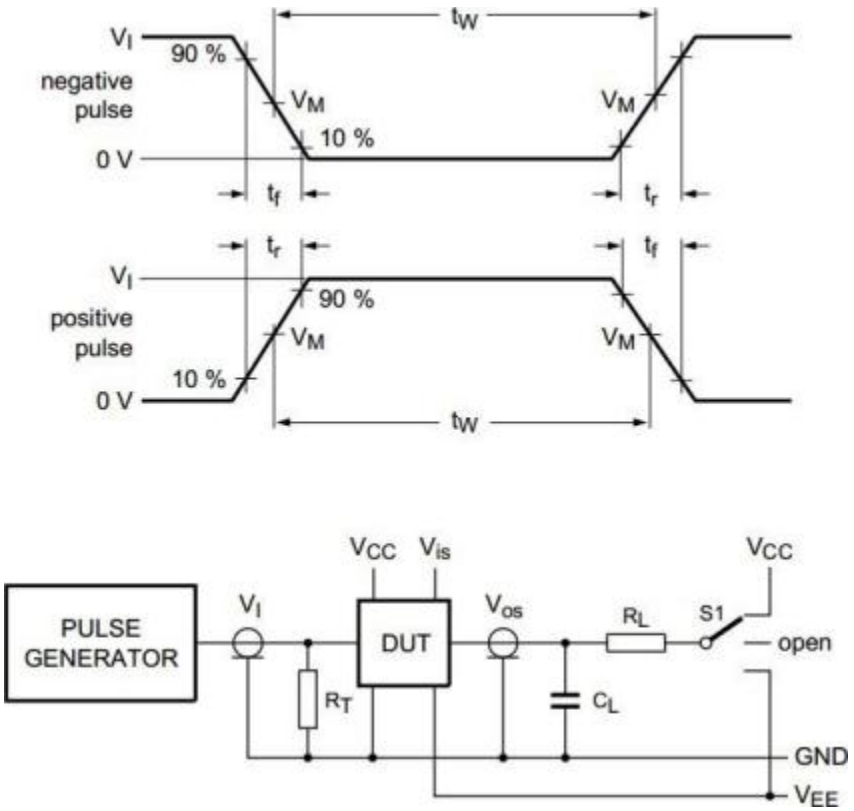


Figure 11. Test circuit for measuring switching times

Definitions for test circuit:
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.
C_L = load capacitance including jig and probe capacitance.
R_L = load resistance.
S1 = Test selection switch.

Test Data

Test	Input				Load		S1 position
	V_I	V_{is}	t_r, t_f		C_L	R_L	
			atf_{max}	other[1]			
t_{PHL}, t_{PLH}	[2]	pulse	< 2ns	6ns	50pF	1kΩ	open
t_{PZH}, t_{PHZ}	[2]	V_{CC}	< 2ns	6ns	50pF	1kΩ	V_{EE}
t_{PZL}, t_{PLZ}	[2]	V_{EE}	< 2ns	6ns	50pF	1kΩ	V_{CC}

Note:

[1] $t_r = t_f = 6$ ns; when measuring f_{max}, there is no constraint to t_r and t_f with 50 % duty factor.

[2] V_I values:

For SN74HC4053: $V_I = V_{CC}$.

AC Testing Circuit 2

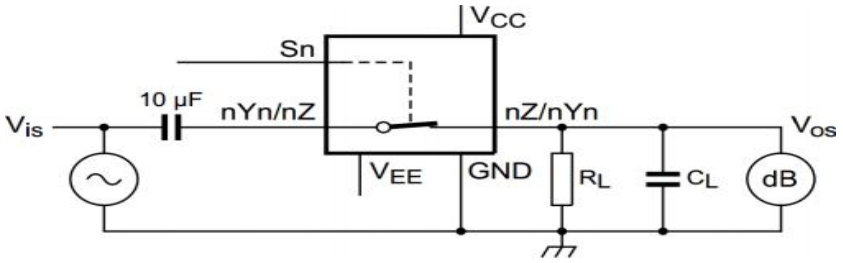
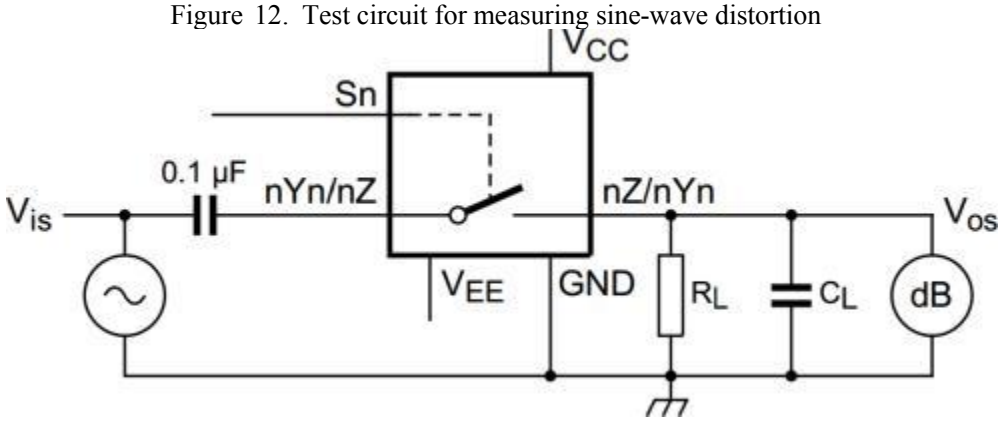
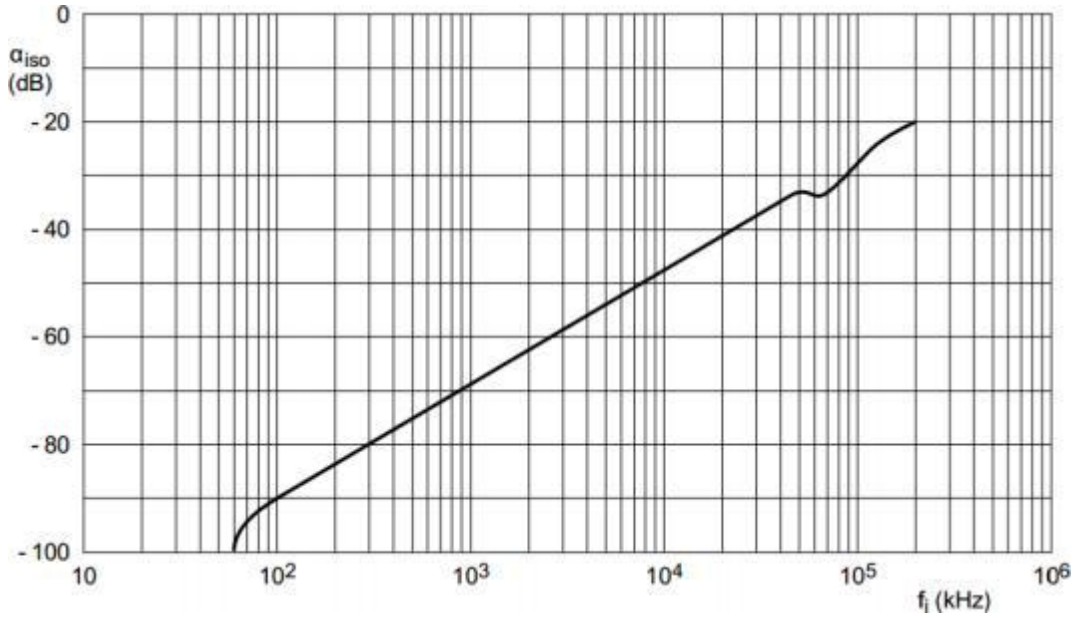


Figure 12. Test circuit for measuring sine-wave distortion



$V_{CC} = 4.5$ V; GND = 0 V; $V_{EE} = -4.5$ V; $R_L = 600\ \Omega$; $R_S = 1$ kΩ.

a.Test circuit

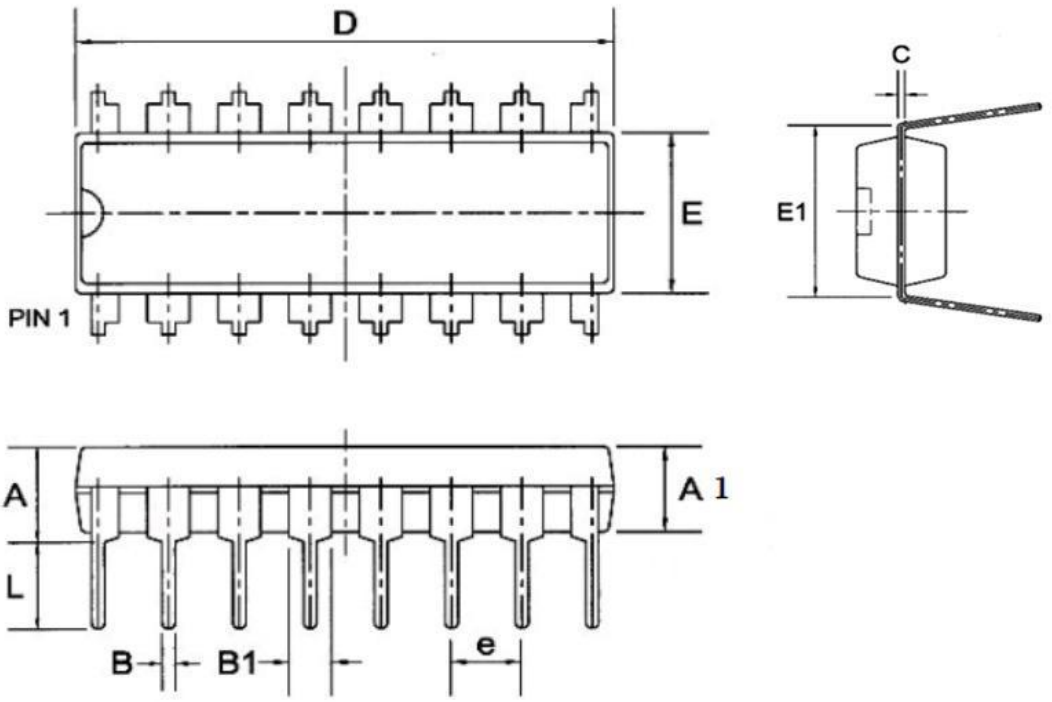


b. Isolation (OFF-state) as a function of frequency

Figure 13. Test circuit for measuring isolation (OFF-state)

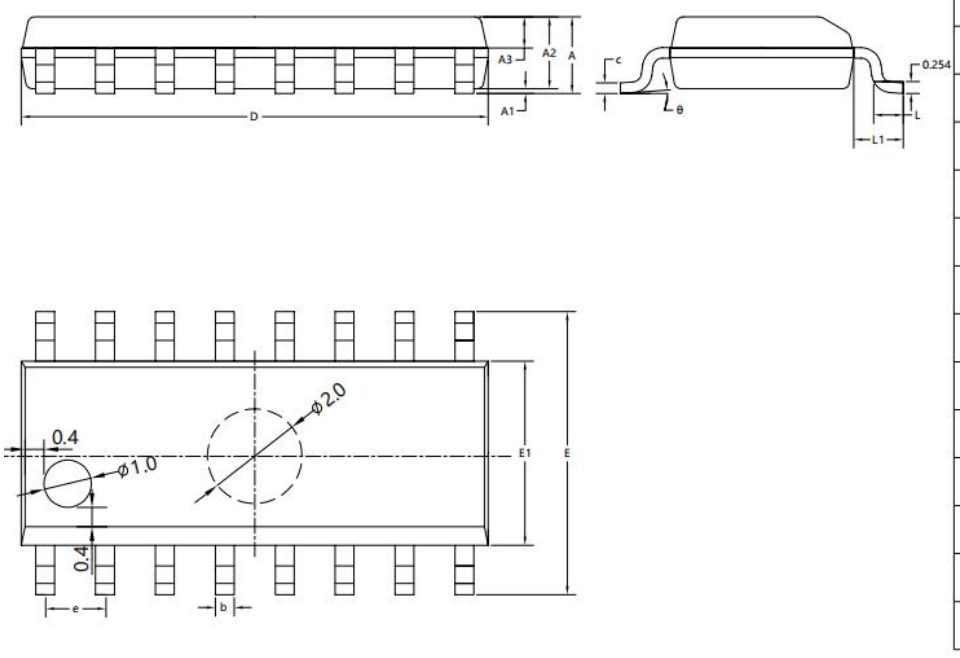
Package Information

DIP16



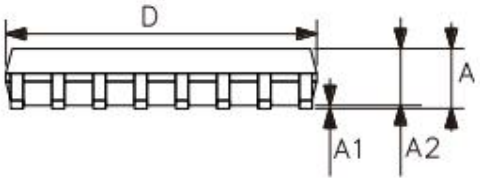
Symbol	Dimensions in Millimeters		
	Min	Nom	Max
A	--	--	4.31
A1	3.15	3.30	3.65
B	--	0.50	--
B1	--	1.6	--
C	--	0.27	--
D	19.00	19.20	19.60
E	6.20	6.50	6.60
E1	--	8.0	--
e	--	2.3	--
L	3.00	3.20	3.60

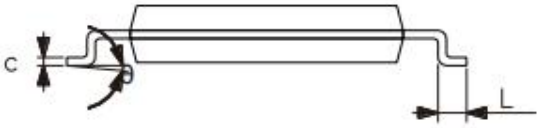
SOP16

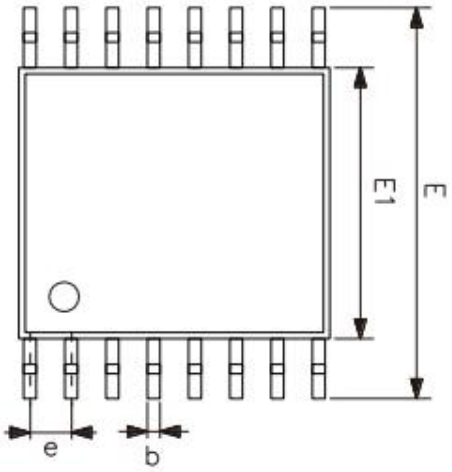


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.50	1.60	1.70
A1	0.10	0.15	0.25
A2	1.40	1.45	1.50
A3	0.60	0.65	0.70
b	0.30	0.40	0.50
c	0.15	0.20	0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.85	3.90	3.95
e	1.27BSC		
L	0.50	0.60	0.70
L1	1.05BSC		
θ	0°	4°	8°

TSSOP16







Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
θ	0°	8°

Statement：

✧ Shenzhen xinbole electronics co., ltd. reserves the right to change the product specifications, without notice! Before placing an order, the customer needs to confirm whether the information obtained is the latest version, and verify the integrity of the relevant information.

✧ Any semiconductor product is liable to fail or malfunction under certain conditions, and the buyer shall be responsible for complying with safety standards in the system design and whole machine manufacturing using Shenzhen xinbole electronics co., ltd products, and take appropriate security measures to avoid the potential risk of failure may result in personal injury or property losses of the situation occurred!

✧ This document is for referenceonly,and the actual use should be based on the application test results.

✧ Product performance is never ending, Shenzhen xinbole electronics co., ltd will be dedicated to provide customers with better performance, better quality of integrated circuit products.