N-channel Enhancement Mode Power MOSFET

Features

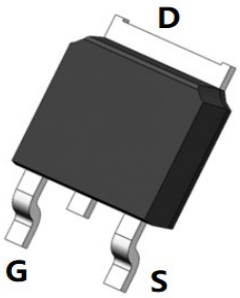
- V_{DS}= 150V, I_D= 50 A
  $R_{DS(ON)}$ < 19 mΩ @ V_{GS} = 10V
  $R_{DS(ON)}$ < 22 mΩ @ V_{GS} =4.5V

General Features

- Advanced Trench Technology
- Provide Excellent RDS(ON) and Low Gate Charge
- Lead Free and Green Available

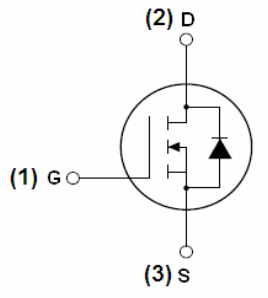
100% UIS TESTED!
100% ΔVds TESTED!

RoHS



TO-252-2L Top View

Pin Assignment



Schematic Diagram

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 175 °C)[b]	T_C = 25 °C	I_D	50	A
	T_C = 125 °C		43	
Pulsed Drain Current		I_{DM}	40	
Continuous Source Current (Diode Conduction)		I_S	43	
Avalanche Current		I_{AS}	3	
Single Pulse Avalanche Energy	L = 0.1 mH	E_{AS}	18	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	96[b]	W
	T_A = 25 °C		3[a]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 175	°C

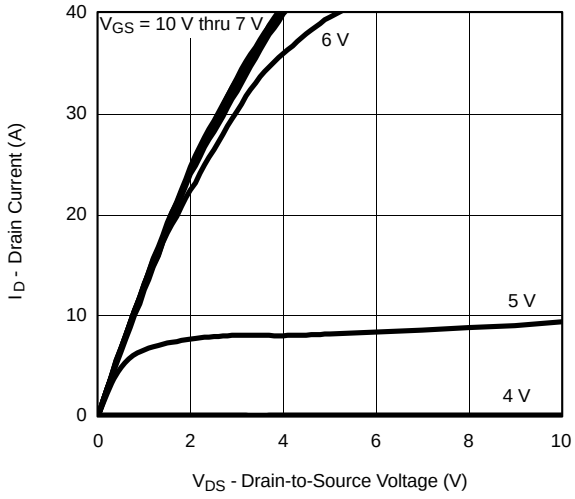
THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Junction-to-Ambient[a]	t ≤ 10 s	R_{thJA}	15	18	°C/W
	Steady State		40	50	
Junction-to-Case (Drain)		R_{thJC}	0.85	1.1	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.[a]**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2		4	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 200 V, V_{GS} = 0 V			1	µA
		V_{DS} = 200 V, V_{GS} = 0 V, T_J = 125 °C			50	
		V_{DS} = 200 V, V_{GS} = 0 V, T_J = 175 °C			250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	40			A
Drain-Source On-State Resistance[b]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 3 A		0.019		Ω
		V_{GS} = 10 V, I_D = 3 A, T_J = 125 °C		0.020		
		V_{GS} = 10 V, I_D = 3 A, T_J = 175 °C		0.025		
		V_{GS} = 6 V, I_D = 3 A		0.039		
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 3 A		35		S
Dynamic[a]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, F = 1 MHz		1800		pF
Output Capacitance	C_{oss}			180		
Reverse Transfer Capacitance	C_{rss}			80		
Total Gate Charge[c]	Q_g	V_{DS} = 100 V, V_{GS} = 10 V, I_D = 3 A		34	51	nC
Gate-Source Charge[c]	Q_{gs}			8		
Gate-Drain Charge[c]	Q_{gd}			12		
Gate Resistance	R_g		0.5		2.9	Ω
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 100 V, R_L = 5.2 Ω I_D ≅ 3 A, V_{GEN} = 10 V, R_g = 2.5 Ω		15	25	ns
Rise Time[c]	t_r			50	75	
Turn-Off Delay Time[c]	$t_{d(off)}$			30	45	
Fall Time[c]	t_f			60	90	
Source-Drain Diode Ratings and Characteristics (T_C = 25 °C)						
Pulsed Current	I_{SM}				5	A
Diode Forward Voltage[b]	V_{SD}	I_F = 3 A, V_{GS} = 0 V		0.9	1.5	V
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 3 A, dI/dt = 100 A/µs		180	250	ns

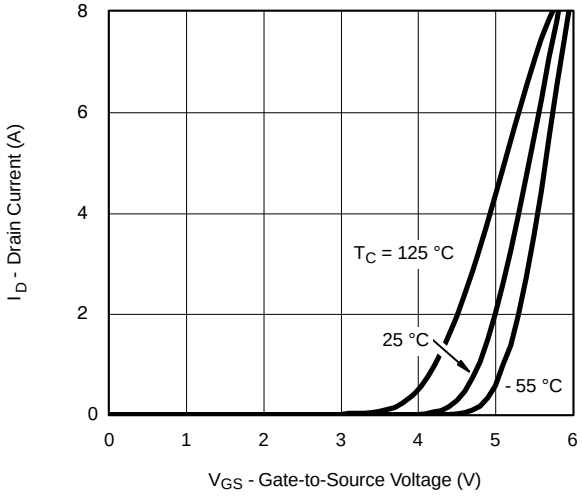
Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

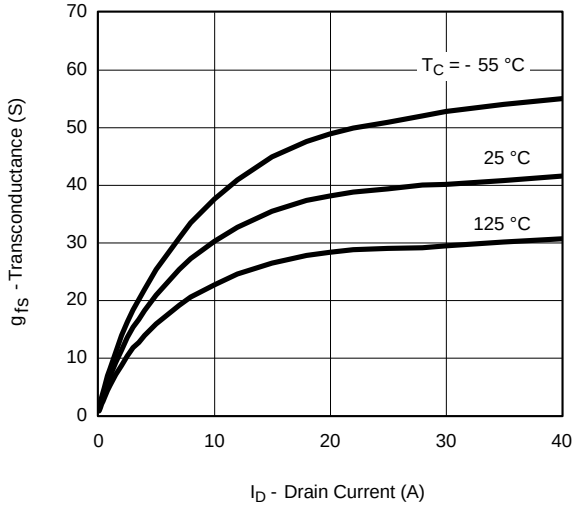
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



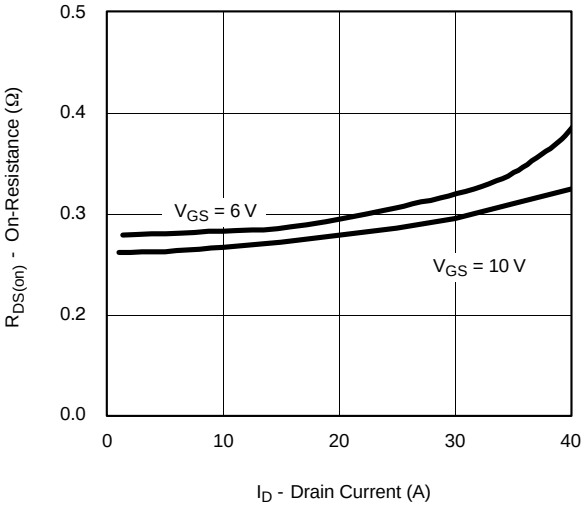
Output Characteristics



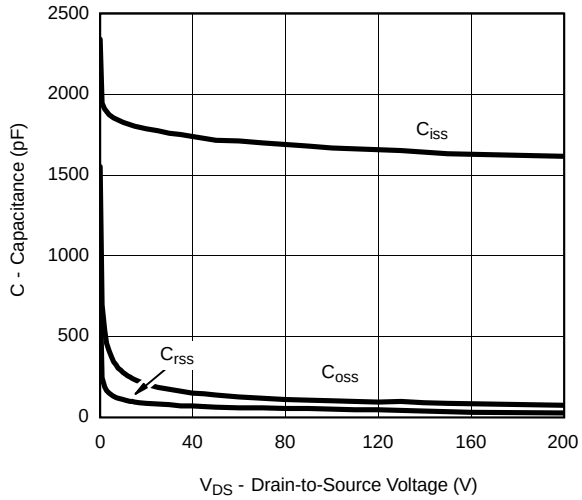
Transfer Characteristics



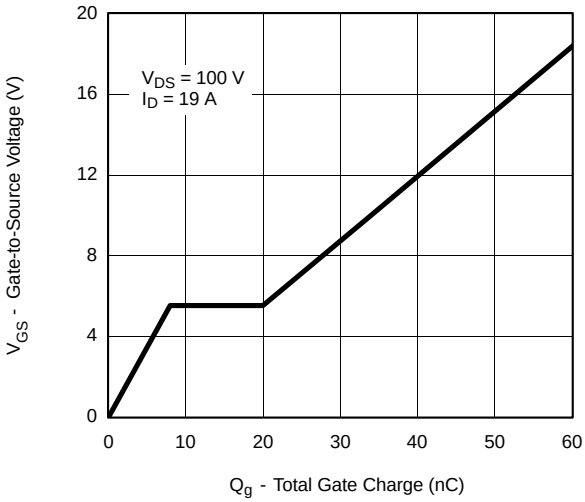
Transconductance



On-Resistance vs. Drain Current

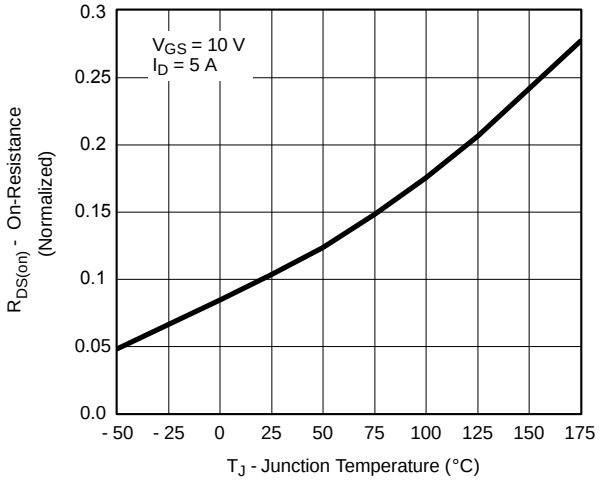


Capacitance

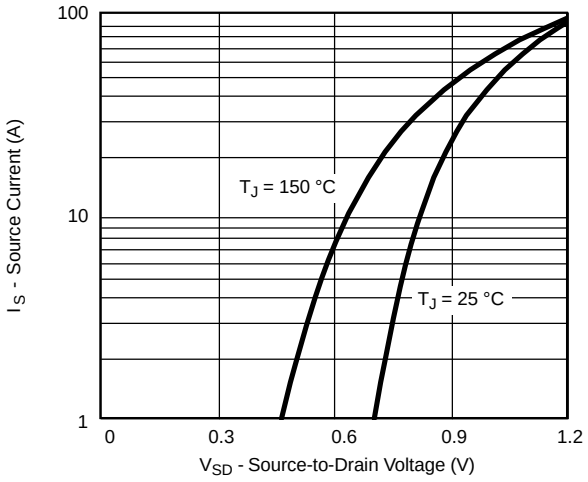


Gate Charge

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

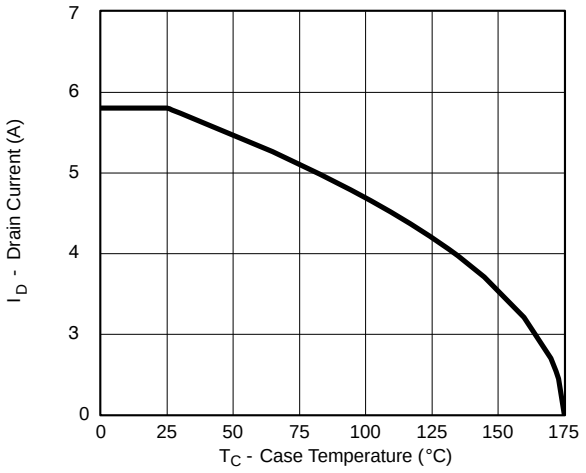


On-Resistance vs. Junction Temperature

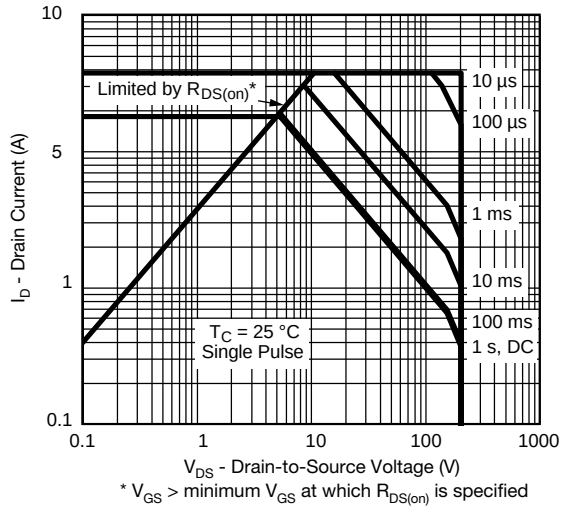


Source-Drain Diode Forward Voltage

THERMAL RATINGS

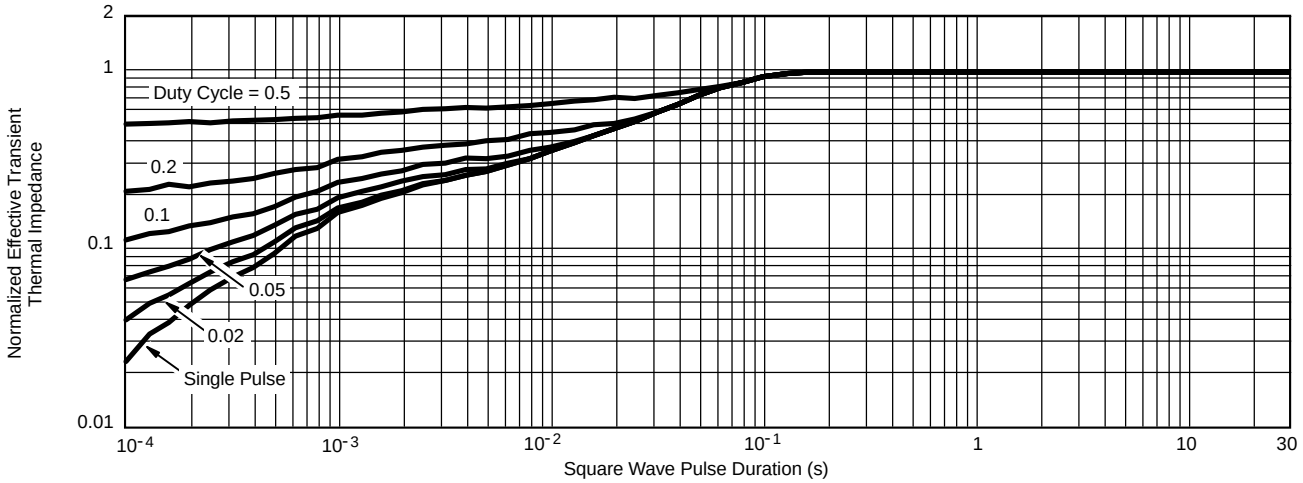


Maximum Avalanche Drain Current vs. Case Temperature



* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case