

N-Channel Enhancement Mode Power MOSFET

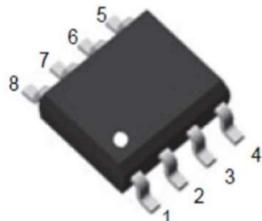
Features

- $V_{DS} = 20V$, $I_D = 12 A$
- $R_{DS(ON)} < 6 m\Omega$ @ $V_{GS} = 4.5V$
- $R_{DS(ON)} < 8 m\Omega$ @ $V_{GS} = 2.5V$

General Features

- Advanced Trench Technology
- Provide Excellent RDS(ON) and Low Gate Charge
- Lead Free and Green Available

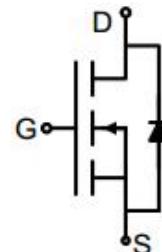
100% UIS TESTED!
100% ΔV_{ds} TESTED!



SOP-8



pin assignment



Schematic diagram

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	V
Drain Current-Continuous	I_D	12	A
Drain Current-Continuous($T_A=100^\circ C$)	$I_D(100^\circ C)$	8	A
Pulsed Drain Current	I_{DM}	40	A
Maximum Power Dissipation	P_D	2.5	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	50	°C/W
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Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

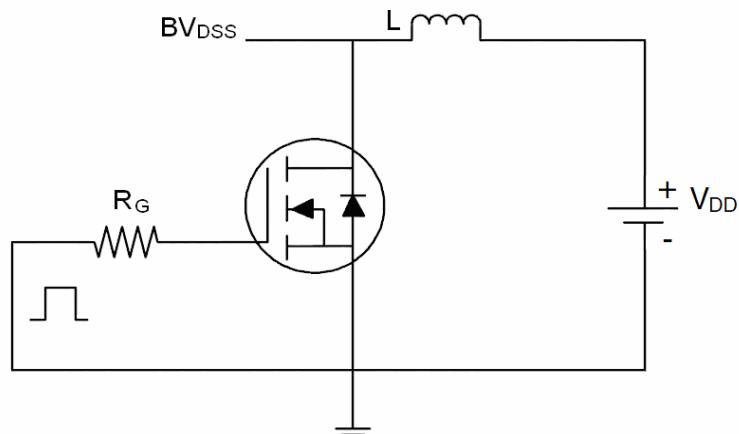
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	20	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=20\text{V}, V_{\text{GS}}=0\text{V}$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{\text{GS}}=\pm 12\text{V}, V_{\text{DS}}=0\text{V}$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	0.5		2.0	V
Drain-Source On-State Resistance	$R_{\text{DS(ON)}}$	$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=6\text{A}$	-		6	$\text{m}\Omega$
		$V_{\text{GS}}=2.5\text{V}, I_{\text{D}}=5\text{A}$			8	$\text{m}\Omega$
Forward Transconductance	g_{FS}	$V_{\text{DS}}=10\text{V}, I_{\text{D}}=6\text{A}$	20	-	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{iss}	$V_{\text{DS}}=10\text{V}, V_{\text{GS}}=0\text{V}, F=1.0\text{MHz}$	-	2000	-	PF
Output Capacitance	C_{oss}		-	402	-	PF
Reverse Transfer Capacitance	C_{rss}		-	170	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{\text{d(on)}}$	$V_{\text{DD}}=10\text{V}, I_{\text{D}}=6\text{A}, V_{\text{GS}}=4.5\text{V}, R_{\text{GEN}}=1\Omega$	-	25	-	nS
Turn-on Rise Time	t_r		-	15	-	nS
Turn-Off Delay Time	$t_{\text{d(off)}}$		-	25	-	nS
Turn-Off Fall Time	t_f		-	15	-	nS
Total Gate Charge	Q_g	$V_{\text{DS}}=10\text{V}, I_{\text{D}}=6\text{A}, V_{\text{GS}}=10\text{V}$	-	42	-	nC
Gate-Source Charge	Q_{gs}		-	10.8	-	nC
Gate-Drain Charge	Q_{gd}		-	9.2	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{\text{GS}}=0\text{V}, I_{\text{S}}=6\text{A}$	-	-	1.2	V
Diode Forward Current (Note 2)	I_{S}		-	-	12	A

Notes:

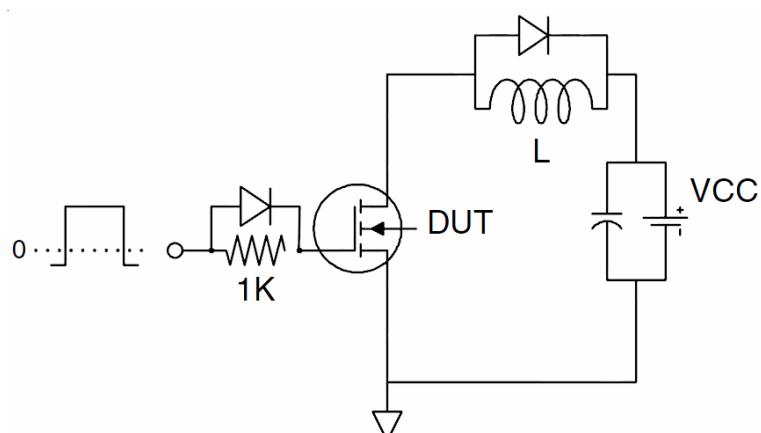
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

Test Circuit

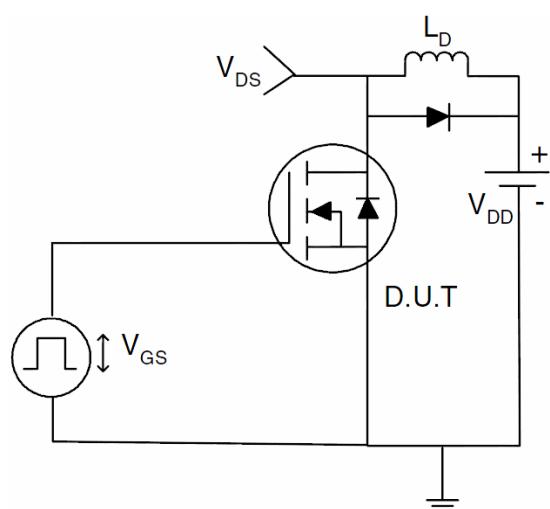
1) E_{AS} Test Circuits



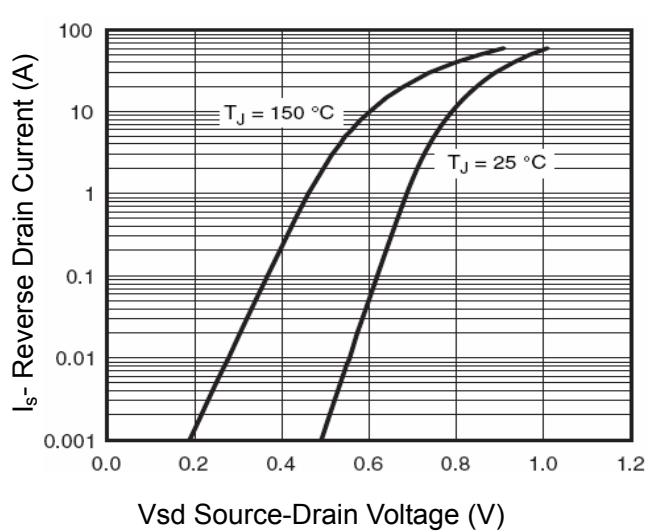
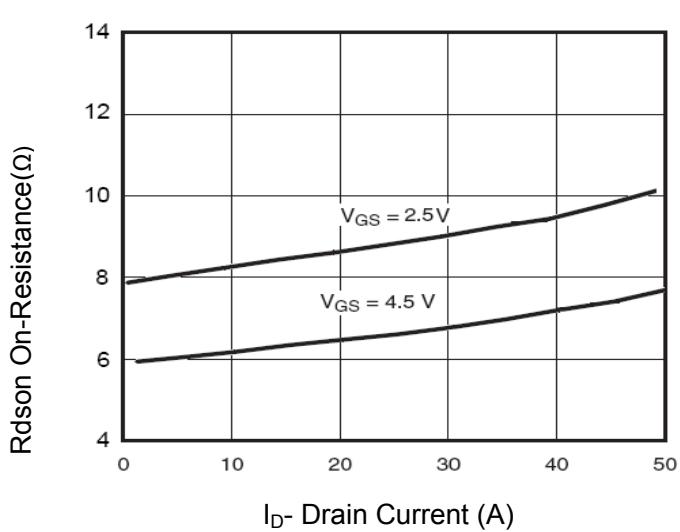
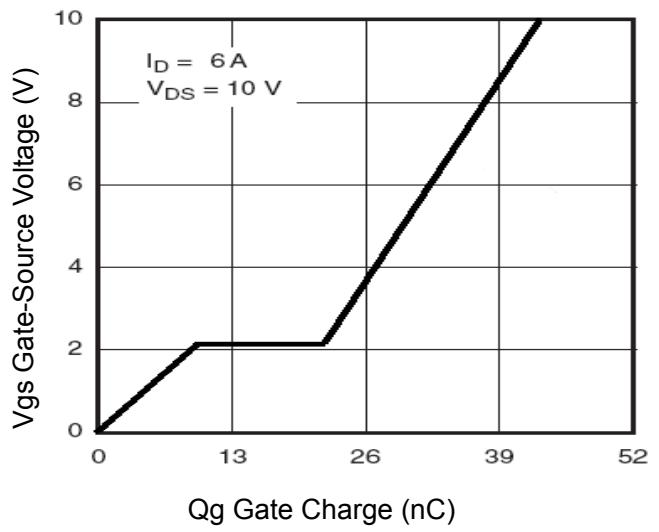
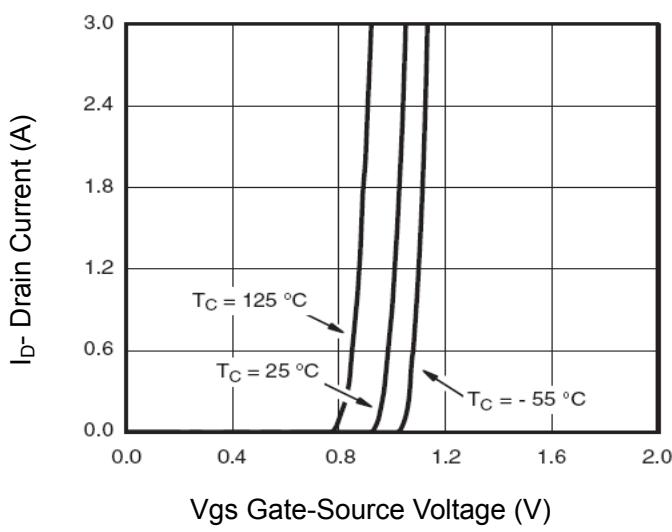
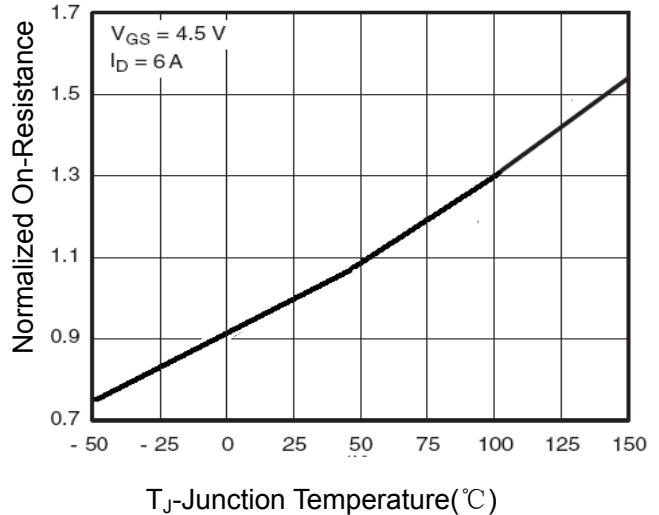
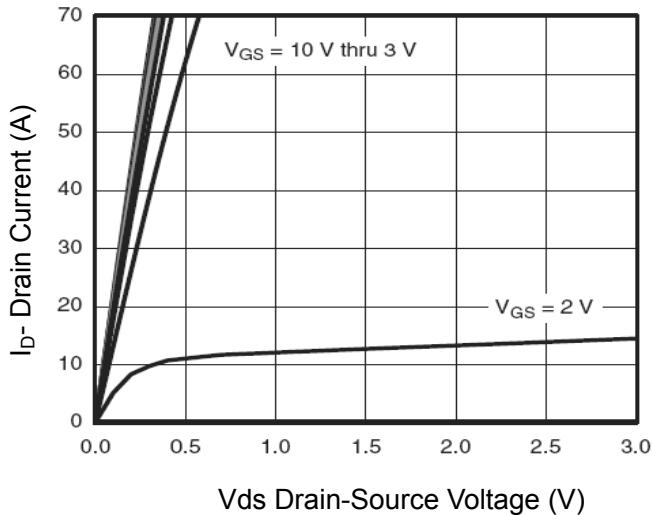
2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)



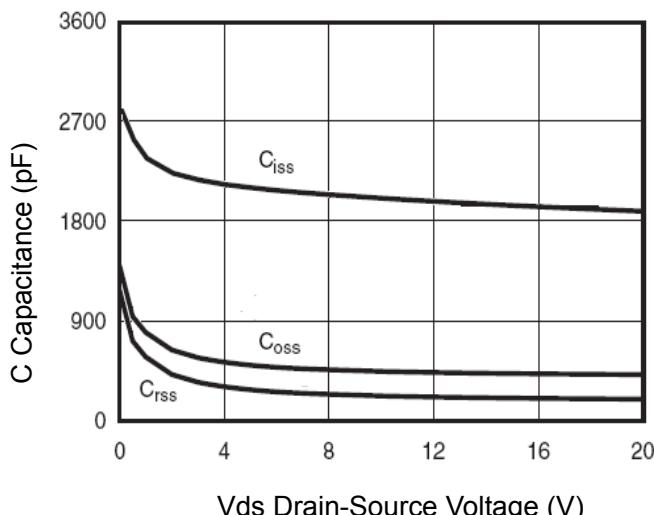


Figure 7 Capacitance vs Vds

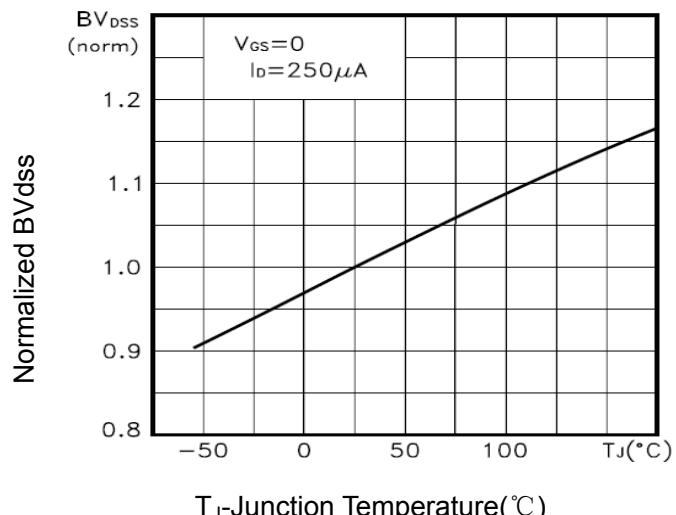


Figure 9 BV_{DSS} vs Junction Temperature

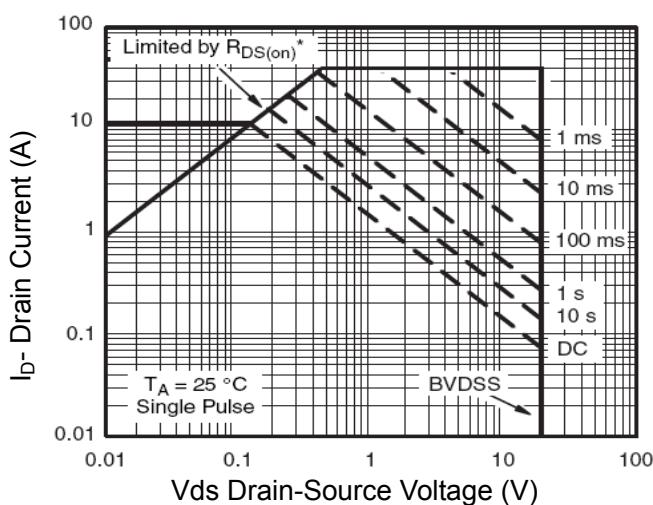


Figure 8 Safe Operation Area

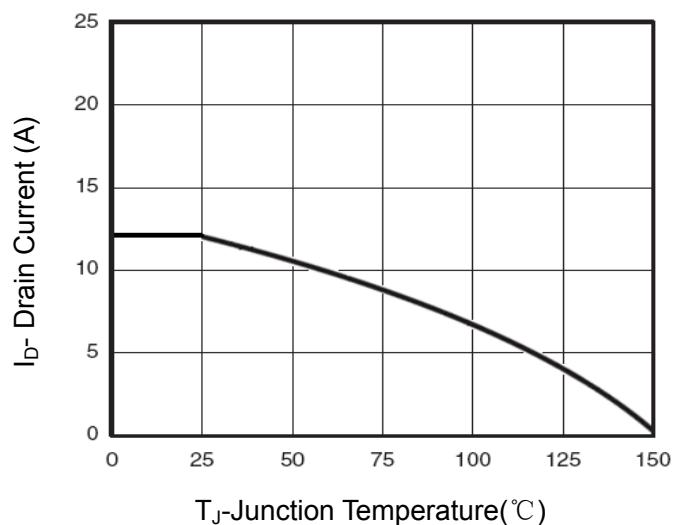


Figure 10 Current vs Junction Temperature

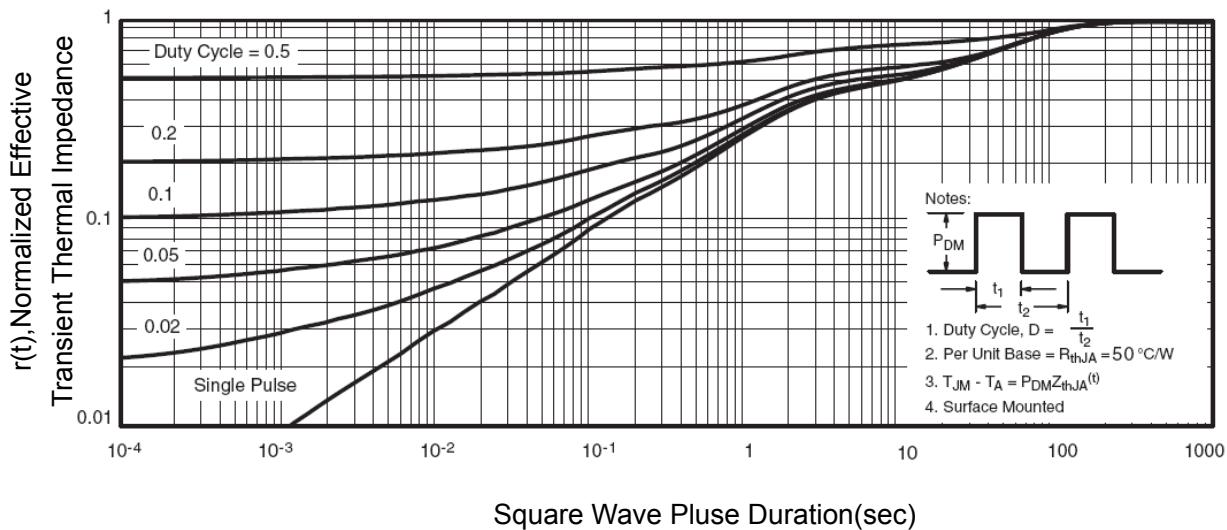


Figure 11 Normalized Maximum Transient Thermal Impedance