

Dual N-Channel Advanced Power MOSFET

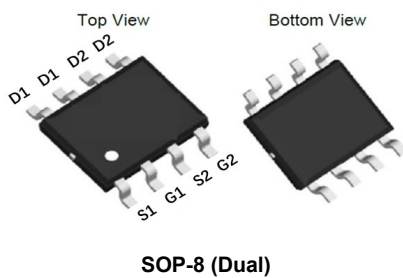
Features

- $V_{DS} = 40V$, $I_D = 11 A$
 $R_{DS(ON)} < 9 m\Omega @ V_{GS} = 10V$
 $R_{DS(ON)} < 11 m\Omega @ V_{GS} = 4.5V$

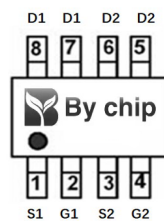
General Features

- Advanced Trench Technology
- Provide Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free and Green Available

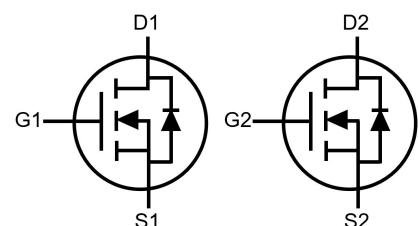
100% UIS TESTED!
 100% ΔV_{ds} TESTED!



SOP-8 (Dual)



Pin Assignment



Schematic diagram

Maximum ratings, at $T_A = 25^\circ C$, unless otherwise specified

Symbol	Parameter	Rating	Unit	
$V_{(BR)DSS}$	Drain-Source breakdown voltage	40	V	
V_{GS}	Gate-Source voltage	± 20	V	
I_S	Diode continuous forward current	$T_A = 25^\circ C$	1.7	A
I_D	Continuous drain current @ $V_{GS} = 10V$	$T_A = 25^\circ C$	11	A
I_D	Continuous drain current @ $V_{GS} = 10V$	$T_A = 70^\circ C$	9	A
I_{DM}	Pulse drain current tested ①	$T_A = 25^\circ C$	44	A
E_{AS}	Avalanche energy, single pulsed ②		64	mJ
P_D	Maximum power dissipation ③	$T_A = 25^\circ C$	2	W
		$T_A = 70^\circ C$	1.3	W
T_{STG}, T_J	Storage and Junction Temperature Range	-55 to 150	$^\circ C$	

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit	
$R_{\theta JL}$	Thermal Resistance, Junction-to-Lead	23	28	$^\circ C/W$	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient④	$t \leq 10s$	52	62.5	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient④	Steady State	78	94	$^\circ C/W$

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	40	--	--	V
IDSS	Zero Gate Voltage Drain Current(T _j =25°C)	V _{DS} =40V, V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T _j =125°C) ⑤	V _{DS} =40V, V _{GS} =0V	--	--	100	μA
IGSS	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
VGS(th)	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.0		2.5	V
RDS(on)	Drain-Source On-State Resistance ⑥	V _{GS} =10V, I _D =10A	--		9	mΩ
		T _j =100°C ⑤	--		10	mΩ
RDS(on)	Drain-Source On-State Resistance ⑥	V _{GS} =4.5V, I _D =6A	--		11	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
Ciss	Input Capacitance ⑤	V _{DS} =20V, V _{GS} =0V, f=1MHz	--	870	--	pF
Coss	Output Capacitance ⑤		--	265	--	pF
Crss	Reverse Transfer Capacitance ⑤		--	20	--	pF
Rg	Gate Resistance	f=1MHz	--	1.8	--	Ω
Qg(10V)	Total Gate Charge ⑤	V _{DS} =20V, I _D =10A, V _{GS} =10V	--	13	--	nC
Qg(4.5V)	Total Gate Charge ⑤		--	6.3	--	nC
Qgs	Gate-Source Charge ⑤		--	2.7	--	nC
Qgd	Gate-Drain Charge ⑤		--	1.6	--	nC
Switching Characteristics ⑤						
Td(on)	Turn-on Delay Time	V _{DD} =20V, I _D =10A, R _G =3Ω, V _{GS} =10V	--	5.6	--	ns
Tr	Turn-on Rise Time		--	29	--	ns
Td(off)	Turn-Off Delay Time		--	15	--	ns
Tf	Turn-Off Fall Time		--	4.6	--	ns
Source- Drain Diode Characteristics @ T_j = 25°C (unless otherwise stated)						
VSD	Forward on voltage	I _{SD} =10A, V _{GS} =0V	--	0.8	1.2	V
Trr	Reverse Recovery Time ⑤	I _{SD} =10A, V _{GS} =0V	--	18	--	ns
Qrr	Reverse Recovery Charge ⑤	di/dt=100A/μs	--	7	--	nC

NOTE:

- ① Single pulse; pulse width ≤ 100μs.
- ② EAS of 64mJ is based on starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 16A, V_{GS} = 10V; 100% FT tested at L = 0.5mH, I_{AS} = 9A.
- ③ The power dissipation P_{DSM} is based on T_J(max), using junction-to-ambient thermal resistance RθJA.
- ④ These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with TA=25°C.
- ⑤ Guaranteed by design, not subject to production testing.
- ⑥ Pulse width ≤ 380μs; duty cycle ≤ 2%.

Typical Characteristics

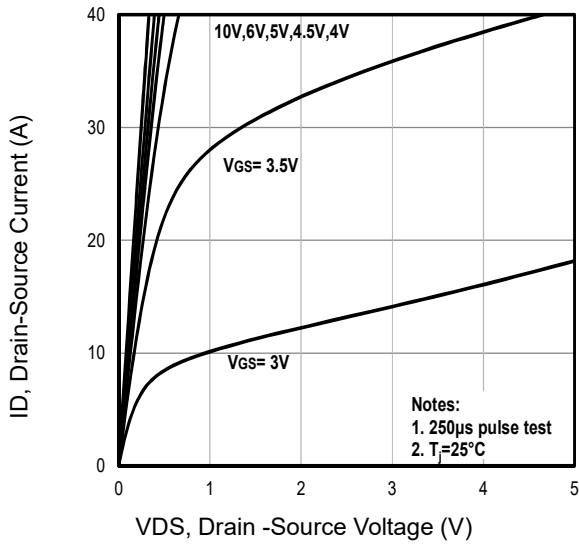


Fig1. Typical Output Characteristics

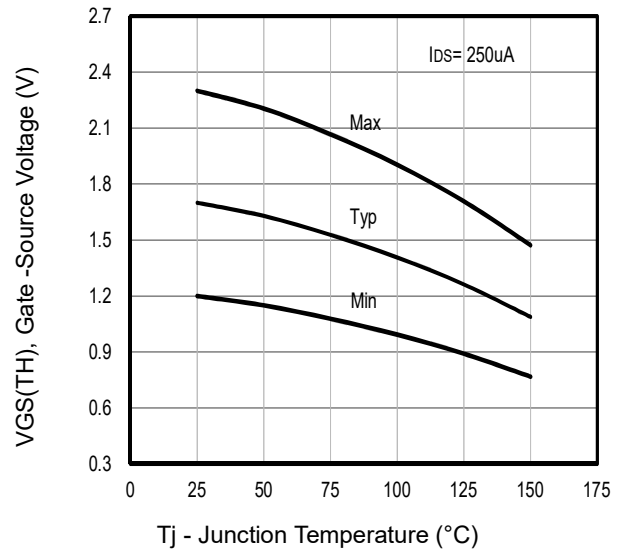


Fig2. Typical $V_{GS(TH)}$ Gate-Source Voltage Vs. T_j

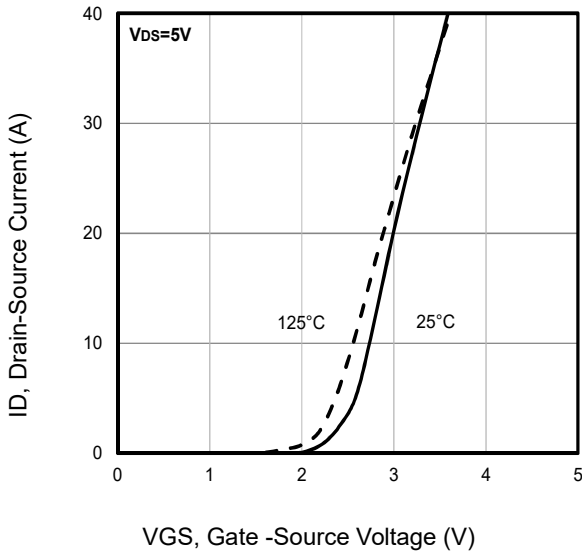


Fig3. Typical Transfer Characteristics

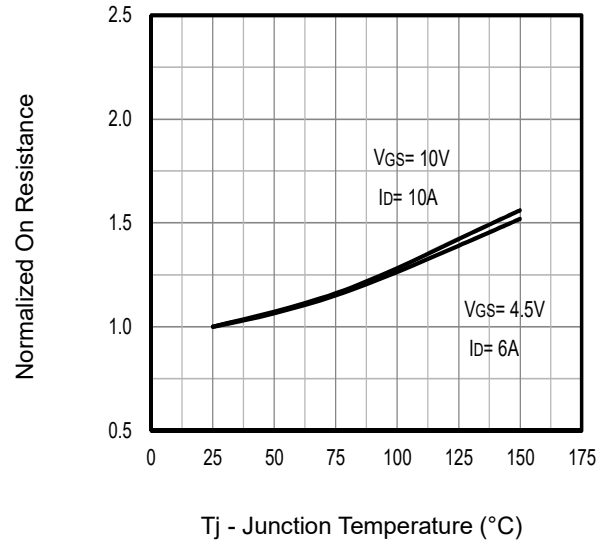


Fig4. Typical Normalized On-Resistance Vs. T_j

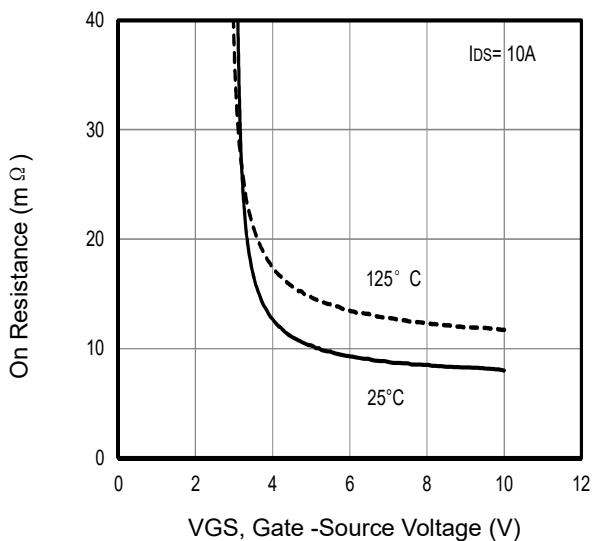


Fig5. Typical On Resistance Vs Gate-Source Voltage

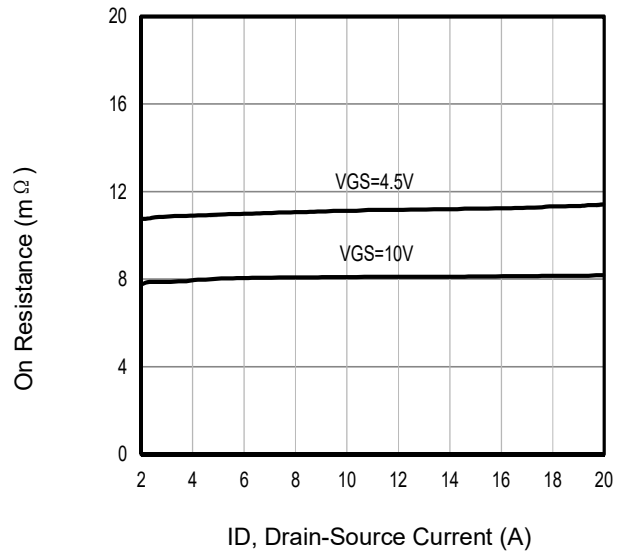


Fig6. Typical On Resistance Vs Drain Current

Typical Characteristics

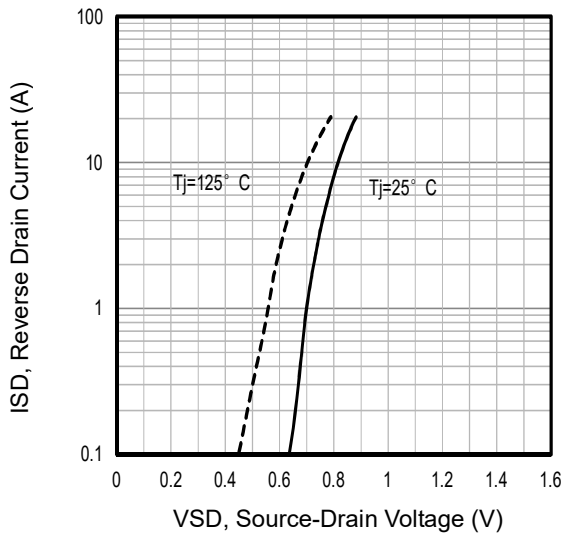


Fig7. Typical Source-Drain Diode Forward Voltage

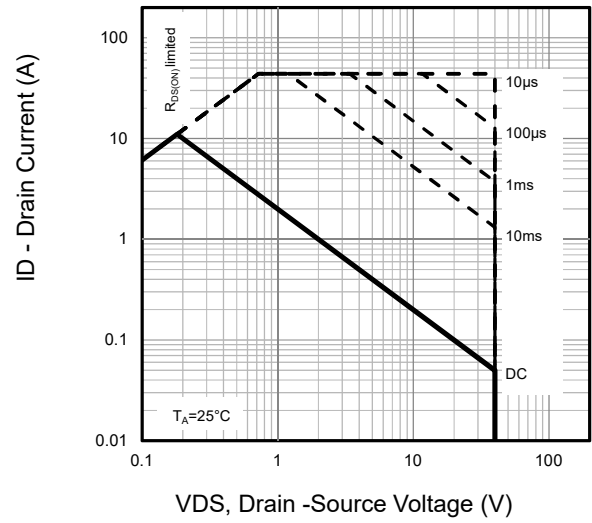


Fig8. Maximum Safe Operating Area

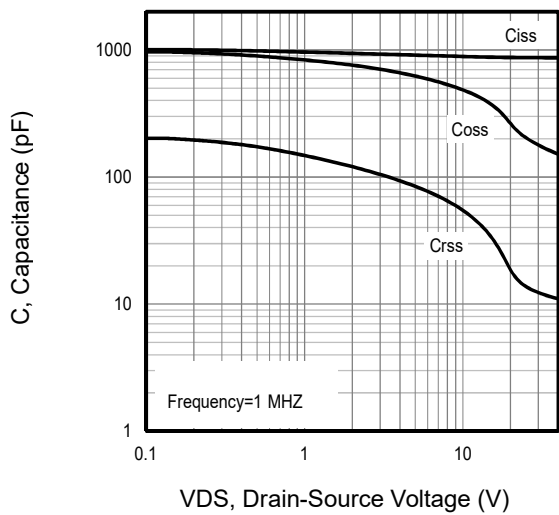


Fig9. Typical Capacitance Vs. Drain-Source Voltage

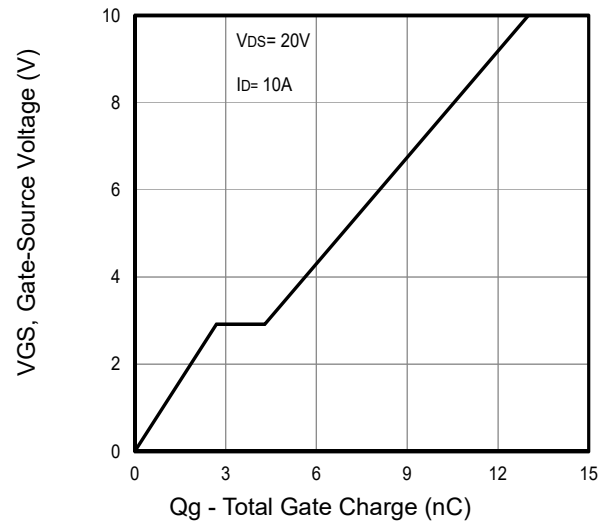


Fig10. Typical Gate Charge Vs. Gate-Source Voltage

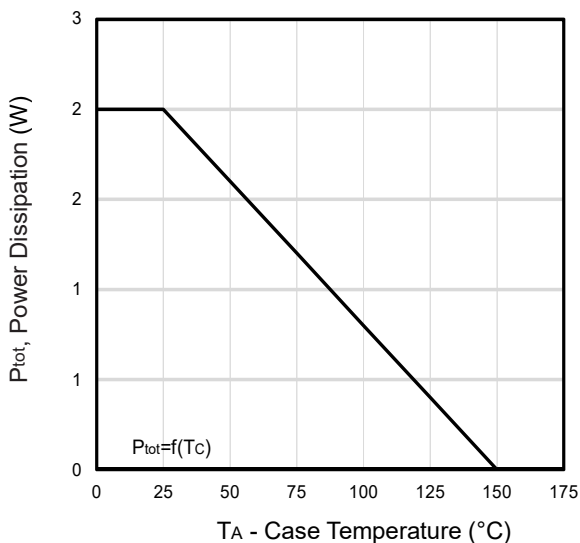


Fig11. Power Dissipation Vs. Case Temperature

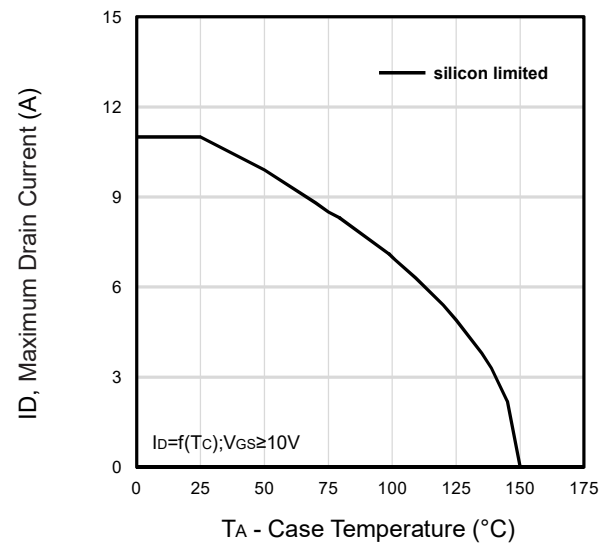


Fig12. Maximum Drain Current Vs. Case Temperature

Typical Characteristics

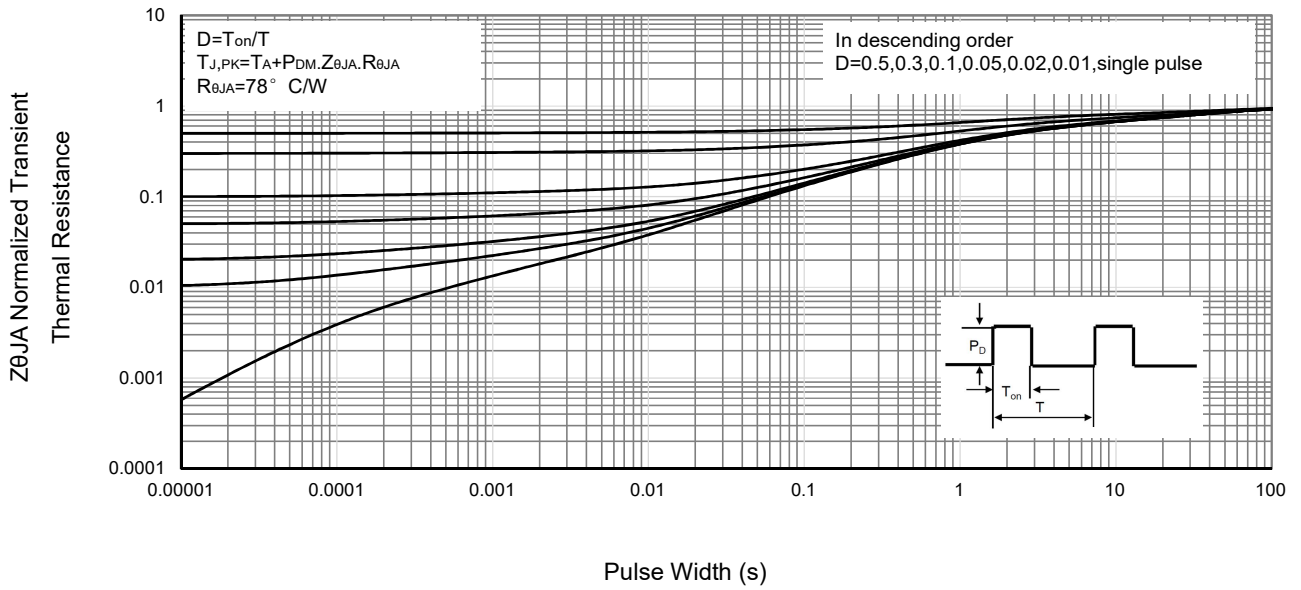


Fig13 . Normalized Maximum Transient Thermal Impedance

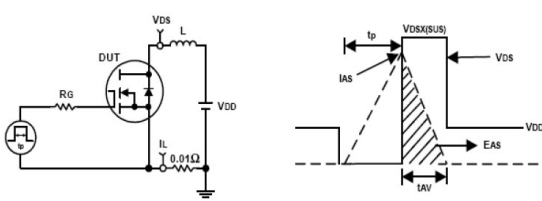


Fig14. Unclamped Inductive Test Circuit and waveforms

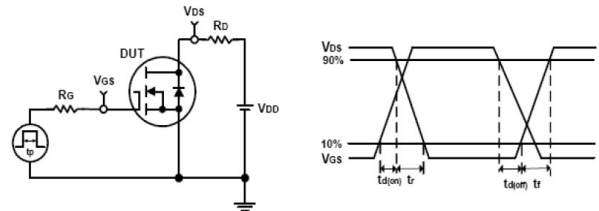


Fig15. Switching Time Test Circuit and waveforms