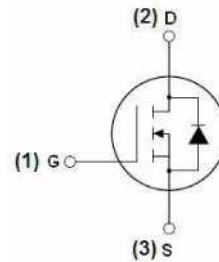


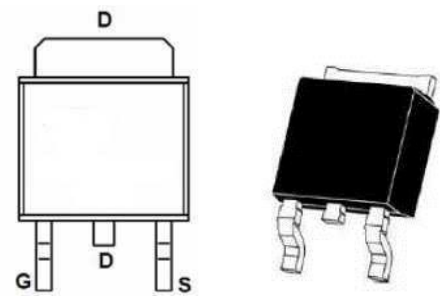
**60V ( $V_{DS}$ ) / 25A ( $I_D$ ) N-Channel Enhancement-Mode MOSFET**



Schematic diagram

## General Features

- $V_{DS}=60V$  ,  $I_D=25A$   $R_{DS(ON)} < 32m\Omega$  @  $V_{GS}=10V$
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high EAS
- Excellent package for good heat dissipation



TO-252

## Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	25	A
		$T_C = 100^\circ\text{C}$	
Drain Current –Pulsed <sup>a</sup>	$I_{DM}$	60	A
Power Dissipation	$P_D$	45	W
Derating factor		0.3	W/ $^\circ\text{C}$
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^\circ\text{C}$
Single pulse avalanche energy (Note 5)	EAS	72	mJ
Thermal Resistance, Junction-to-Ambient <sup>1</sup> (Note2)	$R_{\theta JA}$	3.3	$^\circ\text{C}/\text{W}$

**Absolute Maximum Ratings (TA=25°C unless otherwise noted)**

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	60	—	—	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=60V, V_{GS}=0V$	—	—	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20V, V_{DS}=0V$	—	—	$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.2	1.6	2.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 4.5 A$	—	27	32	m $\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS}=5V, I_D = 5A$	11	—	—	S
Diode Forward Voltage (Note3)	$V_{SD}$	$V_{GS}=0V, I_S=20A$	—	—	1.2	V
Continuous Source Current (Note2)	$I_S$		—	—	20	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ C, I_F = 20A$	—	35	—	nS
Reverse Recovery Charge	$Q_{rr}$	$di/dt = 100A/\mu s$ (Note3)	—	53	—	nC
Input Capacitance	$C_{iss}$	$V_{GS}=0V, V_{DS}=30V,$ $f=1.0MHz$	—	1500	—	pF
Output Capacitance	$C_{oss}$		—	60	—	
Reverse Transfer Capacitance	$C_{rss}$		—	25	—	
Total Gate Charge	$Q_g$	$V_{GS}=10V, V_{DS}=30V,$ $I_D=4.5A$	—	47	—	nC
Gate-Source Charge	$Q_{gs}$		—	6	—	
Gate-Drain Charge	$Q_{gd}$		—	14	—	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, R_L=6.7\Omega$ $R_G=3\Omega, V_{GS}=10V$	—	5	—	ns
Turn-on Rise Time	$t_r$		—	2.6	—	
Turn-off Delay Time	$t_{d(off)}$		—	16.1	—	
Turn-off Fall Time	$t_f$		—	2.3	—	
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

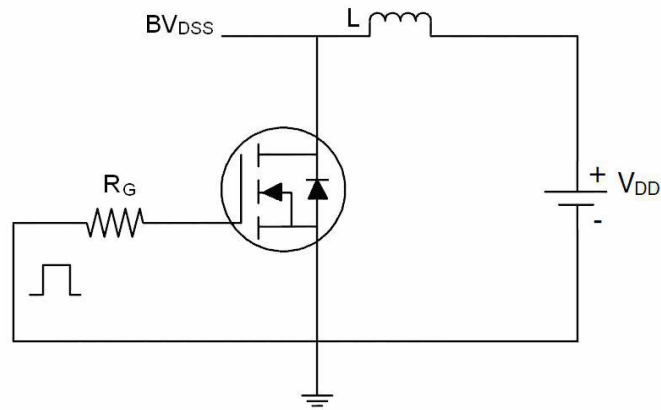
**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Pulse Test: Pulse Width  $\leq 300\mu \leq 10$  sec .
3. Surface Mounted on FR4 Board,s,t Duty Cycle  $\leq 2\%$ .
- 4.Guaranteed by design, not subject to production
5. EAS condition: $T_J=25, V_{DD}=30V, V_G=10V, L=0.5mH, R_g=25\Omega$

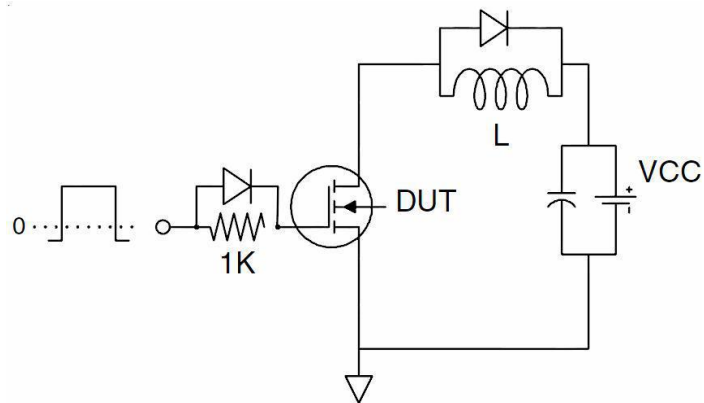


## Test Circuit

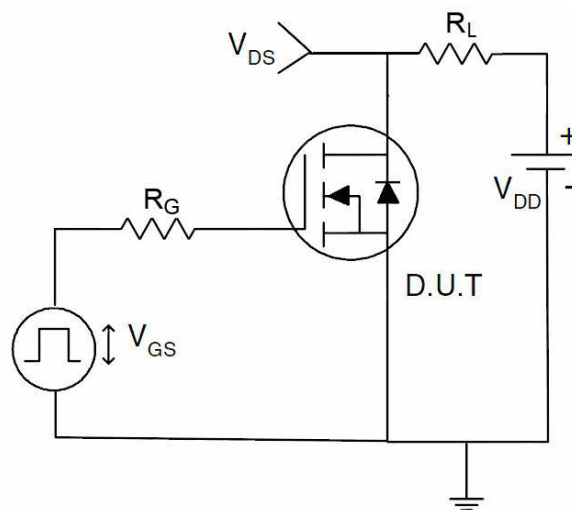
### 1) EAS test Circuit



### 2) Gate charge test Circuit



### 3) Switch Time Test Circuit

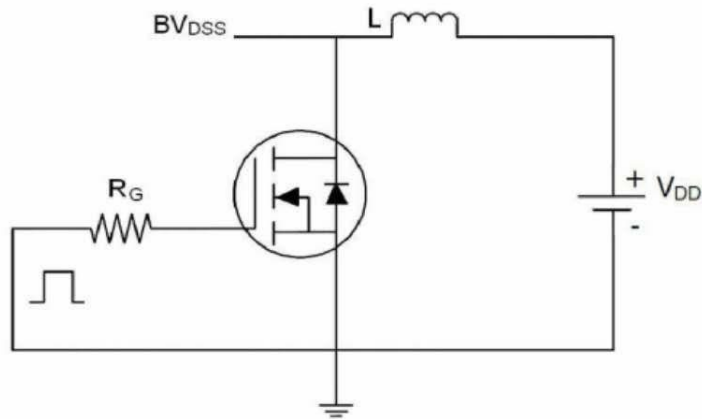




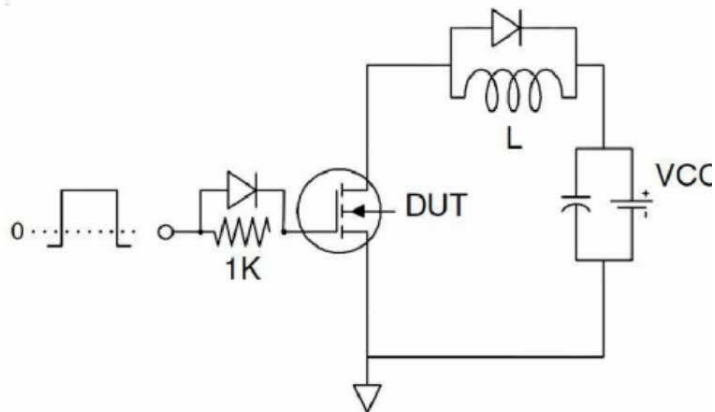
## Typical Electrical and Thermal Characteristics (Curves)

### Test Circuit

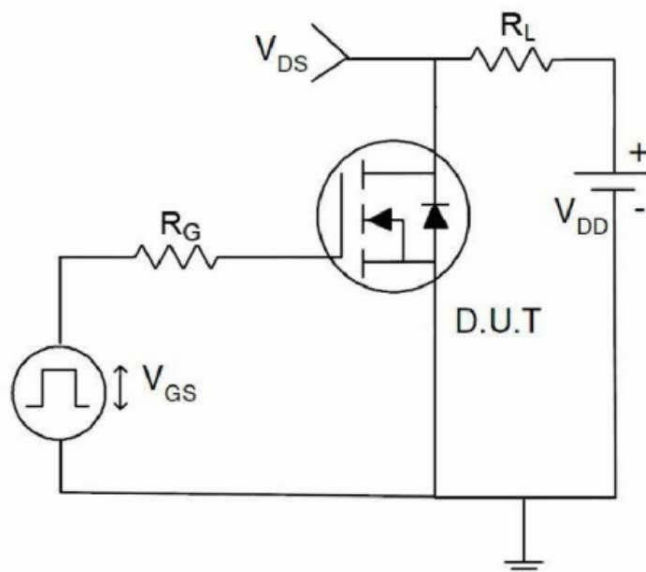
#### 1) EAS test Circuit



#### 2) Gate charge test Circuit



#### 3) Switch Time Test Circuit





60V ( $V_{DS}$ ) / 30A ( $I_D$ ) N-Channel Enhancement-Mode MOSFET

Typical Electrical and Thermal Characteristics (Curves)

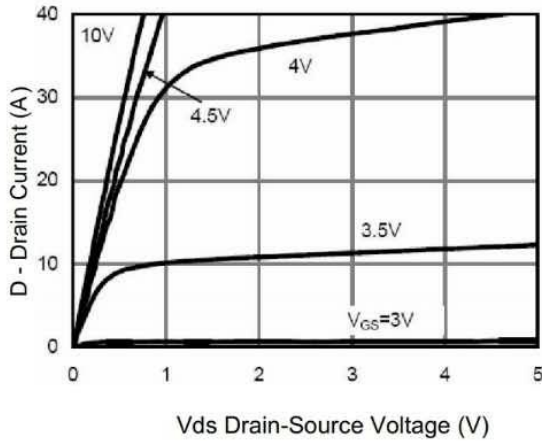


Figure 1 Output Characteristics

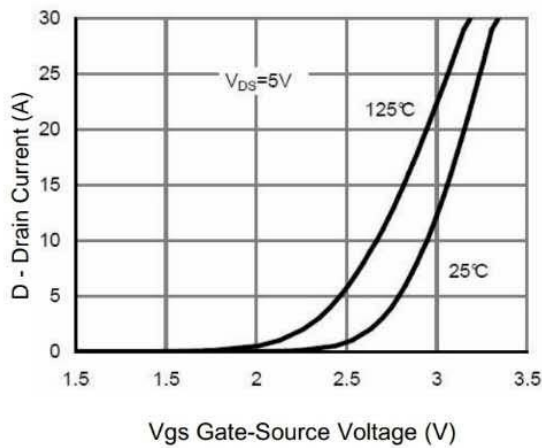


Figure 2 Transfer Characteristics

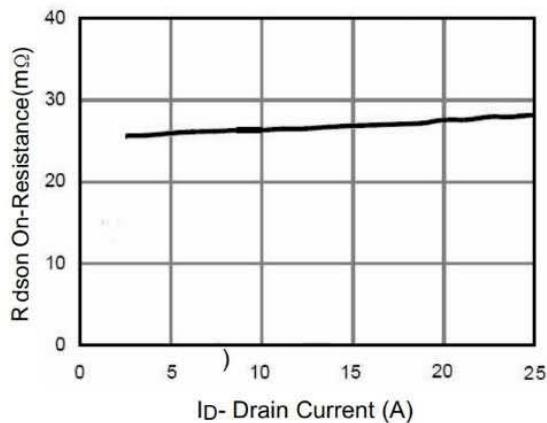


Figure 3  $R_{DS(on)}$ - Drain Current

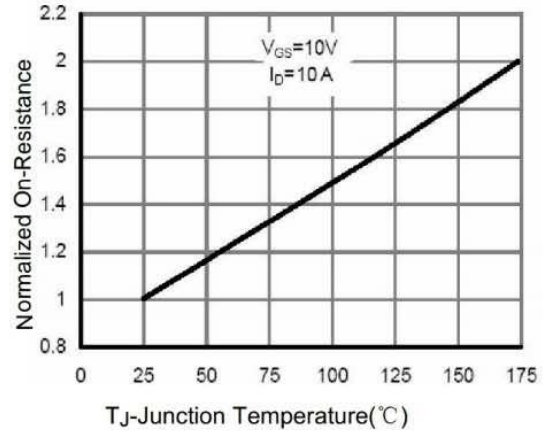


Figure 4  $R_{DS(on)}$ -Junction Temperature

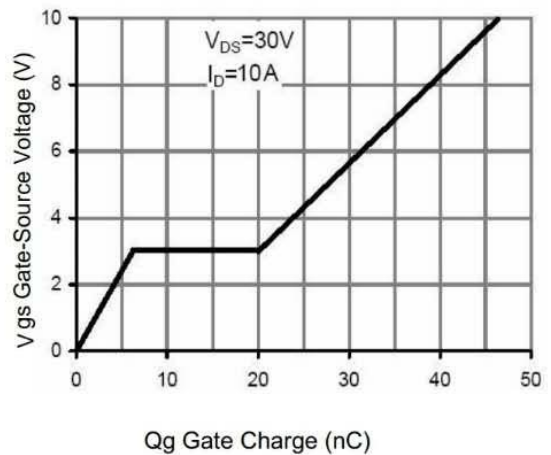


Figure 5 Gate Charge

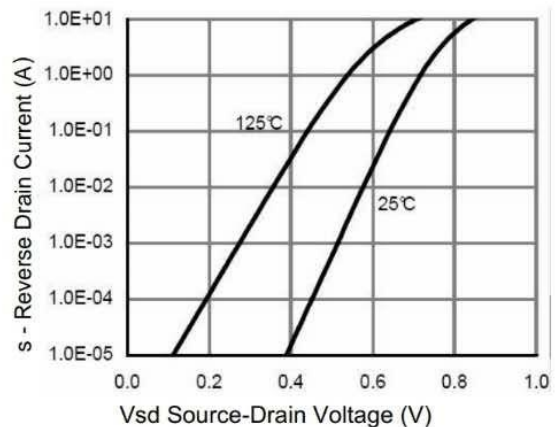


Figure 6 Source- Drain Diode Forward



60V ( $V_{DS}$ ) / 30A ( $I_D$ ) N-Channel Enhancement-Mode MOSFET

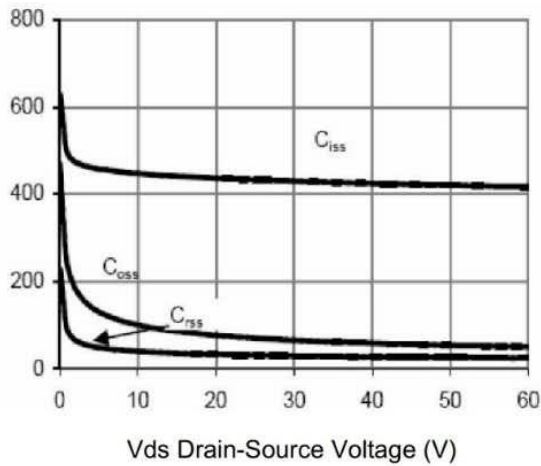


Figure 7 Capacitance vs  $V_{DS}$

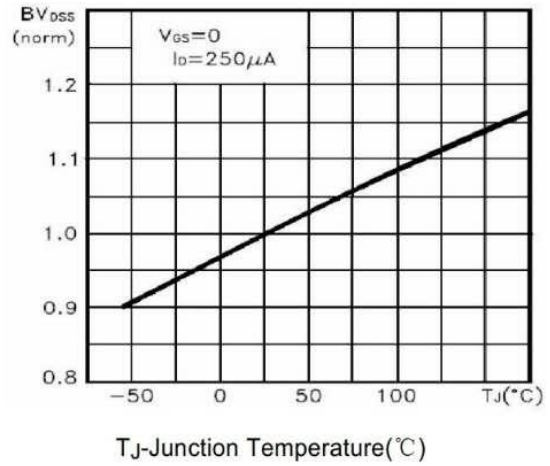


Figure 9  $BV_{DSS}$  vs Junction Temperature

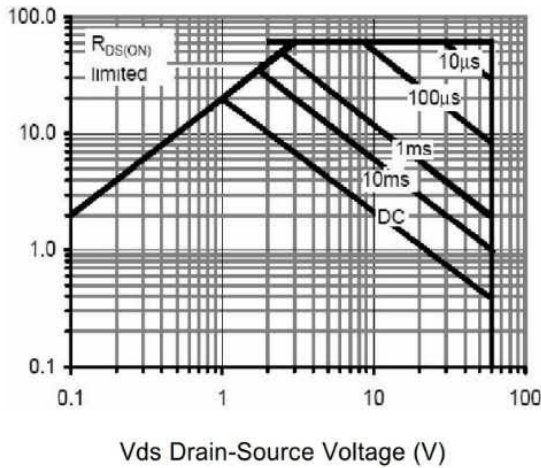


Figure 8 Safe Operation Area

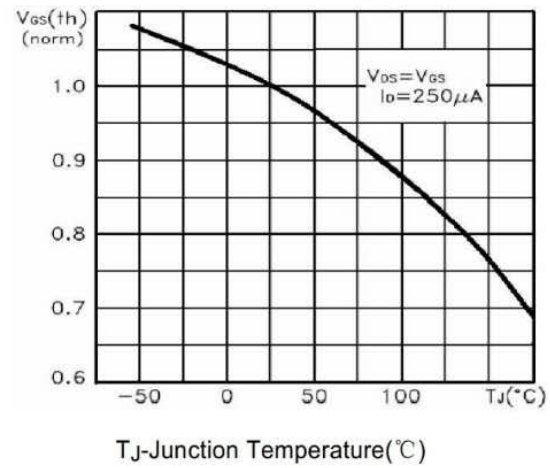


Figure 10  $V_{GS(th)}$  vs Junction Temperature

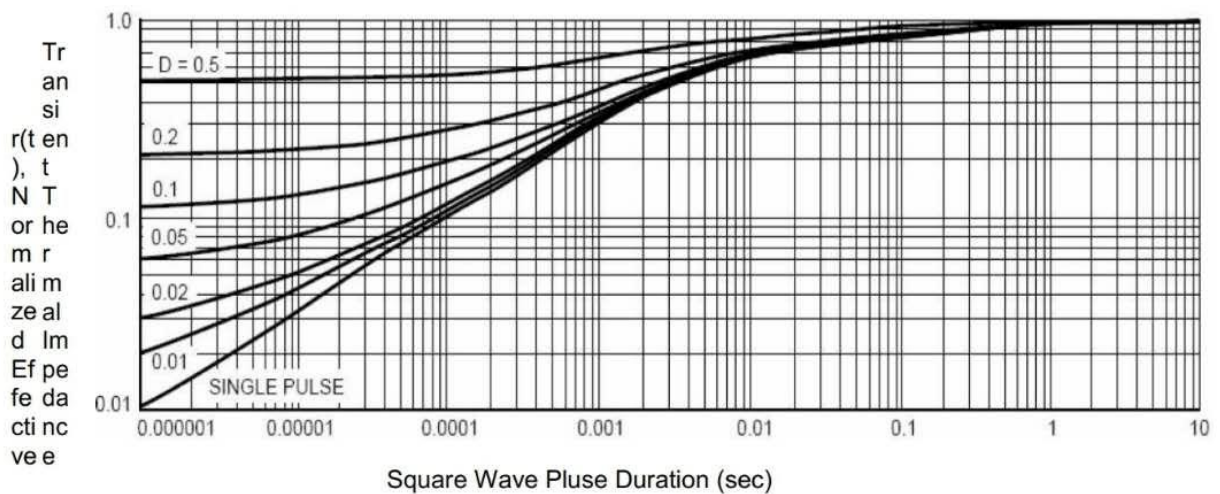
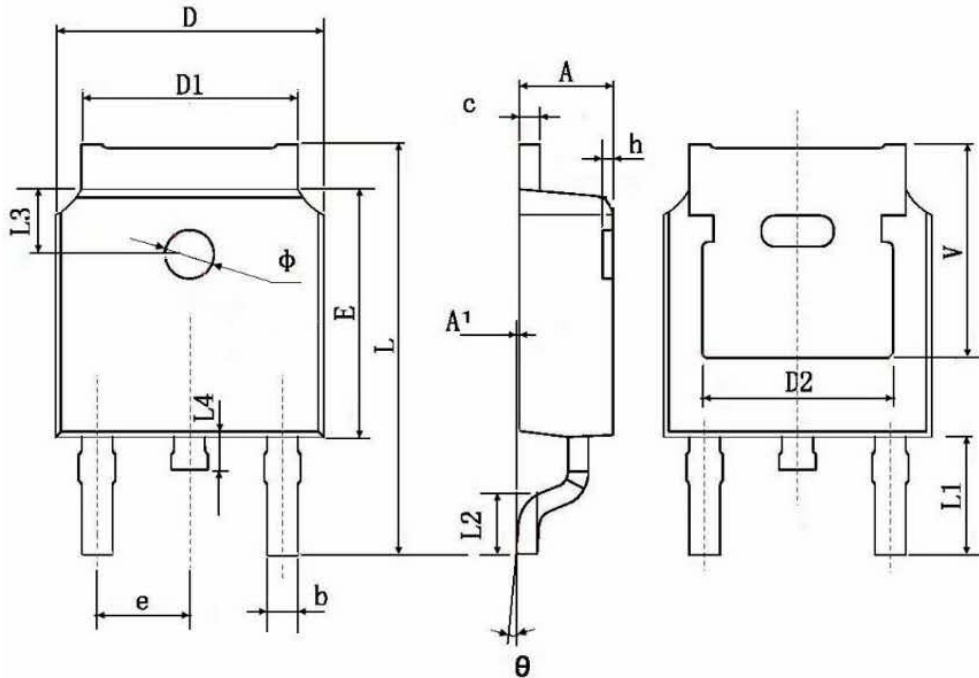


Figure 11 Normalized Maximum Transient Thermal Impedance



**60V (V<sub>DS</sub>) / 30A (I<sub>D</sub>) N-Channel Enhancement-Mode MOSFET**

**TO-252 Package Information**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	0.483 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
phi	1.100	1.300	0.043	0.051
theta	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	