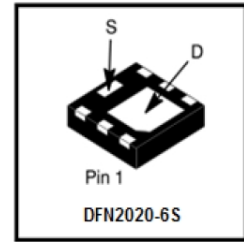


# LP1221DT2AG

## 12V P-Channel Enhancement MOSFET

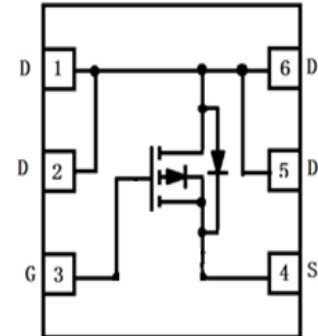
### 1. FEATURES

- $V_{DS} = -12V$ .  
 $R_{DS(ON)} \leq 21.5m\Omega$ ,  $V_{GS@-4.5V}$ .  
 $R_{DS(ON)} \leq 28m\Omega$ ,  $V_{GS@-2.5V}$ .  
 $R_{DS(ON)} \leq 48m\Omega$ ,  $V_{GS@-1.8V}$ .
- Low thermal impedance.
- Fast switching speed.
- We declare that the material of product are Halogen Free and compliance with RoHS requirements.



### 2. APPLICATIONS

- DC/DC Conversion
- Power Routing
- Load Switch



### 3. ORDERING INFORMATION

Device	Marking	Shipping
LP1221DT2AG	A12	4000/Tape&Reel

### 4. MAXIMUM RATINGS(Ta = 25°C unless otherwise stated)

Parameter		Symbol	Limits	Unit
Drain-to-Source Voltage		$V_{DS}$	-12	V
Gate-to-Source Voltage		$V_{GS}$	$\pm 12$	V
Continuous Drain Current(Note 1)	$T_A = 25^\circ C$	$I_D$	-8	A
	$T_A = 70^\circ C$		-7	
Continuous Drain Current(Note 3)	$T_A = 25^\circ C$		-5	
Pulsed Drain Current (Note 2)		$I_{DM}$	-32	A
Pulsed Drain Current (Note 3)			-20	
Power Dissipation(Note 1)	$T_A = 25^\circ C$	PD	1.9	W
	$T_A = 70^\circ C$		1.4	
Power Dissipation(Note 3)	$T_A = 25^\circ C$		1	
Operating Junction and Storage Temperature Range		$T_J, T_{STG}$	-55 ~ +150	$^\circ C$

### 5. THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Unit
Thermal Resistance, Junction-to-Ambient(Note 1)	$R_{\theta JA}$	65	$^\circ C/W$
Thermal Resistance, Junction-to-Ambient(Note 3)	$R_{\theta JA}$	127	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	12	

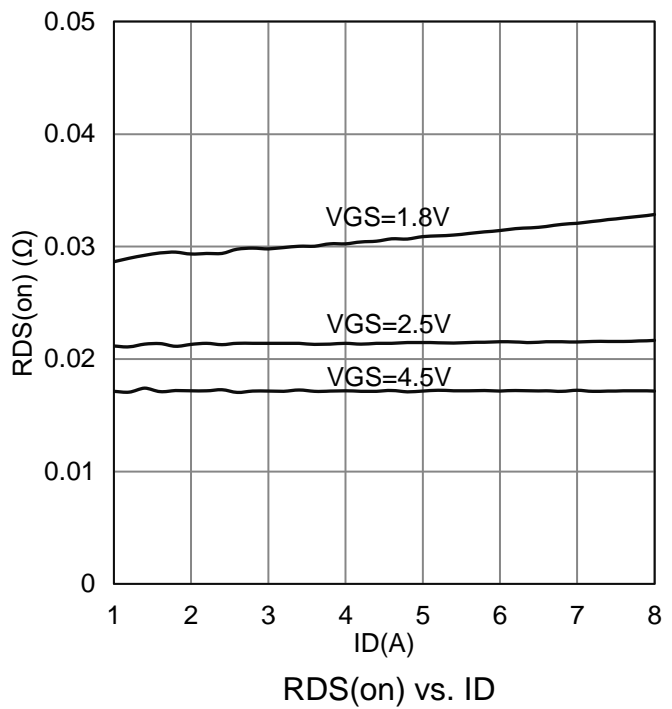
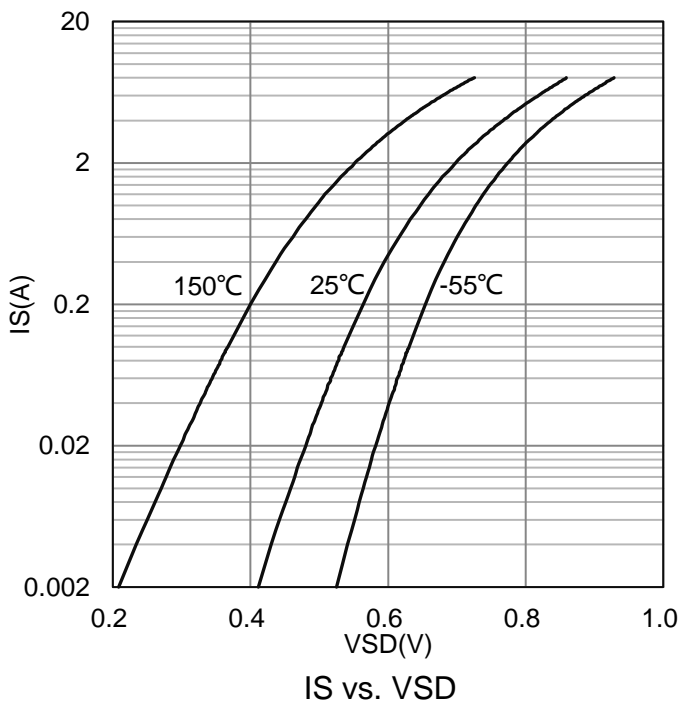
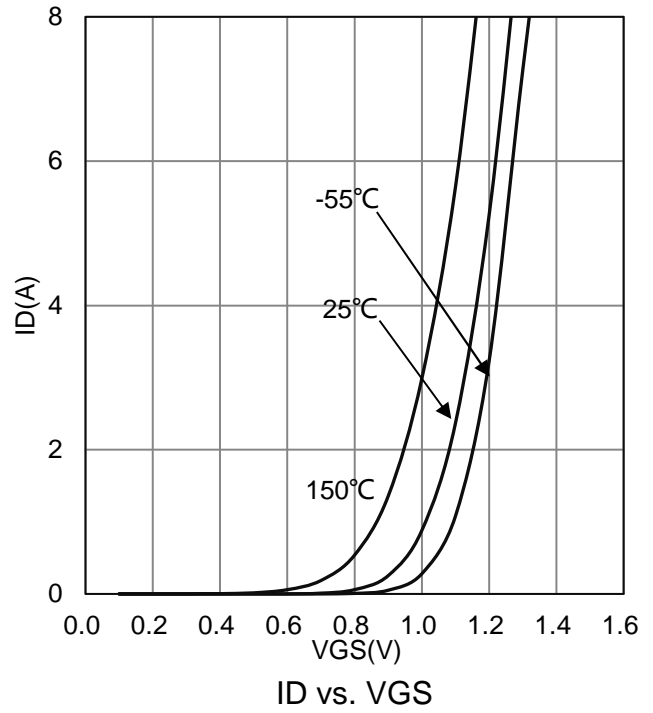
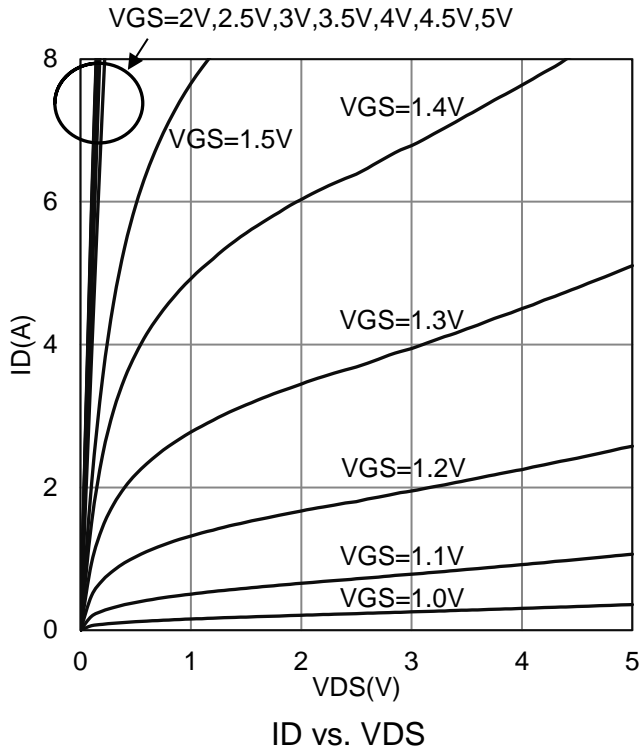
1. Surface mounted on 1.5 x 1.5 FR4 board using 1 sq in pad, 2 oz Cu.
2. Pulse width limited by maximum junction temperature.
3. Surface mounted on FR4 board using the minimum recommended pad size.

## 6. ELECTRICAL CHARACTERISTICS

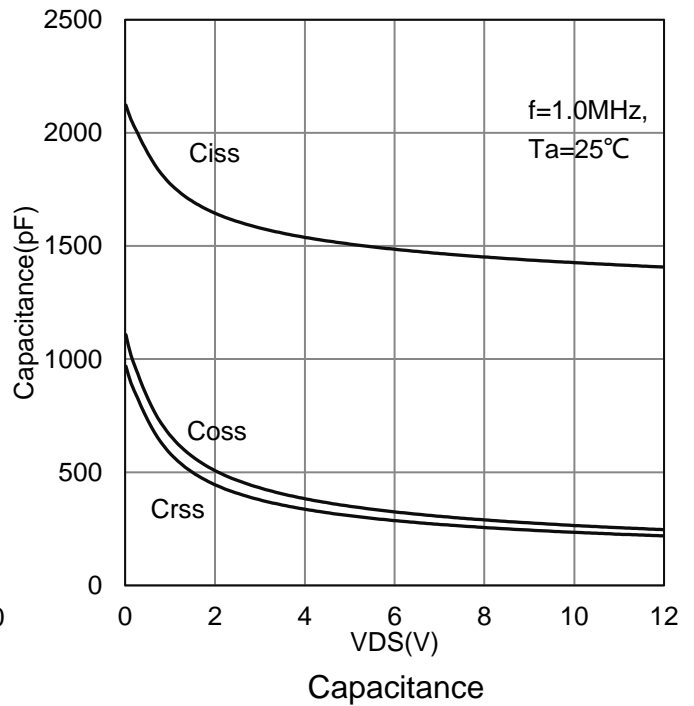
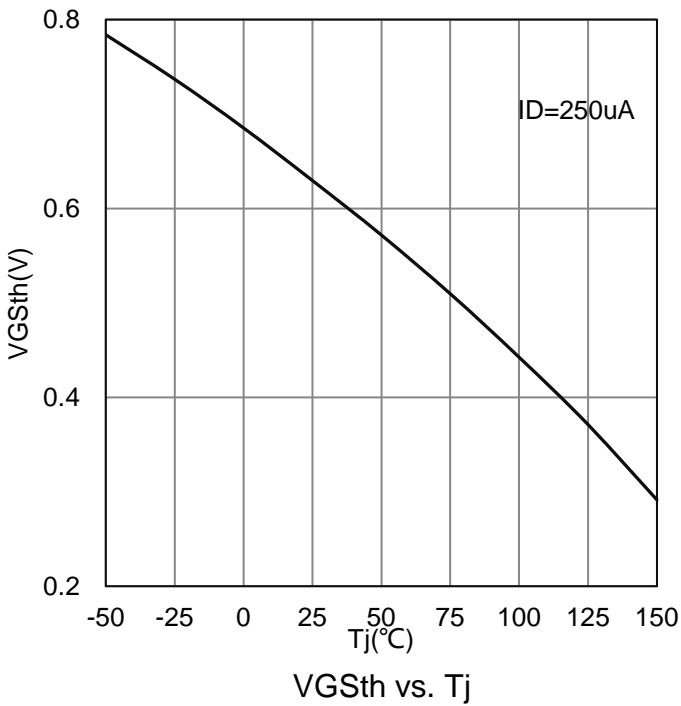
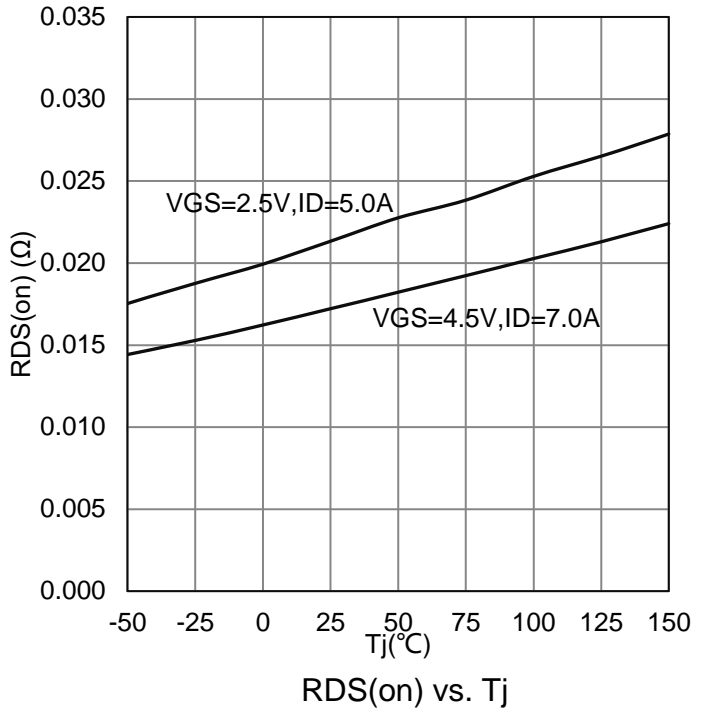
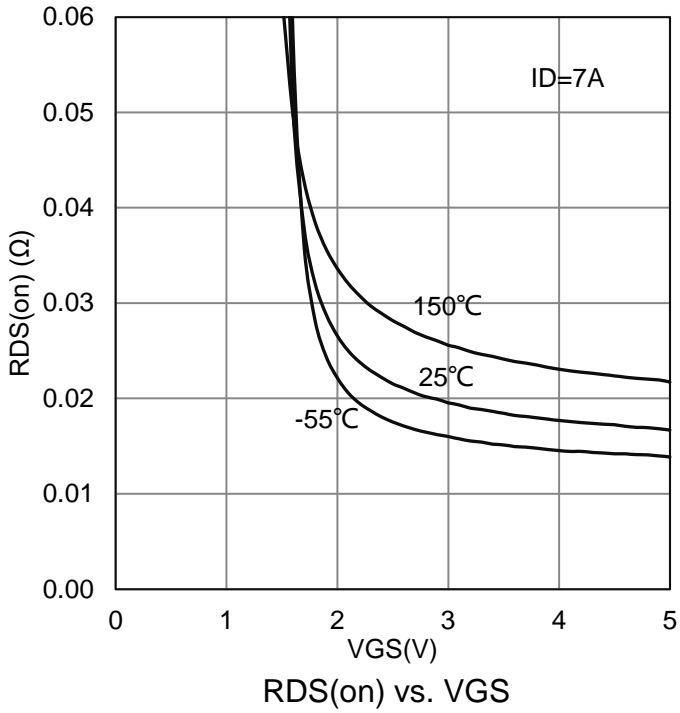
Characteristic	Symbol	Min.	Typ.	Max.	Unit	
<b>Static</b>						
Drain–Source Breakdown Voltage (VGS = 0 V , ID = -250 uA)	V(BR)DSS	-12	-	-	V	
Gate-Source Threshold Voltage (VDS = VGS , ID = -250 uA)	VGS(th)	-0.5	-	-1	V	
Gate-Body Leakage (VDS = 0 V, VGS = ± 12 V)	IGSS	-	-	±10	μA	
Zero Gate Voltage Drain Current (VDS = -12 V, VGS = 0 V)	IDSS	-	-	-1	μA	
Drain-Source On-Resistance(Note 4) (VGS = -4.5 V, ID = -7 A) (VGS = -2.5 V, ID = -5 A) (VGS = -1.8 V, ID = -2 A)	RDS(on)	-	16 19 35	21.5 28 48	mΩ	
Diode Forward Voltage(Note 4) (IS = -1 A, VGS = 0 V)	VSD	-	-	-1.5	V	
<b>Dynamic</b>						
Total Gate Charge	(VDS = -15 V, VGS = -4.5 V, ID = -4 A)	Qg	-	16.5	-	nC
Gate-Source Charge		Qgs	-	2.3	-	
Gate-Drain Charge		Qgd	-	6	-	
Input Capacitance	(VDS = -15 V, VGS = 0 V, f = 1 MHz)	Ciss	-	1400	-	pF
Output Capacitance		Coss	-	232	-	
Reverse Transfer Capacitance		Crss	-	207	-	

4.Pulse test: PW ≤ 300us duty cycle ≤ 2%.

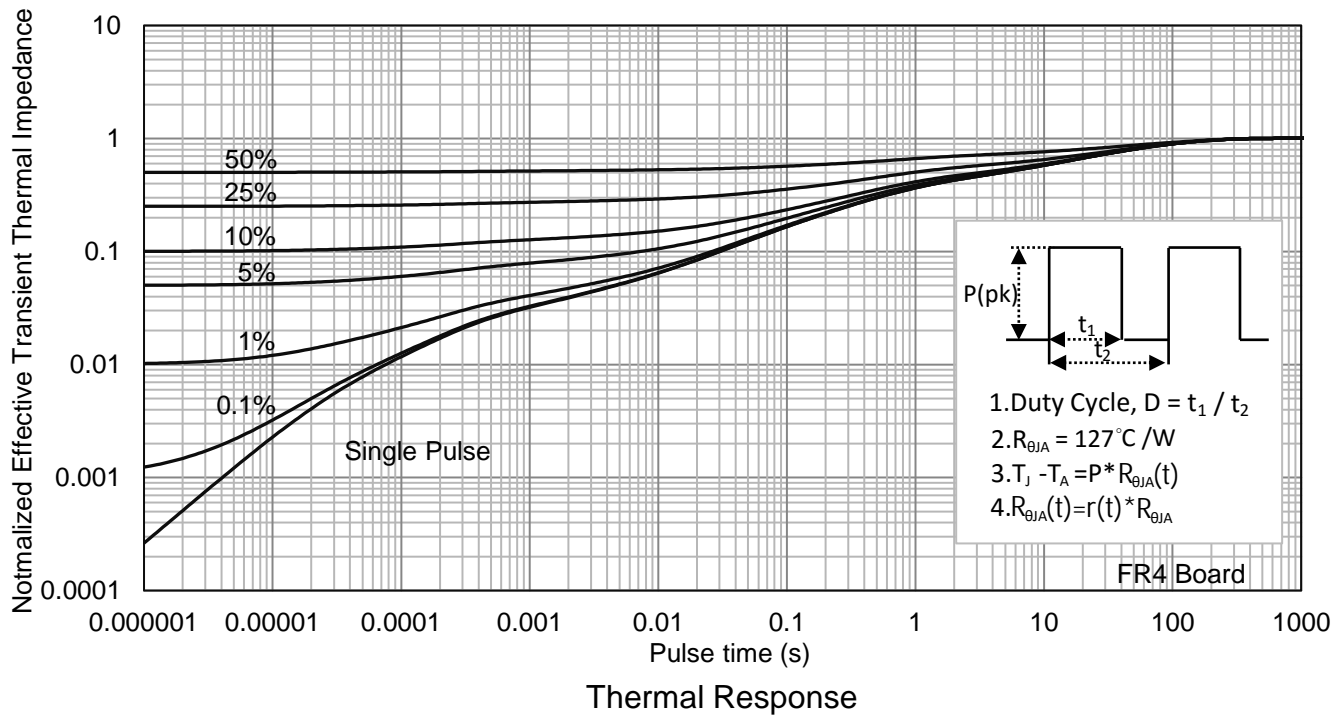
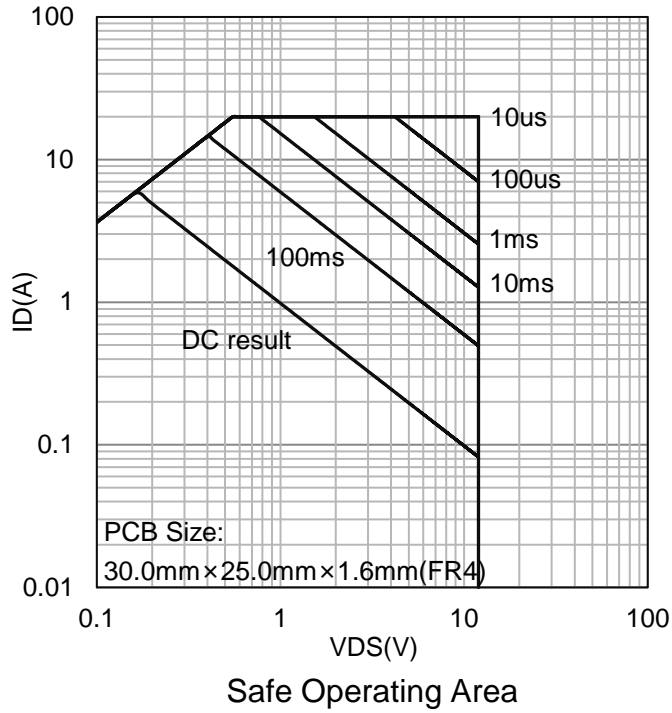
**7. ELECTRICAL CHARACTERISTICS CURVES**



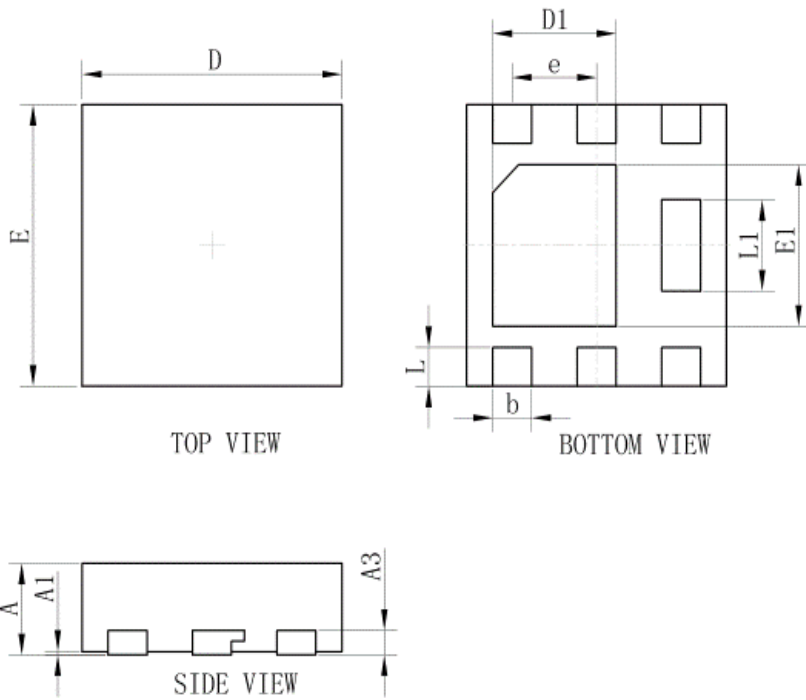
**7. ELECTRICAL CHARACTERISTICS CURVES(Con.)**



**7. ELECTRICAL CHARACTERISTICS CURVES(Con.)**

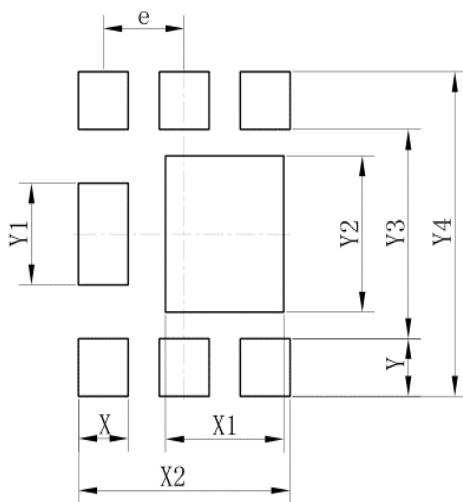


### 8. OUTLINE AND DIMENSIONS



DFN2020-6S			
DIM	MIN	NOR	MAX
A	0.60	0.65	0.70
A1	0.01	0.03	0.05
b	0.25	0.30	0.35
D	1.95	2.00	2.05
E	1.95	2.00	2.05
e	0.65TYP.		
L	0.23	0.28	0.33
L1	0.60	0.65	0.70
D1	0.90	0.95	1.00
E1	1.10	1.15	1.20
A3	0.152REF		
All Dimensions in mm			

### 9. SOLDERING FOOTPRINT



DFN2020-6S	
Dim	(mm)
X	0.40
X1	0.95
X2	1.70
e	0.65
Y	0.43
Y1	0.75
Y2	1.15
Y3	1.54
Y4	2.39

## **DISCLAIMER**

- Curve guarantee in the specification. The curve of test items with electric parameter is used as quality guarantee. The curve of test items without electric parameter is used as reference only.
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