NCE N-Channel Enhancement Mode Power MOSFET

Description

The NCE6050IA uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

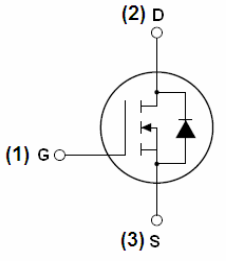
- V_{DS} =60V,I_D =50A
  $R_{DS(ON)}$ <20mΩ @ V_{GS}=10V
  $R_{DS(ON)}$ <25mΩ @ V_{GS}=4.5V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

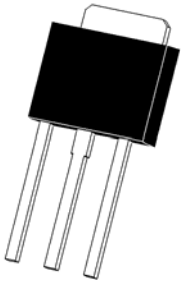
100% UIS TESTED!

100% ΔVds TESTED!



Schematic diagram

Marking and pin assignment



TO-251 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE6050IA	NCE6050IA	TO-251	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	50	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	35.4	A
Pulsed Drain Current	I_{DM}	200	A
Maximum Power Dissipation	P_D	85	W
Derating factor		0.56	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	300	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case (Note 2)	$R_{\theta JC}$	1.8	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

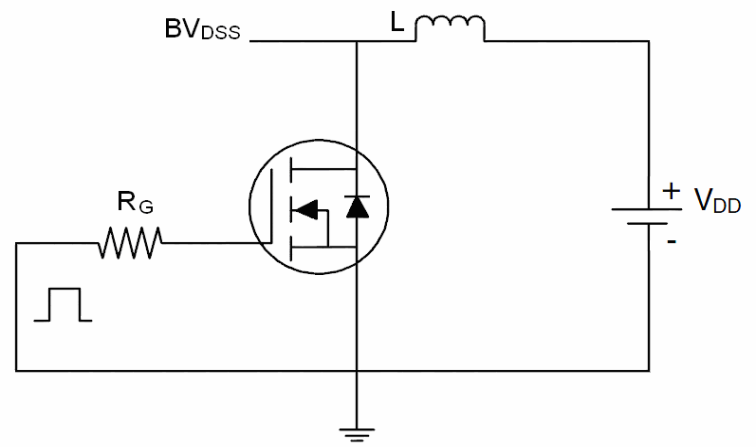
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.0	-	2.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A	-	13	20	mΩ
		V_{GS}=4.5V, I_D=20A	-	17	25	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=20A	18	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=30V,V_{GS}=0V, F=1.0MHz	-	2050	-	PF
Output Capacitance	C_{oss}		-	158	-	PF
Reverse Transfer Capacitance	C_{rss}		-	120	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=30V, R_L=6.7Ω V_{GS}=10V,R_G=3Ω	-	7.4	-	nS
Turn-on Rise Time	t_r		-	5.1	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	28.2	-	nS
Turn-Off Fall Time	t_f		-	5.5	-	nS
Total Gate Charge	Q_g	V_{DS}=30V,I_D=20A, V_{GS}=10V	-	50		nC
Gate-Source Charge	Q_{gs}		-	6		nC
Gate-Drain Charge	Q_{gd}		-	15		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=20A	-		1.2	V
Diode Forward Current (Note 2)	I_S		-	-	50	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF =20A di/dt = 100A/μs (Note3)	-	28	-	nS
Reverse Recovery Charge	Qrr		-	40	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

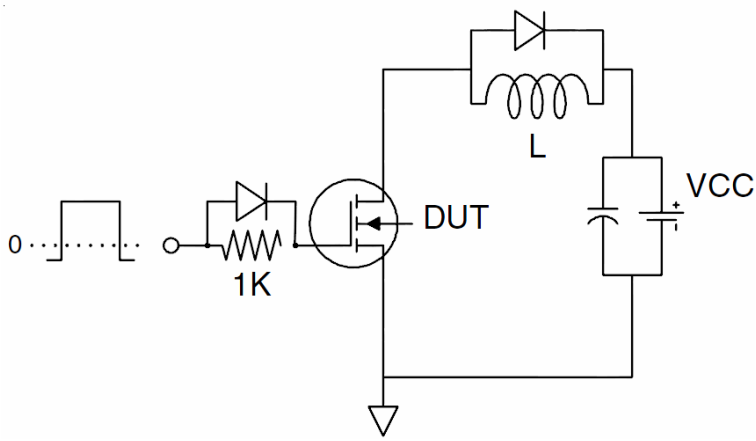
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition : Tj=25℃,VDD=30V,VG=10V,L=0.5mH,Rg=25Ω

Test Circuit

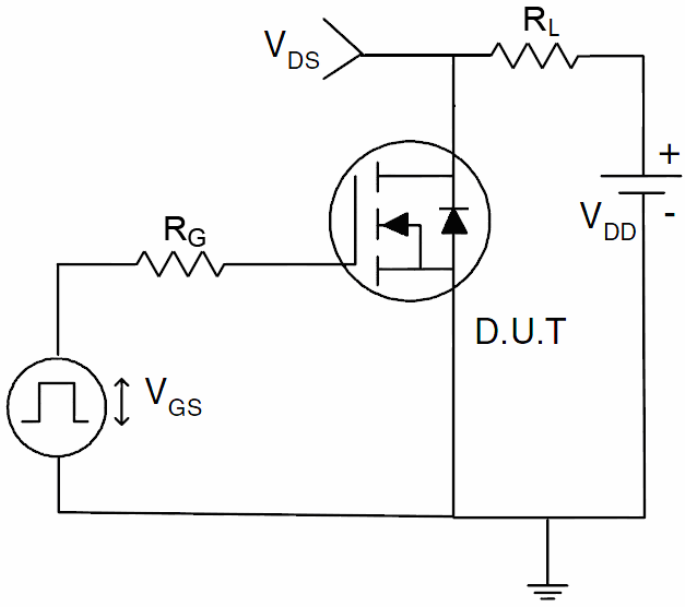
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

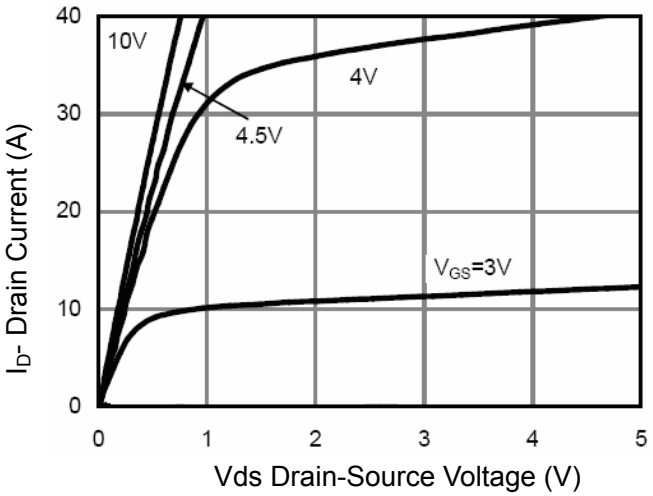


Figure 1 Output Characteristics

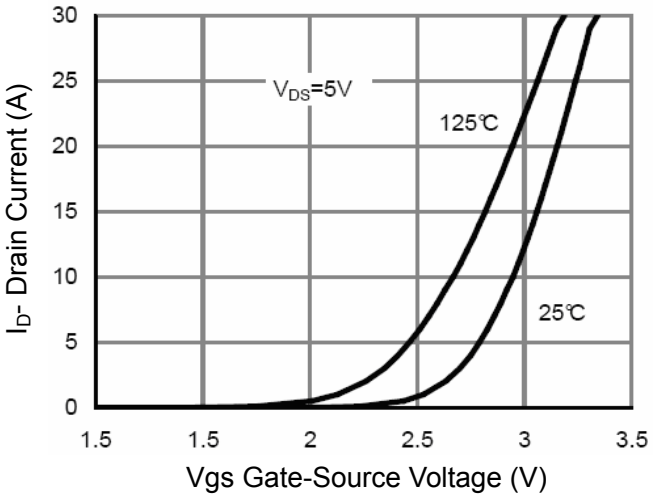


Figure 2 Transfer Characteristics

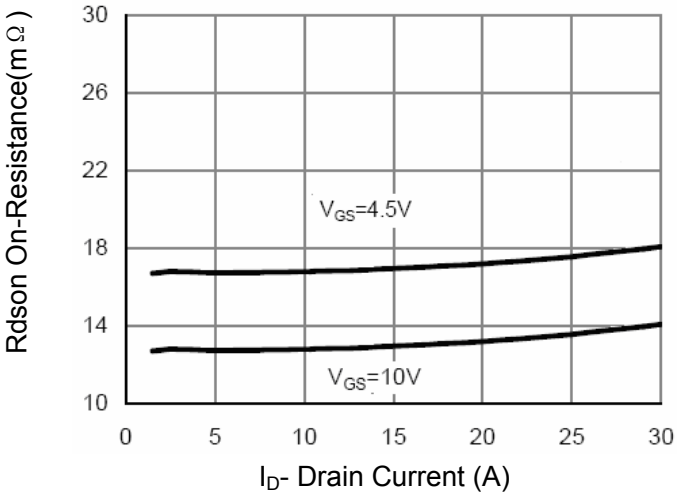


Figure 3 Rdson- Drain Current

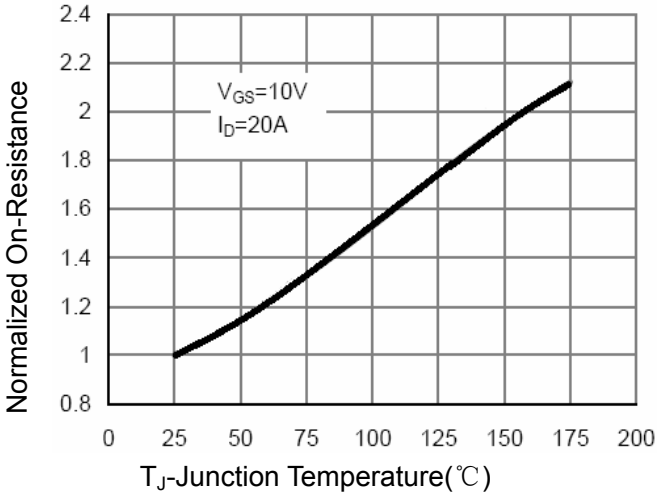


Figure 4 Rdson-Junction Temperature

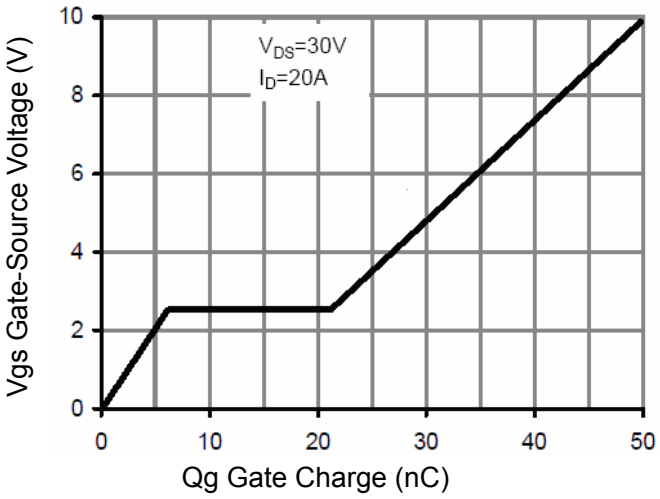


Figure 5 Gate Charge

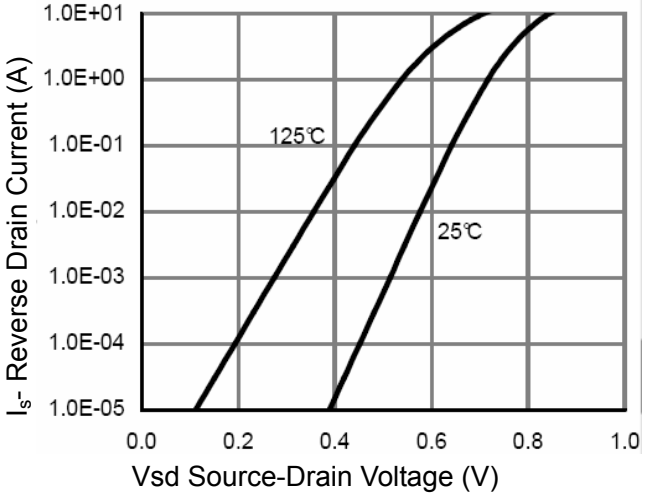


Figure 6 Source- Drain Diode Forward

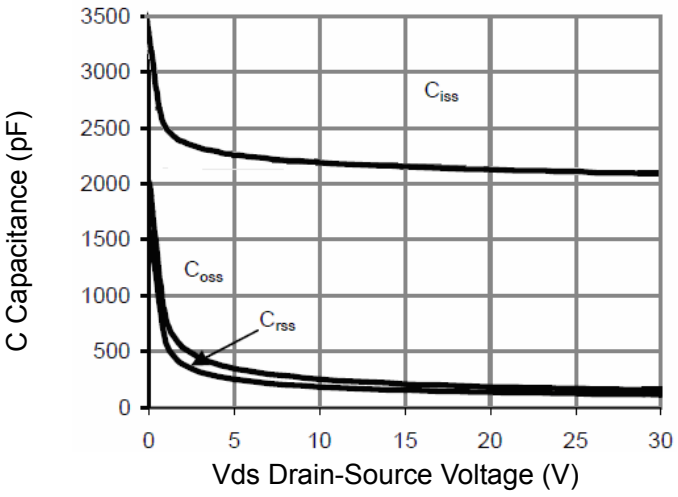


Figure 7 Capacitance vs Vds

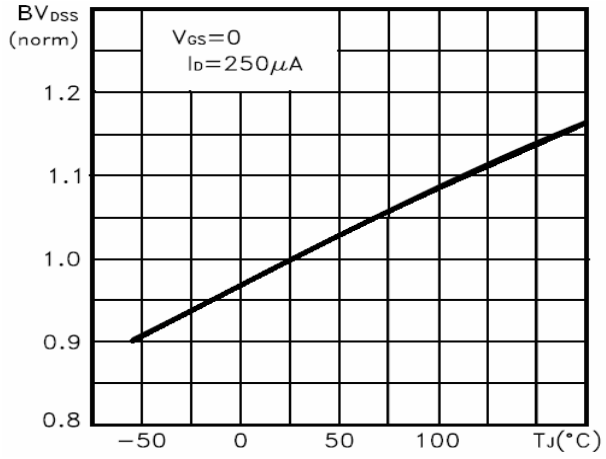


Figure 9 BV_{DSS} vs Junction Temperature

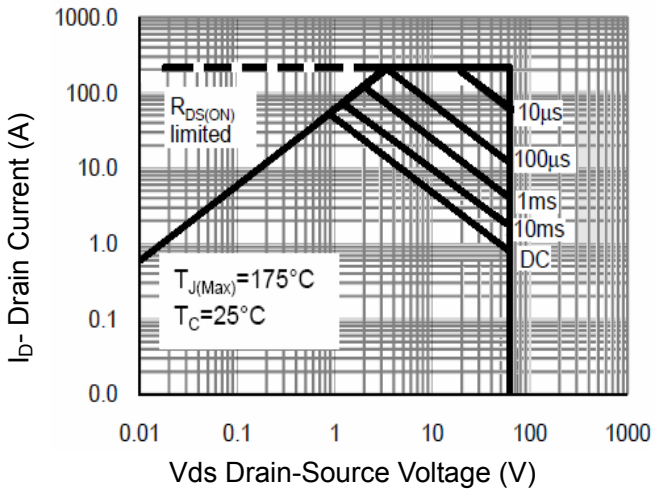


Figure 8 Safe Operation Area

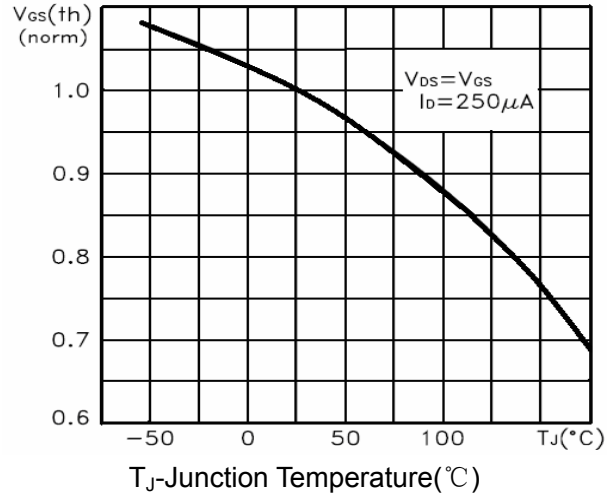


Figure 10 $V_{GS(th)}$ vs Junction Temperature

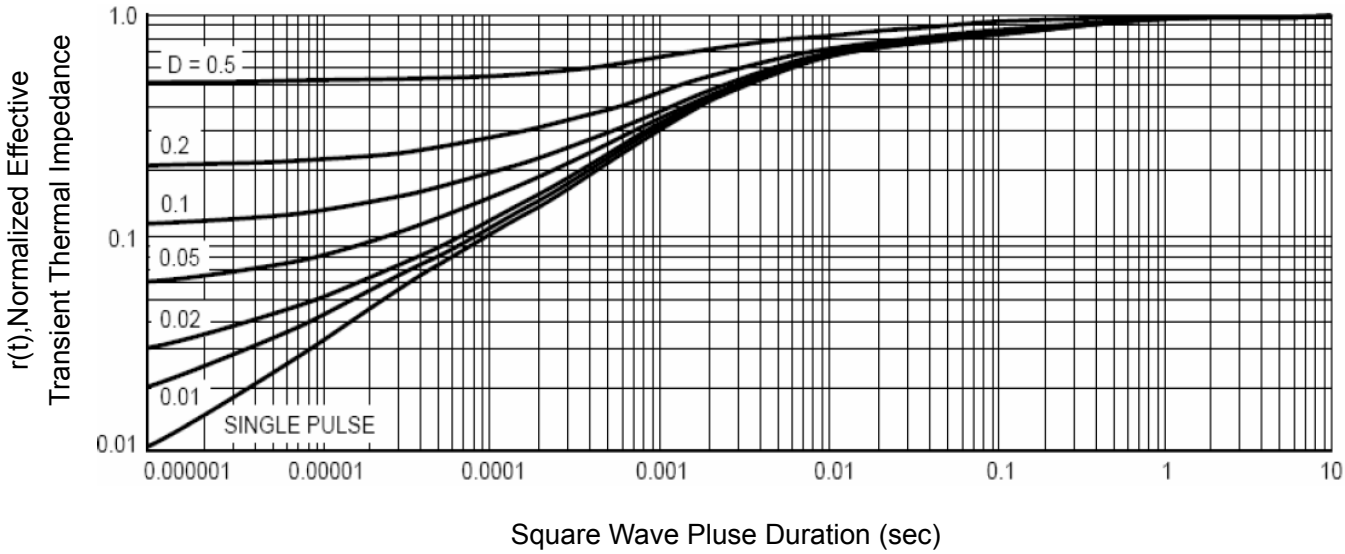
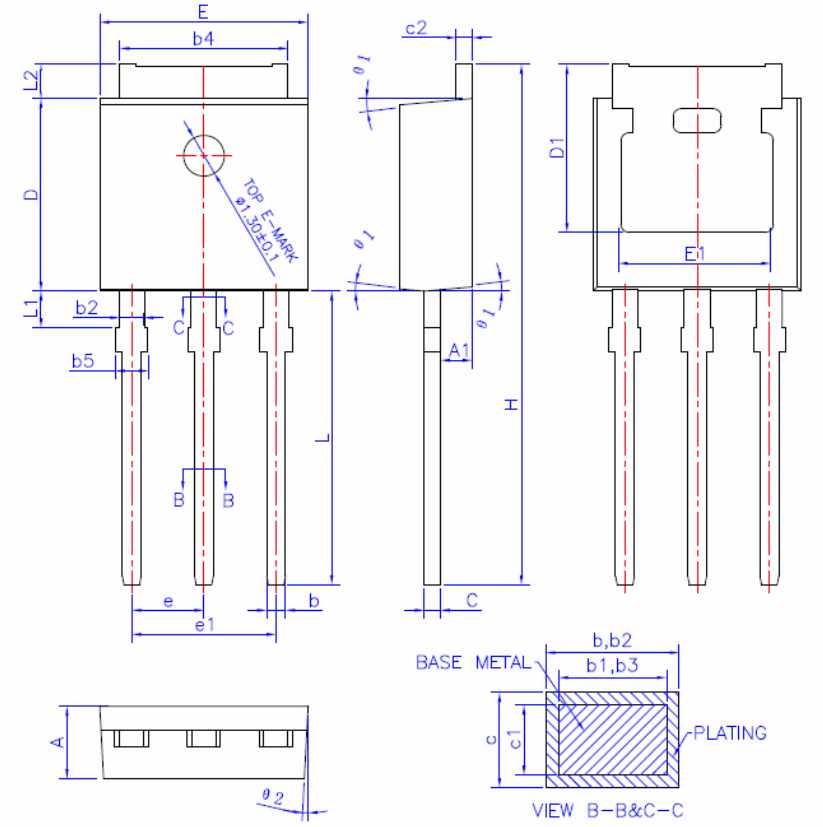


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-251 Package Information



COMMON DIMENSIONS
(UNITS OF MEASURE =MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	2.20	2.30	2.35
A1	0.90	1.01	1.10
b	0.56	---	0.69
b1	0.55	0.60	0.65
b2	0.77	---	0.90
b3	0.76	0.81	0.86
b4	5.23	5.33	5.43
b5	---	---	1.05
c	0.46	---	0.59
c1	0.45	0.51	0.55
c2	0.46	---	0.59
D	6.00	6.10	6.20
D1	5.20	---	---
E	6.50	6.60	6.70
E1	4.60	4.83	5.00
e	2.24	2.29	2.34
e1	4.47	4.57	4.67
H	16.18	16.48	16.78
L	9.00	9.30	9.60
L1	0.95	1.16	1.35
L2	0.90	1.08	1.25
θ1	3°	5°	7°
θ2	1°	3°	5°

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