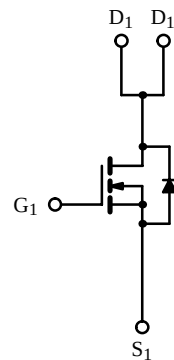
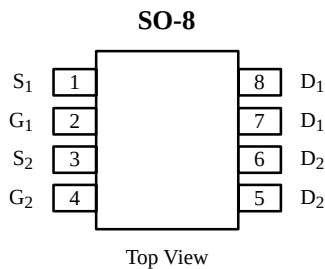


Dual N- and P-Channel 2.5-V (G-S) Rated MOSFET

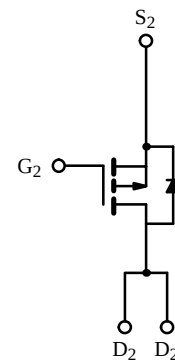
Product Summary

	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.03 @ $V_{GS} = 4.5$ V	± 6
		0.04 @ $V_{GS} = 2.5$ V	± 5.2
P-Channel	-12	0.05 @ $V_{GS} = -4.5$ V	± 5
		0.074 @ $V_{GS} = -2.5$ V	± 4.1

2.5-V Rated



N-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V _{DS}	20	−12	V
Gate-Source Voltage		V _{GS}	± 8	± 8	
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25 °C	I _D	± 6	± 5	A
	T _A = 70 °C		± 4.8	± 4.0	
Pulsed Drain Current		I _{DM}	± 20	± 20	
Continuous Source Current (Diode Conduction) ^a		I _S	1.7	−1.7	
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	2.0		W
	T _A = 70 °C		1.3		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	−55 to 150		°C

Thermal Resistance Ratings

Parameter	Symbol	N- or P- Channel	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70161.

Si9529DY

Specifications (T_J = 25 °C Unless Otherwise Noted)

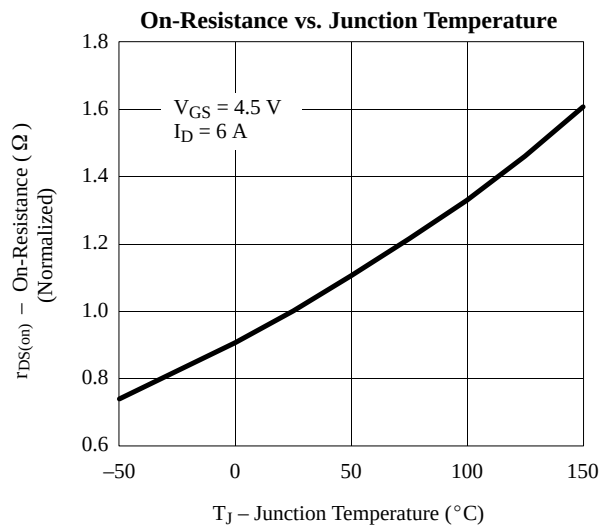
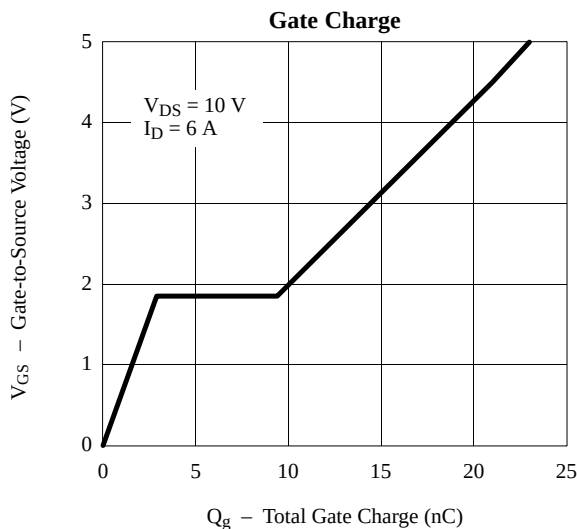
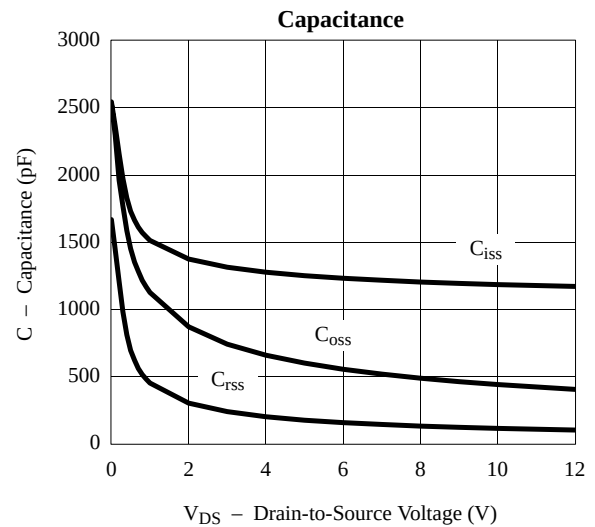
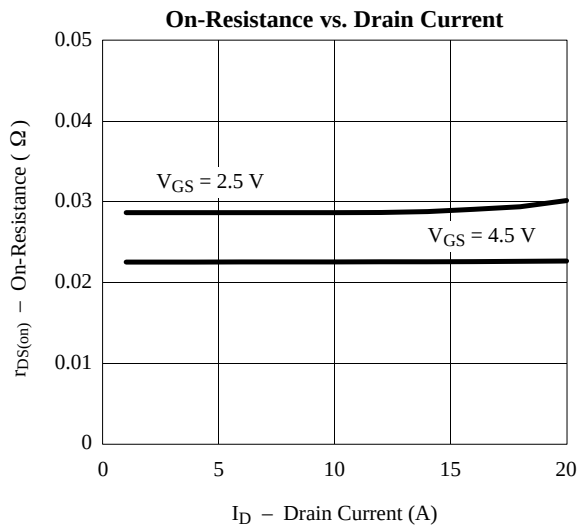
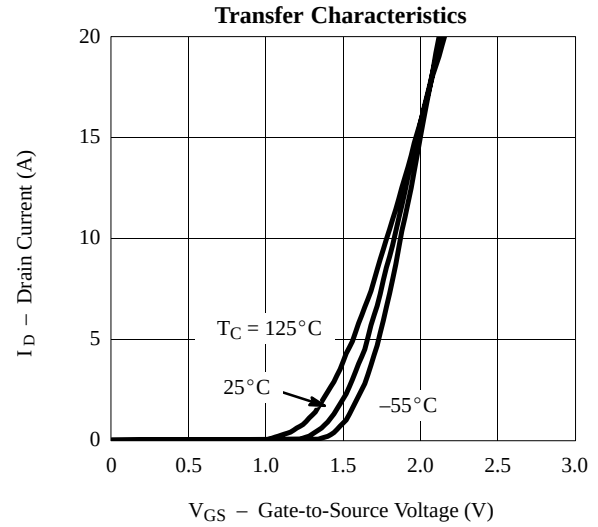
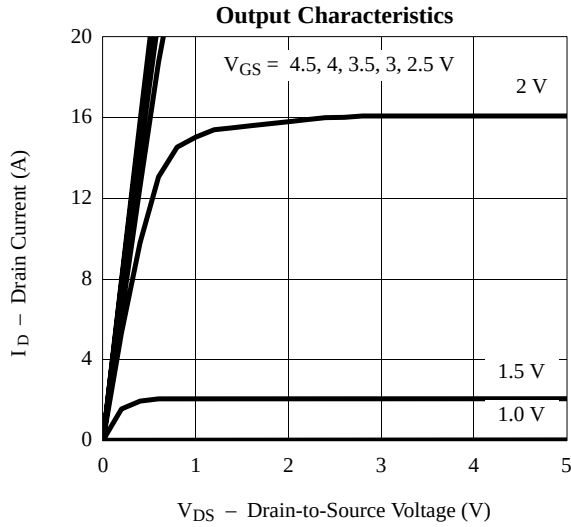
Parameter	Symbol	Test Condition		Min	Typ ^a	Max	Unit	
Static								
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	0.6			V	
		V _{DS} = V _{GS} , I _D = −250 μA	P-Ch	−0.6				
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±8 V	N-Ch			± 100	nA	
			P-Ch			± 100		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	N-Ch			1	μA	
		V _{DS} = −12 V, V _{GS} = 0 V	P-Ch			−1		
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 55°C	N-Ch			5		
		V _{DS} = −12 V, V _{GS} = 0 V, T _J = 55°C	P-Ch			−5		
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	N-Ch	20			A	
		V _{DS} ≤ −5 V, V _{GS} = −4.5 V	P-Ch	−20				
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 6 A	N-Ch		0.023	0.03	Ω	
		V _{GS} = −4.5 V, I _D = −5 A	P-Ch		0.039	0.05		
		V _{GS} = 2.5 V, I _D = 5.2 A	N-Ch		0.028	0.04		
		V _{GS} = −2.5 V, I _D = −4.1 A	P-Ch		0.051	0.074		
Forward Transconductance ^b	g _{fs}	V _{DS} = 10 V, I _D = 6 A	N-Ch		24		S	
		V _{DS} = −9 V, I _D = −5 A	P-Ch		16			
Diode Forward Voltage ^b	V _{SD}	I _S = 1.7 A, V _{GS} = 0 V	N-Ch		0.75	1.2	V	
		I _S = −1.7 A, V _{GS} = 0 V	P-Ch		−0.75	−1.2		
Dynamic ^a								
Total Gate Charge	Q _g	N-Channel V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 6 A P-Channel V _{DS} = −6 V, V _{GS} = −4.5 V, I _D = −5A	N-Ch		21	40	nC	
Gate-Source Charge	Q _{gs}		P-Ch		21	40		
			N-Ch		2.9			
			P-Ch		3			
Gate-Drain Charge	Q _{gd}	N-Ch		6.5				
		P-Ch		6				
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 4.5 V, R _G = 6 Ω P-Channel V _{DD} = −10 V, R _L = 10 Ω I _D ≅ −1 A, V _{GEN} = −4.5 V, R _G = 6 Ω	N-Ch		30	60	ns	
Rise Time	t _r		P-Ch		20	40		
			N-Ch		70	140		
			P-Ch		40	80		
Turn-Off Delay Time	t _{d(off)}		N-Ch		70	140		
			P-Ch		100	200		
Fall Time	t _f		N-Ch		30	60		
			P-Ch		60	120		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 1.7 A, di/dt = 100 A/μs	N-Ch		70	100		
		I _F = −1.7 A, di/dt = 100 A/μs	P-Ch		67	100		

Notes

a. Guaranteed by design, not subject to production testing.

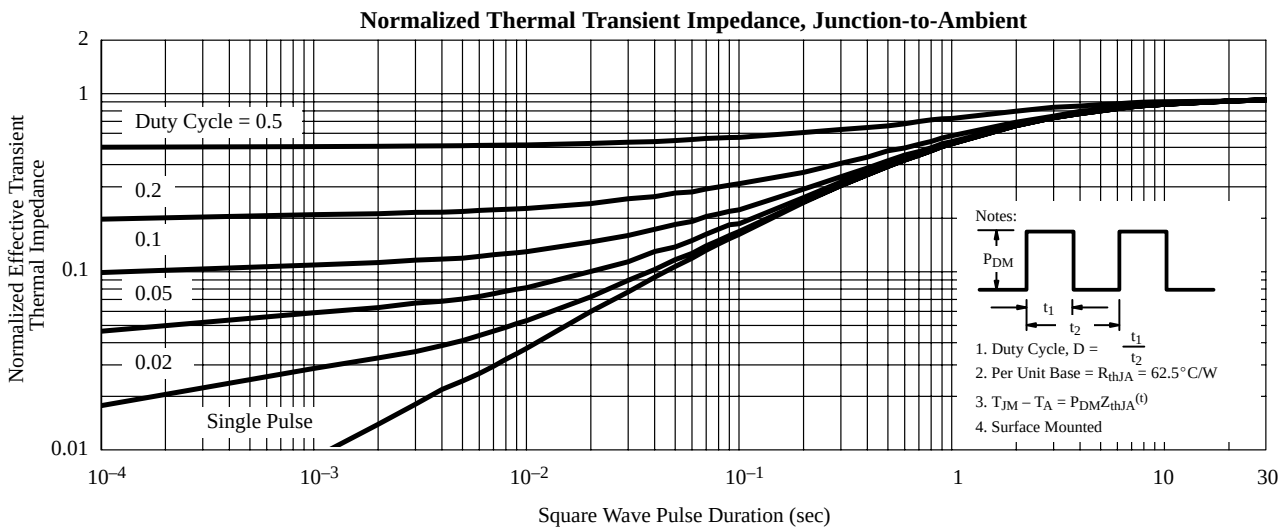
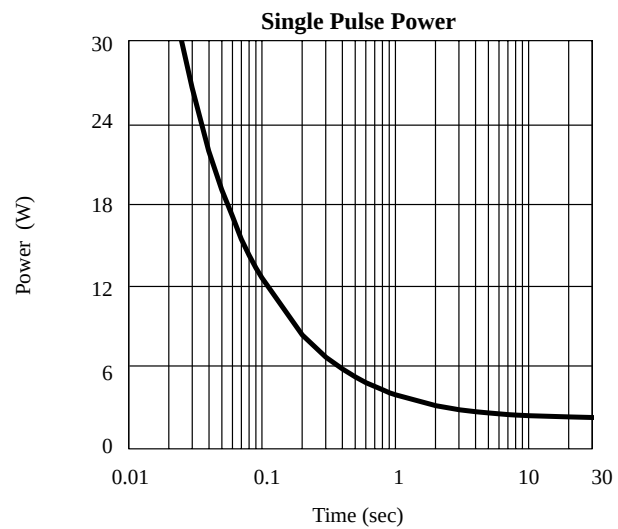
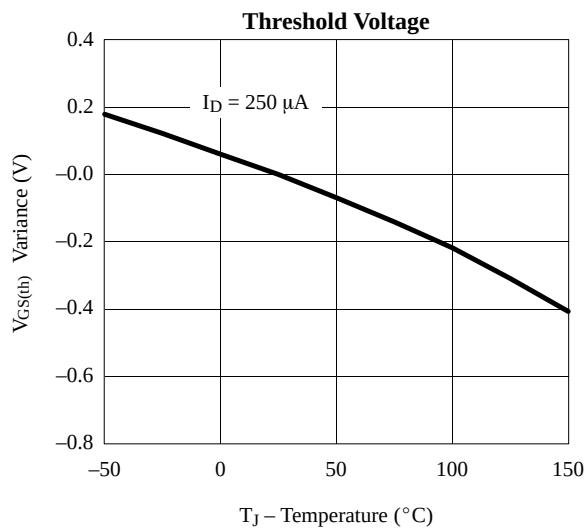
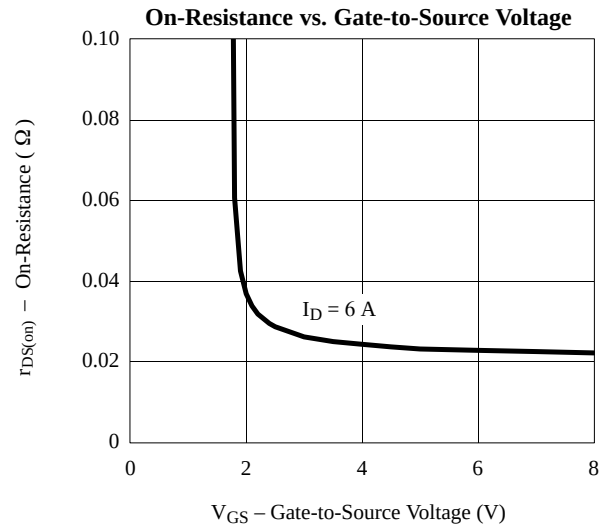
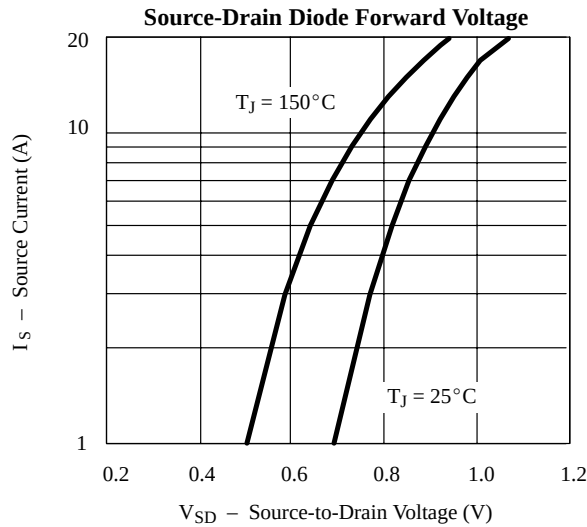
b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

Typical Characteristics (25°C Unless Otherwise Noted) N-Channel

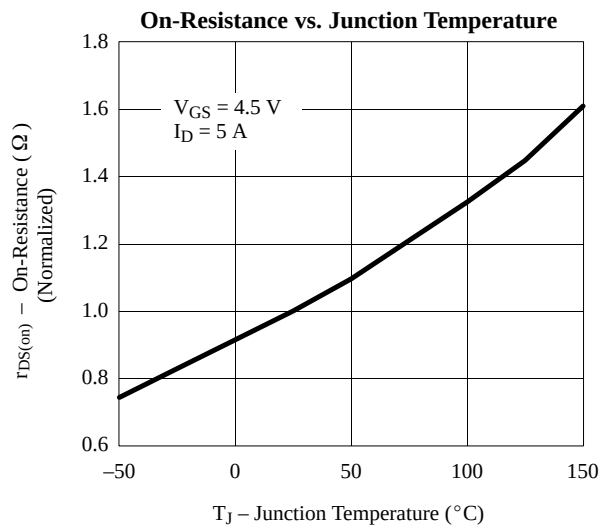
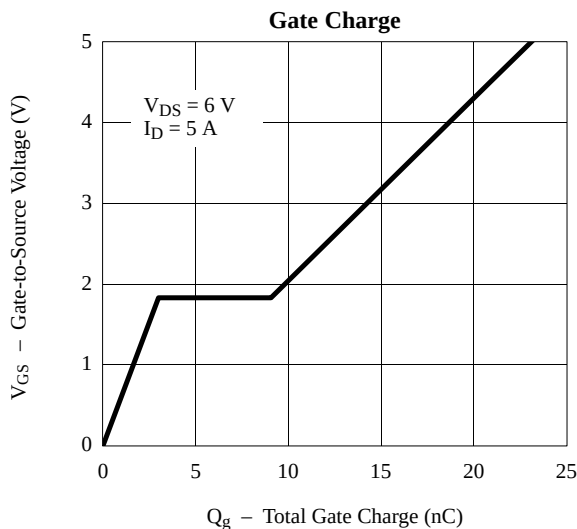
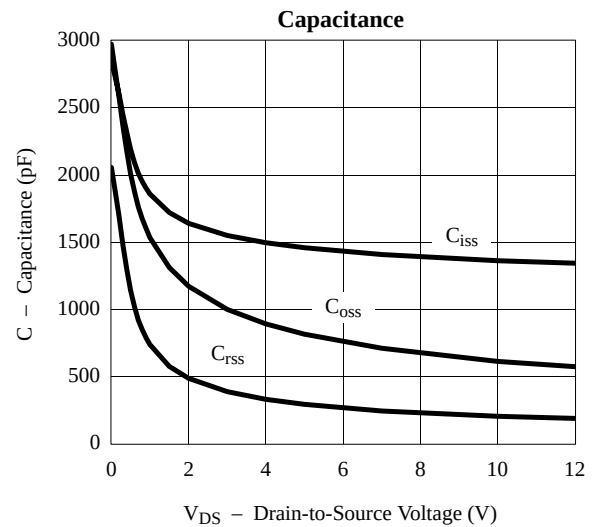
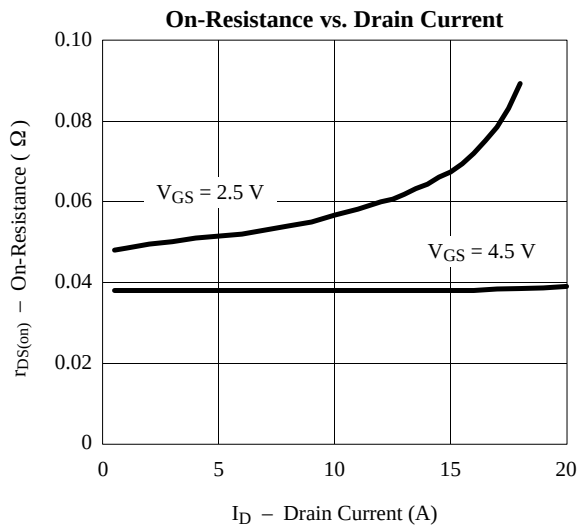
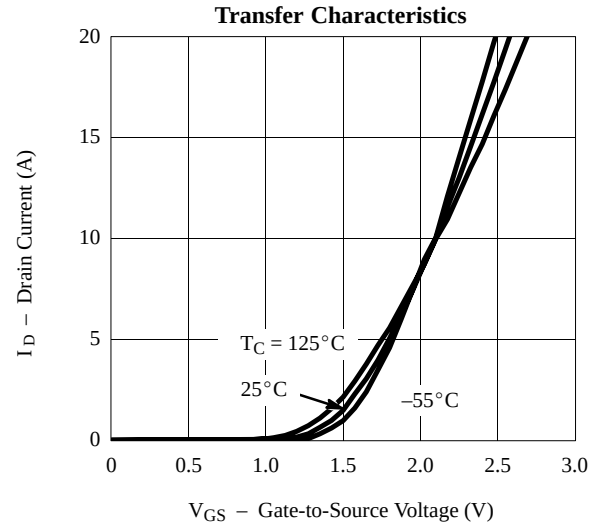
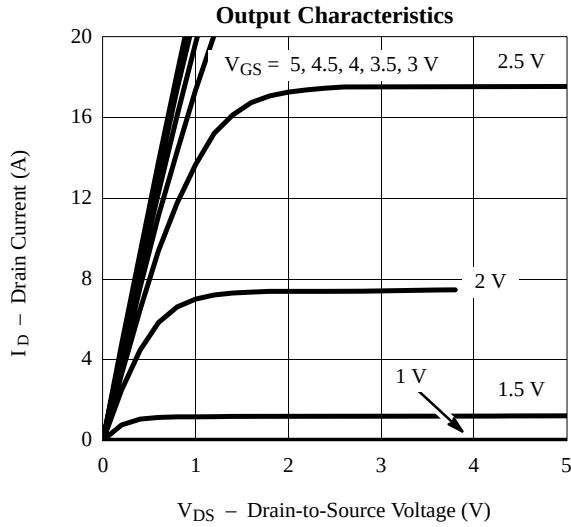


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Typical Characteristics (25°C Unless Otherwise Noted) N-Channel

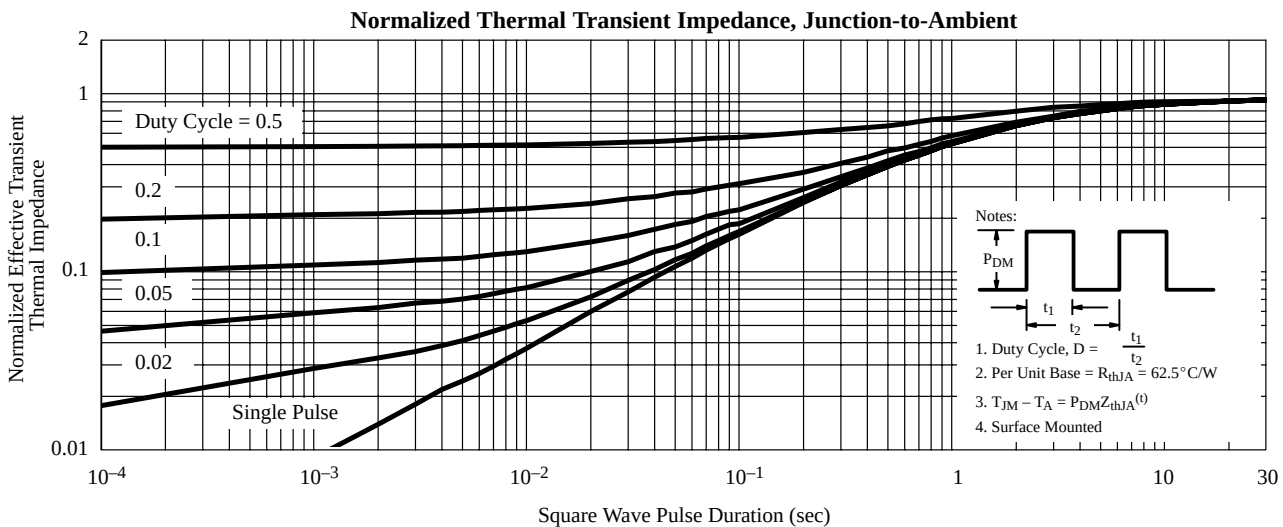
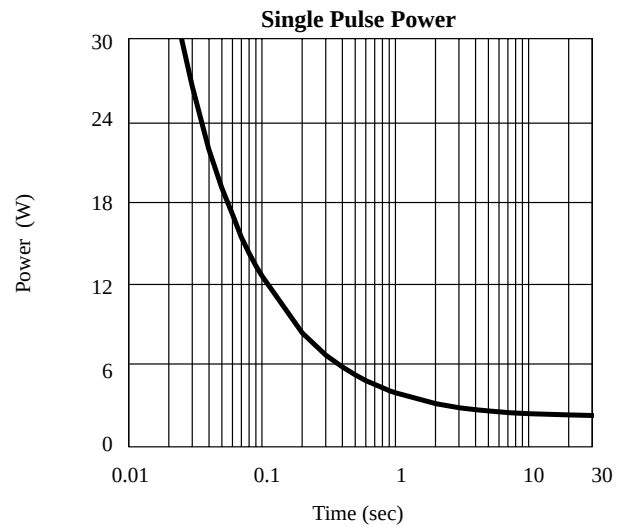
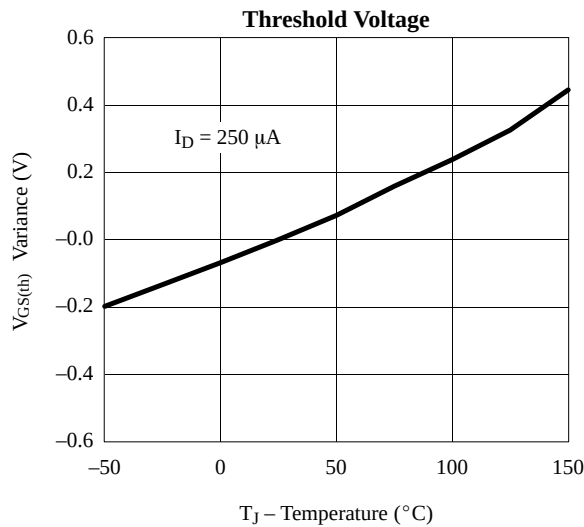
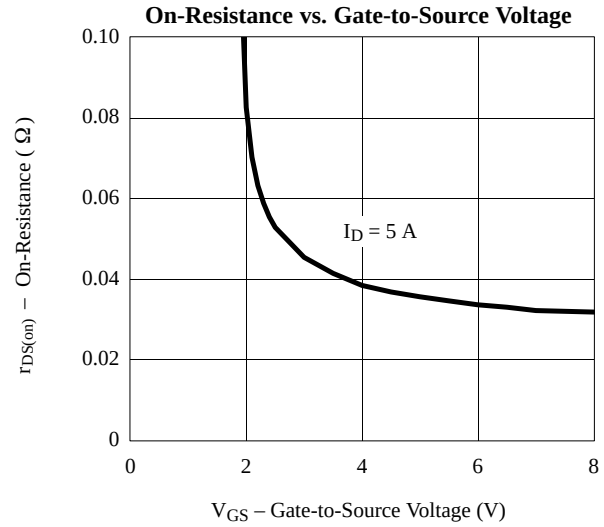
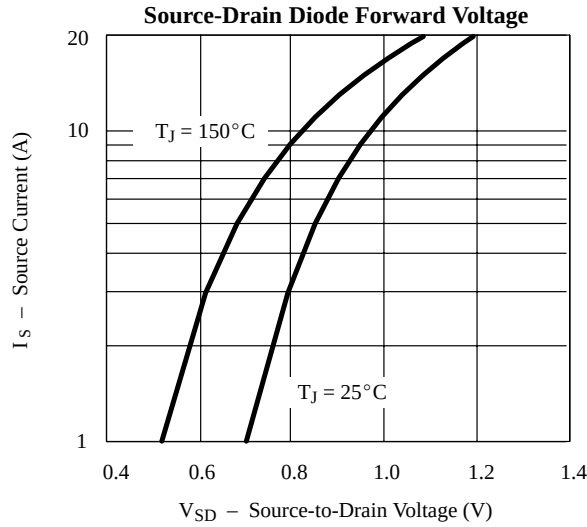


Typical Characteristics (25°C Unless Otherwise Noted) P-Channel



Si9529DY

Typical Characteristics (25°C Unless Otherwise Noted) P-Channel





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