LM3103 Synchronous 1-MHz 0.75-A Step-Down Voltage Regulator

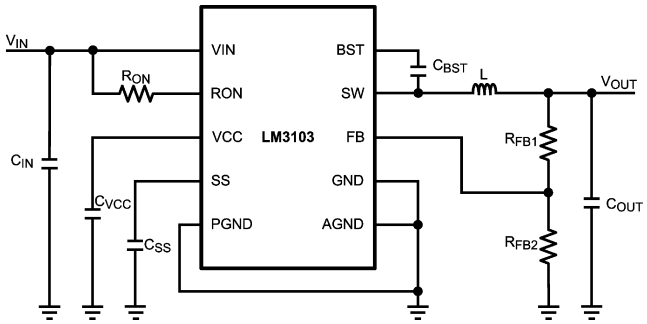
1 Features

- Input Voltage Range 4.5 V to 42 V
- 0.75 A Output Current
- 0.6V, ±2% Reference
- Integrated Dual N-Channel Main and Synchronous MOSFETs
- Low Component Count and Small Solution Size
- Stable with Ceramic and Other Low ESR Capacitors
- No Loop Compensation Required
- High Efficiency at a Light Load by DCM Operation
- Pre-bias Startup
- Ultra-Fast Transient Response
- Programmable Soft-Start
- Programmable Switching Frequency up to 1 MHz
- Valley Current Limit
- Thermal Shutdown
- Output Over-Voltage Protection
- Precision Internal Reference for an Adjustable Output Voltage Down to 0.6 V
- Thermally Enhanced HTSSOP-16 Package

2 Applications

- 5VDC, 12VDC, 24VDC, 12VAC, and 24VAC Systems
- Embedded Systems
- Industrial Control
- Automotive Telematics and Body Electronics
- Point of Load Regulators
- Storage Systems
- Broadband Infrastructure
- Direct Conversion from 2,3,4 Cell Lithium Batteries Systems

Typical Application Schematic



3 Description

The LM3103 Synchronously Rectified Buck Converter features all required functions to implement a highly efficient and cost effective buck regulator. It is capable of supplying 0.75 A to loads with an output voltage as low as 0.6 V. Dual N-Channel synchronous MOSFET switches allow a low component count, thus reducing complexity and minimizing board size.

Different from most other COT regulators, the LM3103 does not rely on output capacitor ESR for stability, and is designed to work exceptionally well with ceramic and other very low ESR output capacitors. It requires no loop compensation, results in a fast load transient response and simple circuit implementation. The operating frequency remains nearly constant with line variations due to the inverse relationship between the input voltage and the on-time. The operating frequency can be externally programmed up to 1 MHz. Protection features include V_{CC} under-voltage lock-out, output over-voltage protection, thermal shutdown, and gate drive under-voltage lock-out. The LM3103 is available in the thermally enhanced HTSSOP-16 package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM3103	HTSSOP-16	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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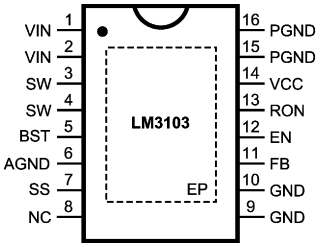
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (April 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	1

5 Pin Configuration and Functions

PWP Package
16-Pin HTSSOP
Top View



Pin Functions

Pin	Name	Description	Application Information
1, 2	VIN	Input supply voltage	Supply pin to the device. Nominal input range is 4.5 V to 42 V.
3, 4	SW	Switch Node	Internally connected to the source of the main MOSFET and the drain of the synchronous MOSFET. Connect to the output inductor.
5	BST	Connection for bootstrap capacitor	Connect a 33 nF capacitor from the SW pin to this pin. This capacitor is charged through an internal diode during the main MOSFET off-time.
6	AGND	Analog Ground	Ground for all internal circuitry other than the PGND pin.
7	SS	Soft-start	A 70 µA internal current source charges an external capacitor of larger than 22 nF to provide the soft-start function.
8	NC	No Connection	This pin should be left unconnected.
9, 10	GND	Ground	Must be connected to the AGND pin for normal operation. The GND and AGND pins are not internally connected.
11	FB	Feedback	Internally connected to the regulation and over-voltage comparators. The regulation setting is 0.6 V at this pin. Connect to feedback resistors.
12	EN	Enable pin	Internal pull-up. Connect to a voltage higher than 1.6 V to enable the device.
13	RON	On-time Control	An external resistor from the VIN pin to this pin sets the main MOSFET on-time.
14	VCC	Startup regulator Output	Nominally regulated to 6 V. Connect a capacitor of larger than 1 µF between the VCC and AGND pins for stable operation.
15, 16	PGND	Power Ground	Synchronous MOSFET source connection. Tie to a ground plane.
DAP	EP	Exposed Pad	Thermal connection pad. Connect to the ground plane.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
VIN, RON to AGND	–0.3	43.5	V
SW to AGND	–0.3	43.5	V
SW to AGND (Transient)		–2 (< 100 ns)	V
VIN to SW	–0.3	43.5	V
BST to SW	–0.3	7	V
VCC to AGND	–0.3	7	V
FB to AGND	–0.3	5	V
All Other Inputs to AGND	–0.3	7	V
Junction Temperature, T_J		150	°C
Storage Temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply Voltage Range (VIN)	4.5	42	V
Junction Temperature Range (T_J)	−40	125	°C

(1) *Absolute Maximum Ratings* are limits beyond which damage to the device may occur. *Recommended Operating Ratings* are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the *Electrical Characteristics*.

6.4 Thermal Information

THERMAL METRIC(1)		LM3103 PWP (HTSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Specifications with standard type are for T_J = 25°C unless otherwise specified. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 18 V, V_{OUT} = 3.3 V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
START-UP REGULATOR, V_{CC}							
V_{CC}	V_{CC} output voltage	C_{VCC} = 1 µF, no load	T_J = –40°C to +125°C	5.6	6.0	6.2	V
$V_{IN} – V_{CC}$	$V_{IN} – V_{CC}$ dropout voltage	I_{CC} = 2 mA	T_J = –40°C to +125°C		55	150	mV
		I_{CC} = 10 mA	T_J = –40°C to +125°C		235	500	
$V_{CC-UVLO}$	V_{CC} undervoltage lockout threshold (UVLO)	V_{IN} increasing	T_J = –40°C to +125°C	3.5	3.7	4.1	V
$V_{CC-UVLO-HYS}$	V_{CC} UVLO hysteresis	V_{IN} decreasing			275		mV
I_{IN}	I_{IN} operating current	No switching, V_{FB} = 1 V	T_J = –40°C to +125°C		1.0	1.25	mA
I_{IN-SD}	I_{IN} operating current, device shutdown	V_{EN} = 0 V	T_J = –40°C to +125°C		20	40	µA
I_{VCC}	V_{CC} current limit	V_{CC} = 0 V	T_J = –40°C to +125°C	20	33	42	mA
SWITCHING CHARACTERISTICS							
$R_{DS-UP-ON}$	Main MOSFET $R_{DS(on)}$	T_J = –40°C to +125°C			0.370	0.7	Ω
$R_{DS-DN-ON}$	Syn. MOSFET $R_{DS(on)}$	T_J = –40°C to +125°C			0.220	0.4	Ω
SOFT-START							
I_{SS}	SS pin source current	V_{SS} = 0 V	T_J = –40°C to +125°C	45	70	95	µA

Electrical Characteristics (continued)

Specifications with standard type are for T_J = 25°C unless otherwise specified. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 18 V, V_{OUT} = 3.3 V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CURRENT LIMIT							
I_{CL}	Syn. MOSFET current limit threshold				0.9		A
ON/OFF TIMER							
t_{on}	ON timer pulse width	V_{IN} = 10 V, R_{ON} = 33 kΩ			0.350		µs
		V_{IN} = 18 V, R_{ON} = 33 kΩ			0.170		
t_{on-MIN}	ON timer minimum pulse width				100		ns
t_{off}	OFF timer pulse width				240		ns
ENABLE INPUT							
V_{EN}	EN Pin input threshold	V_{EN} rising	T_J = –40°C to +125°C		1.6	1.85	V
V_{EN-HYS}	Enable threshold hysteresis	V_{EN} falling			230		mV
I_{EN}	Enable Pull-up Current	V_{EN} = 0 V			1		µA
REGULATION AND OVERVOLTAGE COMPARATOR							
V_{FB}	In-regulation feedback voltage	T_J = –40°C to +125°C		0.588	0.6	0.612	V
V_{FB-OV}	Feedback overvoltage threshold	T_J = –40°C to +125°C		0.655	0.680	0.705	V
I_{FB}					1		nA
THERMAL SHUTDOWN							
T_{SD}	Thermal shutdown temperature	T_J rising			165		°C
T_{SD-HYS}	Thermal shutdown temperature hysteresis	T_J falling			20		°C

6.6 Typical Characteristics

All curves are taken at V_{IN} = 18 V with the configuration in the typical application circuit for V_{OUT} = 3.3 V shown in this datasheet. T_A = 25°C, unless otherwise specified.

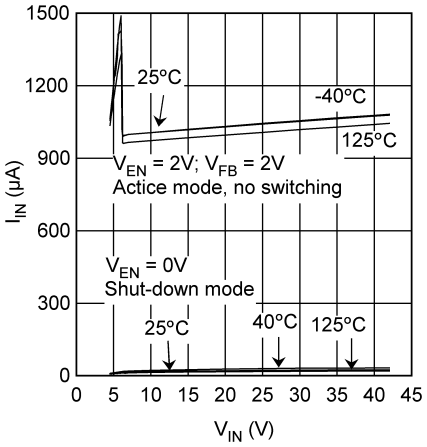


Figure 1. Quiescent Current, I_{IN} vs V_{IN}

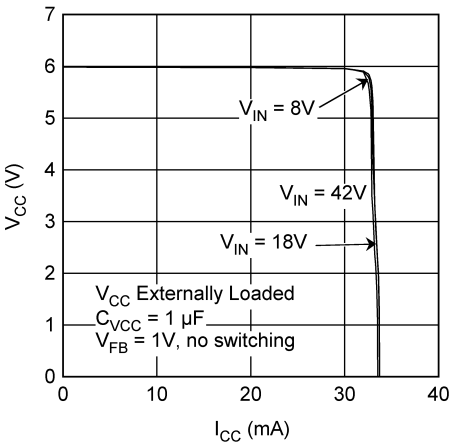


Figure 2. V_{CC} vs I_{CC}

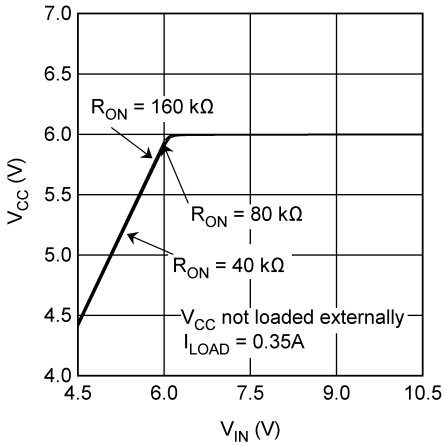


Figure 3. V_{CC} vs V_{IN}

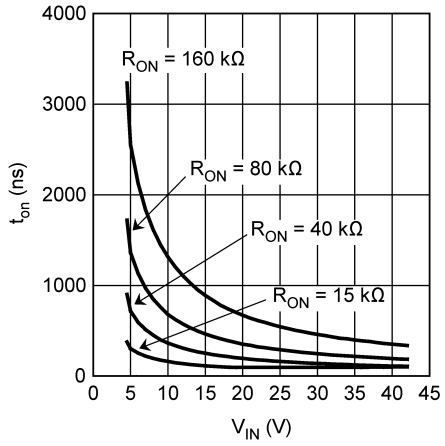


Figure 4. t_{on} vs V_{IN}

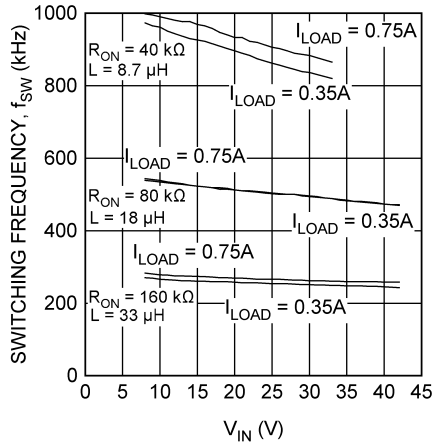


Figure 5. Switching Frequency, f_{SW} vs V_{IN}

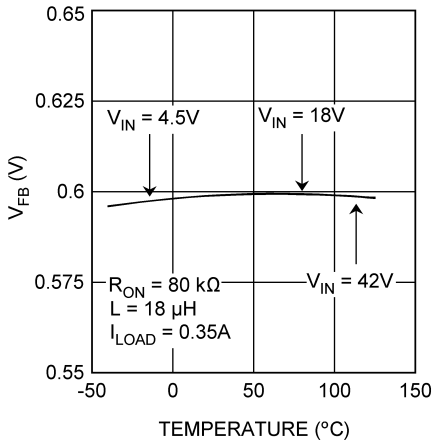


Figure 6. V_{FB} vs Temperature

Typical Characteristics (continued)

All curves are taken at V_{IN} = 18 V with the configuration in the typical application circuit for V_{OUT} = 3.3 V shown in this datasheet. T_A = 25°C, unless otherwise specified.

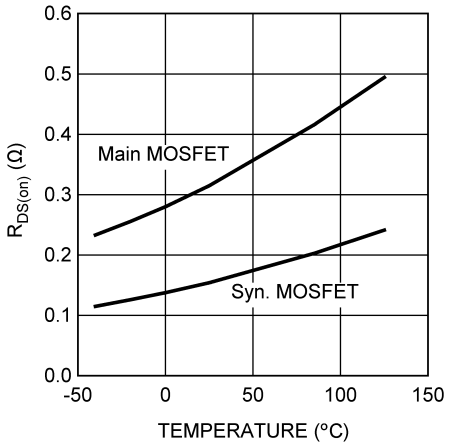


Figure 7. $R_{DS(on)}$ vs Temperature

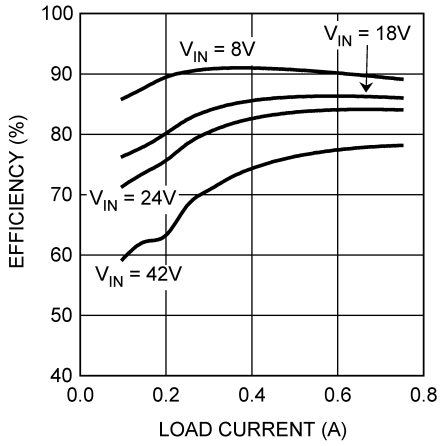


Figure 8. Efficiency vs Load Current (V_{OUT} = 3.3 V)

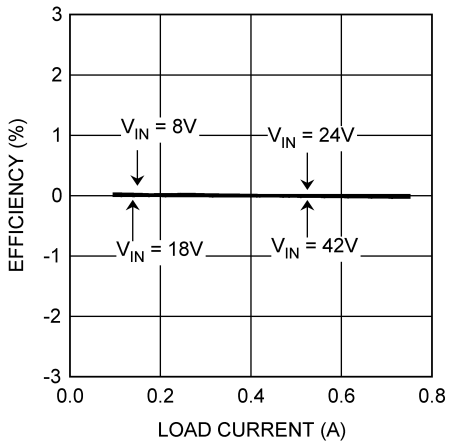


Figure 9. V_{OUT} Regulation vs Load Current (V_{OUT} = 3.3 V)

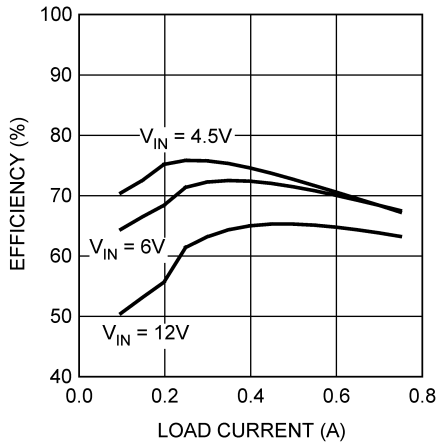


Figure 10. Efficiency vs Load Current (V_{OUT} = 0.6 V)

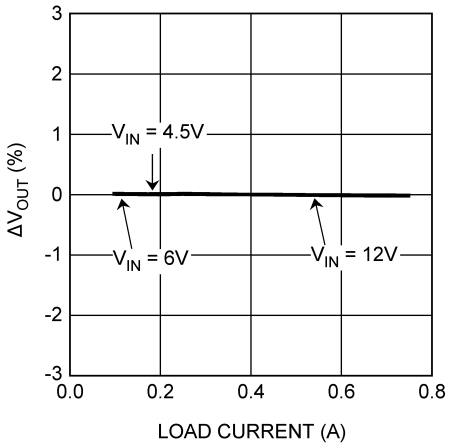


Figure 11. V_{OUT} Regulation vs Load Current (V_{OUT} = 0.6 V)

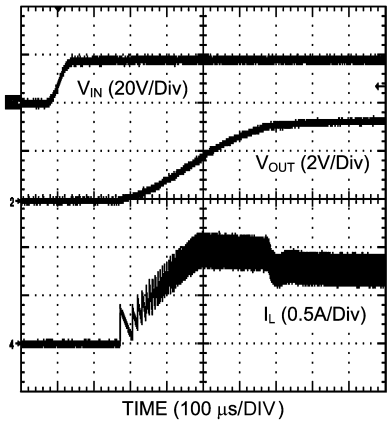


Figure 12. Power Up (V_{OUT} = 3.3 V, 0.75 A Loaded)

Typical Characteristics (continued)

All curves are taken at V_{IN} = 18 V with the configuration in the typical application circuit for V_{OUT} = 3.3 V shown in this datasheet. T_A = 25°C, unless otherwise specified.

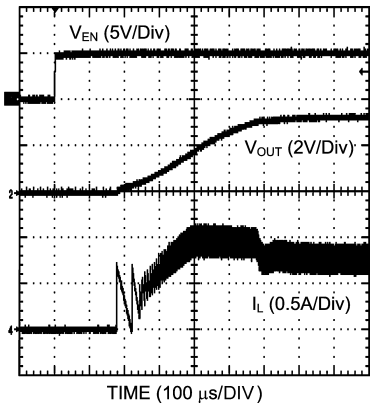


Figure 13. Enable Transient (V_{OUT} = 3.3 V, 0.75 A Loaded)

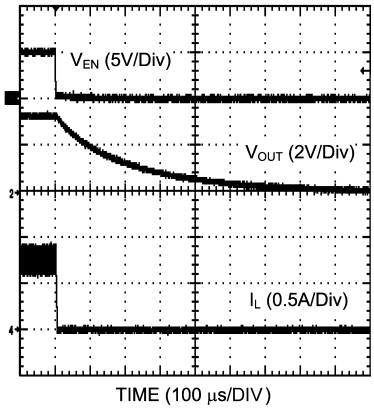


Figure 14. Shutdown Transient (V_{OUT} = 3.3 V, 0.75 A Loaded)

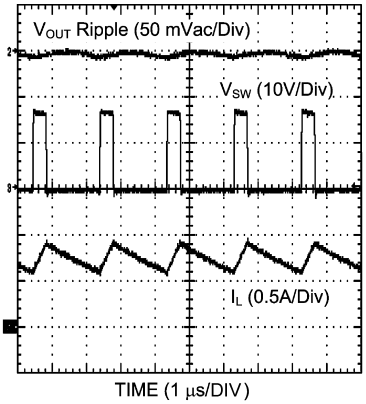


Figure 15. Continuous Mode Operation (V_{OUT} = 3.3 V, 2.5 A Loaded)

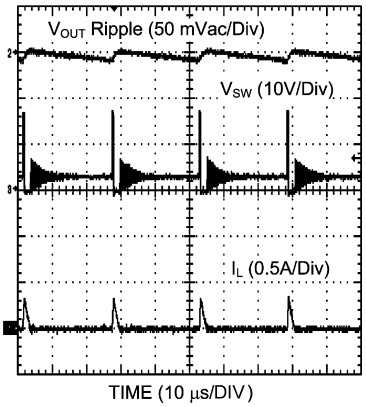


Figure 16. Discontinuous Mode Operation (V_{OUT} = 3.3 V, 0.02 A Loaded)

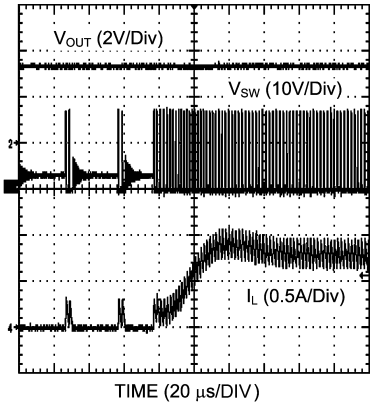


Figure 17. DCM to CCM Transition (V_{OUT} = 3.3 V, 0.01 A - 0.75 A Load)

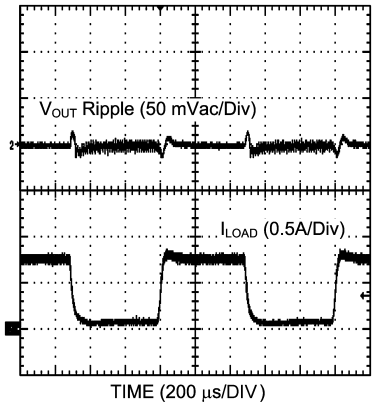
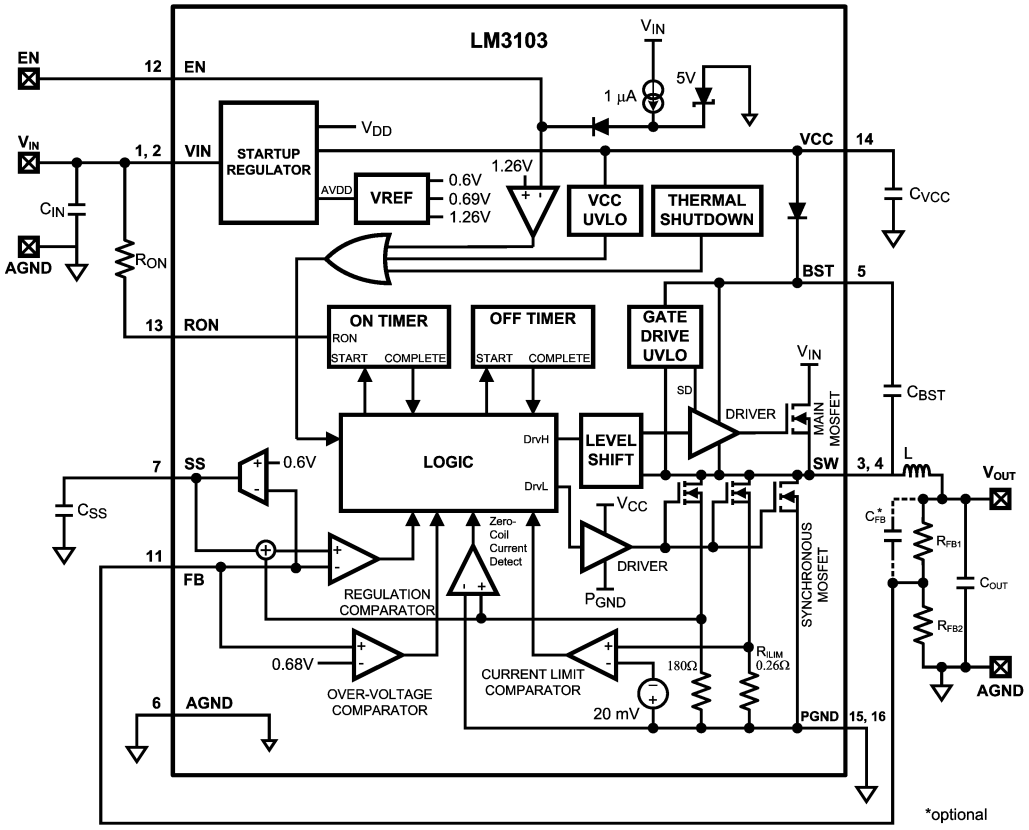


Figure 18. Load Transient (V_{OUT} = 3.3 V, 0.075 A - 0.75 A Load, Current slew-rate: 2.5 A/µs)

7 Detailed Description

7.1 Functional Block Diagram



7.2 Feature Description

The LM3103 Step Down Switching Regulator features all required functions to implement a cost effective, efficient buck power converter which is capable of supplying 0.75 A to loads. It contains dual N-Channel main and synchronous MOSFETs. The Constant ON-Time (COT) regulation scheme requires no loop compensation, results in a fast load transient response and simple circuit implementation. The regulator can function properly even with an all ceramic output capacitor network, and does not rely on the output capacitor's ESR for stability. The operating frequency remains constant with line variations due to the inverse relationship between the input voltage and the on-time. The valley current limit detection circuit, with a limit set internally at 0.9 A, inhibits the main MOSFET until the inductor current level subsides.

The LM3103 can be applied in numerous applications and can operate efficiently for inputs as high as 42 V. Protection features include V_{CC} under-voltage lockout, output over-voltage protection, thermal shutdown, gate drive under-voltage lock-out. The LM3103 is available in the thermally enhanced HTSSOP-16 package.

7.2.1 COT Control Circuit Overview

COT control is based on a comparator and a one-shot on-timer, with the output voltage feedback (feeding to the FB pin) compared with a 0.6 V internal reference. If the voltage of the FB pin is below the reference, the main MOSFET is turned on for a fixed on-time determined by a programming resistor RON and the input voltage V_{IN}, upon which the on-time varies inversely. Following the on-time, the main MOSFET remains off for a minimum of 240 ns. Then, if the voltage of the FB pin is below the reference, the main MOSFET is turned on again for another on-time period. The switching will continue to achieve regulation.

Feature Description (continued)

The regulator will operate in the discontinuous conduction mode (DCM) at a light load, and the continuous conduction mode (CCM) with a heavy load. In the DCM, the current through the inductor starts at zero and ramps up to a peak during the on-time, and then ramps back to zero before the end of the off-time. It remains zero and the load current is supplied entirely by the output capacitor. The next on-time period starts when the voltage at the FB pin falls below the internal reference. The operating frequency in the DCM is lower and varies larger with the load current as compared with the CCM. Conversion efficiency is maintained since conduction loss and switching loss are reduced with the reduction in the load and the switching frequency respectively. The operating frequency in the DCM can be calculated approximately as follows:

$$f_{SW} = \frac{V_{OUT} (V_{IN} - 1) \times L \times 1.18 \times 10^{20} \times I_{OUT}}{(V_{IN} - V_{OUT}) \times R_{ON}^2} \quad (1)$$

In the continuous conduction mode (CCM), the current flows through the inductor in the entire switching cycle, and never reaches zero during the off-time. The operating frequency remains relatively constant with load and line variations. The CCM operating frequency can be calculated approximately as follows:

$$f_{SW} = \frac{V_{OUT}}{8.3 \times 10^{-11} \times R_{ON}} \quad (2)$$

The output voltage is set by two external resistors R_{FB1} and R_{FB2}. The regulated output voltage is

$$V_{OUT} = 0.6V \times (R_{FB1} + R_{FB2})/R_{FB2} \quad (3)$$

7.2.2 Startup Regulator (V_{CC})

A startup regulator is integrated within the LM3103. The input pin VIN can be connected directly to a line voltage up to 42 V. The V_{CC} output regulates at 6 V, and is current limited to 30 mA. Upon power up, the regulator sources current into an external capacitor C_{VCC}, which is connected to the VCC pin. For stability, C_{VCC} must be at least 1 µF. When the voltage on the VCC pin is higher than the under-voltage lock-out (UVLO) threshold of 3.7 V, the main MOSFET is enabled and the SS pin is released to allow the soft-start capacitor C_{SS} to charge.

The minimum input voltage is determined by the dropout voltage of the regulator and the V_{CC} UVLO falling threshold (≅3.4 V). If V_{IN} is less than ≅4.0 V, the regulator shuts off and V_{CC} goes to zero.

7.2.3 Regulation Comparator

The feedback voltage at the FB pin is compared to a 0.6 V internal reference. In normal operation (the output voltage is regulated), an on-time period is initiated when the voltage at the FB pin falls below 0.6 V. The main MOSFET stays on for the programmed on-time, causing the output voltage to rise and consequently the voltage of the FB pin to rise above 0.6 V. After the on-time period, the main MOSFET stays off until the voltage of the FB pin falls below 0.6 V again. Bias current at the FB pin is nominally 1 nA.

7.2.4 Zero Coil Current Detect

The current of the synchronous MOSFET is monitored by a zero coil current detection circuit which inhibits the synchronous MOSFET when its current reaches zero until the next on-time. This circuit enables the DCM operation, which improves the efficiency at a light load.

7.2.5 Over-Voltage Comparator

The voltage at the FB pin is compared to a 0.68 V internal reference. If it rises above 0.68 V, the on-time is immediately terminated. This condition is known as over-voltage protection (OVP). It can occur if the input voltage or the output load changes suddenly. Once the OVP is activated, the main MOSFET remains off until the voltage at the FB pin falls below 0.6 V. The synchronous MOSFET will stay on to discharge the inductor until the inductor current reduces to zero and then switch off.

7.2.6 ON-Time Timer, Shutdown

The on-time of the LM3103 main MOSFET is determined by the resistor R_{ON} and the input voltage V_{IN}. It is calculated as follows:

$$t_{ON} = \frac{8.3 \times 10^{-11} \times R_{ON}}{V_{IN}} \quad (4)$$

Feature Description (continued)

The inverse relationship of t_{on} and V_{IN} gives a nearly constant frequency as V_{IN} is varied. R_{ON} should be selected such that the on-time at maximum V_{IN} is greater than 100 ns. The on-timer has a limiter to ensure a minimum of 100 ns for t_{on}. This limits the maximum operating frequency, which is governed by the following equation:

$$f_{SW(MAX)} = \frac{V_{OUT}}{V_{IN(MAX)} \times 100\ ns} \quad (5)$$

The LM3103 can be remotely shut down by pulling the voltage of the EN pin below 1.6 V. In this shutdown mode, the SS pin is internally grounded, the on-timer is disabled, and bias currents are reduced. Releasing the EN pin allows normal operation to resume because the EN pin is internally pulled up.

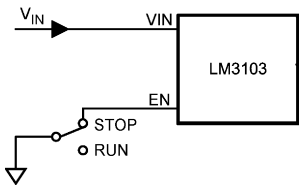


Figure 19. Shutdown Implementation

7.2.7 Current Limit

Current limit detection is carried out during the off-time by monitoring the re-circulating current through the synchronous MOSFET. Referring to the Functional Block Diagram, when the main MOSFET is turned off, the inductor current flows through the load, the PGND pin and the internal synchronous MOSFET. If this current exceeds 0.9 A, the current limit comparator toggles, and as a result the start of the next on-time period is disabled. The next switching cycle starts when the re-circulating current falls back below 0.9 A (and the voltage at the FB pin is below 0.6 V). The inductor current is monitored during the on-time of the synchronous MOSFET. As long as the inductor current exceeds 0.9 A, the main MOSFET will remain inhibited to achieve current limit. The operating frequency is lower during current limit owing to a longer off-time.

Figure 20 illustrates an inductor current waveform. On average, the output current I_{OUT} is the same as the inductor current I_L, which is the average of the rippled inductor current. In case of current limit (the current limit portion of Figure 20), the next on-time will not initiate until that the current drops below 0.9 A (assume the voltage at the FB pin is lower than 0.6 V). During each on-time the current ramps up an amount equal to:

$$I_{LR} = \frac{(V_{IN} - V_{OUT}) \times t_{on}}{L} \quad (6)$$

During current limit, the LM3103 operates in a constant current mode with an average output current $I_{OUT(CL)}$ equal to 0.9 A + I_{LR} / 2.

Feature Description (continued)

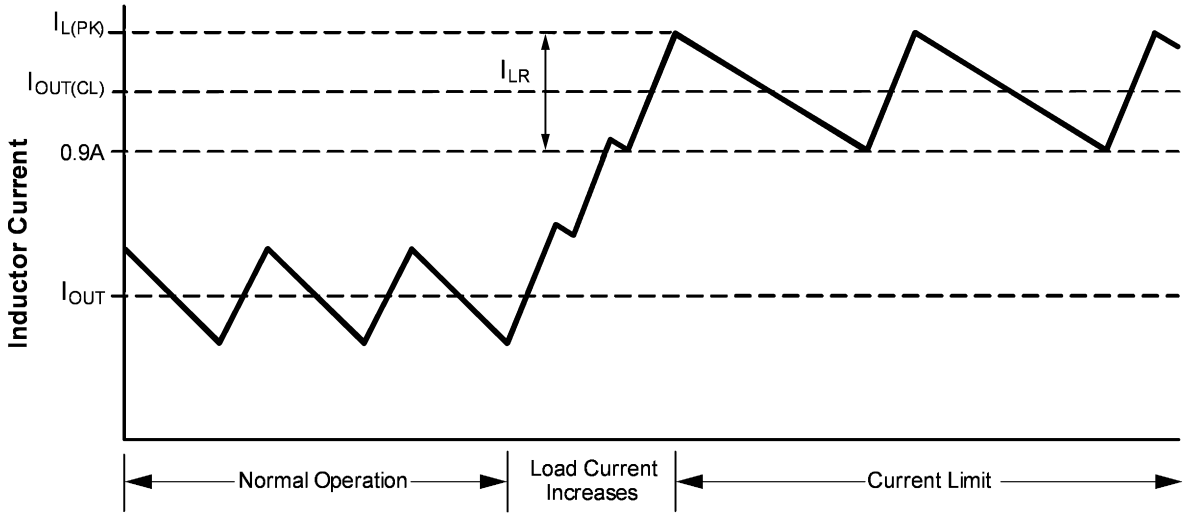


Figure 20. Inductor Current - Current Limit Operation

7.2.8 N-Channel MOSFET and Driver

The LM3103 integrates an N-Channel main MOSFET and an associated floating high voltage main MOSFET gate driver. The gate drive circuit works in conjunction with an external bootstrap capacitor C_{BST} and an internal high voltage diode. C_{BST} connected between the BST and SW pins powers the main MOSFET gate driver during the main MOSFET on-time. During each off-time, the voltage of the SW pin falls to approximately –1 V, and C_{BST} charges from V_{CC} through the internal diode. The minimum off-time of 240 ns provides enough time for charging C_{BST} in each cycle.

7.2.9 Soft-Start

The soft-start feature allows the converter to gradually reach a steady state operating point, thereby reducing startup stresses and current surges. Upon turn-on, after V_{CC} reaches the under-voltage threshold and a 180 µs fixed delay, a 70 µA internal current source charges an external capacitor C_{SS} connecting to the SS pin. The ramping voltage at the SS pin (and the non-inverting input of the regulation comparator as well) ramps up the output voltage V_{OUT} in a controlled manner. An internal switch grounds the SS pin if any of the following three cases happen: (i) V_{CC} is below the under-voltage lockout threshold; (ii) a thermal shutdown occurs; or (iii) the EN pin is grounded. Alternatively, the output voltage can be shut off by connecting the SS pin to the ground using an external switch. Releasing the switch allows the voltage of the SS pin to ramp up and the output voltage to return to normal. The shutdown configuration is shown in Figure 21.

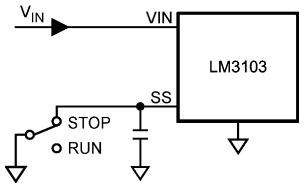


Figure 21. Alternate Shutdown Implementation

7.2.10 Thermal Protection

The junction temperature of the LM3103 should not exceed the maximum limit. Thermal protection is implemented by an internal Thermal Shutdown circuit, which activates (typically) at 165°C to make the controller enter a low power reset state by disabling the main MOSFET, disabling the on-timer, and grounding the SS pin. Thermal protection helps prevent catastrophic failures from accidental device overheating. When the junction temperature falls back below 145°C (typical hysteresis = 20°C), the SS pin is released and normal operation resumes.

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 External Components

The following guidelines can be used to select external components.

R_{FB1} and R_{FB2} : These resistors should be chosen from standard values in the range of 1.0 kΩ to 10 kΩ, satisfying the following ratio:

$$R_{FB1}/R_{FB2} = (V_{OUT}/0.6\ V) - 1 \quad (7)$$

For V_{OUT} = 0.6 V, the FB pin can be connected to the output directly with a pre-load resistor drawing more than 20 µA. This is because the converter operation needs a minimum inductor current ripple to maintain good regulation when no load is connected.

R_{ON}: Equation 2 can be used to select R_{ON} if a desired operating frequency is selected. But the minimum value of R_{ON} is determined by the minimum on-time. It can be calculated as follows:

$$R_{ON} \geq \frac{V_{IN(MAX)} \times 100\ ns}{8.3 \times 10^{-11}} \quad (8)$$

If R_{ON} calculated from Equation 2 is smaller than the minimum value determined in Equation 8, a lower frequency should be selected to re-calculate R_{ON} by Equation 2. Alternatively, $V_{IN(MAX)}$ can also be limited in order to keep the frequency unchanged. The relationship of $V_{IN(MAX)}$ and R_{ON} is shown in Figure 22.

On the other hand, the minimum off-time of 240 ns can limit the maximum duty ratio. This may be significant at low V_{IN}. A larger R_{ON} should be selected in any application requiring a large duty ratio.

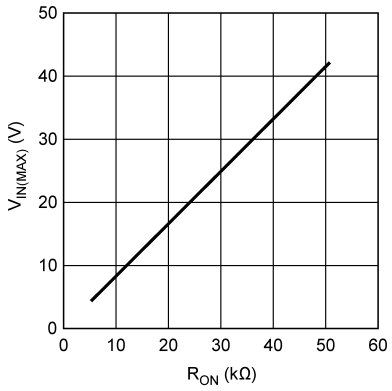


Figure 22. Maximum V_{IN} for selected R_{ON}

L: The main parameter affected by the inductor is the amplitude of the inductor current ripple (I_{LR}), which is recommended to be greater than 0.3 A. Once I_{LR} is selected, L can be determined by:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{I_{LR} \times f_{SW} \times V_{IN}} \quad (9)$$

where V_{IN} is the input voltage and f_{SW} is determined from Equation 2.

Application Information (continued)

If the output current I_{OUT} is known, by assuming that $I_{OUT} = I_L$, the peak and valley of I_{LR} can be determined. Beware that the peak of I_{LR} should not be larger than the saturation current of the inductor and the current rating of the main and synchronous MOSFETs. Also, the valley of I_{LR} must be positive if CCM operation is required.

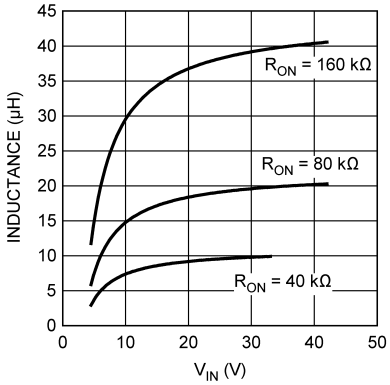


Figure 23. Inductor selection for V_{OUT} = 3.3 V

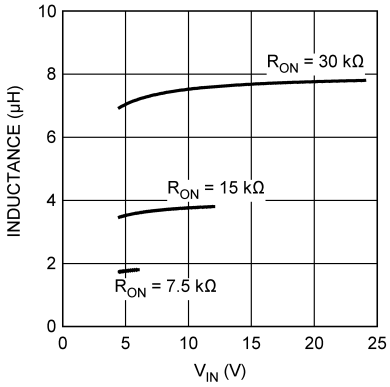


Figure 24. Inductor selection for V_{OUT} = 0.6 V

Figure 23 and Figure 24 show curves on inductor selection for various V_{OUT} and R_{ON}. According to Equation 8, V_{IN} is limited for small R_{ON}. Some curves are therefore limited as shown in the figures.

C_{VCC}: The capacitor on the V_{CC} output provides not only noise filtering and stability, but also prevents false triggering of the V_{CC} UVLO at the main MOSFET on/off transitions. C_{VCC} should be no smaller than 1 µF for stability, and should be a good quality, low ESR, ceramic capacitor.

C_{OUT} and C_{OUT3}: C_{OUT} should generally be no smaller than 10 µF. Experimentation is usually necessary to determine the minimum value for C_{OUT}, as the nature of the load may require a larger value. A load which creates significant transients requires a larger C_{OUT} than a fixed load.

C_{OUT3} is a small value ceramic capacitor located close to the LM3103 to further suppress high frequency noise at V_{OUT}. A 47 nF capacitor is recommended.

C_{IN} and C_{IN3}: The function of C_{IN} is to supply most of the main MOSFET current during the on-time, and limit the voltage ripple at the VIN pin, assuming that the voltage source connecting to the VIN pin has finite output impedance. If the voltage source's dynamic impedance is high (effectively a current source), C_{IN} supplies the difference between the instantaneous input current and the average input current.

At the maximum load current, when the main MOSFET turns on, the current to the VIN pin suddenly increases from zero to the valley of the inductor's ripple current and ramps up to the peak value. It then drops to zero at turn-off. The average current during the on-time is the load current. For a worst case calculation, C_{IN} must be capable of supplying this average load current during the maximum on-time. C_{IN} is calculated from:

Application Information (continued)

$$C_{IN} = \frac{I_{OUT} \times t_{ON}}{\Delta V_{IN}} \quad (10)$$

where I_{OUT} is the load current, t_{on} is the maximum on-time, and ΔV_{IN} is the allowable ripple voltage at V_{IN}.

C_{IN3}'s purpose is to help avoid transients and ringing due to long lead inductance at the VIN pin. A low ESR 0.1 µF ceramic chip capacitor located close to the LM3103 is recommended.

C_{BST}: A 33 nF high quality ceramic capacitor with low ESR is recommended for C_{BST} since it supplies a surge current to charge the main MOSFET gate driver at each turn-on. Low ESR also helps ensure a complete recharge during each off-time.

C_{SS}: The capacitor at the SS pin determines the soft-start time, i.e. the time for the reference voltage at the regulation comparator and therefore, the output voltage to reach their final value. The time is determined from the following equation:

$$t_{SS} = 180\ \mu s + \frac{C_{SS} \times 0.6V}{70\ \mu A} \quad (11)$$

C_{FB}: If the output voltage is higher than 1.6 V, C_{FB} is needed in the Discontinuous Conduction Mode to reduce the output ripple. The recommended value for C_{FB} is 10 nF.

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

9.3 Trademarks

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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3103MH/NOPB	ACTIVE	HTSSOP	PWP	16	92	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM3103 MH	Samples
LM3103MHX/NOPB	ACTIVE	HTSSOP	PWP	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM3103 MH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

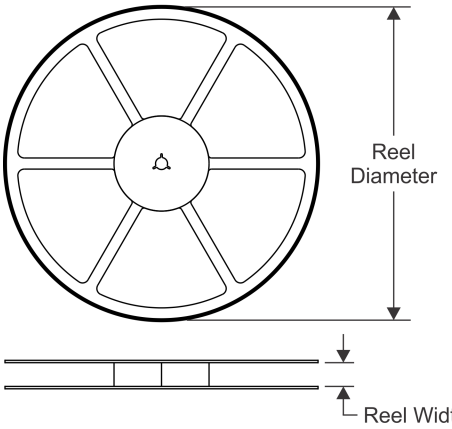
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

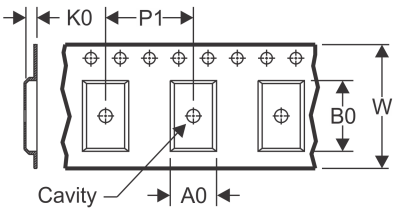
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

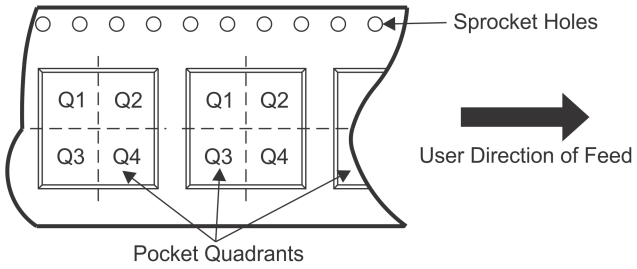


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

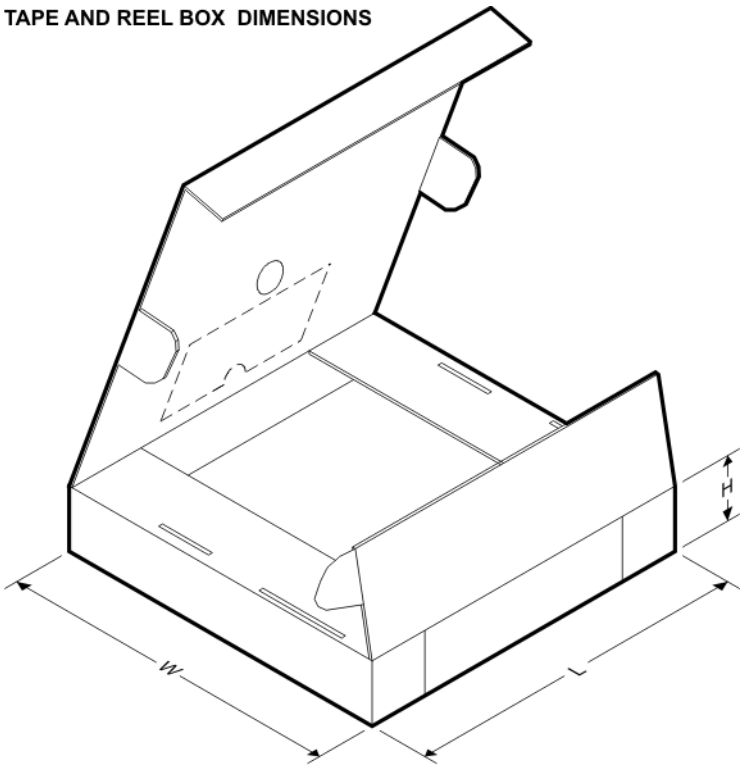
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

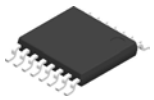
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3103MHX/NOPB	HTSSOP	PWP	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3103MHX/NOPB	HTSSOP	PWP	16	2500	367.0	367.0	35.0

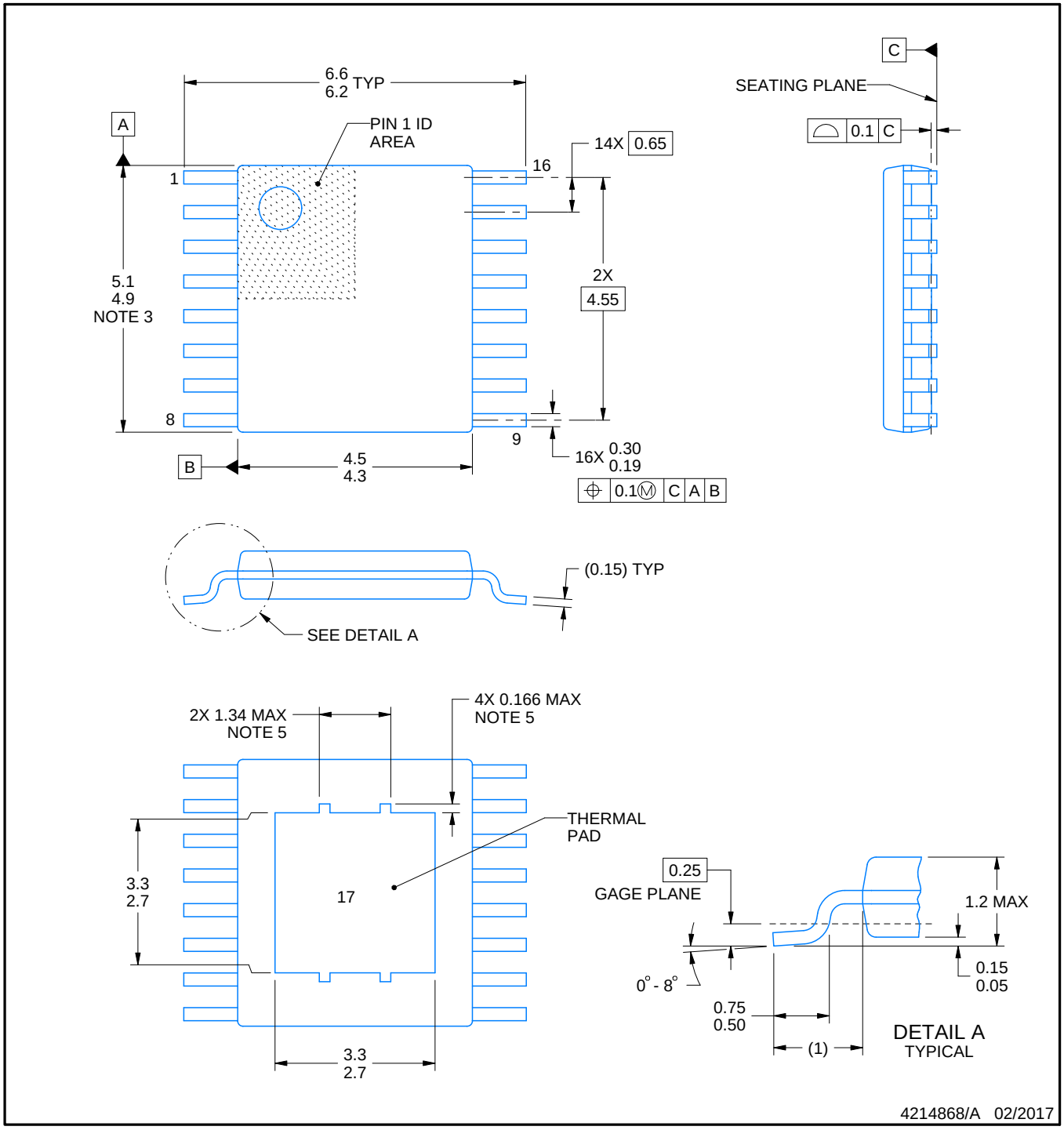


PACKAGE OUTLINE

PWP0016A

PowerPAD ™ HTSSOP - 1.2 mm max height

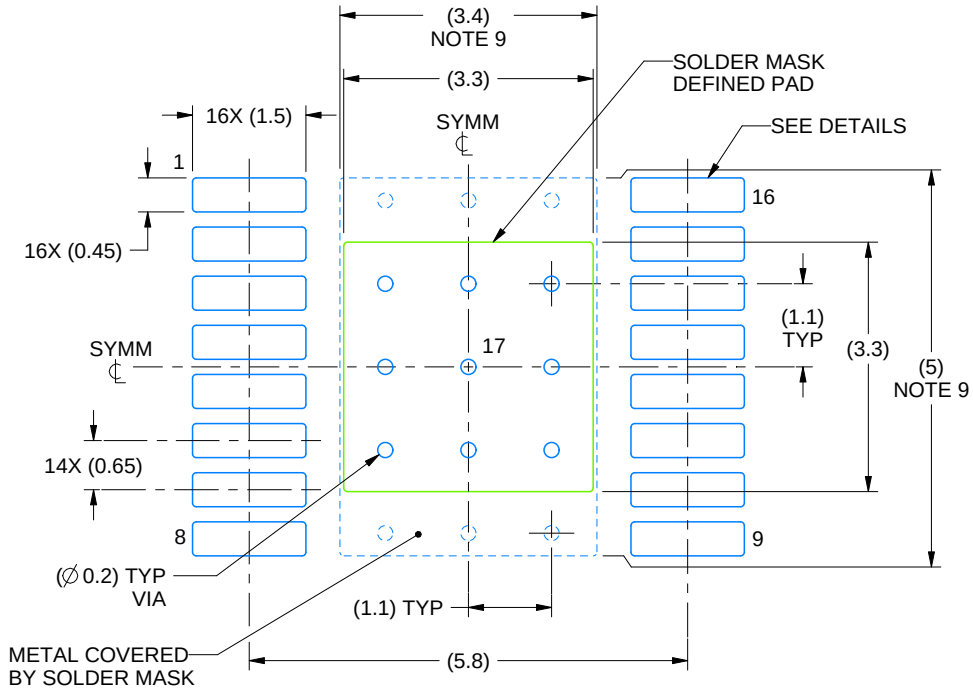
PLASTIC SMALL OUTLINE



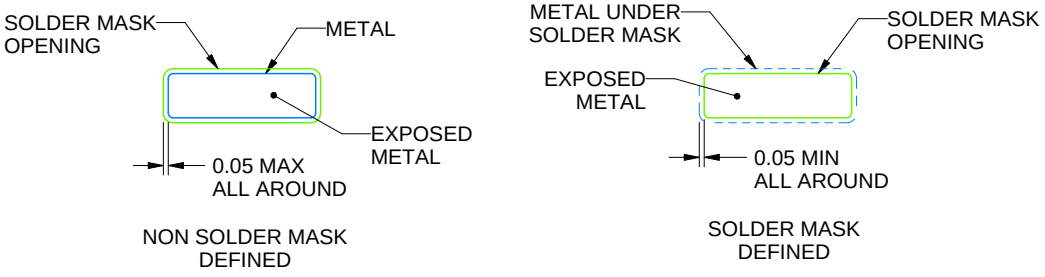
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

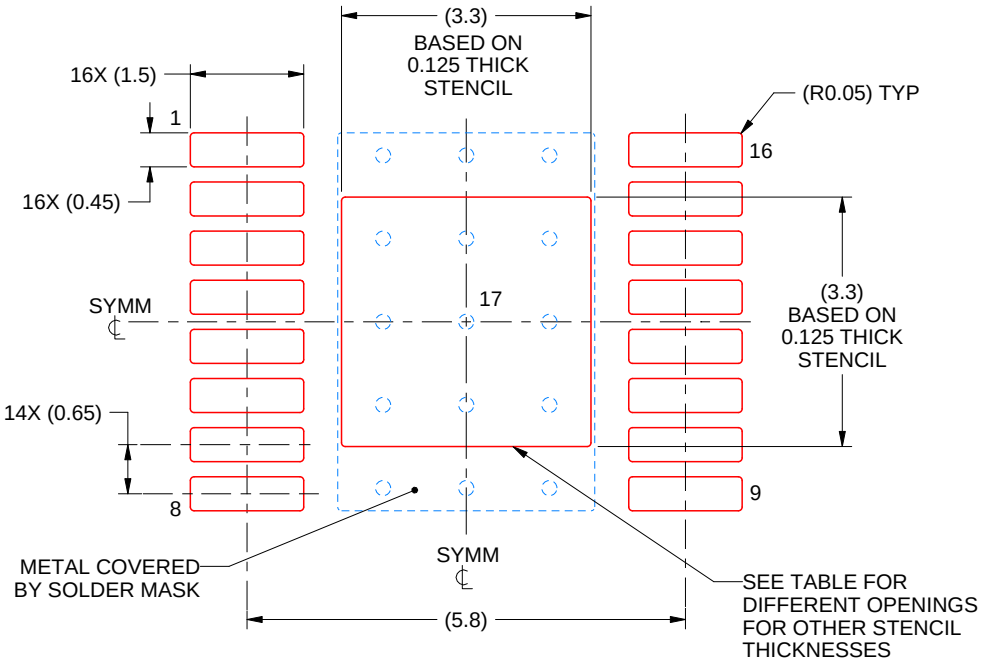


SOLDER MASK DETAILS
PADS 1-16

4214868/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.69 X 3.69
0.125	3.3 X 3.3 (SHOWN)
0.15	3.01 X 3.01
0.175	2.79 X 2.79

4214868/A 02/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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