

IRLI3803P-VB Datasheet

N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^{a, e}	Q _g (Typ)
30	0.004 at V _{GS} = 10 V	140	82 nC
	0.005 at V _{GS} = 4.5 V	120	

FEATURES

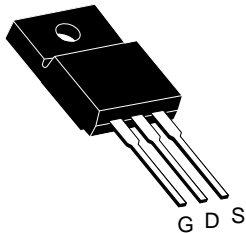
- TrenchFET[®] Power MOSFET
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2011/65/EU



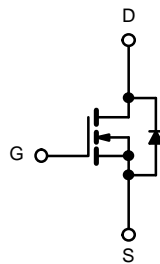
APPLICATIONS

- OR-ing
- Server
- DC/DC

TO-220 FULLPAK



Top View



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	30	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 175 °C)	I _D	T _C = 25 °C	140 ^{a, e}
		T _C = 70 °C	120 ^e
		T _A = 25 °C	28.8 ^{b, c}
		T _A = 70 °C	27 ^{b, c}
Pulsed Drain Current	I _{DM}	168	A
Avalanche Current Pulse	I _{AS}	36	
Single Pulse Avalanche Energy			
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	90 ^{a, e}
		T _A = 25 °C	3.13 ^{b, c}
Maximum Power Dissipation	P _D	T _C = 25 °C	250 ^a
		T _C = 70 °C	175
		T _A = 25 °C	3.75 ^{b, c}
		T _A = 70 °C	2.63 ^{b, c}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typ.	Max.	Unit	
Maximum Junction-to-Ambient ^{b, d}	R _{thJA}	32	40	°C/W	
Maximum Junction-to-Case	R _{thJC}	0.5	0.6		

Notes:

a. Based on T_C = 25 °C.

b. Surface mounted on 1" x 1" FR4 board.

c. t = 10 sec.

d. Maximum under steady state conditions is 90 °C/W.

e. Calculated based on maximum junction temperature. Package limitation current is 90 A.

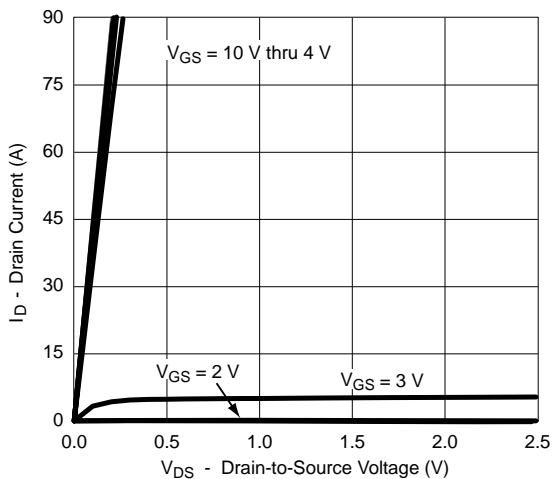
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		35		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-7.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0		2.5	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	90			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 28.8\text{ A}$		0.004		Ω
		$V_{GS} = 4.5\text{ V}, I_D = 27\text{ A}$		0.005		
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 28.8\text{ A}$		160		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		2765		pF
Output Capacitance	C_{oss}			725		
Reverse Transfer Capacitance	C_{rss}			270		
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 28.8\text{ A}$		171		nC
		$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 28.8\text{ A}$		81.5		
Gate-Source Charge	Q_{gs}	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 28.8\text{ A}$		34		
Gate-Drain Charge	Q_{gd}	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 28.8\text{ A}$		29		
Gate Resistance	R_g	$f = 1\text{ MHz}$		1.4	2.1	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 0.625\text{ }\Omega$ $I_D \cong 24\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		18	27	ns
Rise Time	t_r			11	17	
Turn-Off Delay Time	$t_{d(off)}$			70	105	
Fall Time	t_f			10	15	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 0.67\text{ }\Omega$ $I_D \cong 22.5\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		55	83	
Rise Time	t_r			180	270	
Turn-Off Delay Time	$t_{d(off)}$			55	83	
Fall Time	t_f			12	18	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$		168		A
Pulse Diode Forward Current ^a	I_{SM}			168		
Body Diode Voltage	V_{SD}	$I_S = 22\text{ A}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 20\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		52	78	ns
Body Diode Reverse Recovery Charge	Q_{rr}			70.2	105	nC
Reverse Recovery Fall Time	t_a			27		ns
Reverse Recovery Rise Time	t_b			25		

Notes:

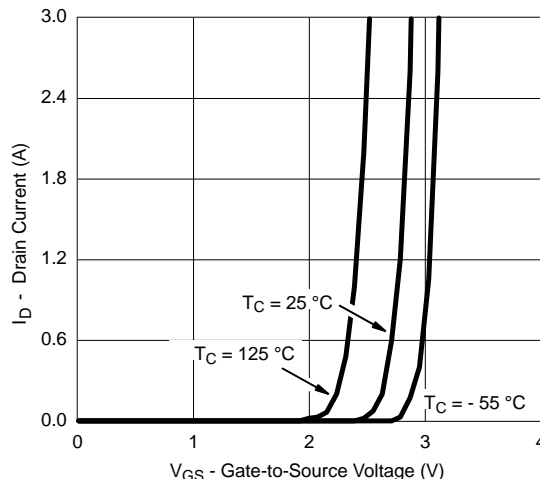
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

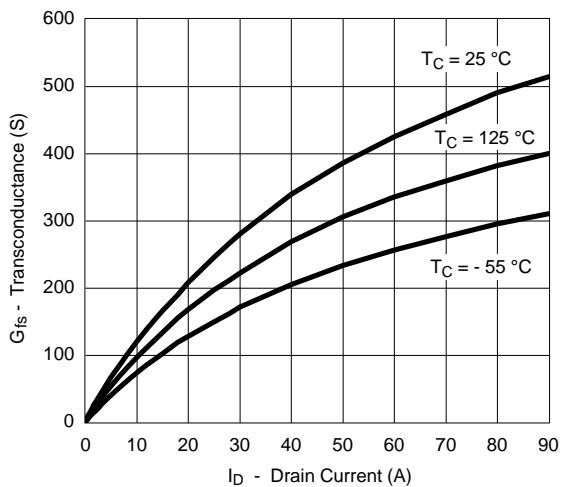
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



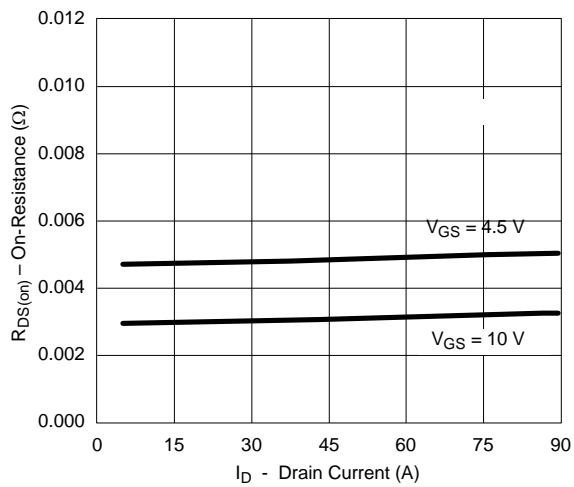
Output Characteristics



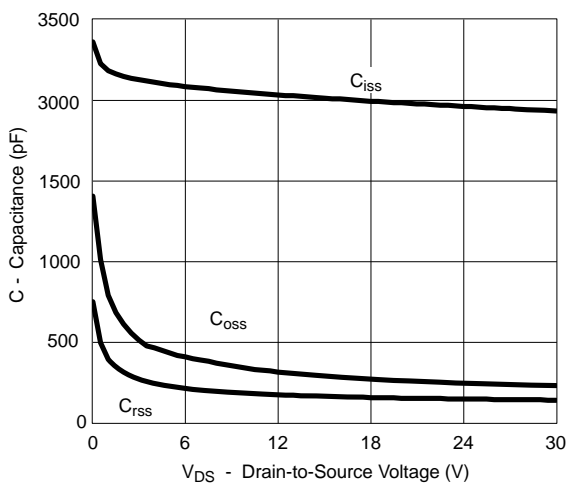
Transfer Characteristics



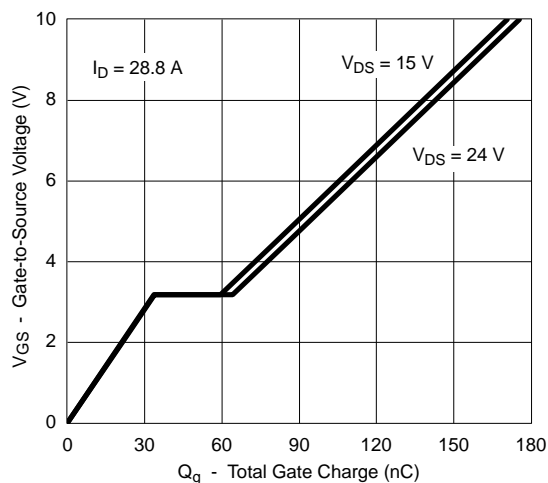
Transconductance



$R_{DS(on)}$ vs. Drain Current

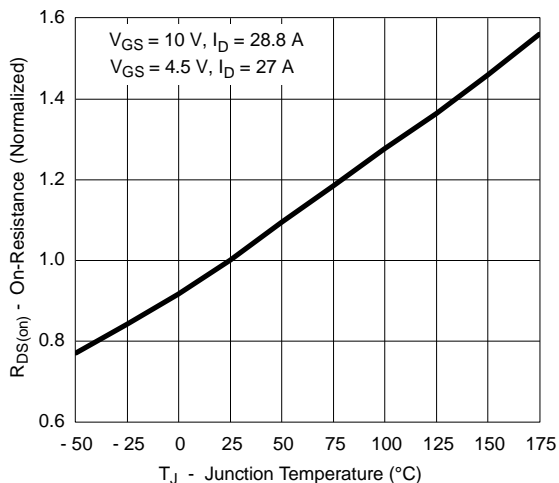


Capacitance

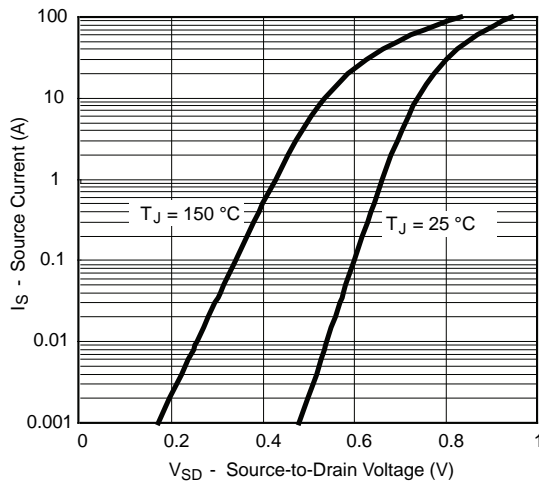


Gate Charge

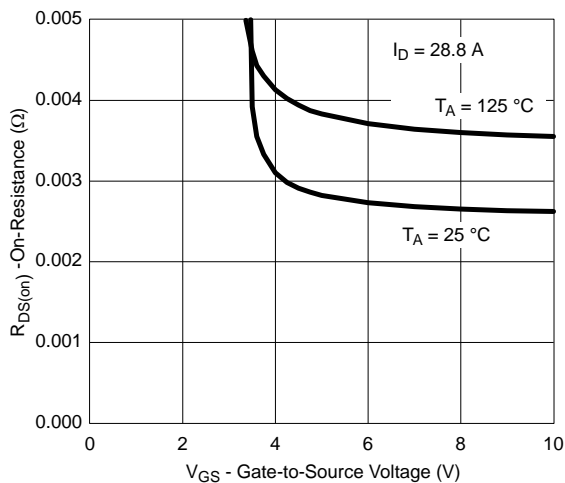
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



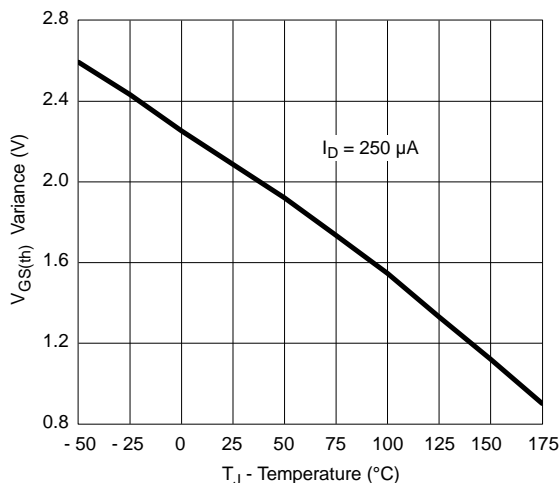
On-Resistance vs. Junction Temperature



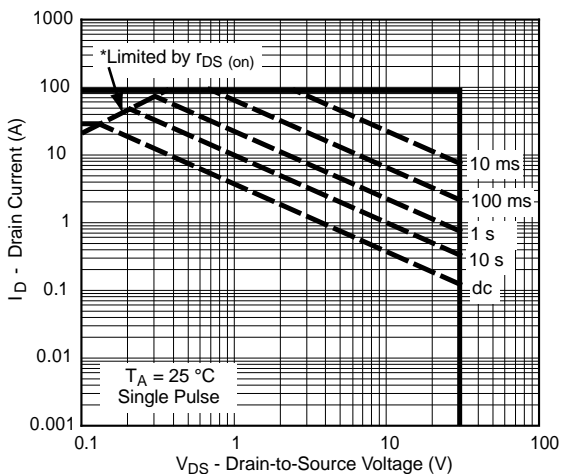
Forward Diode Voltage vs. Temperature



$R_{DS(on)}$ vs. V_{GS} vs. Temperature

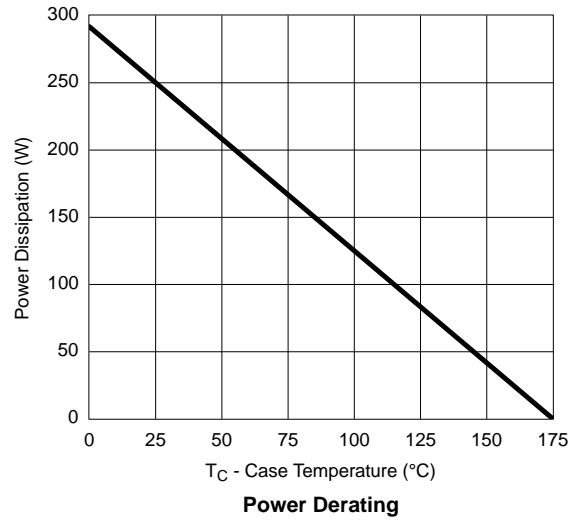
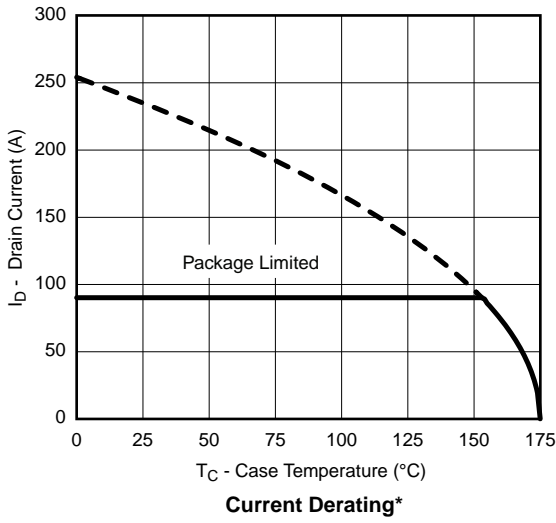


Threshold Voltage

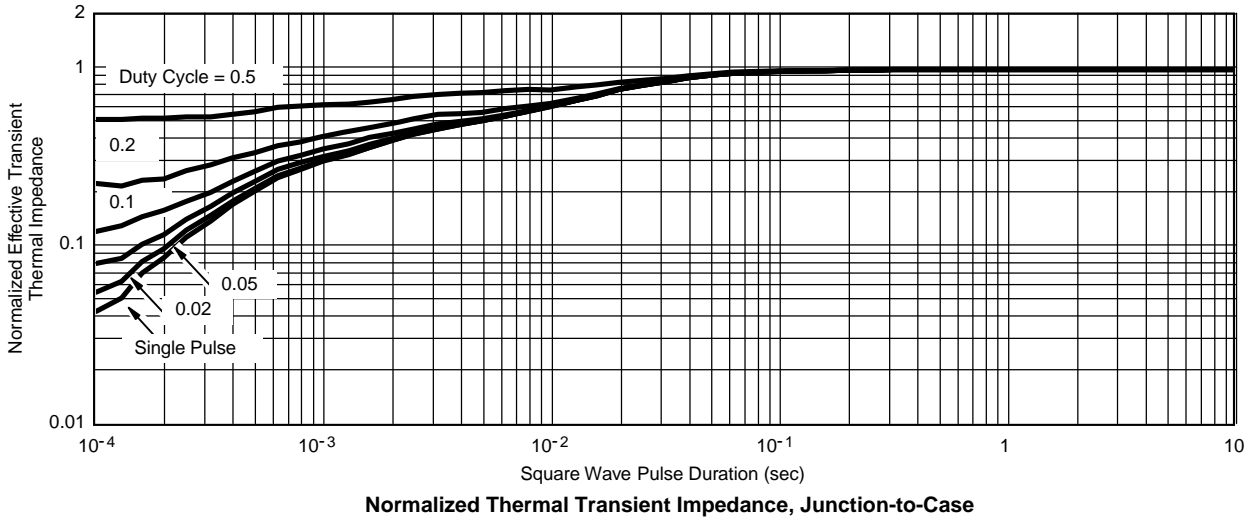


* $V_{GS} >$ minimum V_{GS} at which $r_{DS(on)}$ is specified
Safe Operating Area, Junction-to-Ambient

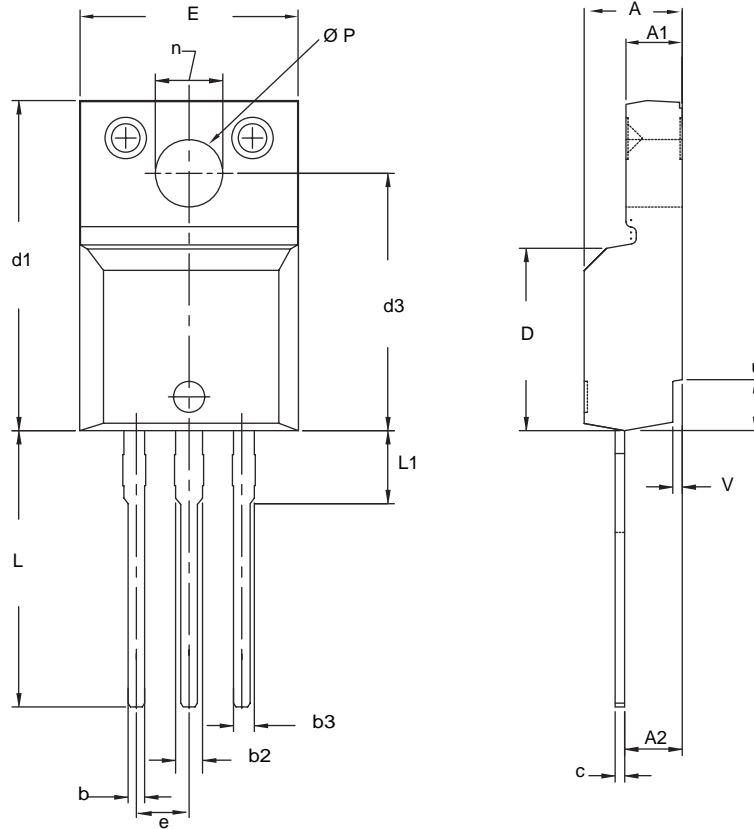
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



*The power dissipation P_D is based on T_{J(max)} = 175 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TO-220 FULLPAK (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
v	0.400	0.500	0.016	0.020

ECN: X09-0126-Rev. B, 26-Oct-09
DWG: 5972

Notes

1. To be used only for process drawing.
2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
3. All critical dimensions should C meet $C_{pk} > 1.33$.
4. All dimensions include burrs and plating thickness.
5. No chipping or package damage.

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