ANNA-B402

Stand-alone Bluetooth 5.1 low energy module

Data sheet

Abstract

This technical data sheet describes the ultra-compact ANNA-B402 stand-alone Bluetooth® 5.1 low energy module. Packed into a small, System-in-Package design, ANNA-B402 is available with external and internal antenna options. ANNA-B402 provides an open CPU architecture with a powerful MCU for customer applications, while ANNA-B412 is delivered with pre-flashed u-connectXpress software that supports OEMs with the shortest time-to-market. ANNA-B402 offers a flexible approach to development and allows OEMs to embed their own application on top of the integrated Bluetooth low energy stack, using an integrated development environment (IDE).

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This document applies to the following products:

Product name	**Type number**	**Software**	**Hardware version**	**PCN reference**	**Product status**
ANNA-B402	ANNA-B402-00B-00	Open CPU	03	N/A	Mass production

Contents

1 Functional description

1.1 Overview

ANNA-B402 is a small, stand-alone Bluetooth® 5.1 Low Energy (LE) wireless module packed into a System-in-Package (SiP) design that is particularly suited for harsh professional environments.

Based on the Nordic Semiconductor nRF52833 chip that includes an integrated RF core and powerful Arm® Cortex®-M4 with FPU processor, ANNA-B402 operates in all Bluetooth 5.1 modes – as well as 802.15.4 (Thread and Zigbee) and Nordic proprietary modes.

Featuring Angle of Arrival (AoA) and Angle of Departure (AoD) transceivers, ANNA-B402 supports the Bluetooth 5.1 Direction Finding service. The service can be used for indoor positioning, wayfinding, and asset tracking.

ANNA-B402 modules need only a single supply voltage in the range of 1.7 to 3.6 V and, as the supply voltage level can also be used as the I/O reference level, can be easily integrated into simple, single voltage rail systems. The broad supply voltage range makes ANNA-B402 particularly useful in battery powered systems. An additional 5 V supply is required if the USB interface is used.

With the same physical size and mechanical design of ANNA-B1 module, ANNA-B402 offers a natural upgrade path for existing ANNA-B1 applications. Four additional pins on the ANNA-B402, included to increase the number of supported GPIOs module, can be conveniently accommodated within a common module footprint. The upper limit of the operating temperature range for ANNA-B402 modules is extended beyond that specified for ANNA-B1 from 85 °C to 105 °C. See also the ANNA-B112 data sheet [7] and ANNA-B402 product summary [5].

1.2 Example applications

- Industrial automation
- Smart buildings and cities
- Low power sensors
- Wireless-connected and configurable equipment
- Point-of-sales
- Health devices
- Real-time Location, RTLS
- Indoor positioning
- Asset tracking
- Wearables

1.3 Block diagram

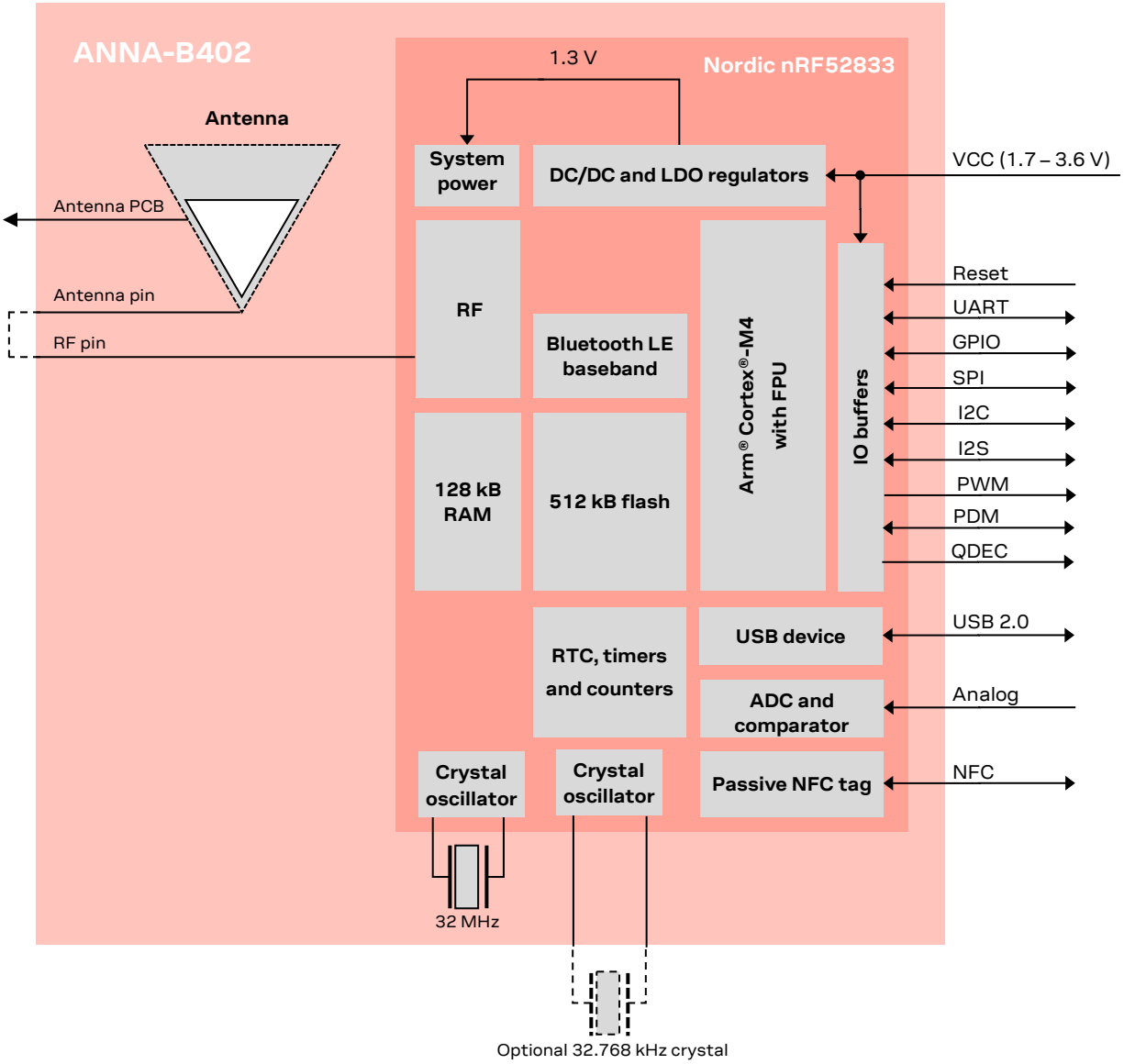


Figure 1: Block diagram of ANNA-B402

The ANNA-B402 SiP module includes an integrated antenna. The RF signal pin can either be connected directly to the adjacent antenna pin for use with the internal antenna or be routed to an external antenna or antenna connector. See also 2.4 GHz radio and internal antenna.

The module does not have an integrated low power oscillator (LPO) and, depending on the power consumption requirement, end users could connect an external LPO crystal or oscillator. See also Low frequency clock.

An integrated DC/DC converter is used for higher efficiency under heavy load situations. See also Module supply input (VCC).

1.4 Product description

Item	ANNA-B402
Chip inside	Nordic Semiconductor nRF52833
Bluetooth version	5.1
Band support	2.4 GHz, 40 channels
Typical conducted output power	+8 dBm
Max radiated output power with internal antenna (EIRP)	+9 dBm
Max radiated output power with external antenna (EIRP)	+13 dBm
RX sensitivity, 1 Mbps (conducted)	-94 dBm
RX sensitivity, 125 kbps(conducted)	-103 dBm
Supported 2.4 GHz radio modes	Bluetooth Low Energy IEEE 802.15.4 Proprietary 2.4 GHz modes
Supported Bluetooth LE data rates	1 Mbps 2 Mbps 500 kbps (Coded PHY, S=2) 125 kbps (Coded PHY, S=8)
Module size	6.5 x 6.5 x 1.2 mm

Table 1: ANNA-B402 characteristics summary

1.5 Software options

ANNA-B402 modules are integrated with an Arm® Cortex®-M4 application processor with FPU, 512 kB flash memory and 128 kB RAM.

The structure of any software running on ANNA-B402 includes the following components:

- Radio stack
- Bootloader (optional)
- Application

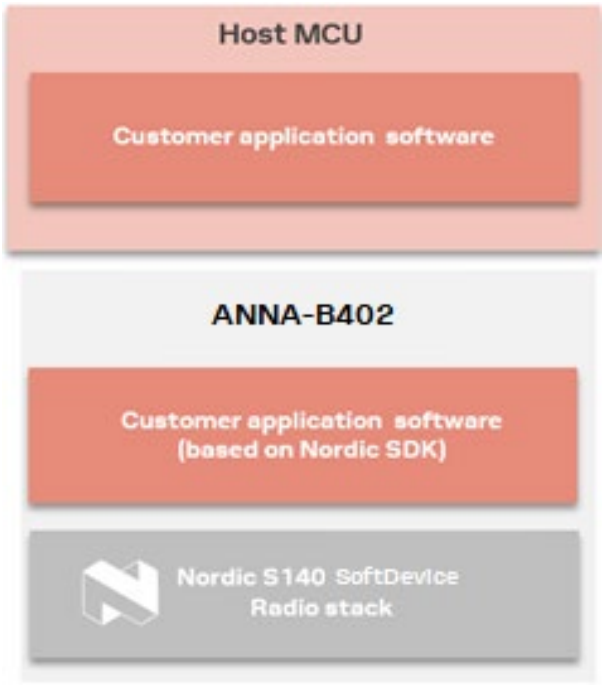


Figure 2: ANNA-B402 software structure and available software options

1.5.1 Open CPU

The open CPU architecture of ANNA-B402 allows module integrators to build their own applications. u-blox recommends Nordic software to speed up the development process.

Nordic Semiconductor software provides a rich and well-tested software development environment for nRF52 based devices. It includes a broad selection of drivers, libraries, and example applications. It also accommodates other radio stacks other than S140.

2 Interfaces

2.1 Power management

2.1.1 Module supply input (VCC)

ANNA-B402 modules use integrated step-down converters to transform the supply voltage presented at the **VCC** pin into a stable system voltage. Consequently, the module is compatible for use in battery powered designs – without the need of an additional voltage converter.

ANNA-B402 supports two on-board converters:

- Low-dropout (LDO)
- DC/DC buck

ANNA-B402 modules automatically switch between these converters to suit the prevailing current consumption. The DC/DC converter is more efficient under high loads when the radio is active, while the LDO converter is better suited for power saving modes.

☞ ANNA-B402 modules only support normal voltage mode as the supply voltage pin VDD is shorted to pin VDDH on the modules. For further information about supply voltage mode of nRF52833, see the Nordic specification.

2.2 RF antenna interfaces

2.2.1 2.4 GHz radio and internal antenna

The RF pin (**ANT**) of ANNA-B402 module is connected to the single-ended Tx/Rx antenna conection of the 2.4 GHz radio transceiver in nRF52833 chip. The nRF52833 chip has an integrated balun but requires an external filter/matching circuitry which is integrated inside of the ANNA-B402 module. The RF pin (**ANT**) of the module is matched to 50 ohms.

The internal antenna pin (**ANT_INT**) of ANNA-B402 is connected to the feeding point of the internal chip antenna in the module. In addition to the **ANT_INT** pin, three pins on ANNA-B402 (**ANT_PCB**, **ANT_GND1** and **ANT_GND2**) are also connected to the internal antenna. Matching circuitry for the internal antenna is also integrated in the ANNA-B402 module.

ANNA-B402 offers both internal and external antenna options:

- With the internal chip antenna option, the **ANT** pin shall be connected to the feeding point of the internal antenna through the **ANT_INT** pin of the module. In addition, the **ANT_PCB** pin or the **ANT_GND1** and **ANT_GND2** pins shall be connected to an external antenna strip. The pins that need to be connected, **ANT_PCB** or **ANT_GND1** and **ANT_GND2**, depends on the physical placement of the module in the application design.
- When implementing an external antenna option, the external antenna or antenna connector shall be connected to **ANT** pin through a controlled impedance trace.

☞ For information about antenna reference designs, integration instructions, and approved external antennas, see also the ANNA-B4 system integration manual [3].

2.2.2 Near Field Communication (NFC)

ANNA-B402 includes a Near Field Communication interface that can operate as a 13.56 MHz NFC tag with bit rate of 106 kbps.

As an NFC tag, data can be read from or written to the ANNA-B402 module using an NFC reader. ANNA-B402 is not capable of reading other tags or initiating NFC communications.

The NFC interface can be used to wake the module from sleep mode, which means that the module can be kept in the deepest power save mode and still wake up properly to react to an NFC field.

Two pins are available for connecting to an external NFC antenna: **NFC1** and **NFC2**.

2.2.3 Direction finding (AoA/AoD)

ANNA-B402 modules support a location Bluetooth 5.1 service called Bluetooth Direction Finding. The service is based on two solution architectures: Angle of Arrival (AoA) and Angle of Departure (AoD). Bluetooth Direction Finding is supported in 1 Mbps and 2 Mbps Bluetooth LE modes and is used for indoor positioning, wayfinding, and asset tracking.

These phase-based functions require an antenna array, estimation algorithms and processing power to make it possible to triangulate and detect the direction of a Bluetooth signal down to a sub-meter accuracy. The AoA receiver and AoD transmitter use antenna arrays, where individual antennas in the array are switched on one by one. This switching sequence allows the direction of a peer device to be calculated. The derived IQ samples are used to determine the relative path lengths between the antenna pairs and subsequent location of the transmitter.

2.3 System functions

2.3.1 Power modes

ANNA-B402 modules use power-efficient LDO and DC/DC regulators that can operate in different power modes and configurations. The various functional parts of ANNA-B402 can be powered off when they are not needed, and complex wake-up events can be generated from different external and internal inputs.

2.3.1.1 System OFF mode

System OFF mode is the deepest power saving mode. It is in this mode that ANNA-B402 sleeps, so all the core functionality is stopped to ensure minimum power consumption. The module can be put into System OFF mode by using SYSTEMOFF register.

An external event is required to wake up the module from sleep in the system OFF mode. Although ANNA-B402 always reboots after waking up from the system OFF mode, some non-volatile registers in RAM can be configured so that they remain intact during and after going to the system OFF mode.

You can switch on or reboot ANNA-B402 in any of the following ways:

- Module reset. See also Module reset
- Programmable digital or analog sensor event. In response to a rising voltage level flag from an analog comparator pin, or similar.
- NFC field detection
- 5 V supply to the **VBUS** pin (USB interface plug in)

2.3.1.2 System ON mode

When powered on or reset, ANNA-B402 returns to the default configuration set by the application software flashed in the module. In System ON mode all functional blocks and system peripherals are available in either RUN mode or in IDLE mode. The software configuration and the application under execution determines the mode of operation.

System ON mode has two optional sub-power modes, Constant Latency and Low-Power. Designers can choose which sub-power mode is most appropriate for the application, but only one can be enabled at any given time. These modes are active when the CPU or other peripherals are idling.

2.3.1.2.1 Constant latency

You can configure the CPU and other programmable peripherals to use minimal resources. The module can be turned on from sleep (System OFF mode) with constant and predictable CPU wakeup latency, but not without introducing some degradation in the power efficiency.

2.3.1.2.2 Low-Power mode

ANNA-B402 draws least power in the (default) Low-power mode. The automatic power management system in the Nordic chip limits the minimum power consumption. ANNA-B402 is turned on from sleep with varying CPU wakeup latency and peripherals tasks.

2.3.2 Module reset

A reset on ANNA-B402 module can be triggered with following different ways:

- Pin reset: A low level on the **RESET_N** input pin. If used, the software should configure a pull-up on this pin. The low-level state causes an “external” or “hardware” reset of the module.
- Power-on: Reset when VCC rises above the power-on threshold.
- Wake from System OFF: reset when module wakes from System OFF mode.
- Soft reset: Reset using the reset control register.
- Watchdog timer (WDT): Reset when module watchdog timer times out.
- Brownout: Reset when **VCC** drops below brownout threshold voltage.

2.3.3 CPU and memory

The Nordic Semiconductor nRF52833 chip in ANNA-B402 includes a powerful Arm® Cortex®-M4 with FPU processor. The processor works with a superset of 16 and 32-bit instructions (Thumb-2) at 64 MHz clock speed. It can use up to 37 interrupt vectors and 3 priority bits.

The nRF52833 chip has 512 kB of flash and 128 KB of RAM for code and data storage.

2.3.4 Direct Memory Access

All interfaces described in this data sheet support Direct Memory Access (DMA) to move any data generated from the interface directly into the RAM, without involving the CPU. This ensures fluent operation of the CPU with minimal need for interruption. To reduce the overall power consumption, DMA should be used as often as possible.

2.3.5 Programmable Peripheral Interconnect

The Nordic Semiconductor nRF52833 chip in the ANNA-B402 module includes a programmable peripheral interconnect (PPI) switch matrix that connects various control signals between different interfaces and system functions. The switch allows most interfaces to bypass the CPU when triggering a system function. In this way, an incoming data packet can trigger a counter on the falling voltage level on an ADC or toggle a GPIO – without having to send an interrupt to the CPU. This functionality facilitates the development of smart, power-efficient applications that wake up the CPU only when it is necessary.

2.3.6 Real Time Counter (RTC)

A key system feature of the module is the Real Time Counter (RTC). This counter can generate and send multiple interrupts and events to the internal and external hardware blocks, CPU, and radio. The events can be precisely timed and range from microseconds up to hours and leveraged for periodic Bluetooth LE advertising and other applications – without involving the CPU.

2.4 Low frequency clock

ANNA-B402 modules use two clocks: one high frequency clock and one low frequency clock. The high frequency clock is provided on-module by a high-accuracy 32 MHz crystal. The low frequency clock can either be provided internally by the RC oscillator, synthesized from the fast clock, or externally by a 32.768 kHz crystal. To reach minimum current consumption in some power save modes an external high precision 32.768 kHz crystal must be used. For further information see the ANNA-B4 System integration manual [3].

For information about the external 32.768 kHz crystal operating parameters and performance of the clock, see also LFXO crystal specifications.

☞ The LFXO debounce time is 0.25 s within the Normal operating temperature range (-40 to 85 °C). When using an external crystal with ANNA-B402 at operating temperatures above 85 °C, the LFXO debounce time must be set to 0.50 s in the LFXODEBOUNCE register. Increasing the LFXO debounce time lengthens the LFXO start-up time. See the Nordic nRF52833 specification [9] for further information about setting the LFXO debounce time in the LFXODEBOUNCE register.

2.5 Serial interfaces

ANNA-B402 modules provide the following serial communication interfaces:

- 2x UART interfaces: 4-wire universal asynchronous receiver/transmitter.
- 4x SPI interfaces: Up to four serial peripheral interfaces can be used simultaneously.
- 2x I2C interfaces: Inter-Integrated Circuit (I2C) interface for communication with digital sensors.
- 1x I2S interface: Used to communicate with external audio devices.
- 1x USB 2.0 device interface: The USB device interface to connect to the upstream host.

☞ Most digital interface pins on the module are shared between the digital, analog interfaces and GPIOs. Unless otherwise stated, all functions can be assigned to any pin that is not already occupied.

☞ Two of the SPI interfaces share common hardware with the I2C interfaces. These interfaces cannot be used simultaneously.

2.5.1 Universal Asynchronous Receiver/Transmitter (UART)

The 4-wire UART interface supports hardware flow control and a wide range of baud rates up to 1 Mbps. Other characteristics of the UART interface are listed below:

- Pin configuration:
  - **TXD**, data output pin
  - **RXD**, data input pin
  - **RTS**, Request To Send, flow control output pin (optional)
  - **CTS**, Clear To Send, flow control input pin (optional)
- Hardware flow control or no flow control is supported.
- Power saving indication available on the hardware flow control output (**RTS** pin): The line is driven to the OFF state when the module is not ready to accept data signals.
- Frame format configuration:
  - 8 data bits
  - Even or no-parity bit
  - 1 stop bit
- Default frame configuration is 8N1 means eight (8) data bits, no (N) parity bit, and one (1) stop bit.
- Frames are transmitted in such a way that the least significant bit (LSB) is transmitted first.

2.5.2 Serial peripheral interface (SPI)

ANNA-B402 supports up to four Serial Peripheral Interfaces with serial clock frequencies up to 8 MHz. One high speed interface, SPIM3, allows clock frequencies of up to 32 MHz. Characteristics of the SPI interfaces include:

- Pin configuration as main node:
  - **SCLK**, Serial clock output
  - **MOSI**, Main node Output Sub node Input data line
  - **MISO**, Main node Input Sub node Output data line
  - **CS**, Chip/Sub node select output, active low, selects which sub node on the bus to talk to. Only one select line is enabled by default but more can be added by customizing a GPIO pin
  - **DCX**, Data/Command signal, this signal is optional but is sometimes used by the SPI sub nodes to distinguish between SPI commands and data
- Pin configuration as sub node:
  - **SCLK**, Serial clock input
  - **MOSI**, Main node Output, Sub node Input data line
  - **MISO**, Main node Input, Sub node Output data line
  - **CS**, Chip/Sub node select input, active low, connects/disconnects the sub node interface from the bus.
- Both main node and sub nodes are supported on all the interfaces.
- The serial clock supports both normal and inverted clock polarity (CPOL) and data should be captured on rising or falling clock edge (CPHA).

2.5.3 Inter-Integrated Circuit interface (I2C)

The Inter-Integrated Circuit (I2C) interfaces can be used to transfer and/or receive data on a 2-wire bus network. ANNA-B402 can operate as both main node and sub node on the I2C bus using standard (100 kbps), fast (400 kbps), and 250 kbps transmission speeds. The interface supports clock stretching, which allows ANNA-B402 to temporarily pause any I2C communications. Up to 127 individually addressable I2C devices can be connected to the same two signals.

- Pin configuration:
  - **SCL**, clock output in main node mode, input in sub node mode
  - **SDA**, data input/output pin

This interface requires external pull-up resistors to work properly in the main node mode. See also I2C pull-up resistor values.

The pull-up resistors are also required in sub node mode and these should be placed at the main node end of the interface.

2.5.4 Inter-IC Sound interface (I2S)

The Inter-IC Sound (I2S) interface can be used to transfer audio sample streams between ANNA-B402 and external audio devices such as codecs, DACs, and ADCs. It supports original I2S and left or right-aligned interface formats in both main node and sub node modes.

- Pin configuration:
  - **MCK**, main node clock
  - **LRCK**, left right/word/sample clock
  - **SCK**, serial clock
  - **SDIN**, serial data in
  - **SDOUT**, serial data out

The main node side of an I2S interface always provides the **LRCK** and **SCK** clock signals, but some main node devices cannot generate a **MCK** clock signal. ANNA-B402 can supply a **MCK** clock signal at both main node and sub node sides to provide to those external systems that cannot generate their own clock signal. The two data signals - **SDIN** and **SDOUT** allow for simultaneous bi-directional audio streaming. The interface supports 8, 16, and 24-bit sample widths with up to 48 kHz sample rates.

2.5.5 USB 2.0 interface

ANNA-B402 includes a full speed Universal Serial Bus (USB) device interface which is compliant to version 2.0 of the USB specification. Characteristics of the USB interface include:

- Full speed device, up to 12 Mbit/s transfer speed
- MAC and PHY implemented in the hardware
- Pin configuration:
  - **VBUS**, 5 V supply input, required to use the interface
  - **USB_DP**, **USB_DM**, differential data pair
- Automatic or software-controlled pull up of the **USB_DP** pin

The USB interface has a dedicated power supply that requires a 5 V supply voltage to be applied to the **VBUS** pin. This allows the USB interface to be used even though the rest of the module might be battery powered or supplied by a 1.8 V supply.

2.6 Digital interfaces

2.6.1 Pulse Width Modulation (PWM)

ANNA-B402 provides 4x four channels PWM units that can be used to generate complex waveforms. The waveforms can be used to control motors, dim LEDs, or as audio signals if connected to the speakers. Duty-cycle sequences may be stored in the RAM to be chained and looped into complex sequences without CPU intervention. Each channel uses a single GPIO pin as output.

2.6.2 Pulse Density Modulation (PDM)

The pulse density modulation interface is used to read signals from external audio frontends like digital microphones. It supports single or dual-channel (left and right) data input over a single GPIO pin. It supports up to 16 kHz sample rate and 16-bit samples. The interface uses the DMA to automatically move the sample data into RAM without CPU intervention. The interface uses two signals: **CLK** to output the sample clock and **DIN** to read the sample data.

2.6.3 Quadrature Decoder (QDEC)

The quadrature decoder is used to read quadrature encoded data from mechanical and optical sensors in the form of digital waveforms. Quadrature encoded data is often used to indicate rotation of a mechanical shaft in either a positive or negative direction. The QDEC uses two inputs – **PHASE_A** and **PHASE_B**, and an optional **LED** output signal. The interface has a selectable sample period ranging from 128 µs to 131ms.

2.7 Analog interfaces

8 out of the 33 digital GPIOs can be multiplexed to analog functions. The following analog functions are available:

- 1x 8-channel ADC
- 1x Analog comparator*
- 1x Low-power analog comparator*

*Only one comparator can be used at any given point in time

2.7.1 Analog to Digital Converter (ADC)

The Analog to Digital Converter (ADC) is used to sample analog voltage on the analog function enabled pins of ANNA-B402. Any of the eight analog inputs can be used. Characteristics of the ADC include:

- Full swing input range of 0 V to **VCC**.
- 8/10/12-bit resolution
- 14-bit resolution while using oversampling
- Up to 200 kHz sample rate
- Single shot or continuous sampling
- Two operation modes: Single-ended or Differential
- Single-ended mode:
  - A single input pin is used
- Differential mode:
  - Two inputs are used and the voltage level difference between them is sampled

If the sampled signal level is much lower than the **VCC**, it is possible to lower the input range of the ADC to better encompass the wanted signal and achieve higher resolution. Continuous sampling can be configured to sample at a configurable time interval, or at different internal or external events, without CPU involvement.

2.7.2 Comparator

The analog comparator compares the analog voltage on one of the analog enabled pins in ANNA-B402 with a highly configurable internal or external reference voltage. Events can be generated and distributed to the rest of the system when the voltage levels cross. Further characteristics of the comparator include:

- Full swing input range of 0 V to VCC
- Two operation modes: Single-ended or Differential
- Single-ended mode: A single reference level or an upper and lower hysteresis selectable from a 64-level reference ladder with a range from 0 V to VREF, as described in Table 2.
- Differential mode: Two analog pin voltage levels are compared, optionally with a 50 mV hysteresis.
- Three selectable performance modes - High speed, balanced, or power save
- Analog comparator options. See also Analog comparator.

2.7.3 Low power comparator

In addition to the power save mode available for the comparator, there is a separate low power comparator available on the ANNA-B402 module. This allows for even lower power operation, at a slightly lower performance and with less configuration options. Characteristics of the low power comparator include:

- Full swing input range of 0 to **VCC**
- Two operation modes: Single-ended or Differential
- Single-ended mode:
  - The reference voltage **LP_VIN** is selected from a 15-level reference ladder
- Differential mode:
  - **GPIO_19** or **GPIO_20** is used as reference voltage
  - **LP_VIN** can be used to wake the system from sleep (system OFF mode)

Table 2 shows the analog pin options. For the electrical specifications for the different analog comparator options, see also Analog comparator.

Since the run current of the low power comparator is very low, it can be used as an analog trigger to wake up the CPU when the module sleeps in the System OFF mode. See also Power modes.

2.7.4 Analog pin options

Table 2 shows the supported connections of the analog functions.

☞ An analog pin may not be simultaneously connected to multiple functions.

Symbol	Analog function	Can be connected to
ADCP	ADC single-ended or differential positive input	Any analog pin or VCC
ADCN	ADC differential negative input	Any analog pin or VCC
VIN+	Comparator input	Any analog pin
VREF	Comparator single-ended mode reference ladder input	Any analog pin, VCC, 1.2 V, 1.8V or 2.4 V
VIN-	Comparator differential mode negative input	Any analog pin
LP_VIN+	Low-power comparator IN+	Any analog pin
LP_VIN-	Low-power comparator IN-	GPIO_19 or GPIO_20, 1/16 to 15/16 VCC in steps of 1/16 VCC

Table 2: Possible uses of the analog pins

2.8 GPIO

ANNA-B402 modules have a versatile pin-out. With no dedicated analog or digital interfaces, all module interfaces and functions must be allocated to a specific GPIO pin.

ANNA-B402 modules have 33 GPIO pins. Eight of these are analog-enabled pins can be assigned to an analog function.

In addition to the serial interfaces, Table 3 describes the digital and analog functions that can be assigned to a GPIO pin. Two GPIOs are optional NFC, and two GPIOs optional for implementing an external LFCLK crystal, namely XL1 and XL2.

Function	Description	Default pin	Configurable GPIOs
General purpose input	Digital input with configurable pull-up, pull-down, edge detection and interrupt generation		Any
General purpose output	Digital output with configurable drive strength, push-pull, open-collector, or open-emitter output		Any
Pin disabled	Pin is disconnected from the input and output buffers	All*	Any
Timer/ counter	High precision time measurement between two pulses/ Pulse counting with interrupt/event generation		Any
Interrupt/ Event trigger	Interrupt/event trigger to the software application/ Wake up event		Any
HIGH/LOW/Toggle on event	Programmable digital level triggered by internal or external events without CPU involvement		Any
ADC input	8/10/12/14-bit analog to digital converter		Any analog
Analog comparator input	Compare two voltages, capable of generating wake-up events and interrupts		Any analog
PWM output	Output simple or complex pulse width modulation waveforms		Any

Table 3: GPIO custom functions configuration

2.8.1 Drive strength

All GPIO pins are normally configured for low current consumption. Using this standard low-drive strength, any pin configured as an output can only source or sink a certain amount of current. If the timing requirements of any digital interface cannot be met, or if an LED requires more current than is available in this mode, a high drive strength mode is available so the digital output can draw more current. See also Digital pins.

☞ Some GPIOs can introduce noise in the system when they are configured for high drive strength or connected to a signal with a switching speed higher than 10 kHz. See also Pin assignment open CPU.

2.9 Debug interfaces

2.9.1 SWD

ANNA-B402 provides a Serial Wire Debug (SWD) interface for flashing and debugging. The SWD interface consists of two pins, **SWDCLK** and **SWDIO**.

2.9.2 Trace – Serial Wire Output

A serial trace option is available on the ANNA-B402 module as an additional pin, **SWO**. The Serial Wire Output (SWO) is used to:

- Support `printf` style debugging
- Trace OS and application events
- Emit diagnostic system information

A debugger that supports Serial Wire Viewer (SWV) is required.

2.9.3 Parallel trace

ANNA-B402 also supports parallel trace output. This allows output from the Embedded Trace Macrocell (ETM) and Instrumentation Trace Macrocell (ITM) resources in the Arm® Cortex®-M4 core of the nRF52833 chip in the ANNA-B402. The ETM trace data allows a user to record exactly how the application goes through the CPU instructions in real time. The parallel trace interface uses one clock signal and four data signals: **TRACE_CLK**, **TRACE_D0**, **TRACE_D1**, **TRACE_D2** and **TRACE_D3**.

3 Pin definition

3.1 Pin assignment open CPU

Figure 3 shows the ANNA-B402 pin-out in an unconfigured state, where:

- GND pins are shown in gray in Figure 3.
- Most of the digital or analog functions shown here and described in this data sheet can be freely assigned to any GPIO pin. Analog functions are limited to analog capable pins. For more information about the pins, see also Table 4.
- Signals shown in red are not freely assignable but are fixed to a specific pin.

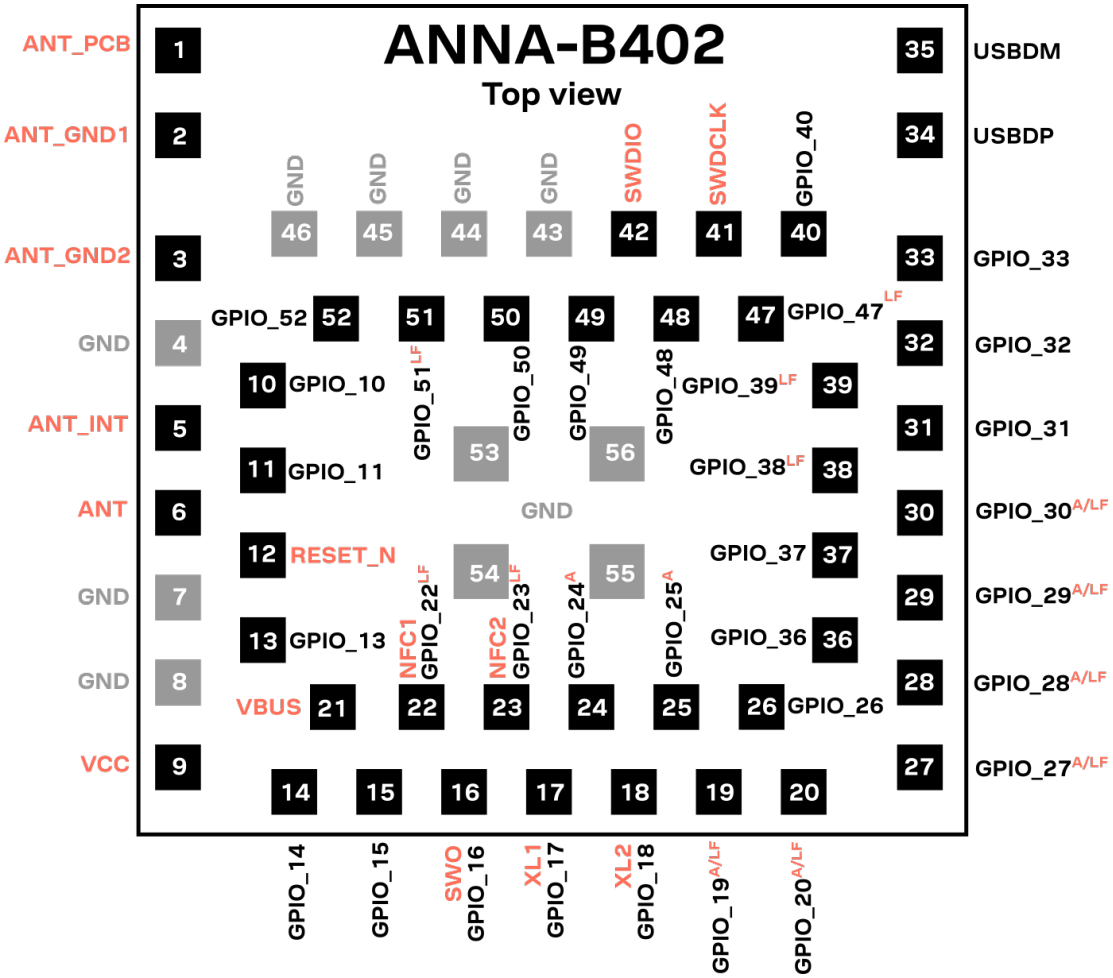


Figure 3: ANNA-B402 pin assignment (top view)

All digital or analog functions described in this data sheet may be freely assigned to any GPIO pin. Analog functions are limited to analog-capable pins.

⚠ Do not apply an NFC field to the NFC pins when they are configured as GPIOs. Applying the field in these circumstances can cause permanent damage to the module. When driving different logic levels on these pins in GPIO mode a small current leakage is expected. Ensure that NFC pins are set to the same logic level before entering any of the power saving modes. See also Digital pins.

Table 4 shows the ANNA-B402 pinout. As all GPIO pins shown as “standard drive, low-frequency I/O only” in “Remark” column of the table are physically close to the radio part of the RF chip, avoid using these pins for high-speed digital interfaces or sinking/sourcing large currents through them. Digital noise on these pins can reduce radio sensitivity.

No.	Name	nRF52 port	I/O[1]	Description	Remarks
1	ANT_PCB		-	Antenna pattern on carrier board if the module is mounted in a corner	Should only be connected if the module is mounted in a corner. See also 2.4 GHz radio and internal antenna.
2	ANT_GND1		-	Antenna ground pattern if the module is mounted in the middle of a side	Should only be connected if the module is mounted in the middle of a side. See also 2.4 GHz radio and internal antenna.
3	ANT_GND2		-	Antenna grounding if the module is mounted in the middle of a side	Should only be connected if the module is mounted in the middle of a side. See also 2.4 GHz radio and internal antenna.
4	GND		-	Ground	
5	ANT_INT		-	Feeding to internal antenna of the module	Connect to ANT pin if the internal antenna is used. See also 2.4 GHz radio and internal antenna.
6	ANT		-	Tx/Rx antenna interface	50 Ω nominal characteristic impedance. Connect to ANT_INT pin if the internal antenna is used. See also 2.4 GHz radio and internal antenna.
7-8	GND		-	Ground	
9	VCC		I	Module supply voltage input	1.7-3.6 V range.
10	GPIO_10	P0.20	I/O	General purpose I/O	
11	GPIO_11	P0.14	I/O	General purpose I/O	
12	RESET_N	P0.18	I	System reset input	Active low
13	GPIO_13	P1.09	I/O	General purpose I/O	Used as trace buffer TRACEDATA3
14	GPIO_14	P0.11	I/O	General purpose I/O	Used as trace buffer TRACEDATA2
15	GPIO_15	P0.12	I/O	General purpose I/O	Used as trace buffer TRACEDATA1
16	SWO/GPIO_16	P1.00	I/O	Serial Wire debug trace data output	Used as trace buffer TRACEDATA0; serial wire output (SWO)
17	XL1/GPIO_17	P0.00	I/O	Connection for 32.768 kHz crystal (LFXO)	May be used as a GPIO. If not used ground XL1 and XL2.
18	XL2/GPIO_18	P0.01	I/O	Connection for 32.768 kHz crystal (LFXO)	If an external clock source is used instead of a crystal: Apply external low swing signal to XL1, ground XL2. Apply external full swing signal to XL1. Leave XL2 grounded or unconnected See also the RC-oscillator configuration application note [8].
19	GPIO_19	P0.03	I/O	Analog function enabled GPIO	Pin is analog capable, standard drive, low-frequency I/O only
20	GPIO_20	P0.02	I/O	Analog function enabled GPIO	Pin is analog capable, standard drive, low-frequency I/O only
21	VBUS	VBUS	I	USB Power input (5V)	Must be connected to 5 V for the USB interface to work
22	NFC1/GPIO_22	P0.09	I/O	NFC pin 1 (default)	May be used as a GPIO, standard drive, low-frequency I/O only
23	NFC2/GPIO_23	P0.10	I/O	NFC pin 2 (default)	May be used as a GPIO, standard drive, low-frequency I/O only
24	GPIO_24	P0.05	I/O	Analog function enabled GPIO	Pin is analog capable
25	GPIO_25	P0.04	I/O	Analog function enabled GPIO	Pin is analog capable
26	GPIO_26	P0.21	I/O	General purpose I/O	
27	GPIO_27	P0.31	I/O	Analog function enabled GPIO	Pin is analog capable, standard drive, low-frequency I/O only

No.	Name	nRF52 port	I/O[1]	Description	Remarks
28	GPIO_28	P0.30	I/O	Analog function enabled GPIO	Pin is analog capable, standard drive, low-frequency I/O only
29	GPIO_29	P0.29	I/O	Analog function enabled GPIO	Pin is analog capable, standard drive, low-frequency I/O only
30	GPIO_30	P0.28	I/O	Analog function enabled GPIO	Pin is analog capable, standard drive, low-frequency I/O only
31	GPIO_31	P0.27	I/O	General purpose I/O	
32	GPIO_32	P0.06	I/O	General purpose I/O	
33	GPIO_33	P0.26	I/O	General purpose I/O	
34	USBDP	USBDP	I/O	USB differential data signal	
35	USBDM	USBDM	I/O	USB differential data signal	
36	GPIO_36	P0.16	I/O	General purpose I/O	
37	GPIO_37	P0.22	I/O	General purpose I/O	
38	GPIO_38	P0.19	I/O	General purpose I/O	Standard drive, low frequency I/O only
39	GPIO_39	P0.23	I/O	General purpose I/O	Standard drive, low frequency I/O only
40	GPIO_40	P0.15	I/O	General purpose I/O	
41	SWDCLK	SWDCLK	I	Serial wire debug clock input for debug programming	
42	SWDIO	SDWIO	I/O	Serial wire debug I/O for debug and programming	
43-46	GND		-	Ground	
47	GPIO_47	P1.07	I/O	General purpose I/O	Standard drive, low frequency I/O only
48	GPIO_48	P0.07	I/O	General purpose I/O	Used as trace buffer clock
49	GPIO_49	P0.17	I/O	General purpose I/O	
50	GPIO_50	P0.08	I/O	General purpose I/O	
51	GPIO_51	P1.01	I/O	General purpose I/O	Standard drive, low frequency I/O only
52	GPIO_52	P0.13	I/O	General purpose I/O	
53-56	GND		-	Ground	The exposed pins in the center of the module should be connected to GND

Table 4: ANNA-B402 pin-out open CPU

[1] I/O notations: I=Input, O=Output, I/O=Input or Output, PU=Pull Up, PD=Pull Down, D=Default, PP=Push-Pull, OD=Open Drain, AI/AO=Analog Input/Output, NC=Not Connected

4 Electrical specifications

Stressing the device above one or more of the ratings listed in the Absolute maximum ratings section may cause permanent damage. These are stress ratings only.

Operating the module at these or at any conditions other than those specified in the Operating conditions should be avoided. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

☞ All given application information is only advisory and does not form part of the specification.

4.1 Absolute maximum ratings

Symbol	Description	Condition	Min	Max	Unit
VCC	Module supply voltage	Input DC voltage at VCC pin	–0.3	3.9	V
V_DIO	Digital pin voltage	Input DC voltage at any digital I/O pin, VCC ≤ 3.6 V	–0.3	VCC + 0.3	V
		Input DC voltage at any digital I/O pin, VCC > 3.6 V	–0.3	3.9	V
P_ANT	Maximum power at receiver	Input RF power at antenna pin		+10	dBm

Table 5: Absolute maximum ratings

☞ The product is not protected against overvoltage or reversed voltages. Use appropriate protection devices to avoid voltage spikes that might otherwise exceed the power boundary values shown in Table 5.

4.1.1 Maximum ESD ratings

Parameter	Min	Typical	Max	Unit	Remarks
ESD sensitivity for all pins			2	kV	Human body model class 2 according to JEDEC JS001
			500	V	Charged device model according to JESD22-C101
ESD indirect contact discharge			±8*	kV	According to EN 301 489-1

*Tested on ANNA-B4 evaluation board

Table 6: Maximum ESD ratings

⚠ ANNA-B402 modules are Electrostatic Sensitive Device that require special precautions while handling. See also ESD precautions for ESD handling instructions.

4.2 Operating conditions

☞ Unless otherwise specified, all given operating condition specifications are taken at an ambient temperature of 25 °C with a supply voltage of 3.3 V.

⚠ Operation beyond the specified operating conditions is not recommended. Any extended exposure outside of these specific limits can affect the device reliability.

4.2.1 Operating temperature range

Parameter	Min	Max	Unit
Storage temperature	-40	+105	°C
Operating temperature	-40	+105	°C

Table 7: Temperature range

4.2.2 Supply/Power pins

Symbol	Parameter	Min	Typ	Max	Unit
VCC	Input supply voltage	1.7	3.3	3.6	V
t_RVCC	Supply voltage rise time			60	ms

Table 8: Input characteristics of voltage supply pins

4.2.3 Current consumption

Table 9 shows the typical current consumption of ANNA-B402 modules at 3V supply – regardless of the software that is used. A 20 ppm external crystal is used for the low frequency clock.

Condition	Typ	Unit
System OFF, no RAM retention.	600	nA
System OFF, full 128 kB RAM retention.	1.3	µA
System ON, full 128 kB RAM retention. System running on 32.768 kHz clock from internal oscillator.	2.6	µA
CPU running CoreMark benchmarking tests @ 64 MHz from flash, DC/DC	3.3	mA
Radio RX only @ 1 Mbps Bluetooth LE mode	6.0	mA
Radio TX only, 0 dBm output power	6.0	mA
Radio TX only, +8 dBm output power	15.5	mA

Table 9: Module VCC current consumption

⚠ Make sure that the configured output power of your application product does not exceed the maximum allowed limits for your intended target market(s). For information about the applicable limits and other regulatory requirements for each market area, see also the ANNA-B4 system integration manual [3].

4.2.4 RF performance

Parameter	Test condition	Min	Typ	Max	Unit
Receiver input sensitivity	Conducted at 25 °C, 1 Mbps Bluetooth LE mode		–94		dBm
	Conducted at 25 °C, 2 Mbps Bluetooth LE mode		–91		dBm
	Conducted at 25 °C, 500 kbps Bluetooth LE mode		–97		dBm
	Conducted at 25 °C, 125 kbps Bluetooth LE mode		–103		dBm
Maximum output power	Conducted at 25 °C		+8		dBm
Internal antenna gain	Mounted on an EVB-ANNA-B4		+0.5		dBi

Table 10: RF performance

4.2.5 Flash memory

Table 11 describes the endurance and retention characteristics for the flash memory.

Flash memory	Comment	Min.	Unit
Endurance		10 000	Write/erase cycles
Retention at 85 °C		10	Years
Retention at 105 °C	Limited to 1000 write/erase cycles	3	Years
Retention at 105 °C 85 °C, execution split	Limited to 1000 write/erase cycles. 75% execution time at 85 °C or less	6.7	Years

Table 11: Flash memory endurance and retention

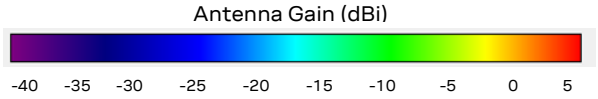
4.2.6 LFXO crystal specifications

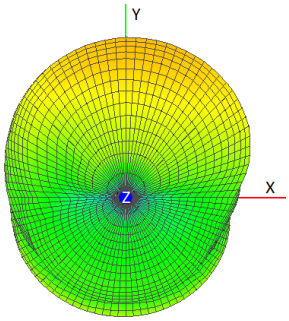
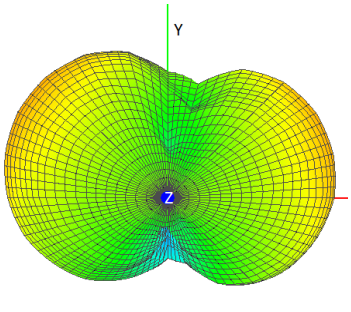
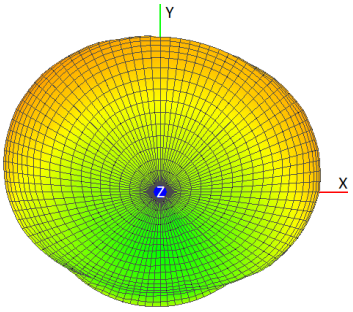
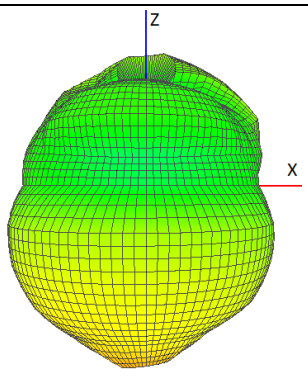
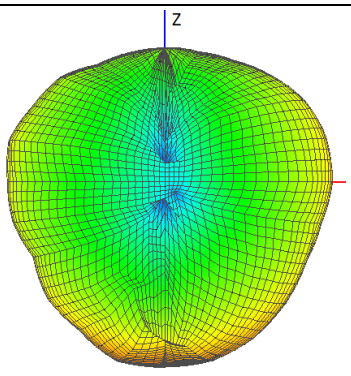
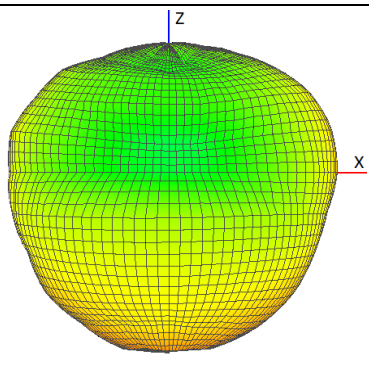
Symbol	Parameter	Typ.	Max.	Unit
F_{NOM_LFXO}	Crystal frequency	32.768	-	kHz
$F_{TOL\_LFXO\_BLE}$	Frequency tolerance, Bluetooth low energy applications[2]	-	±500	ppm
$f_{TOL\_LFXO\_ANT}$	Frequency Tolerance, ANT applications[3]	-	±50	ppm
C_{L_LFXO}	Load Capacitance	-	12.5	pF
C_{0_LFXO}	Shunt Capacitance	-	2	pF
R_{S_LFXO}	Equivalent series resistance	-	100	kΩ
C_{pin}	Input Capacitance on XL1 and XL2 pads	5	-	pF

Table 12: 32.768 kHz crystal (LFXO)

4.2.7 ANNA-B402 radiation patterns

Table 13 describes the radiation patterns for ANNA-B402. The antenna radiation test setup utilizes the reference design that comprises an evaluation board with ANNA-B402 situated in the corner of the EVK-ANNA-B402 board. For more information about the antenna reference design, see also the ANNA-B402 system integration manual [3].



View	Vertical polarization	Horizontal polarization	Total
Top view Z 			
Side view –Y 			

[2] $f_{TOL\_LFXO\_BLE}$ and $f_{TOL\_LFXO\_ANT}$ are the maximum allowed frequency tolerances for Bluetooth low energy and ANT applications. Actual tolerance depends on the crystal used.
[3] The ANT protocol requires the use of an external crystal.

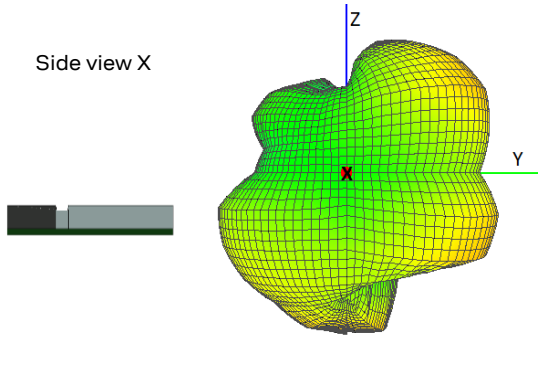
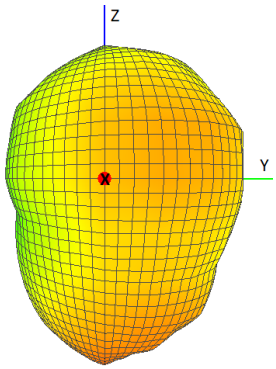
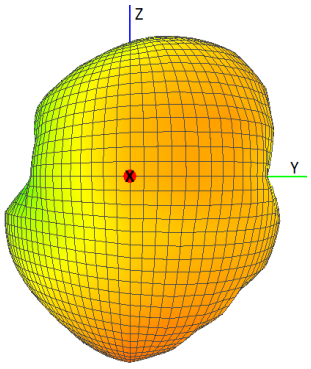
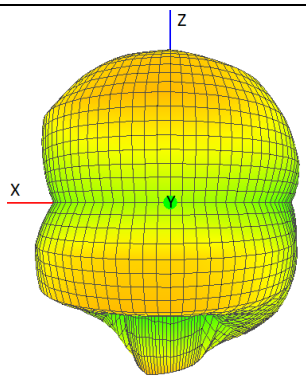
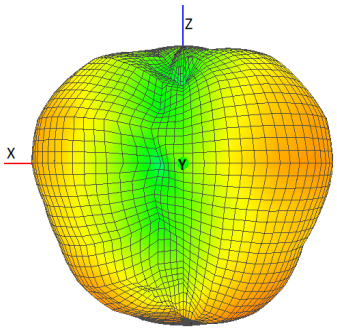
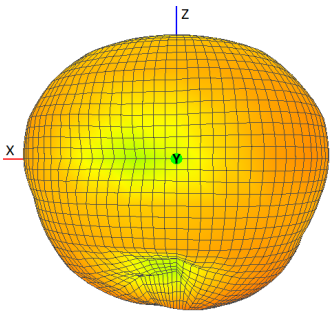
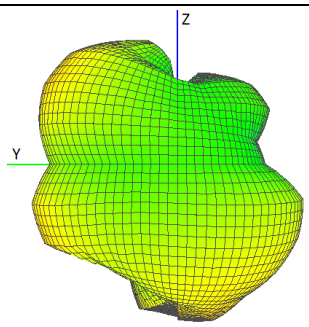
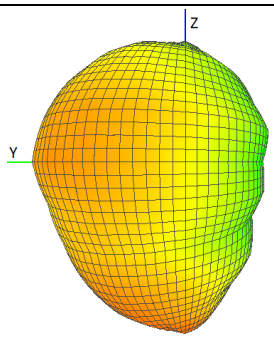
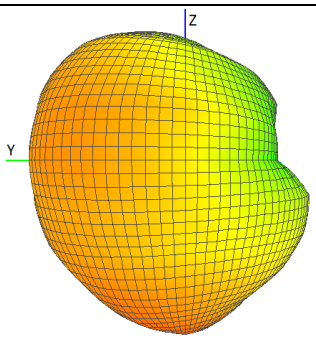
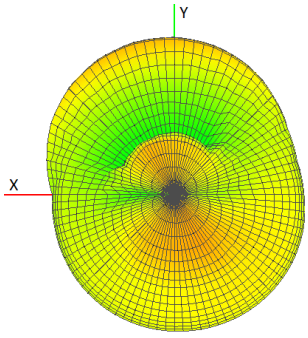
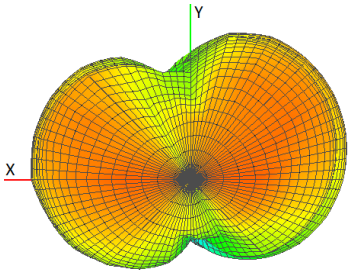
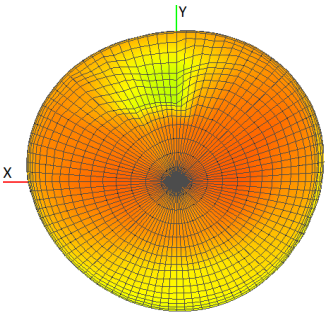
View	Vertical polarization	Horizontal polarization	Total
Side view X			
Side view Y			
Side view -X			
Bottom view –Z			

Table 13: Antenna radiation patterns

4.2.8 RESET_N pin

Pin name	Parameter	Min	Typ	Max	Unit	Remarks
RESET_N	Low-level input	0		0.3*VCC	V	
	Internal pull-up resistance		13		kΩ	
	RESET duration			55	ms	Time taken to release a pin reset.

Table 14: RESET_N pin characteristics

4.2.9 Digital pins

Pin name	Parameter	Min	Typ	Max	Unit	Remarks
Any digital pin	Input characteristic: Low-level input	0		0.3*VCC	V	
	Input characteristic: high-level input	0.7*VCC		VCC	V	
	Output characteristic: Low-level output	0		0.4	V	Standard drive strength
		0		0.4	V	High drive strength
	Output characteristic: High-level output	VCC-0.4		VCC	V	Standard drive strength
		VCC-0.4		VCC	V	High drive strength
	Sink/Source current	1	2	4	mA	Standard drive strength
		3			mA	High drive strength, VCC < 2.7 V
		6	10	15	mA	High drive strength, sink, VCC ≥ 2.7 V
		6	9	14	mA	High drive strength, source, VCC ≥ 2.7 V
	Rise/Fall time		9 – 25		ns	Standard drive strength, depending on load capacitance
			4 – 8		ns	High drive strength, depending on load capacitance
	Input pull-up resistance	11	13	16	kΩ	Can be added to any GPIO pin configured as input
	Input pull-down resistance	11	13	16	kΩ	Can be added to any GPIO pin configured as input
GPIO_22, GPIO_23	Leakage current		1	10	µA	When not configured for NFC and driven to different logic levels, Operating temperature < 85 °C
			1	15	µA	When not configured for NFC and driven to different logic levels, Operating temperature > 85 °C

Table 15: Digital pin characteristics

4.2.10 I2C pull-up resistor values

Symbol	Parameter	Bus capacitance	Min	Typ	Max	Unit
R_PUstandard	External pull-up resistance required on I2C interface in standard mode (100 kbps)	50 pF	1	-	23	kΩ
		200 pF	1	-	6	kΩ
		400 pF	1	-	5	kΩ
R_PUfast	External pull-up resistance required on I2C interface in fast mode (400 kbps)	50 pF	1	-	7	kΩ
		200 pF	1	-	1.75	kΩ
		400 pF	1	-	1	kΩ

Table 16: Suggested pull-up resistor values

4.2.11 Analog comparator

Symbol	Parameter	Min	Typ	Max	Unit
t_powersave	Time to generate interrupt/event when the comparator is in power save mode		0.6		µs
t_balanced	Time to generate interrupt/event when the comparator is in balanced mode		0.2		µs
t_speed	Time to generate interrupt/event when the comparator is in high-speed mode		0.1		µs

Table 17: Electrical specification of the two analog comparators

5 Mechanical specifications

Figure 4 shows a side view of the mechanical outline and the critical dimensions of the ANNA-B402 package.

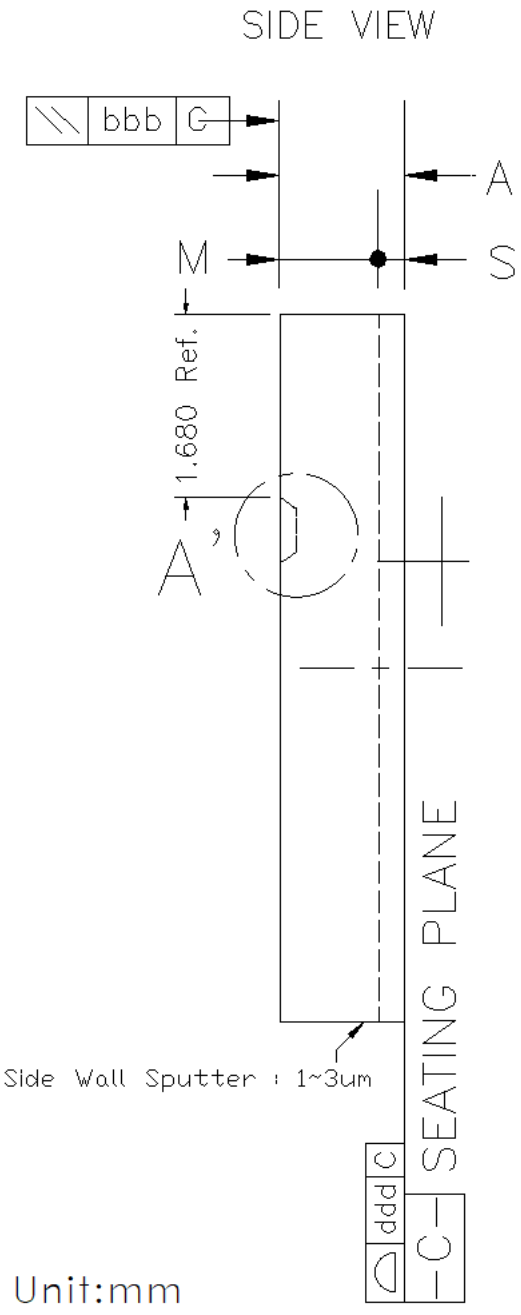


Figure 4: ANNA-B402 physical package – side view

Figure 5 shows a bottom view of the mechanical outline and the critical dimensions of the ANNA-B402 package.

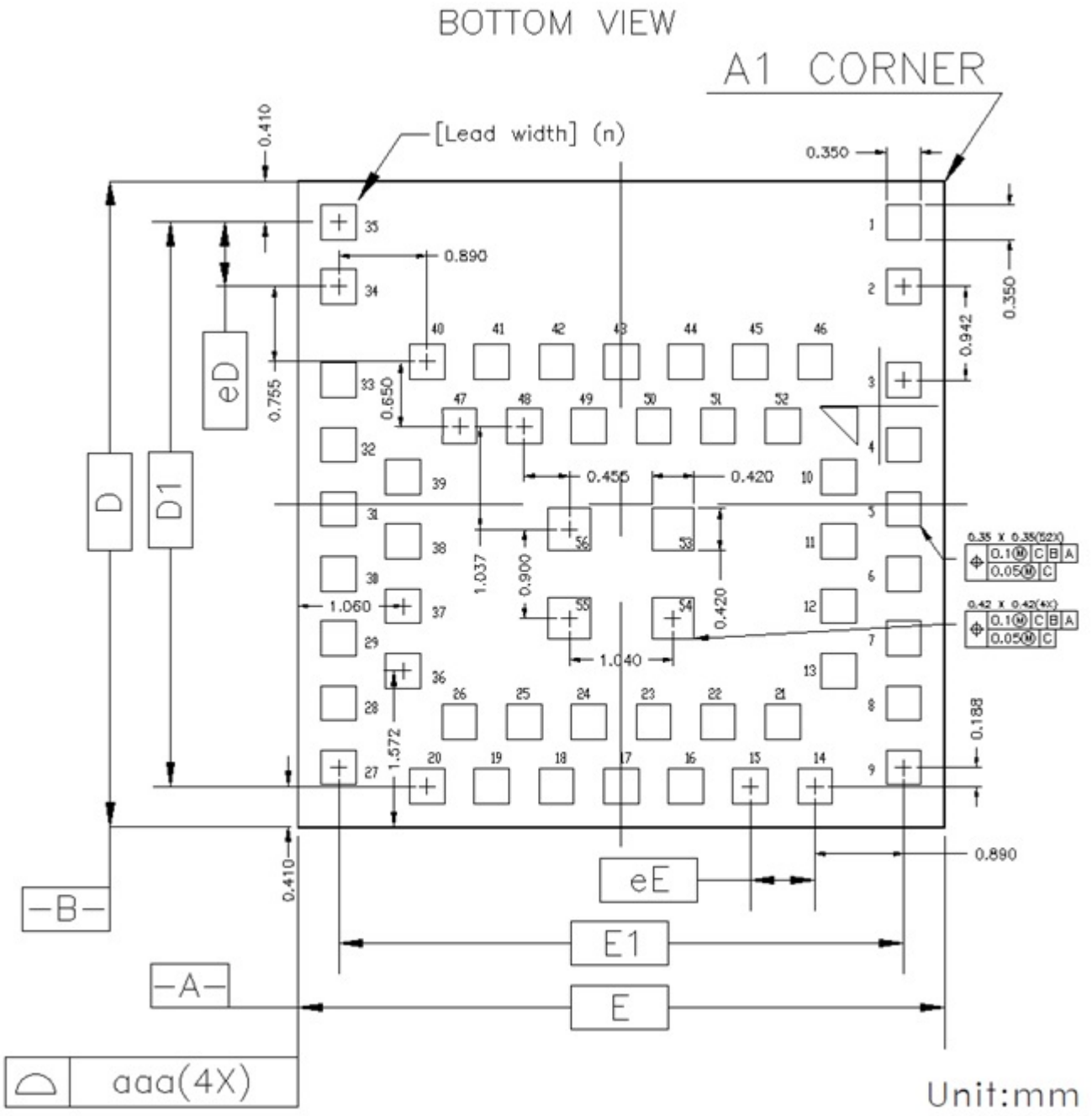


Figure 5: ANNA-B402 physical package outline – bottom view

Figure 6 describes the minimum, nominal, and maximum dimensions together with the symbols for the physical package outline of the ANNA-B402 module.

Description		Symbol	Dimensions(mm)		
			MIN	NOM	MAX
Package :			PIM		
Body Size:	X	E	6.400	6.500	6.600
	Y	D	6.400	6.500	6.600
Lead Pitch :	X	eE	0.650		
	Y	eD	0.650		
Total Thickness :		A	1.150 +/- 0.100		
Mold Thickness :		M	0.910		
Substrate Thickness :		S	0.240		
Lead width:			0.350x0.350 / 0.420x0.420		
Package Edge Tolerance :		aaa	0.100		
Mold Flatness :		bbb	0.100		
Coplanarity:		ddd	0.100		
Lead Count :		n	56		
Edge Lead Center to Center :	X	E1	5.680		
	Y	D1	5.680		

Figure 6: ANNA-B402 physical package - parameters, symbols, and dimensions

6 Qualification and approvals

6.1 Country approvals

The ANNA-B402 module is certified for use in the following countries/regions:

Country/region	ANNA-B402
Europe	Approved
Great Britain (UKCA)	Approved
USA	Approved
Canada	Approved
Japan	Approved
Taiwan	Approved
South Korea	Approved
Brazil	Approved
Australia	Approved
New Zealand	Approved
South Africa	Approved

☞ For detailed information about the regulatory requirements that must be met when using ANNA-B402 in an end product, see also the ANNA-B4 system integration manual [3].

6.2 Bluetooth qualification

The ANNA-B402 module is a Bluetooth qualified design, listed in accordance with the Bluetooth 5.1 specification.

All products that use Bluetooth technology must be qualified with the Bluetooth Special Interest Group (SIG) to obtain its own declaration ID. This is applicable also for products that are using an already Bluetooth qualified module.

The Bluetooth Qualification Process is initiated at the Bluetooth SIG Launch Studio website. When submitting the qualification, use the “Qualification without required testing” path, and combine the QDID for the Host Subsystem (the Bluetooth stack) with the QDID of the SoftDevice Controller Subsystem according to the table at the Nordic TechDocs web page [1]. The QDIDs to be selected depends on the software version.

Product type	QDID
Host subsystem	See table at Nordic TechDocs [1]
SoftDevice controller subsystem	See table at Nordic TechDocs [1]

Table 18: Bluetooth qualified design IDs for ANNA-B402

7 Product handling

7.1 Packaging

ANNA-B402 modules are delivered as hermetically sealed, reeled tapes to enable efficient production, production lot set-up and tear-down.

7.2 Reels

Information about the reel types for ANNA-B4 modules are provided in Table 19. See also the Packaging information reference guide [1]

Model	Reel type	Reel part number	Qty
ANNA-B402	F	MYR-131-BB	500 pcs/reel

Table 19: Reel type for ANNA-B402

7.3 Tapes

Figure 7 shows the position and orientation of ANNA-B4 modules as they are delivered on tape.

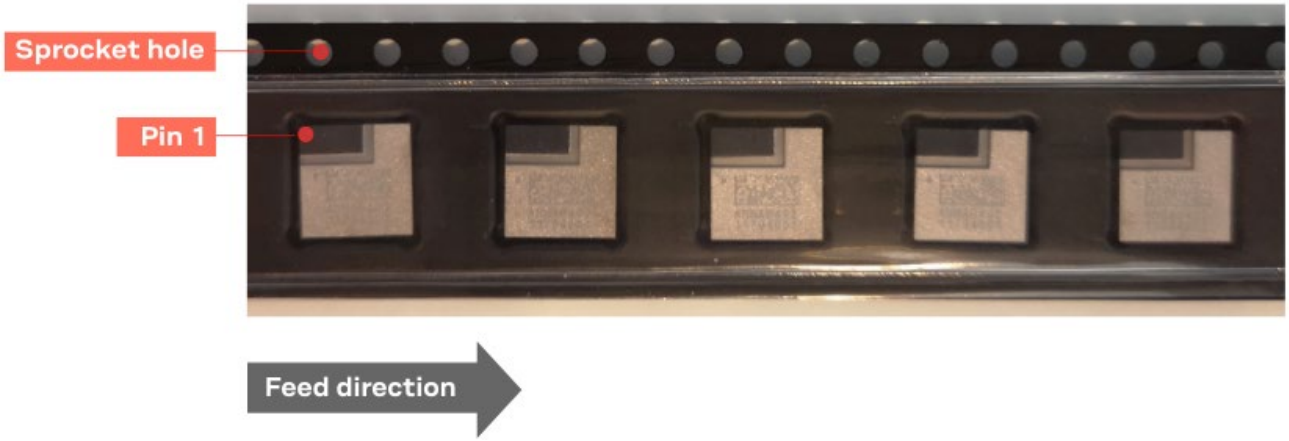
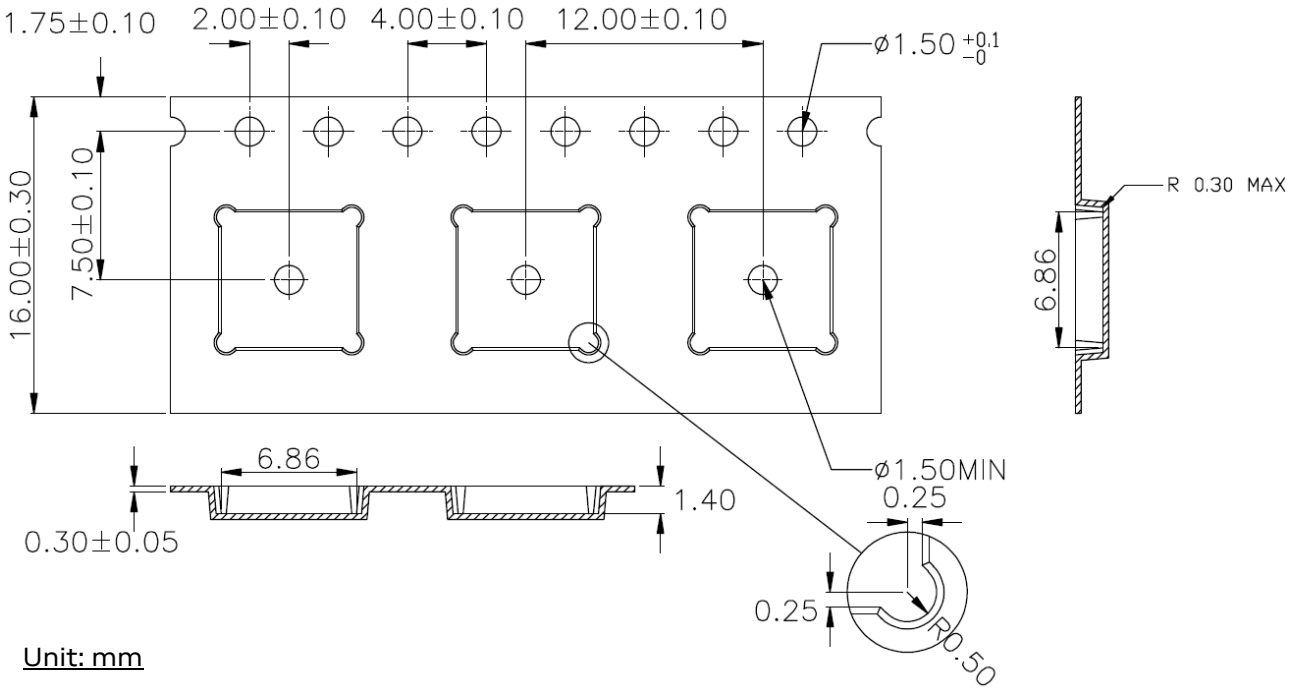


Figure 7: Orientation of ANNA-B4 modules on tape

Figure 8 shows the critical dimensions of the tapes. See also the Packaging information reference guide [1].



Unit: mm

Sprocket hole pitch cumulative tolerance ±0.20.
Carrier camber is within 1mm in 250mm.
Material: Black Conductive Polyester Allow (ABS+PS).
All dimensions meet EIA-481-D requirements.
Thickness: 0.30±0.05 mm.
Surface resistivity: 105~109 Ω/sq.

Figure 8: ANNA-B4 tape dimensions

7.4 Moisture sensitivity levels

ANNA-B402 modules are rated as MSL Level 3 devices in accordance with the IPC/JEDEC J STD-020 standard. For more information, see the moisture sensitive warning label on the MBB (Moisture Barrier Bag).

After opening the dry pack, the modules must be mounted within 168 hours in factory conditions of maximum 30 °C/60% RH or must be stored at less than 10% RH. The modules require baking if the humidity indicator card shows more than 10% when read at 23±5 °C or if the conditions mentioned above are not met. For information about the bake procedure, see also the J-STD-033B standard.

For more information about the MSL (Moisture Sensitivity Level), labeling, and storage, see also the Packaging information guide [1].

7.5 Reflow soldering

ANNA-B402 modules are approved for two-time reflow processes.

Reflow soldering profiles must be selected in accordance with u-blox soldering recommendations described in the ANNA-B4 system integration manual [3]. Failure to observe these recommendations can result in severe damage to the device.

7.6 ESD precautions

ANNA-B402 modules are Electrostatic Sensitive Devices that demand the observance of special handling precautions against static damage. Failure to observe these precautions can result in severe damage to the product. See also Maximum ESD ratings.

Proper ESD handling and packaging procedures must be applied throughout the processing, handling, and operation of any application that incorporates the module. ESD precautions are particularly relevant when handling the application board on which the module is mounted.

For further information about the handling of ANNA-B402 modules, see also the ANNA-B4 system integration manual [3].

8 Labelling and ordering information

8.1 Product marking

Figure 9 and Table 20 describe the laser markings on ANNA-B402 modules.

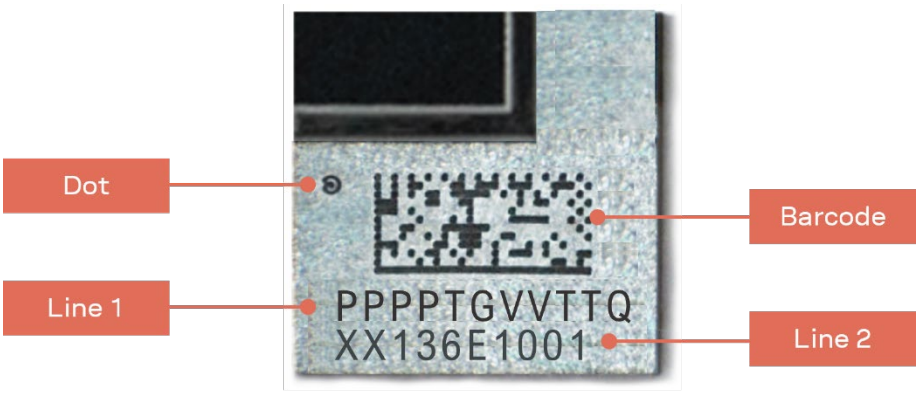


Figure 9: Product marking layout

Item	Description	Example
Dot	Pin 1 corner indication for assembly orientation	-
Line 1	**Product name, major version, and product grade**	
Pos 1–8	Product name	ANNAB402
Pos 9-10	Major product version	00
Pos 11	Quality grade	B
Line 2	**Minor version and production date**	
Pos 1–2	Minor product version	00
Pos 3	Last digit of production year	1
Pos 4–5	Week number of production date	36
Pos 6–7	Assembly mother lot, last digits	E1
Pos 8–10	Assembly sub lot number	001

2D barcode		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
		Year	**Assembly mother lot#**						**Sub lot#**			**Strip#**		**X axis**		**Y axis**	
	Example	8	3	6	U	B	E	1	0	0	1	0	1	0	1	0	1

Table 20: ANNA-B402 laser marking data

See also Product identifiers and Identification codes.

8.2 Product identifiers

Table 21 describes the three product identifiers; specifically, the Product name, Ordering code and Type number.

Format	Description	Nomenclature
Product name	Describes the form factor, platform technology and platform variant. Used mostly in product documentation like this data sheet, the product name represents the most common identity for all u-blox products	PPPPTGVV (Line1, position 1–8)
Ordering code	Comprises the product name – with additional identifiers to describe the major product version and quality grade	PPPPTGVVTTQ (Line1, position 1–11)
Type number	Comprises the product name and ordering code – with additional identifiers to describe minor product versions.	PPPP -TGVV-TTQ-XX (Line1, position 1–11) (Line 2, position 1–2)

Table 21: Product code formats

8.3 Identification codes

Table 22 explains the parts of the product code.

Code	Meaning	Example
PPPP	Form factor	ANNA

TG	Platform (Technology and Generation)
	• T – Dominant technology, For example,
	  ○ W: Wi-Fi,
	  ○ B: Bluetooth
	• G – Generation
		B4: Bluetooth Generation 4

VV	Variant based on the same platform; range [00…99]	02: default mounting, with internal antenna
TT	Major Product Version	00: first revision
Q	Quality grade • A: Automotive • B: Professional • C: Standard	B: professional grade
XX	Minor product version (not relevant for certification)	Default value is 00

Table 22: Part identification code

8.4 Ordering information

Ordering code	Product
ANNA-B402-00B	ANNA-B402 module with the option to use either an internal antenna or an external antenna.

Table 23: Product ordering codes

Appendix

A Glossary

Abbreviation	Definition
ADC	Analog to digital converter
BLE	Bluetooth Low Energy
BPF	Band pass filter
CTS	Clear to send
ESD	Electrostatic discharge
FCC	Federal Communications Commission
GATT	Generic ATTribute profile
GPIO	General purpose input/output
IC	Industry Canada
I2C	Inter-integrated circuit
LPO	Low power oscillator
MCU	Micro controller unit
MSD	Moisture sensitive device
RF	Radio frequency
RTOS	Real time operating system
SiP	System in package
SPI	Serial peripheral interface
UART	Universal asynchronous receiver/transmitter

Table 24: Explanation of the abbreviations and terms used

Related documents

[1] Packaging information reference, UBX-14001652
[2] u-connectXpress AT commands manual, UBX-14044127
[3] ANNA-B4 system integration manual, UBX-21000517
[4] u-connectXpress software user guide, UBX-16024251
[5] ANNA-B402 product summary, UBX-20017979
[6] ANNA-B412 product summary, UBX-21025292
[7] ANNA-B112 data sheet, UBX-18011707
[8] RC oscillator configuration, application note, UBX-20009242
[9] Nordic nRF52833 product specification, 4452_021
[10] Nordic Semiconductor Tech Docs site with Bluetooth QDIDs, Bluetooth QDIDs

For product change notifications and regular updates of u-blox documentation, register on our website, www.u-blox.com.

Revision history

Revision	Date	Name	Comments
R01	12-Mar-2021	bcur, asoh	Initial draft
R02	16-July-2021	yach	Updated product status to Prototype. Updated Rx Sensitivity levels in Table 1 and Table 10. Updated internal antenna gain in Table 10. Updated storage temperature in Table 7. Revised labelling information and included other minor editorial updates.
R03	19-Oct-2021	lalb	Revised metadata and disclosure restriction class.
R04	21-Jan 2022	yach	Updated product status to Engineering Sample. Updated internal antenna gain in Table 10. Updated max radiated output power with external antenna (EIRP) to 13 dBm in Table 1. Updated antenna radiation patterns in Table 13. Updated pictures of ANNA-B402 outline and dimensions with better resolution in Figure 6. Corrected the description by swapping X and Y axis in the 2D barcode laser marking in Table 20. Removed “ANNA-B4 series certification application note” from the Related Documents section and included reference to the related information in the “ANNA-B4 system integration manual” instead. Removed obsolete Antennas section with added references to information in the System integration manual. Removed ambiguous description of operating condition ranges in Electrical specifications. Updated information describing Moisture sensitivity levels, Reflow soldering, and ESD precautions. Revised Maximum ESD ratings.
R05	21-Sept-2022	yach, fkru	Updated product status to Initial production (hardware version to 03) in the Document information. Added details about the completed Bluetooth SIG qualification / listing in section Bluetooth qualification. Removed “pending” in section Country approvals for the now completed country certifications in US, Canada, Europe, Great Britain, Japan, Australia, New Zealand, South Korea, and Brazil. Removed unapplicable information ‘VCC_IO’ in the Block diagram, Module supply input (VCC) and Supply/Power pins sections. Added information about the supply voltage mode of ANNA-B402 modules in Module supply input (VCC). Clarified information describing the use of an external crystal with ANNA-B402 at operating temperatures above 85 °C in Low frequency clock. Removed unapplicable information “VCC_ripple” from Table 8. As it is mostly standard baud rates that are supported in the module, removed the bullet previously describing non-standard baud rates support in section Universal Asynchronous Receiver/Transmitter (UART). Revised the orientation of ANNA-B4 modules on tape in Figure 7. Added table data for endurance and data retention in Flash memory. Added y-direction distance of pad 40 and pad 47 in Figure 5: ANNA-B402 physical package outline – bottom view. Updated contact information. Included other minor editorial updates throughout the document.
R06	29-Feb-2024	mape, lalb, yach	Updated product status to Mass production in the Document information. Added more information about the Bluetooth declaration process in Bluetooth qualification. Changed description of PWM units in Pulse Width Modulation (PWM). Changed the approval status to “Approved” for Taiwan and South Africa in Country approvals. Updated from target values to final values for ESD sensitivity and added ESD sensitivity for ANT pin in Maximum ESD ratings.

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