LMP91051 Configurable AFE for Nondispersive Infrared (NDIR) Sensing Applications

Check for Samples: LMP91051

FEATURES

- **Dual Channel Input**
- **Programmable Gain Amplifier**
- **"Dark Signal" Offset Cancellation**
- **Supports External Filtering**
- **Common Mode Generator and 8 Bit DAC**
- **Package 14 Pin TSSOP**

APPLICATIONS

- **NDIR Sensing**
- **Demand Control Ventilation**
- **Building Monitoring**
- **CO2 Cabin Control — Automotive**
- **Alcohol Detection — Automotive**
- **Industrial Safety and Security**
- **GHG & Freons Detection Platforms**

KEY SPECIFICATIONS

- **Programmable Gain … 167V/V to 7986V/V**
- **Low Noise (0.1 to 10 Hz) … 0.1µVRMS**
- **Gain Drift … 20 ppm/°C (typ)**
- **Phase Delay Drift … 300 ns (typ)**
- **Power supply voltage range … 2.7V to 5.5V**

DESCRIPTION

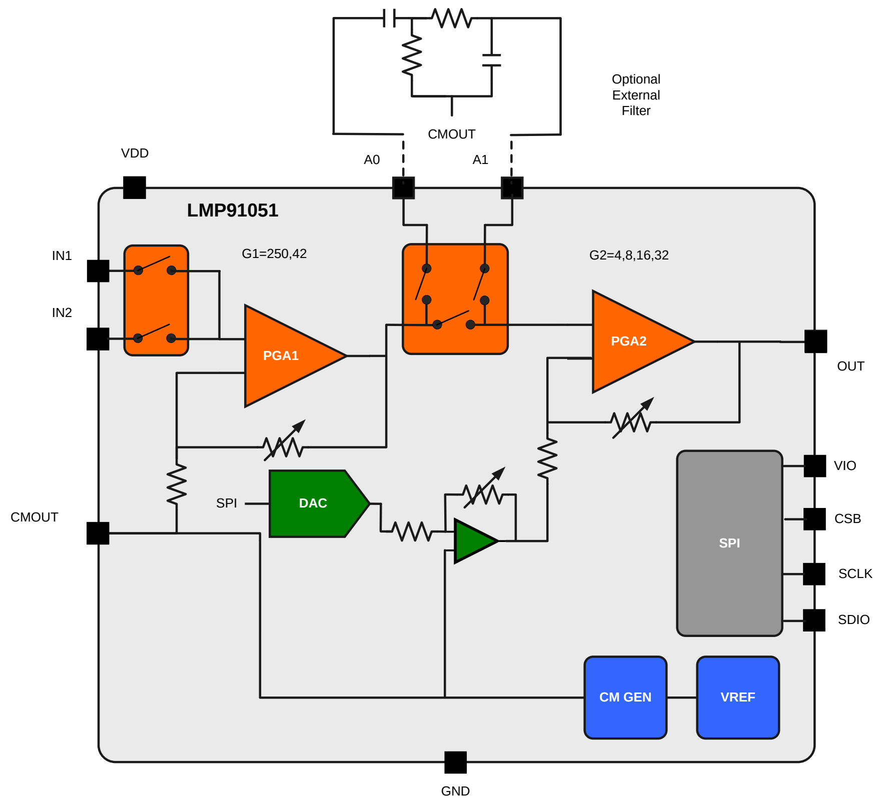
The LMP91051 is a dual channel programmable integrated Sensor Analog Front End (AFE) optimized for thermopile sensors, as typically used in NDIR applications. It provides a complete signal path solution between a sensor and microcontroller that generates an output voltage proportional to the thermopile voltage. The LMP91051's programmability enables it to support multiple thermopile sensors with a single design as opposed to the multiple discrete solutions.

The LMP91051 features a programmable gain amplifier (PGA), "dark phase" offset cancellation, and an adjustable common mode generator (1.15V or 2.59V) which increases output dynamic range. The PGA offers a low gain range of 167V/V to 1335V/V plus a high gain range of 1002V/V to 7986V/V which enables the user to utilize thermopiles with different sensitivities. The PGA is highlighted by low gain drift (20 ppm/°C), output offset drift (230 mV/°C at G = 1002 V/V), phase delay drift (300 ns) and noise specifications (0.1 µVRMS 0.1 to 10Hz) . The offset cancellation circuitry compensates for the "dark signal" by adding an equal and opposite offset to the input of the second stage, thus removing the original offset from the output signal. This offset cancellation circuitry allows optimized usage of the ADC full scale and relaxes ADC resolution requirements.

The LMP91051 allows extra signal filtering (high pass, low pass or band pass) through dedicated pins A0 and A1, in order to remove out of band noise. The user can program through the on board SPI interface. Available in a small form factor 14 pin TSSOP package, the LMP91051 operates from –40 to +105°C.

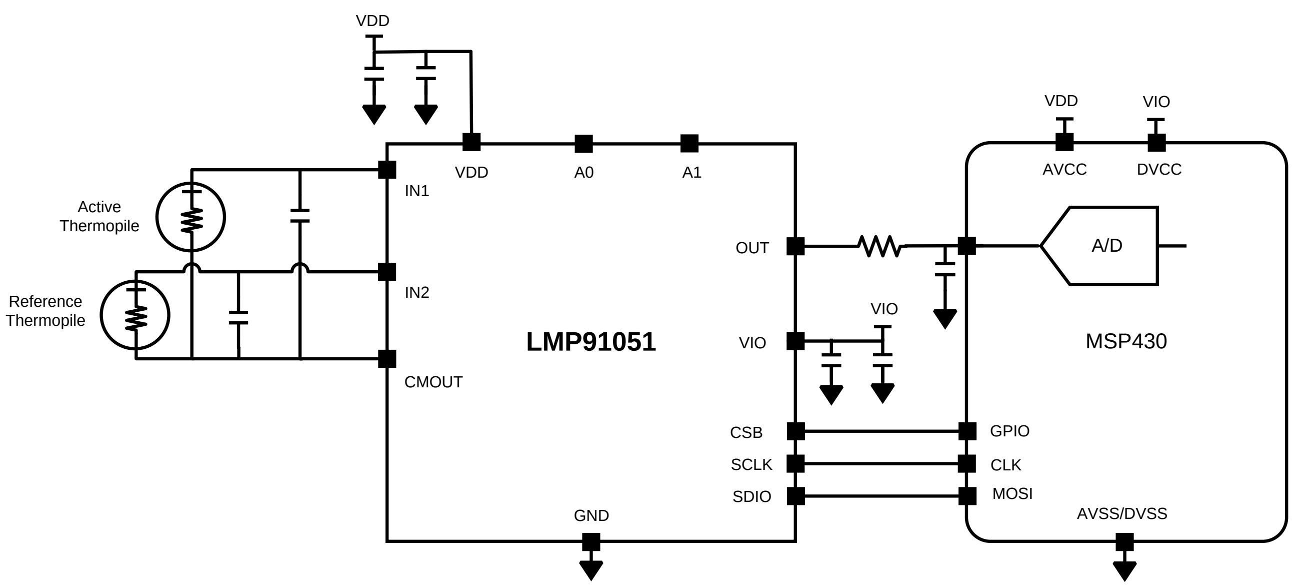
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

BLOCK DIAGRAM



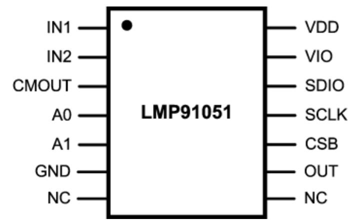
Configurable AFE for NDIR

TYPICAL APPLICATION



Typical NDIR Sensing Application Circuit

CONNECTION DIAGRAM



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PIN DESCRIPTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1	1	Analog Input	Signal Input
IN2	2	Analog Input	Signal Input
CMOUT	3	Analog Output	Common Mode Voltage Output
A0	4	Analog Output	First Stage Output
A1	5	Analog Input	Second Stage Input
GND	6	Power	Ground
NC	7	—	No Connect
NC	8	—	No Connect
OUT	9	Analog Output	Signal Output, reference to the same potential as CMOUT
CSB	10	Digital Input	Chip Select, active low
SCLK	11	Digital Input	Interface Clock
SDIO	12	Digital Input / Output	Serial Data Input / Output
VIO	13	Power	Digital Input/Output Supply
VDD	14	Power	Positive Supply

ABSOLUTE MAXIMUM RATINGS[1][2]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	ESD Tolerance[3]	Human Body Model		1000	V
		Charged Device Model		250	
VDD	Supply Voltage		–0.3	6.0	V
VIO	Digital I/O supply		–0.3	6.0	V
	Voltage at Any Pin		—0.3	VDD + 0.3	V
	Input Current at Any Pin			5	mA
	Storage Temperature Range		65	150	°C
	Junction Temperature[4]			150	°C
	For soldering specifications: see product folder at www.national.com and www.national.com/ms/MS/MS-SOLDERING.pdf				

(1) “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Operating Ratings is not implied. Operating Ratings indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field- Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is $P_{DMAX} = (T_{J(MAX)} - T_A)/ \theta_{JA}$ All numbers apply for packages soldered directly onto a PC board.

OPERATING CHARACTERISTICS[1]

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Supply Voltage		2.7		5.5	V
	Junction Temperature Range[2]		–40		105	°C
θ_{JA}	Package Thermal Resitance	Package 14 pin TSSOP			140	°C/W

(1) “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Operating Ratings is not implied. Operating Ratings indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is $P_{DMAX} = (T_{J(MAX)} - T_A)/ \theta_{JA}$ All numbers apply for packages soldered directly onto a PC board.

ELECTRICAL CHARACTERISTICS[1]

The following specifications apply for VDD = 3.3V, VIO = 3.3V, VCM = 1.15V, **Bold** values for T_A = -40°C to +85°C unless otherwise specified. All other limits apply to $T_A = T_J$ = +25°C.

PARAMETER		TEST CONDITIONS	MIN[2]	TYP[3]	MAX[2]	UNIT
Power Supply						
VDD	Supply Voltage		2.7	3.3	5.5	V
VIO	Digital I/O supply		2.7	3.3	5.5	V
IDD	Supply Current	All analog block ON	3.1	3.6	4.2	mA
	Power Down Supply Current	All analog block OFF	45	75	121	µA
	Digital Supply Current			8		µA

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

ELECTRICAL CHARACTERISTICS(1) (continued)

The following specifications apply for VDD = 3.3V, VIO = 3.3V, VCM = 1.15V, **Bold** values for T_A = -40°C to +85°C unless otherwise specified. All other limits apply to $T_A = T_J$ = +25°C.

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
Offset Cancellation (Offset DAC)						
	Resolution			256		steps
	LSB	All gains		33.8		mV
	DNL		–1		+2	LSB
	Error	Output referred offset error, all gains		±100		mV
	Offset adjust Range	Output referred, all gains	0.2		VDD – 0.2	V
	DAC settling time			480		µs
Programmable Gain Amplifier (PGA) 1st Stage, R_L = 10 kΩ, C_L = 15 pF						
IBIAS	Bias Current			5	**200**	pA
VINMAX _HGM	Max input signal High gain mode	Referenced to CMOUT voltage, it refers to the maximum voltage at the IN pin before clipping; It includes dark voltage of the thermopile and signal voltage.		±2		mV
VINMAX _LGM	Max input signal Low gain mode			±12		mV
VOS	Input Offset Voltage			–165		µV
G _HGM	Gain High gain mode			250		V/V
G_LGM	Gain Low gain mode			42		V/V
GE	Gain Error	Both HGM and LGM		2.5		%
VOUT	Output Voltage Range		0.5		VDD – 0.5	V
PhDly	Phase Delay	1mV input step signal, HGM, Vout measured at Vdd/2		6		µs
TCPhDly	Phase Delay variation with Temperature	1mV input step signal, HGM, Vout measured at Vdd/2,		416		ns
SSBW	Small Signal Bandwidth	Vin = 1mVpp, Gain = 250 V/V		18		kHz
Cin	Input Capacitance			100		pF
Programmable Gain Amplifier (PGA) 2nd Stage, R_S = 1kΩ, C_L = 1µF						
VINMAX	Max input signal	GAIN = 4 V/V		1.65		V
VINMIN	Min input signal			0.82		V
G	Gain	Programmable in 4 steps	4		32	V/V
GE	Gain Error	Any gain		2.5		%
VOUT	Output Voltage Range		0.2		VDD – 0.2	V
PhDly	Phase Delay	100mV input sine 35kHz signal, Gain = 8, VOUT measureed at 1.65V, RL = 10 kΩ		1		µs
TCPhDly	Phase Delay variation with Temperature	250mV input step signal, Gain = 8, Vout measured at Vdd/2		84		ns
SSBW	Small Signal Bandwidth	Gain = 32 V/V		360		kHz
Cin	Input Capacitance			5		pF
CLOAD, OUT	OUT Pin Load Capacitance	Series RC		1		µF
RLOAD, OUT	OUT Pin Load Resistance	Series RC		1		kΩ

ELECTRICAL CHARACTERISTICS(1) (continued)

The following specifications apply for VDD = 3.3V, VIO = 3.3V, VCM = 1.15V, **Bold** values for T_A = -40°C to +85°C unless otherwise specified. All other limits apply to $T_A = T_J$ = +25°C.

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
Combined Amplifier Chain Specification						
en	Input-Referred Noise Density	Combination of both current and voltage noise, with a 86kΩ source impedance at 5Hz, Gain = 7986		30		nV√Hz
	Input-Referred Integrated Noise	Combination of both current and voltage noise, with a 86kΩ source impedance 0.1Hz to 10Hz, Gain = 7986		0.1	0.12(4)	µVrms
G	Gain	PGA1 GAIN = 42, PGA2 GAIN = 4		167		V/V
		PGA1 GAIN = 42, PGA2 GAIN = 8		335		
		PGA1 GAIN = 42, PGA2 GAIN = 16		669		
		PGA1 GAIN = 42, PGA2 GAIN = 3		1335		
		2 PGA1 GAIN = 250, PGA2 GAIN = 4		1002		
		PGA1 GAIN = 250, PGA2 GAIN = 8		2004		
		PGA1 GAIN = 250, PGA2 GAIN = 16		4003		
		PGA1 GAIN = 250, PGA2 GAIN = 32		7986		
GE	Gain Error	Any gain		5		%
TCCGE	Gain Temp Coefficient(5)	Gain = 167 V/V, 335 V/V, 669 V/V, 1335 V/V		6		ppm/°C
		Gain = 1002 V/V, 2004 V/V, 4003 V/V, 7986V/V		20		
PSRR	Power Supply Rejection Ratio	DC, 3.0V to 3.6V supply, gain = 1002V/V	90	110		dB
PhDly	Phase Delay	1mV input step signal, Gain = 1002, Vout measured at Vdd/2		9		µs
TCPhDly	Phase Delay variation with Temperature(6)	1mV input step signal, Gain=1002, Vout measured at Vdd/2		300		ns
TCVOS	Output Offset Voltage Temperature Drift(5)	Gain = 167 V/V		70		µV/°C
		Gain = 335 V/V		100		
		Gain = 669 V/V		160		
		Gain = 1335 V/V		290		
		Gain = 1002 V/V		230		
		Gain = 2004 V/V		420		
		Gain = 4003 V/V		800		
		Gain = 7986V/V		1550		
Common Mode Generator						
VCM	Common Mode Voltage	VDD = 3.3V		1.15		V
		VDD = 5V		2.59		
	VCM accuracy			2		%
CLOAD	CMOut Load Capacitance			10		nF

(4) Guaranteed by design and characterization. Not tested on shipped production material.
(5) TCCGE and TCVOS are calculated by taking the largest slope between –40°C and 25°C linear interpolation and 25°C and 85°C linear interpolation.
(6) TCPhDly is largest change in phase delay between –40°C and 25°C measurements and 25°C and 85°C measurements.

SPI INTERFACE(1)

The following specifications apply for VDD = 3.3V, VIO = 3.3V, VCM = 1.15V, C_L = 15pF, **Bold** values for T_A = –40°C to +85°C unless otherwise specified. All other limits apply to T_A = T_J = +25°C.

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
V_{IH}	Logic Input High		0.7 × VDD			V
V_{IL}	Logic Input Low				0.8	V
V_{OH}	Logic Output High		2.6			V
V_{OL}	Logic Output Low				0.4	V
IIH/IIL	Input Digital Leakage Current		–100 **–200**		100 **200**	nA

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(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

TIMING CHARACTERISTICS(1)

The following specifications apply for VDD = 3.3V, VIO = 3.3V, VCM = 1.15V, C_L = 15pF, **Bold** values for T_A = –40°C to +85°C unless otherwise specified. All other limits apply to T_A = T_J = +25°C.

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
t_{WU}	Wake up time			1		ms
f_{SCLK}	Serial Clock Frequency				10	MHz
t_{PH}	SCLK Pulse Width High		$0.4/f_{SCLK}$			ns
t_{PL}	SCLK Pulse Width Low		$0.4/f_{SCLK}$			ns
t_{CSS}	CSB Setup Time		10			ns
t_{CSH}	CSB Hold Time		10			ns
t_{SU}	SDI Setup Time prior to rise edge of SCLK		10			ns
t_{SH}	SDI Hold Time prior to rise edge of SCLK		10			ns
t_{DOD1}	SDO Disable Time after rise edge of CSB				45	ns
t_{DOD2}	SDO Disable Time after 16th rise edge of SCLK				45	ns
t_{DOE}	SDO Enable Time from the fall edge of 8th SCLK				35	ns
t_{DOA}	SDO Access Time after the fall edge of SCLK				35	ns
t_{DOH}	SDO hold time after the fall edge of SCLK		5			ns
t_{DOR}	SDO Rise time			5		ns
t_{DOF}	SDO Fall time			5		ns

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
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(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

Timing Diagrams

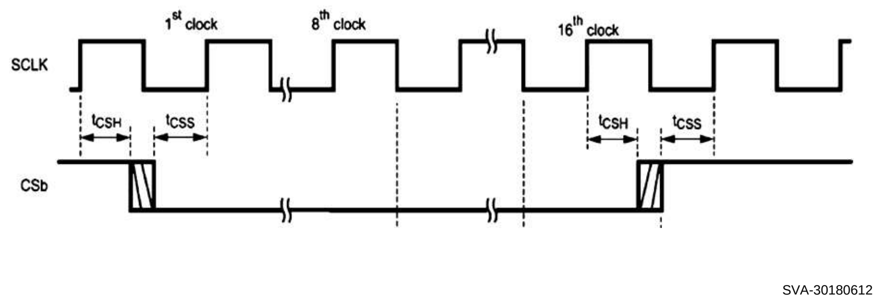


Figure 1. SPI Timing Diagram

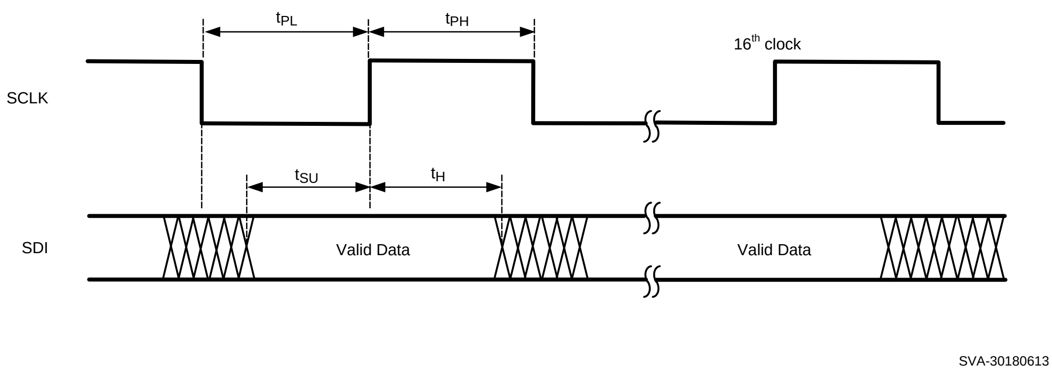


Figure 2. SPI Set-up Hold Time

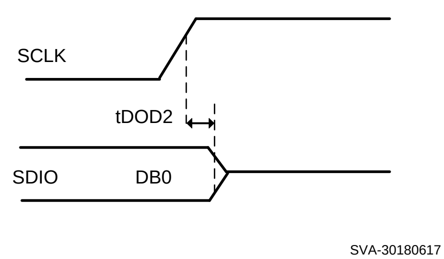


Figure 3. SDO Disable Time After 16th Rise Edge of SCLK

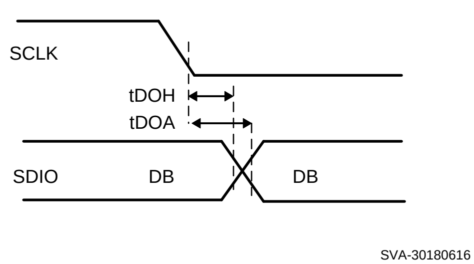


Figure 4. SDO Access Time (t_{DOA}) and SDO Hold Time (t_{DOH}) After the Fall Edge of SCLK

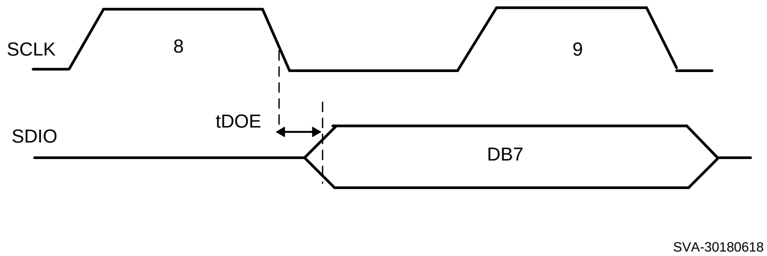


Figure 5. SDO Enable Time From the Fall Edge of 8th SCLK

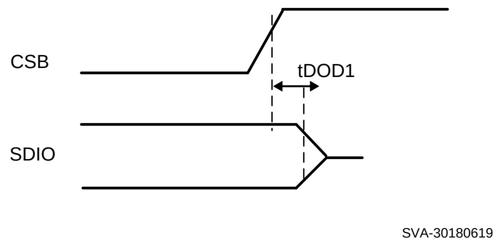


Figure 6. SDO Disable Time After Rise Edge of CSB

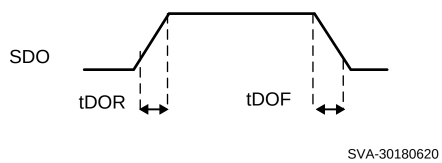
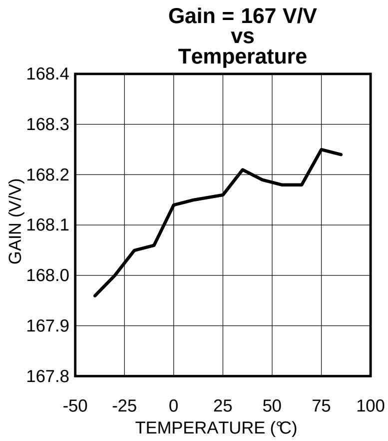


Figure 7. SDO Rise and Fall Times

TYPICAL PERFORMANCE CHARACTERISTICS

VDD = +3.3V, VCM = 1.15V, and T_A = 25°C unless otherwise noted



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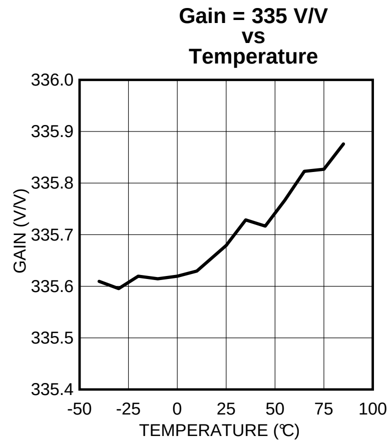

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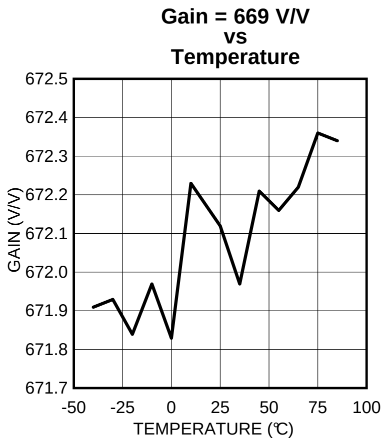

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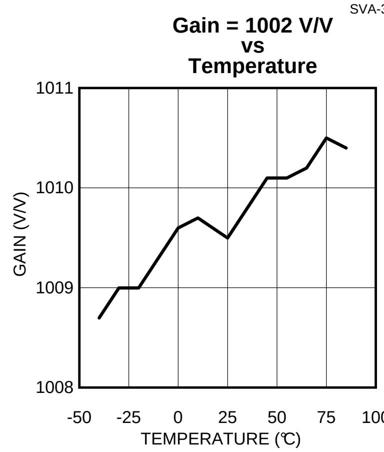

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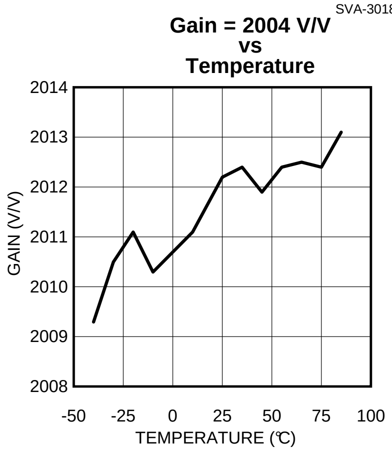

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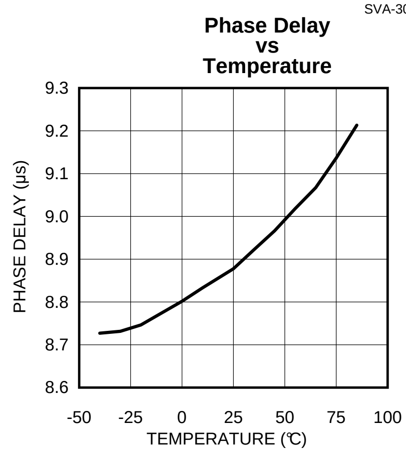

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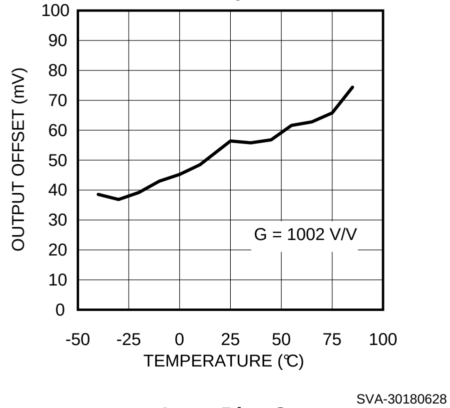
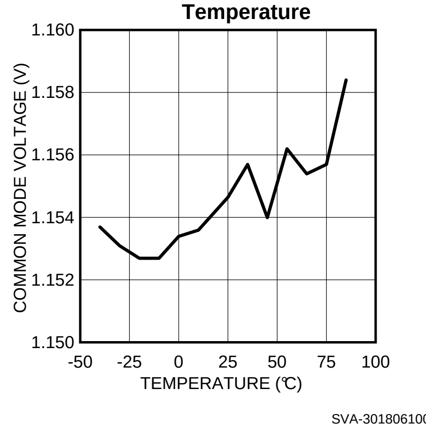
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

VDD = +3.3V, VCM = 1.15V, and T_A = 25°C unless otherwise noted

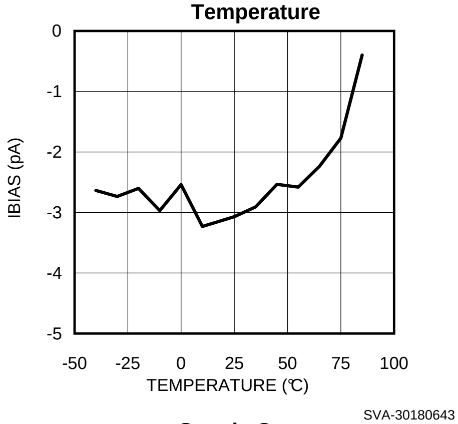
Output Offset vs Temperature



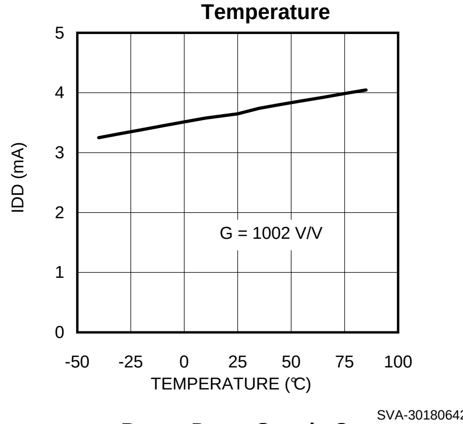
Common Mode Voltage vs Temperature



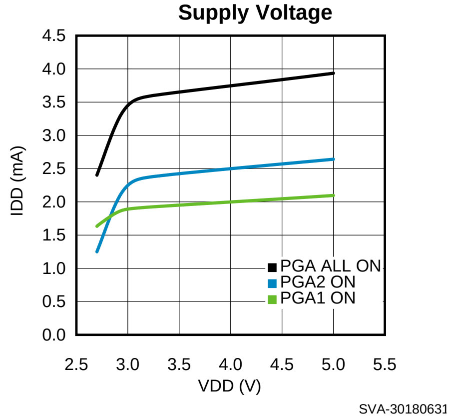
Input Bias Current vs Temperature



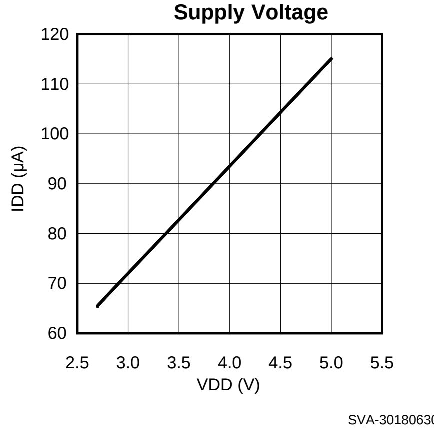
Supply Current vs Temperature



Supply Current vs Supply Voltage



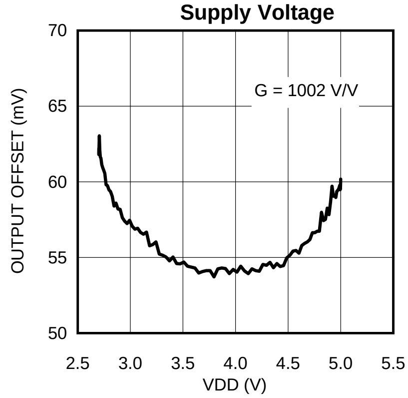
Power Down Supply Current vs Supply Voltage



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

VDD = +3.3V, VCM = 1.15V, and T_A = 25°C unless otherwise noted

Output Offset vs Supply Voltage



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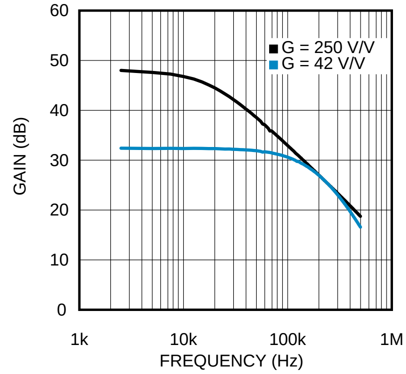
PGA1 Small Signal Bandwidth



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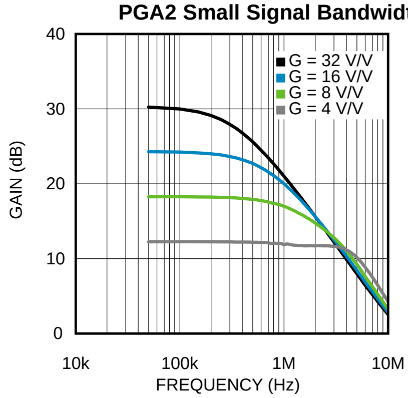
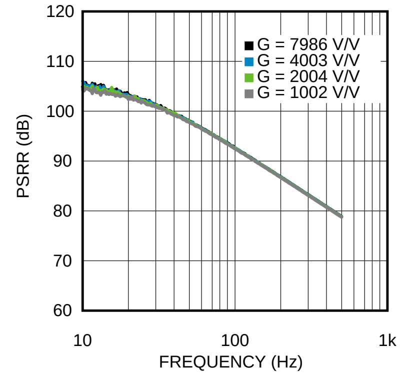
PGA2 Small Signal Bandwidth



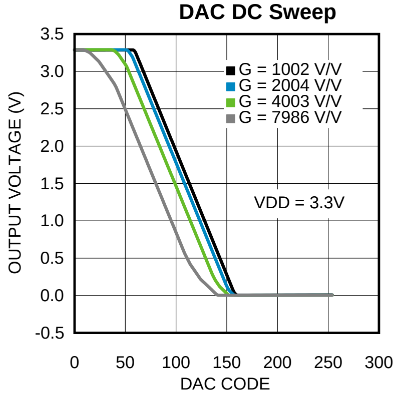
SVA-30180632

Power Supply Rejection Ratio vs Frequency



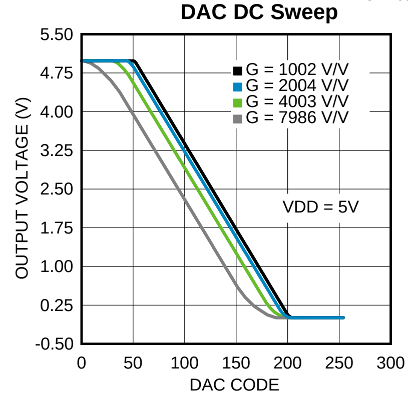
SVA-30180634

DAC DC Sweep



SVA-30180639

DAC DC Sweep



SVA-30180640

FUNCTIONAL DESCRIPTION

PROGRAMMABLE GAIN AMPLIFIER

The LMP91051 offers two programmable gain modes (low/high) with four programmable gain settings each. The purpose of the gain mode is to enable thermopiles with larger dark voltage levels. All gain settings are accessible through bits GAIN1 and GAIN2 [1:0]. The low gain mode has a range of 167 V/V to 1335 V/V while the high gain mode has a range of 1002 V/V to 7986 V/V. The PGA is referenced to the internally generated VCM. Input signal, referenced to this VCM voltage, should be within +/-2mV (see VINMAX_HGM specification) in high gain mode. In the low gain mode the first stage will provide a gain of 42 V/V instead of 250 V/V, thus allowing a larger maximum input signal up to +/-12mV (VINMAX_LGM).

Table 1. Gain Modes

BIT SYMBOL	GAIN
GAIN1	**0: 250 (default)** 1: 42
GAIN2 [1:0]	**00: 4 (default)** 01: 8 10: 16 11: 32

EXTERNAL FILTER

The LMP91051 offers two different measurement modes selectable through EXT_FILT bit. EXT_FILT bit is present in the Device configuration register and is programmable through SPI.

Table 2. Measurement Modes

BIT SYMBOL	MEASUREMENT MODE
EXT_FILT	**0: The signal from the thermopile is being processed by the internal PGAs, without additional external decoupling or filtering (default).**
	1: The signal from the thermopile is being processed by the first internal PGA and fed to the A0 pin. An external low pass, high pass or band pass filter can be connected through pins A0, A1.

An external filter can be applied when EXT_FILT = 1. A typical band pass filter is shown in the picture below. Resistor and capacitor can be connected to the CMOUT pin of the LMP91051 as shown. Discrete component values have been added for reference.

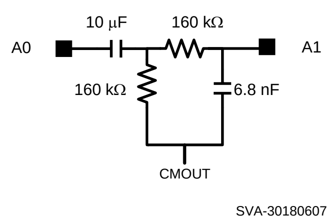


Figure 8. Typical Bandpass Filter

OFFSET ADJUST

Procedure of the offset adjust is to first measure the “dark signal”, program the DAC to adjust, and then measure in a second cycle the residual of the dark signal for further signal manipulation within the µC. The signal source is expected to have an offset component (dark signal) larger than the actual signal. During the “dark phase”, the time when no light is detected by the sensor, the µC can program LMP91051 internal DAC to compensate for a measured offset. A low output offset voltage temperature drift (TCVOS) ensures system accuracy over temperature.

COMMON MODE GENERATION

As the sensor's offset is bipolar, there is a need to supply a VCM to the sensor. This can be programmed as 1.15V or 2.59V (approximately mid rail of 3.3V or 5V supply). It is not recommended to use 2.59V VCM with 3.3V supply.

SPI INTERFACE

An SPI interface is available in order to program the device parameters like PGA gain of two stages, enabling external filter, enabling power for PGAs, offset adjust and common mode (VCM) voltage.

Interface Pins

The Serial Interface consists of SDIO (Serial Data Input / Output), SCLK (Serial Interface Clock) and CSB (Chip Select Bar). The serial interface is write-only by default. Read operations are supported after enabling the SDIO mode by programming the SDIO_MODE_EN register. This is discussed in detail later in the document.

CSB

Chip Select is a active-low signal. CSB needs to be asserted throughout a transaction. That is, CSB should not pulse between the Instruction Byte and the Data Byte of a single transaction.

Note that CSB de-assertion always terminates an on-going transaction, if it is not already complete. Likewise, CSB assertion will always bring the device into a state, ready for next transaction, regardless of the termination status of a previous transaction.

CSB may be permanently tied low for a 2-wire SPI communication protocol.

SCLK

SCLK can idle High or Low for a write transaction. However, for a READ transaction, SCLK should idle high. SCLK features a Schmitt-triggered input and although it has hysterisis, it is recommened to keep SCLK as clean as possible to prevent glitches from inadvertently spoiling the SPI frame.

Communication Protocol

Communication on the SPI normally involves Write and Read transactions. Write transaction consists of single Write Command Byte, followed by single Data byte. The following figure shows the SPI Interface Protocol for write transaction.

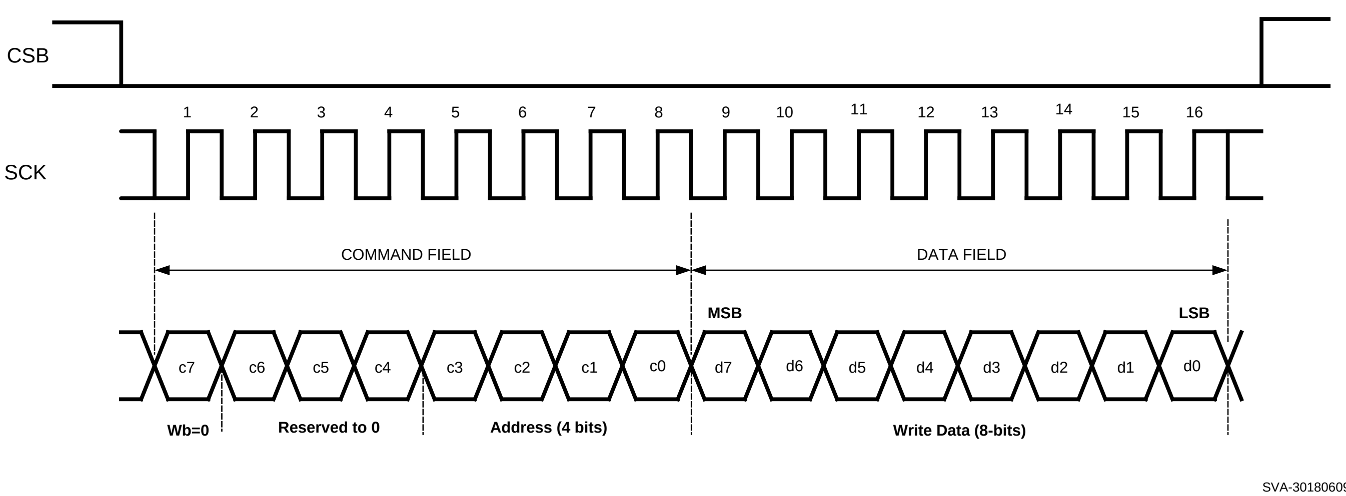


Figure 9. SPI Interface Protocol

For Read transactions, user first needs to write into a SDIO mode enable register for enabling the SPI read mode. Once the device is enabled for Reading, the data is driven out on the SDIO pin during the Data field of the Read Transaction. SDIO pin is designed as a bidirectional pin for this purpose. Figure 6 shows the Read transaction. The sequence of commands that need to be issued by the SPI Master to enable SPI read mode is illustrated in Figure 11.

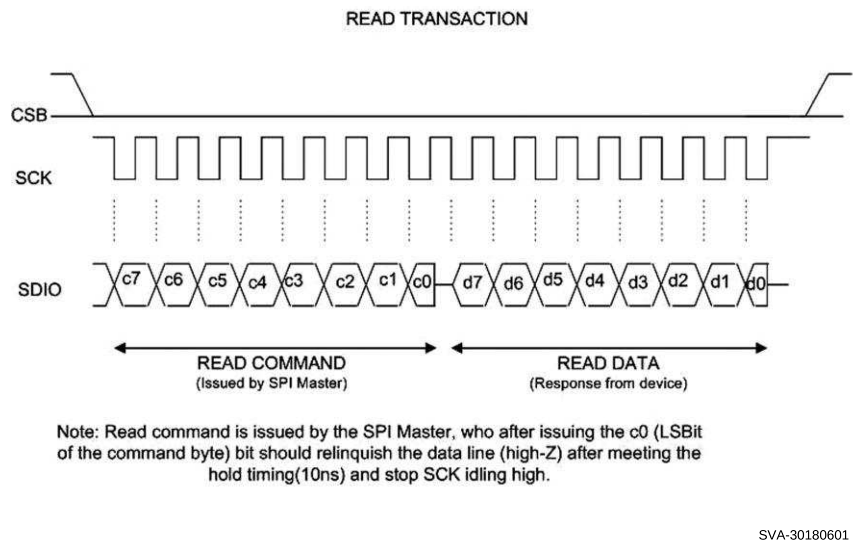


Figure 10. Read Transaction

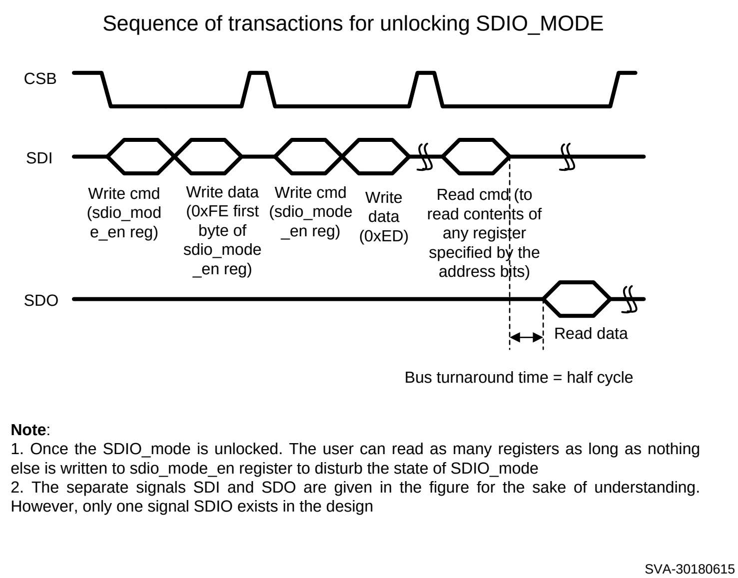


Figure 11. Enable SDIO Mode for reading SPI registers

Registers Organization

Configuring the device is achieved using 'Write' of the designated registers in the device. All the registers are organized into individually addressable byte-long registers that have a unique address. The format of the Write/ Read instruction is as shown below.

Table 3. Write / Read Instruction Format

BIT[7]	BIT[6:4](1)	BIT[3:0]
0 : Write Instruction 1 : Read Instruction	Reserved to 0	Address

(1) Specifying any value other than zero in Bit[6:4] is prohibited.

REGISTERS

This section describes the programmable registers and the associated programming sequence, if any, for the device. The following table shows the summary listing of all the registers that are available to the user and their power-up values.

TITLE	ADDRESS (HEX)(1)	TYPE	POWER-UP/RESET VALUE (HEX)
Device Configuration	0x0	Read-Write (Read allowed in SDIO Mode)	0x0
DAC Configuration	0x1	Read-Write (Read allowed in SDIO Mode)	0x80
SDIO Mode Enable	0xF	Write-only	0x0

(1) Recommended values must be programmed where they are indicated in order to avoid unexpected results. Avoid writing to addresses not mentioned in the document; this could cause unexpected results.

Device Configuration – Device Configuration Register (Address 0x0)

BIT	BIT SYMBOL	DESCRIPTION
7	INP_SEL	**0: IN1 (default)** 1: IN2
[6:5]	EN	**00: PGA1 OFF PGA2 OFF (default)** 01: PGA1 OFF, PGA2 ON 10: PGA1 ON, PGA2 OFF 11: PGA1 ON, PGA2 ON
4	EXT_FILT	**0: PGA1 to PGA2 direct (default)** 1: PGA1 to PGA2 via external filter
3	CMN_MODE	**0 : 1.15V (default)** 1 : 2.59V
[2:1]	GAIN2	**00: 4 (default)** 01: 8 10: 16 11: 32
0	GAIN1	**0: 250 (default)** 1: 42

DAC Configuration – DAC Configuration Register (Address 0x1)

The output DC level will shift according to the formula Vout_shift = –33.8mV * (NDAC – 128).

BIT	BIT SYMBOL	DESCRIPTION
[7:0]	NDAC	128 (0×80): Vout_shift = –33.8mV * (128 – 128) = 0mV (default)

SDIO Mode – SDIO Mode Enable Register (Address 0xf) Write-only

BIT	BIT SYMBOL	DESCRIPTION
[7:0]	SDIO_MODE_EN	To enter SDIO Mode, write the successive sequence 0×FE and 0×ED. Write anything other than this sequence to get out of mode.

APPLICATION INFORMATION

NDIR Gas Sensing Principle

NDIR technology, a type of IR spectroscopy, is based on the principle that gas molecules absorb IR light and absorption of a certain gas occurs at a specific wavelength. Typically, a thermopile with a built-in filter is used to detect the amount of a specific gas. For instance, since CO2 has a strong absorbance at a wavelength of 4.26 µm, a band-pass filter is used to remove all light outside of this wavelength. Figure below shows the basic NDIR gas sensor working principle.

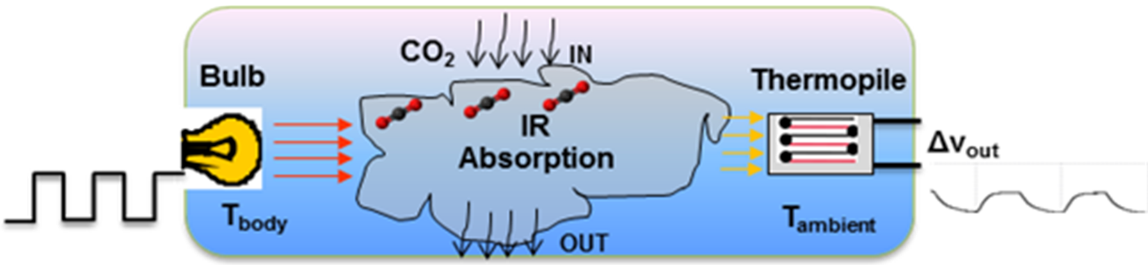


Figure 12. NDIR Gas Sensor Principle

Gas molecules will absorb radiation energy from the lamp emission. Absorption follows the Lambert-Beer law:

$$I = I_0 * e^{-kcl}$$

Where I is the transmitted IR intensity at the thermopile detector side, I_0 is the initial intensity at the IR source, k is the gas specific absorption coefficient of the target gas, c is the gas concentration, and l is the length of the absorption path from light source to thermopile detector.

The thermopile is used to detect the light intensity change. Its output voltage will follow:

$$V = n * \Delta\alpha * (T_{body} - T_{amb})$$

Where Δα is the difference of the Seebeck coefficients of the thermopile materials and n is the number of thermocouples in thermopile detector. T_{body} is the blackbody temperature that is emitting thermal radiation (i.e. the IR lamp), and T_{amb} is the temperature of the surrounding ambient.

Inside the gas chamber, the IR lamp radiation energy could be regarded as ideal black body radiation. The radiation emitted by a blackbody as a result of the temperature difference between the blackbody and ambient is known as thermal radiation. According to Stefan-Boltzmann law, thermal radiation per unit area is expressed with the following equation:

$$R_T = \sigma * (T_{body}^4 - T_{amb}^4)$$

where $\sigma = 5.67 * 10^{-8}$ W/(m^2 *K^4) is the Stefan-Boltzmann constant.

Assuming no loss in light intensity while traveling through the chamber, then R_T = I. After rearranging the equations above the equation for thermopile output voltage becomes:

$$V = n * \Delta\alpha * [I_0 * e^{-kcl}] / [\sigma * (T_{body}^2 + T_{amb}^2) * (T_{body} + T_{amb})]$$

If we examine this equation it makes sense that the thermopile output voltage will be affected by the ambient temperature and the IR lamp intensity uncertainty with a complex relationship. In order to maintain better accuracy of the system, special consideration should be taken in the design implementation. We can see that temperature compensation is an effective way to maintain system accuracy. To accomplish this thermistors are commonly integrated into the thermopile sensor and their resistance changes depending on the surrounding ambient temperature. For better measurement accuracy, having a stable constant voltage to excite the thermistor is a good choice.

Traditional Discrete Op Amp Signal Conditioning

Traditionally discrete op amps have been employed for the gain stage of NDIR systems. AC coupling is required in order to eliminate the signal chain offset. To handle a two channel system one could use a quad op amp configured in a dual channel 2 stage front end. Active filtering is built into the signal path.

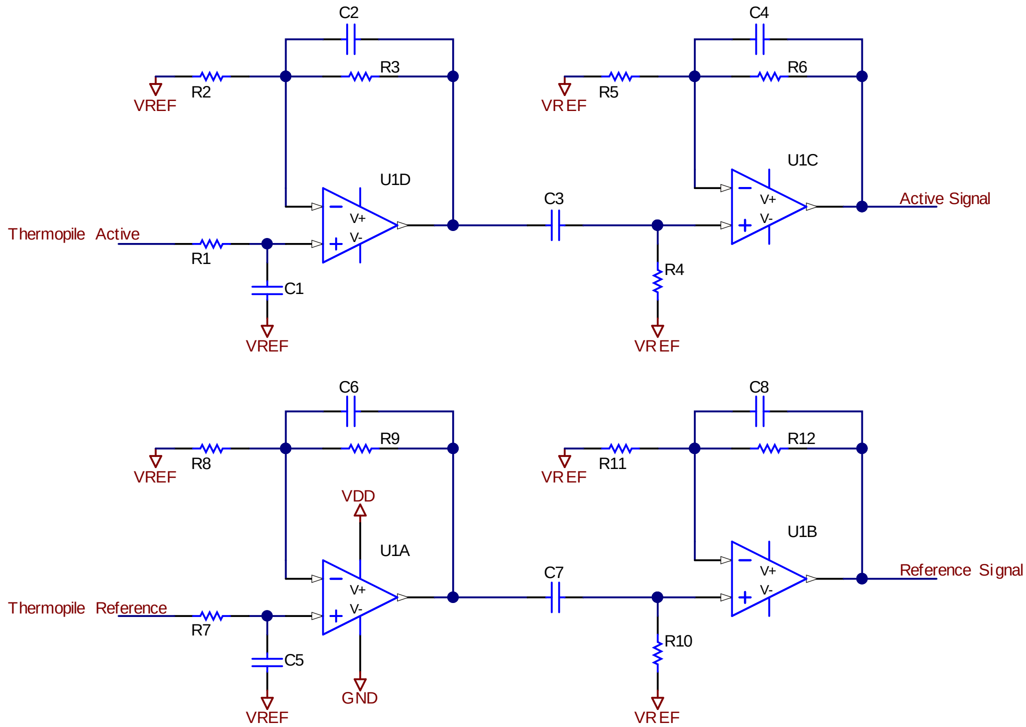


Figure 13. Discrete Op Amp Based System

LMP91051 Sensor AFE for NDIR Gas Sensing

An integrated analog front-end (AFE) can save design time and complexity by incorporating the features of a discrete op amp solution into one chip. The LMP91051 AFE contains a two channel PGA which allows easy interface to a two channel NDIR sensor. By cancelling out errors due to light source deviation optimum accuracy is obtained in a two channel system. This deviation results in long-term drift, which occurs over large periods of time. Hence, the requirement to simultaneously sample both the reference and active channel simultaneously is not required. You can use the input multiplexer (MUX) to switch between the two channels, reducing system cost and complexity, while maintaining accuracy.

The LMP91051 also has fully programmable gain and offset adjustment. This helps ensure that the small thermopile output (100's µV) is matched to the dynamic range of the sampling Analog to Digital converter (A/D) and improves system resolution. The LMP91051 also provides a common mode bias which level-shifts the thermopile sensor signal away from the negative rail, allowing for accurate sensing in the presence of sensor offset voltages.

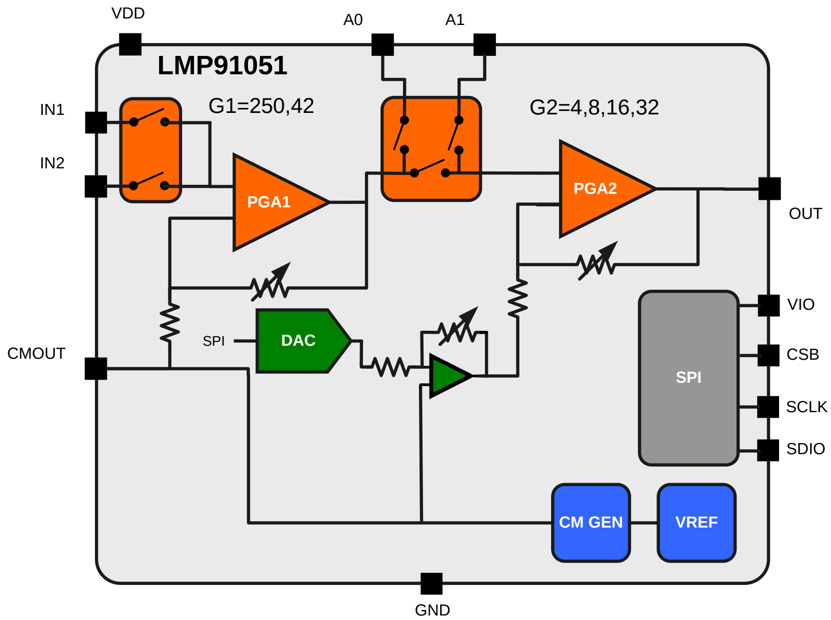


Figure 14. LMP91051 Sensor AFE for NDIR Sensing

LMP91051 Gas Detection System

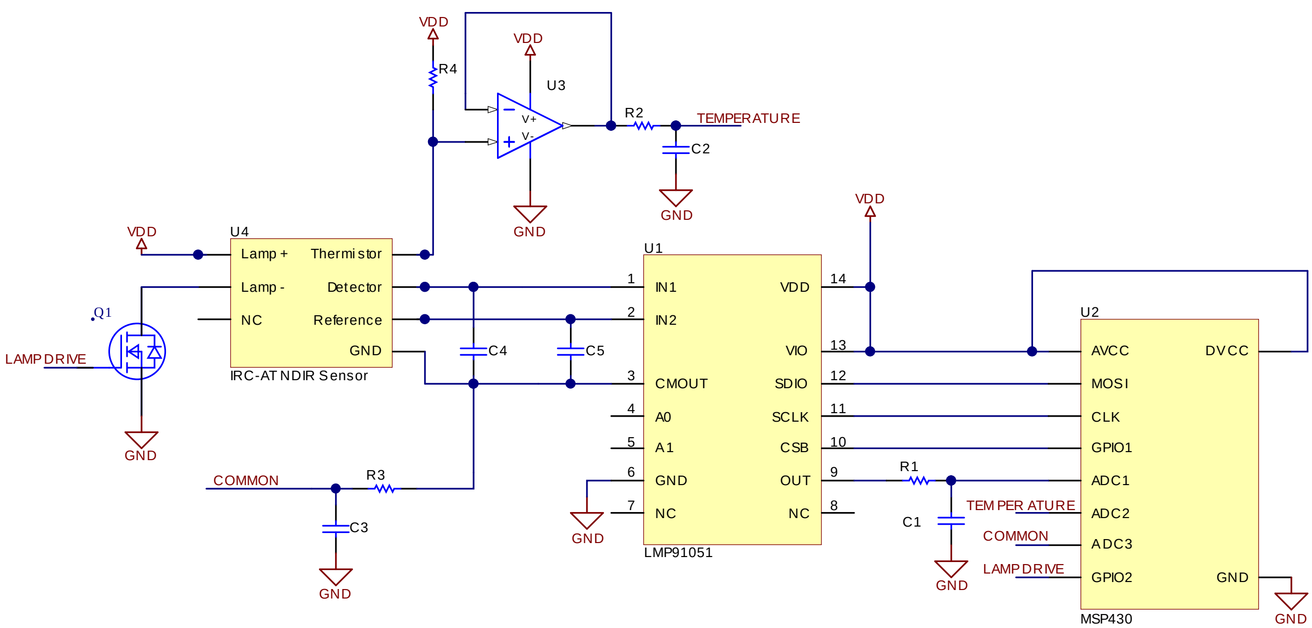


Figure 15. LMP91051 CO2 Gas Detection System

The NDIR sensor used in the proposed system is a Alphasense IRC-AT. The sensor is composed of an IR lamp, two thermopile channels, and a thermistor which is used for temperature calibration. To save power and to avoid overheating the device the lamp source is modulated typically with a 50% duty cycle with a frequency of 1 to 3Hz. The Detector (Active) and Reference channel output are connected directly to the inputs of the LMP91051. Filter capacitors are connected from each input to the common mode reference, CMOUT, to provide low pass filtering. LMP91051 external filtering option is disabled and pins A0 and A1 are shorted internally in the chip. No high pass filtering (AC coupling) is required because the internal offset DAC is used to cancel offset error in the signal chain. This facilitates faster measurements over the traditional AC coupled system which will be discussed further later in this application note. The NDIR sensor has an internal thermistor which is connected to a resistor bridge then buffered by an amplifier.

The MSP430 microcontroller programs the LMP91051 via SPI. The microcontroller utilizes an internal 12 bit muxed A/D to sample the LMP91051 output, buffered thermistor output, and system common mode. The entire system can be powered off of a single supply of 3V.

Gas Detection Method and Settings

In a 2 channel NDIR system the integrated IR lamp is pulsed (typical 1 to 3Hz) with a 50% duty cycle resulting in small 100's uV RC waveforms seen on both the output of the active and reference channel. To improve measurement accuracy these signals are amplified and the peak to peak waveform voltage of both the active channel and reference channel are compared. In a DC coupled single supply system, active DC offset adjustment is required in order to ensure the output of the gain stage doesn't saturate and to remove signal chain offset errors.

In a Muxed 2 channel system toggling between channels is done at an increased rate (i.e 100Hz) in order to reliably reconstruct both channels. To ensure accurate sampling, multiple samples should be taken on each channel prior to switching channels. Preferably sampling is synced to the lamp pulses to ensure data is being capture at the expected time relative to the lamp switching and the same sample within one lamp cycle can be looked at over many lamp cycles to determine noise performance. Figure below provides a visual explanation of the proposed gas detection method.

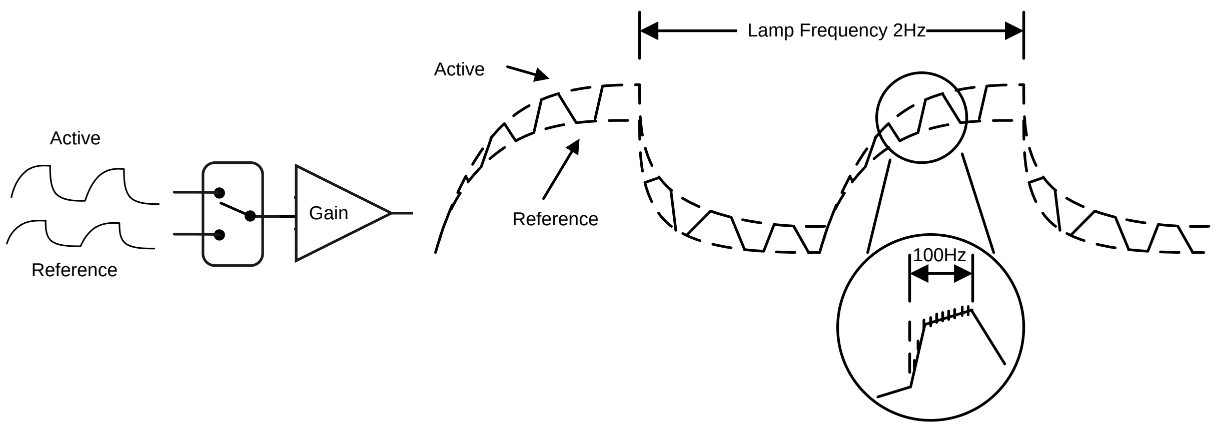


Figure 16. Example Gas Detection Method

A system was constructed with the following settings. Image below shows actual system RC waveform.

Lamp Pulse Frequency: 2 Hz

System Gain: 2000 V/V

System Offset: Apx. -700mV

Input Channel Mux Toggle Frequency: 100Hz

Number of Ch. Samples per Ch. Toggle: 10

ADC Sampling Rate: 1ksps

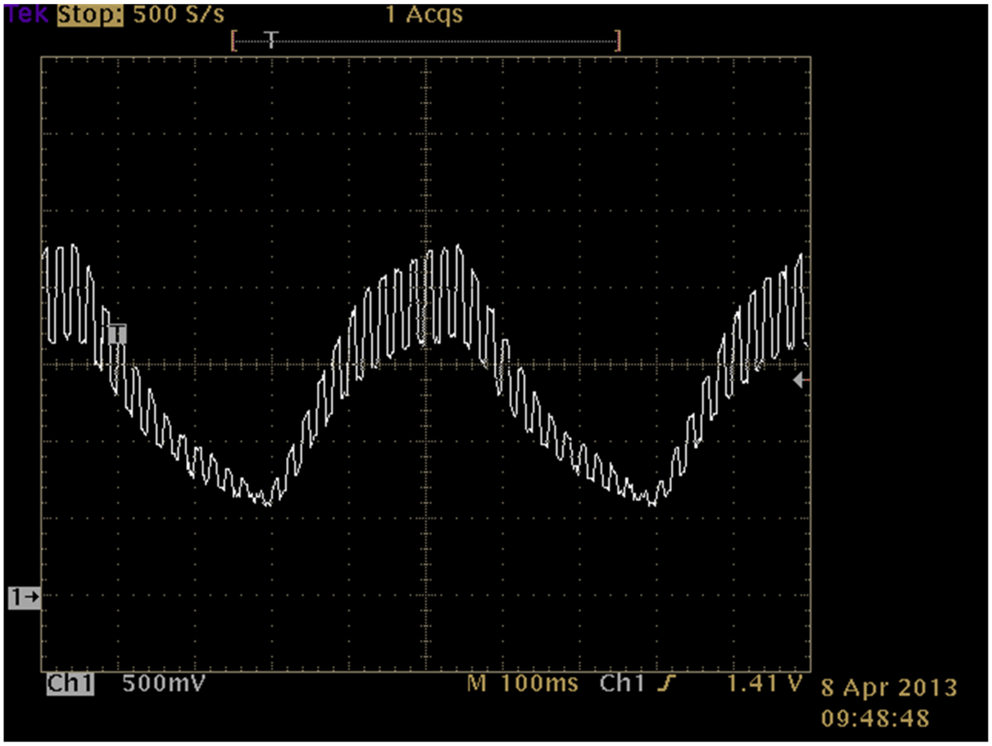


Figure 17. System Waveform

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMP91051MT/NOPB	ACTIVE	TSSOP	PW	14	94	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	LMP910 51MT	Samples
LMP91051MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	LMP910 51MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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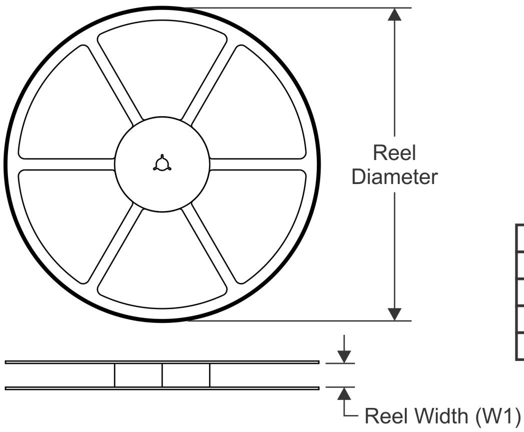
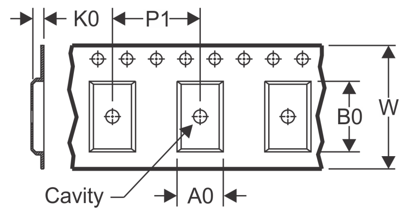
TAPE AND REEL INFORMATION

REEL DIMENSIONS

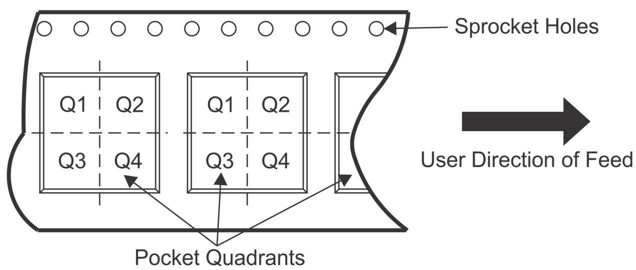


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

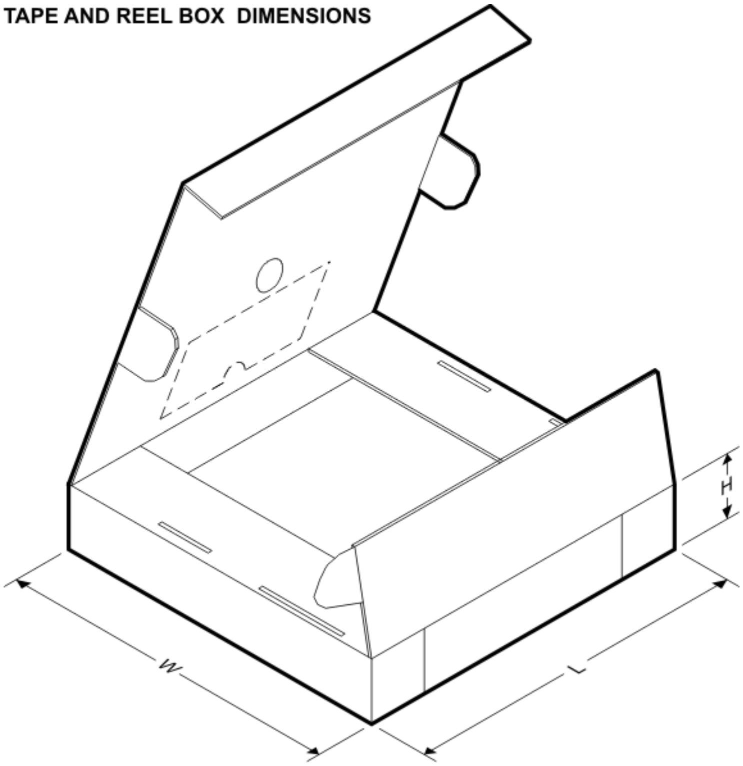
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP91051MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

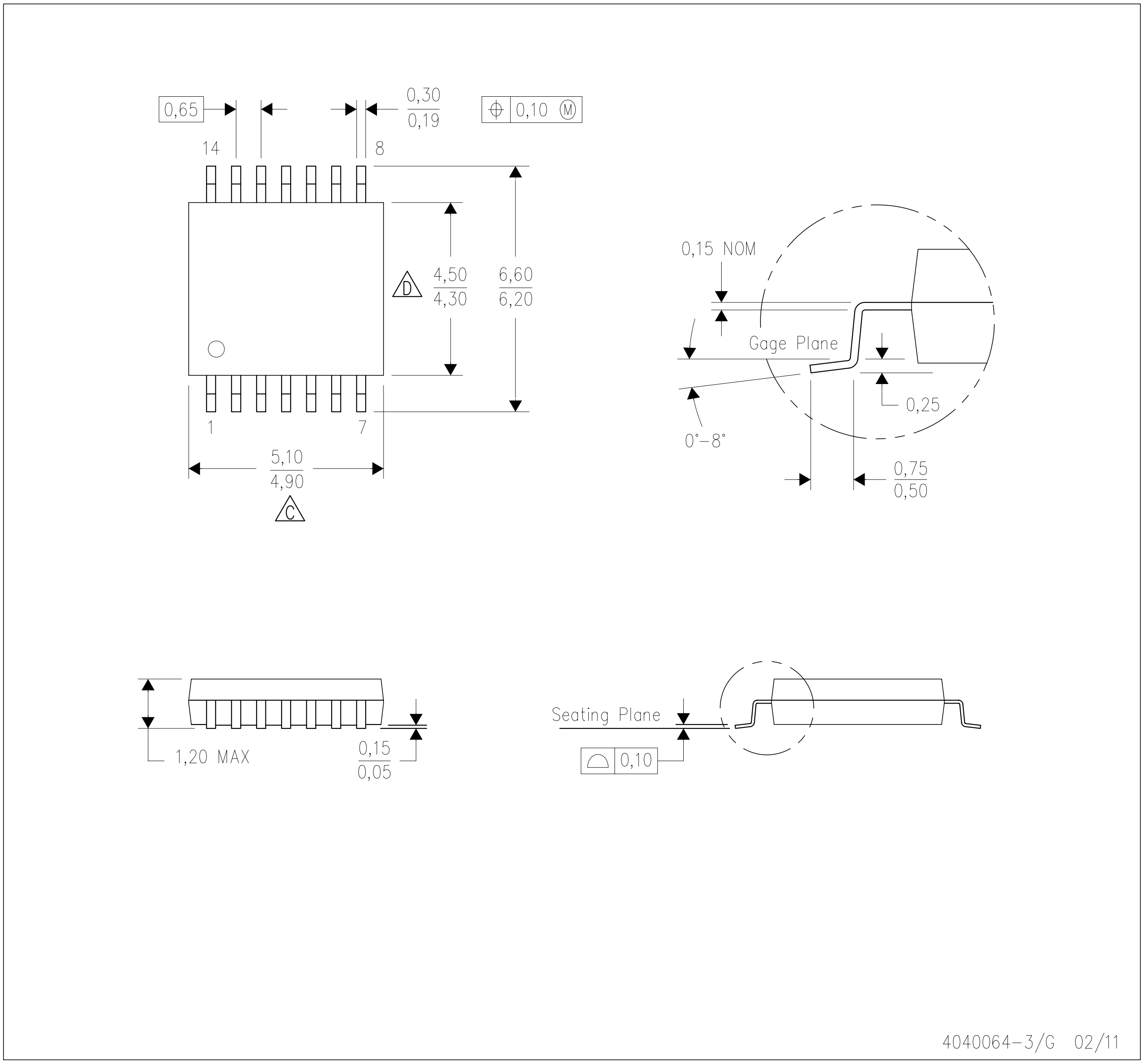
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

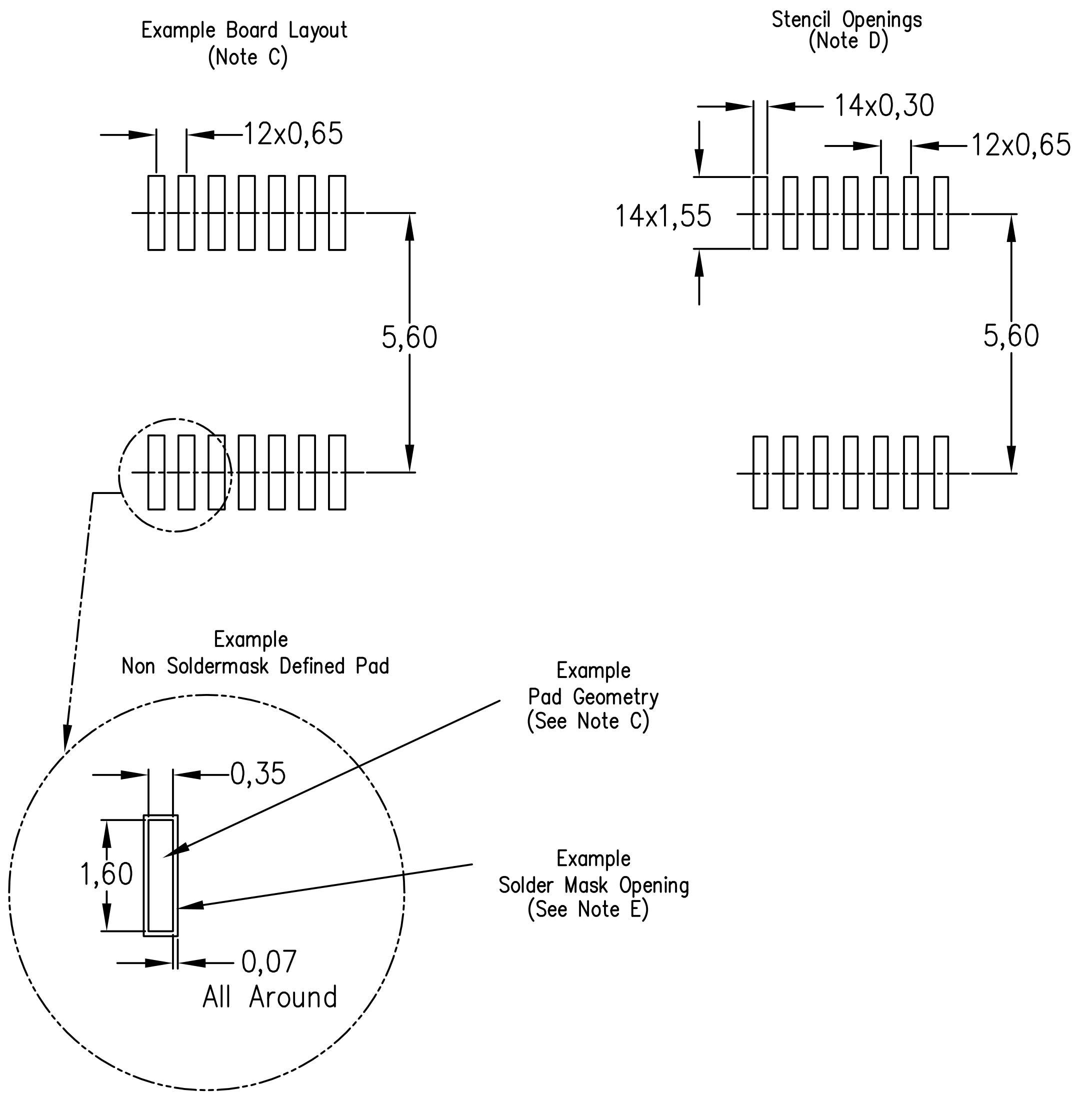
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP91051MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



4211284-2/G 08/15

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265