74LVC157
Quad 2-Input Multiplexer

GENERAL DESCRIPTION

The 74LVC157 is a quad 2-input multiplexer designed for 1.2V to 3.6V operating voltage. The inputs from 3.3V or 5V devices make this device can be used as a translator in a mixed 3.3V and 5V system environment.

The enable input ($\overline{E}$) is active low. When $\overline{E}$ is held high, the 1Y to 4Y outputs are forced to low-state no matter what the conditions of the inputs are. When pin $\overline{E}$ is held low, four bits of data are selected from one of two sources that are determined by the state of the common data selection input (S), and are routed to the four outputs. The four outputs present the true (non-inverting) selected data. The S input can also be used as function generator.

FEATURES

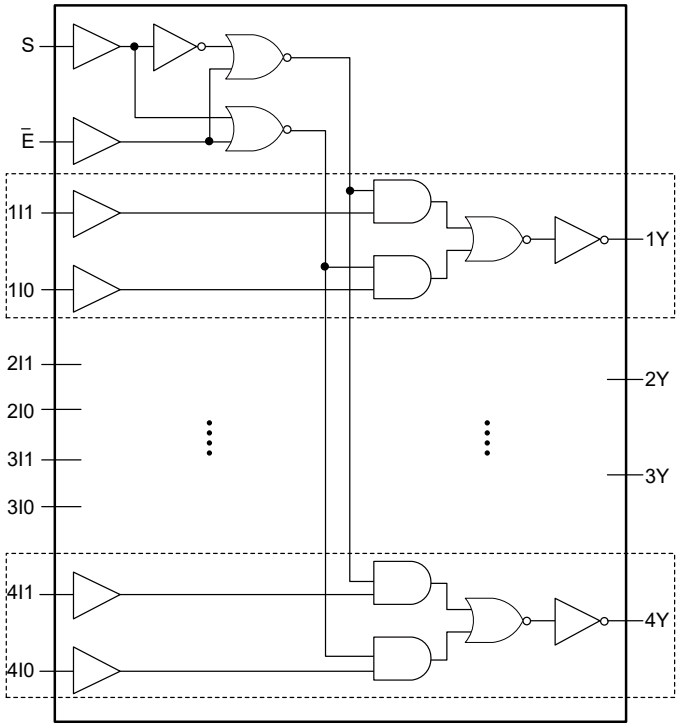
- **Wide Supply Voltage Range: 1.2V to 3.6V**
- **Inputs Accept Voltages up to 5V with 5V Logic**
- **CMOS Low Power Consumption**
- **Direct Interface with TTL Levels**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green TQFN-2.5×3.5-16L, SOIC-16 and TSSOP-16 Packages**

FUNCTION TABLE

CONTROL INPUT		INPUT		OUTPUT
$\overline{E}$	S	nI0	nI1	nY
H	*X*	*X*	*X*	L
L	L	L	*X*	L
L	L	H	*X*	H
L	H	*X*	L	L
L	H	*X*	H	H

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

LOGIC DIAGRAM

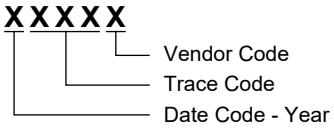


PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74LVC157	TQFN-2.5×3.5-16L	-40℃ to +125℃	74LVC157XTRG16G/TR	R5ARG XXXXX	Tape and Reel, 6000
	SOIC-16	-40℃ to +125℃	74LVC157XS16G/TR	74LVC157XS16 XXXXX	Tape and Reel, 2500
	TSSOP-16	-40℃ to +125℃	74LVC157XTS16G/TR	74LVC157 XTS16 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage, V_{CC} ..... -0.5V to 6.5V
Input Voltage, V_I (2) ..... -0.5V to 6.5V
Output Voltage, V_O (2) .....-0.5V to V_{CC} + 0.5V
Input Clamping Current, I_{IK} (V_I < 0V).....-50mA
Output Clamping Current, I_{OK} (V_O > V_{CC} or V_O < 0V)
.....±50mA
Output Current, I_O (V_O = 0V to V_{CC})
High-State .....-50mA
Low-State.....50mA
Supply Current, I_{CC} 100mA
Ground Current, I_{GND}.....-100mA
Junction Temperature (3).....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility
HBM.....6000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{CC}.....1.65V to 3.6V
Data Retention Only, V_{CC}.....1.2V to 3.6V
Input Voltage, V_I.....0V to 5.5V
Output Voltage, V_O..... 0V to V_{CC}
Input Transition Rise and Fall Rate, Δt/ΔV
V_{CC} = 1.65V to 2.7V ..... 20ns/V (MAX)
V_{CC} = 2.7V to 3.6V ..... 10ns/V (MAX)
Operating Temperature Range .....-40℃ to +125℃

OVERSTRESS CAUTION

1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

2. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

3. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

ESD SENSITIVITY CAUTION

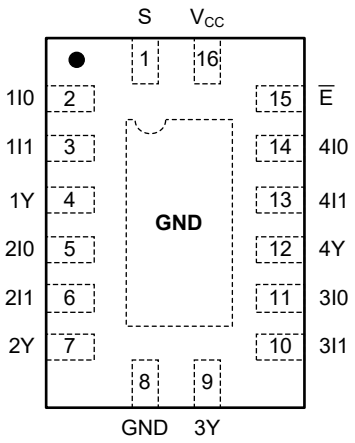
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

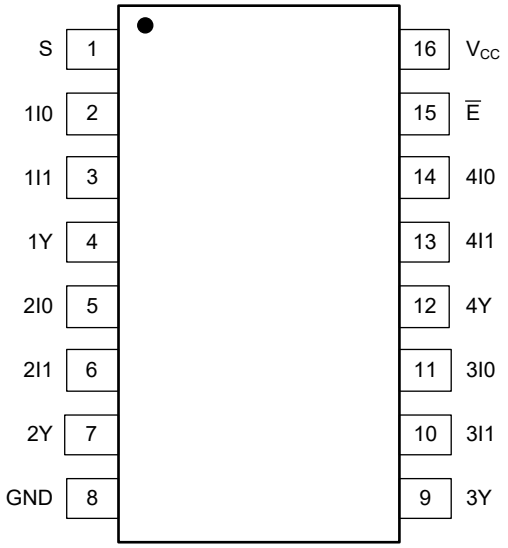
PIN CONFIGURATIONS

(TOP VIEW)



TQFN-2.5×3.5-16L

(TOP VIEW)



SOIC-16/TSSOP-16

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	S	Common Data Selection Input.
2, 5, 11, 14	1I0, 2I0, 3I0, 4I0	Source 0 Data Inputs.
3, 6, 10, 13	1I1, 2I1, 3I1, 4I1	Source 1 Data Inputs.
4, 7, 9, 12	1Y, 2Y, 3Y, 4Y	Multiplexer Outputs.
8	GND	Ground.
15	$\overline{E}$	Enable Input (Active Low).
16	V_{CC}	Supply Voltage.
Exposed Pad	GND	TQFN-2.5×3.5-16L package only. This is not a supply pin. The exposed pad can be left floating or soldered to the ground.

ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, all typical values are measured at V_{CC} = 3.3V and T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
High-Level Input Voltage	V_{IH}	V_{CC} = 1.2V		Full	1.05			V
		V_{CC} = 1.65V to 1.95V		Full	0.65 × V_{CC}			
		V_{CC} = 2.3V to 2.7V		Full	1.5			
		V_{CC} = 2.7V to 3.6V		Full	1.8			
Low-Level Input Voltage	V_{IL}	V_{CC} = 1.2V		Full			0.4	V
		V_{CC} = 1.65V to 1.95V		Full			0.35 × V_{CC}	
		V_{CC} = 2.3V to 2.7V		Full			0.7	
		V_{CC} = 2.7V to 3.6V		Full			0.8	
High-Level Output Voltage	V_{OH}	V_I = V_{IH} or V_{IL}	V_{CC} = 1.65V to 3.6V, I_O = -100μA	Full	V_{CC} - 0.05	V_{CC} - 0.005		V
			V_{CC} = 1.65V, I_O = -4mA	Full	1.45	1.55		
			V_{CC} = 2.3V, I_O = -8mA	Full	2.05	2.15		
			V_{CC} = 2.7V, I_O = -12mA	Full	2.4	2.55		
			V_{CC} = 3.0V, I_O = -18mA	Full	2.55	2.75		
			V_{CC} = 3.0V, I_O = -24mA	Full	2.45	2.7		
Low-Level Output Voltage	V_{OL}	V_I = V_{IH} or V_{IL}	V_{CC} = 1.65V to 3.6V, I_O = 100μA	Full		0.005	0.05	V
			V_{CC} = 1.65V, I_O = 4mA	Full		0.1	0.2	
			V_{CC} = 2.3V, I_O = 8mA	Full		0.15	0.25	
			V_{CC} = 2.7V, I_O = 12mA	Full		0.15	0.3	
			V_{CC} = 3.0V, I_O = 24mA	Full		0.3	0.55	
Input Leakage Current	I_I	V_{CC} = 3.6V, V_I = 5.5V or GND		Full		±0.05	±10	μA
Supply Current	I_{CC}	V_{CC} = 3.6V, V_I = V_{CC} or GND, I_O = 0A		Full		0.05	10	μA
Additional Supply Current	ΔI_{CC}	Per input pin, V_{CC} = 2.7V to 3.6V, V_I = V_{CC} - 0.6V, I_O = 0A		Full		0.05	20	μA
Input Capacitance	C_I	V_{CC} = 0V to 3.6V, V_I = GND to V_{CC}		+25℃		7		pF

DYNAMIC CHARACTERISTICS

(For test circuit, see Figure 1. Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃ and V_{CC} = 1.2V, 1.8V, 2.5V, 2.7V and 3.3V respectively, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN (1)	TYP	MAX (1)	UNITS
Propagation Delay (2)	t_{PD}	nI0, nI1 to nY, see Figure 2	V_{CC} = 1.2V	+25℃		15.0		ns
			V_{CC} = 1.65V to 1.95V	Full	0.5	7.0	16.5	
			V_{CC} = 2.3V to 2.7V	Full	0.5	4.0	10.0	
			V_{CC} = 2.7V	Full	0.5	4.0	10.0	
			V_{CC} = 3.0V to 3.6V	Full	0.5	4.0	8.5	
		$\overline{E}$ to nY, see Figure 3	V_{CC} = 1.2V	+25℃		12.0		ns
			V_{CC} = 1.65V to 1.95V	Full	0.5	6.0	19.0	
			V_{CC} = 2.3V to 2.7V	Full	0.5	4.0	11.0	
			V_{CC} = 2.7V	Full	0.5	4.0	11.0	
			V_{CC} = 3.0V to 3.6V	Full	0.5	4.0	9.5	
		S to nY, see Figure 2	V_{CC} = 1.2V	+25℃		14.0		ns
			V_{CC} = 1.65V to 1.95V	Full	0.5	8.0	18.0	
			V_{CC} = 2.3V to 2.7V	Full	0.5	4.0	10.5	
			V_{CC} = 2.7V	Full	0.5	4.0	10.5	
			V_{CC} = 3.0V to 3.6V	Full	0.5	4.0	9.0	
Output Skew Time	$t_{SK(O)}$	V_{CC} = 3.0V to 3.6V		Full		0.5	1.5	ns
Power Dissipation Capacitance (3)	C_{PD}	V_I = GND to V_{CC}	V_{CC} = 1.65V to 1.95V	+25℃		15		pF
			V_{CC} = 2.3V to 2.7V	+25℃		16		
			V_{CC} = 3.0V to 3.6V	+25℃		17		

NOTES:

1. Specified by design and characterization; not production tested.
2. t_{PD} is the same as t_{PLH} and t_{PHL}.
3. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$

   where:

   f_i = Input frequency in MHz.

   f_o = Output frequency in MHz.

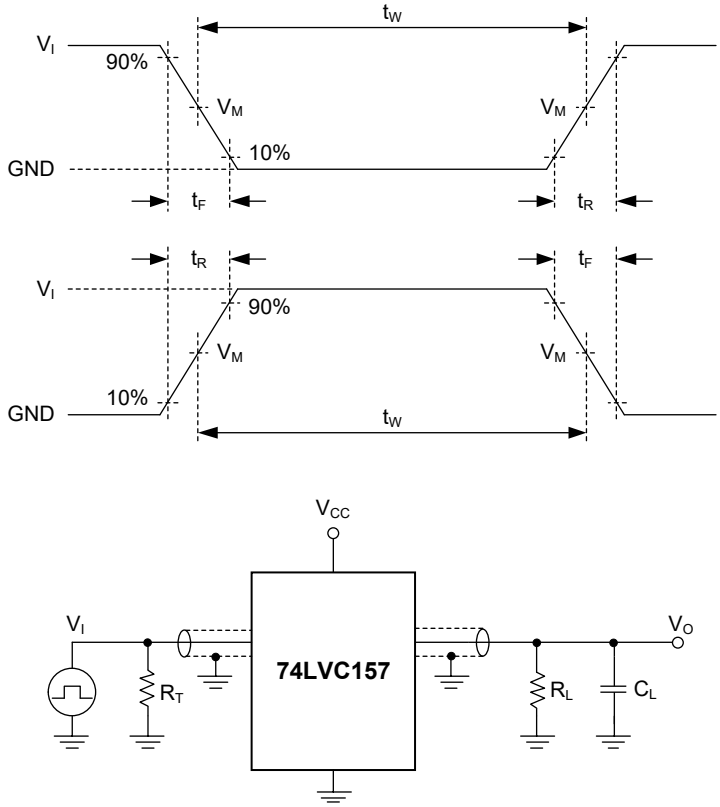
   C_L = Output load capacitance in pF.

   V_{CC} = Supply voltage in Volts.

   N = Number of inputs switching.

   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of outputs.

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions for test circuit:

R_L: Load resistance.

C_L: Load capacitance (includes jig and probe).

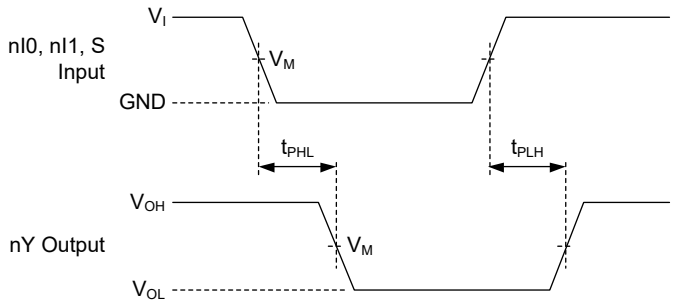
R_T: Termination resistance (equals to output impedance Z_O of the pulse generator).

Figure 1. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

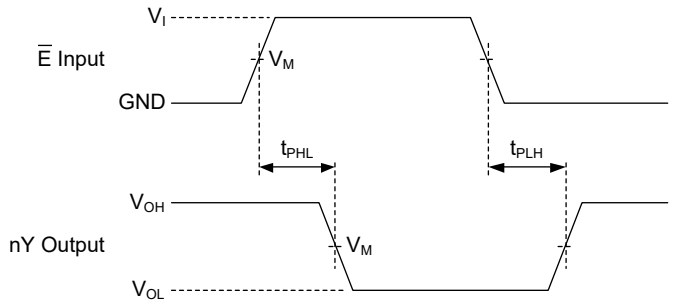
SUPPLY VOLTAGE	INPUT		LOAD	
V_{CC}	V_I	t_R, t_F	C_L	R_L
1.2V	V_{CC}	≤ 2ns	30pF	1kΩ
1.65V to 1.95V	V_{CC}	≤ 2ns	30pF	1kΩ
2.3V to 2.7V	V_{CC}	≤ 2ns	30pF	500Ω
2.7V	2.7V	≤ 2.5ns	50pF	500Ω
3.0V to 3.6V	2.7V	≤ 2.5ns	50pF	500Ω

WAVEFORMS



Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 2. Data Inputs (nI0, nI1) and Common Data Selection Input (S) to Output (nY) Propagation Delays



Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 3. Enable Input ($\overline{E}$) to Output (nY) Propagation Delays

Table 2. Measurement Points

SUPPLY VOLTAGE	INPUT		OUTPUT
V_{CC}	V_I	V_M (1)	V_M
1.2V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}
1.65V to 1.95V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}
2.3V to 2.7V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}
2.7V	2.7V	1.5V	1.5V
3.0V to 3.6V	2.7V	1.5V	1.5V

NOTE:
1. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 2.5ns.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

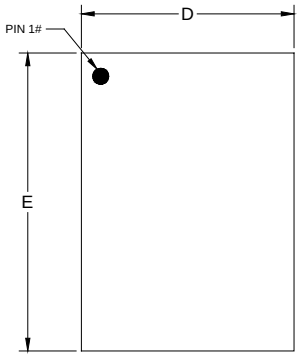
AUGUST 2022 – REV.A to REV.A.1	Page
Updated Electrical Characteristics section	4
Updated Dynamic Characteristics section	5
Added SOIC-16/TSSOP-16 packages	All

OCTOBER 2021 – REV.A to REV.A.1	Page
Updated Dynamic Characteristics section	5
Added Table 2 and note in Waveforms section	7

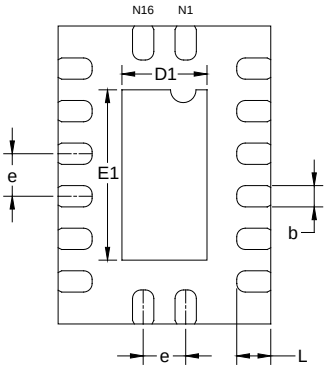
Changes from Original (FEBRUARY 2021) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

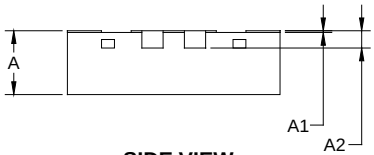
TQFN-2.5×3.5-16L



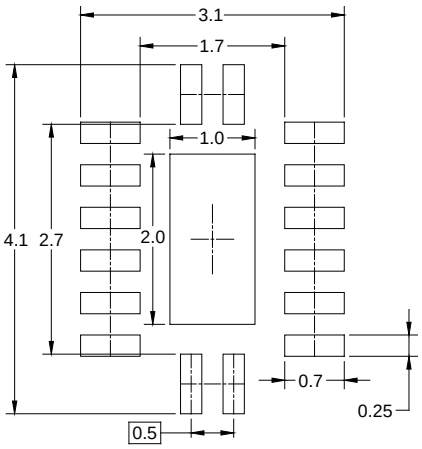
TOP VIEW



BOTTOM VIEW



SIDE VIEW



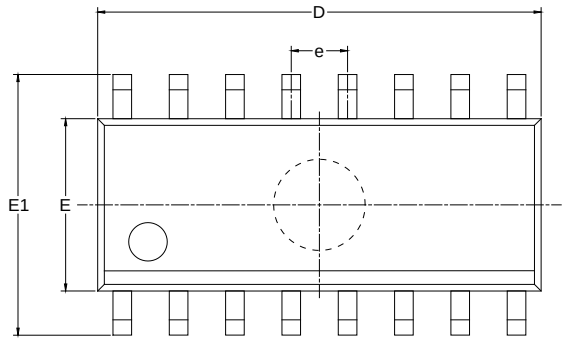
RECOMMENDED LAND PATTERN (Unit: mm)

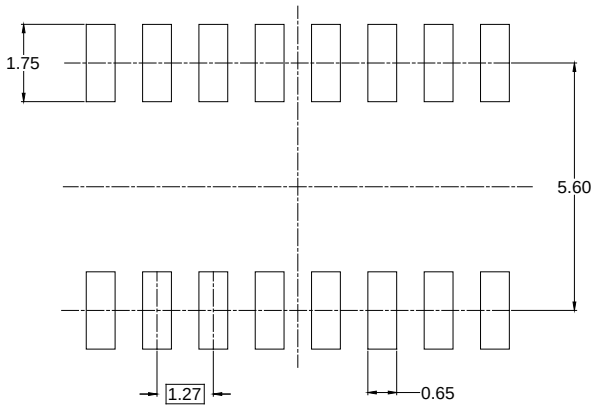
Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.203 REF		
b	0.20	0.25	0.30
D	2.40	2.50	2.60
D1	0.85	1.00	1.15
E	3.40	3.50	3.60
E1	1.85	2.00	2.15
e	0.45	0.50	0.55
L	0.30	0.40	0.50

NOTE: This drawing is subject to change without notice.

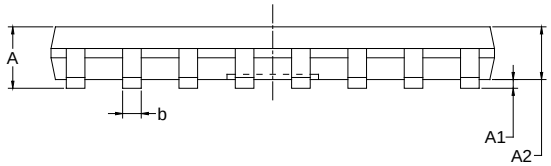
PACKAGE OUTLINE DIMENSIONS

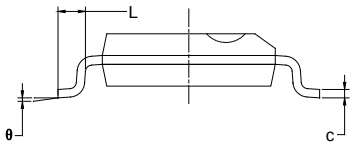
SOIC-16





RECOMMENDED LAND PATTERN (Unit: mm)



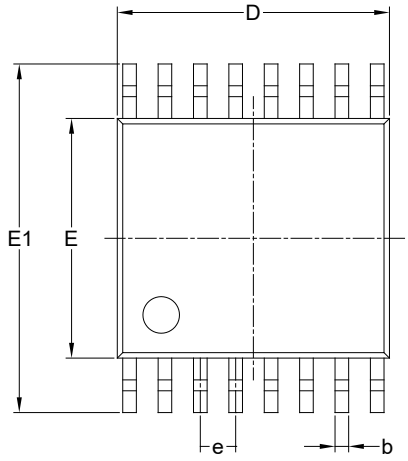


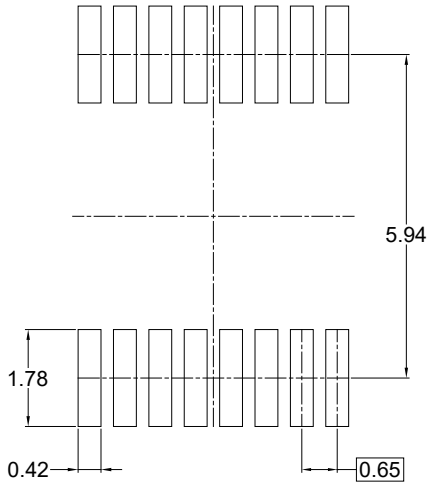
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

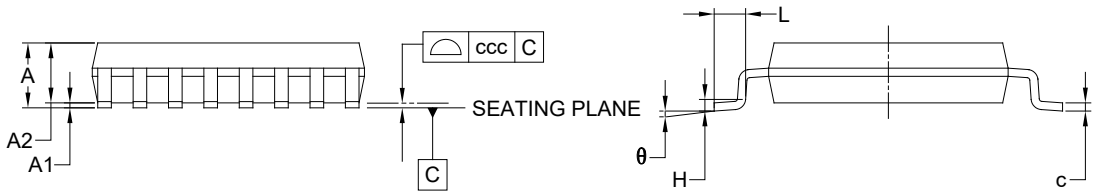
PACKAGE OUTLINE DIMENSIONS

TSSOP-16





RECOMMENDED LAND PATTERN (Unit: mm)

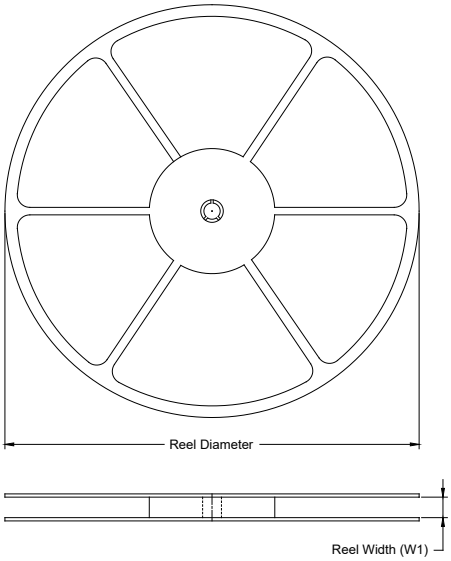


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	4.860	-	5.100
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

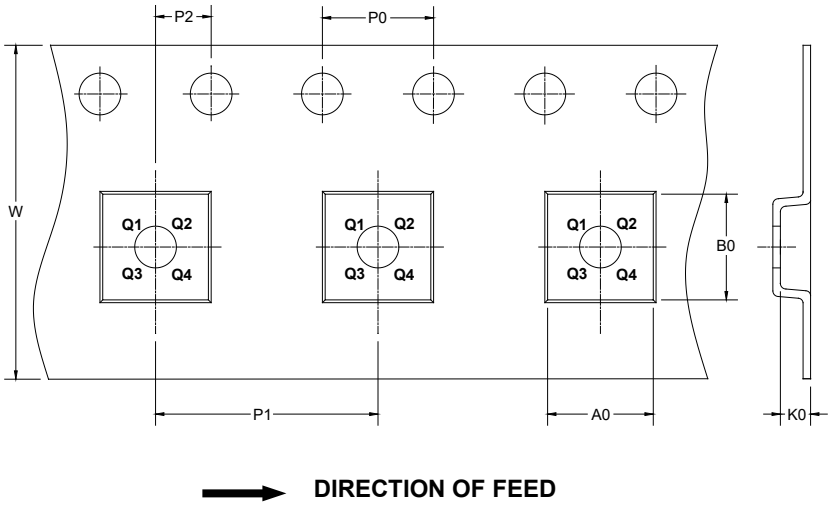
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

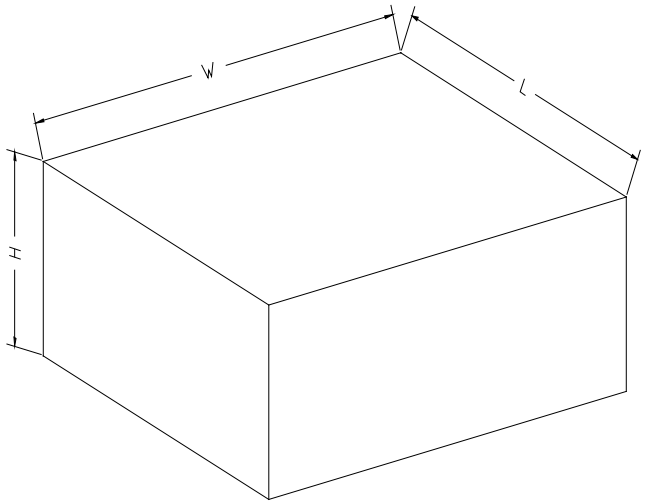
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-2.5×3.5-16L	13″	12.4	2.80	3.80	0.95	4.0	8.0	2.0	12.0	Q1
SOIC-16	13″	16.4	6.50	10.30	2.10	4.0	8.0	2.0	16.0	Q1
TSSOP-16	13″	12.4	6.90	5.60	1.50	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002