www.ablic.com

LOW CHARGE INJECTION 32-CHANNEL 8Ω HIGH-VOLTAGE ANALOG SWITCHES

Rev.1.0_00

The ABLIC S-UM6522E is a low charge injection 32-channel single-pole, single-throw (SPST) high-voltage analog switch IC operated only by a single 5V for ultrasound imaging applications.
Users can select either Serial Digital Interface (SDI) or Bank Interface.
The S-UM6522E has the same packaging and pinout as the HDL6M06522BN with improved Con/Coff and off isolation performance.

■ Functions

- 32-channel high-voltage SPST analog switches with user-selectable SDI or Bank interface

■ Features

- 0V to ±100V analog signal voltage range allowing ±150V voltage overshoot
- 10kHz to 85MHz analog signal frequency range
- 2A peak analog signal current per channel
- 8Ω switch on-resistance
- 40kΩ bleed resistor on probe side
- 32-bit shift registers
- Low on/off-capacitance
- 15pC charge injection to 1000pF
- -75dB off-isolation at analog small-signal 5MHz
- -60dB switch crosstalk
- Selectable Serial Digital Interface (32-bit shift registers) or Bank Interface (1 bank of 32-channel)
- 1.8V to 5V CMOS logic interface
- Single +5V power supply (NO HIGH-VOLTAGE POWER SUPPLY required)
- Low power dissipation (static 5mW)
- Embedded thermal protection flag indicator
- Unique pin configuration for easy PCB traces
- RoHS compliant 84-lead 10x10mm QFN

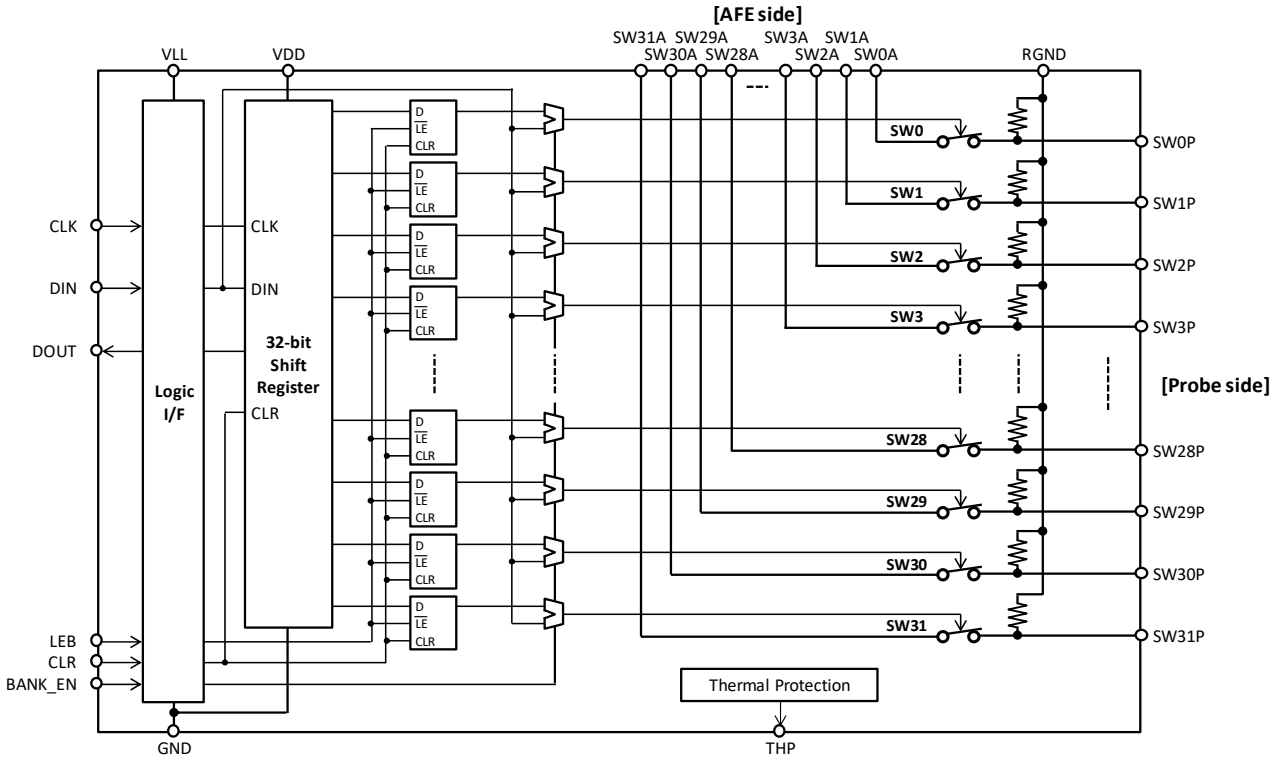


Figure 1 Block Diagram

■ Absolute Maximum Ratings

T_A=25°C unless otherwise noted.

Table 1 Absolute Maximum Ratings

No.	Items	Symbol	Value	Units	Condition
1	Positive logic supply voltage	V_{LL}	-0.4 to +7	V	
2	Positive supply voltage	V_{DD}	-0.4 to +7	V	
3	Logic input voltage	DIN, LEB, CLK, CLR_BSEL, BANK_EN	-0.4 to +7	V	
4	Logic output voltage	DOUT, THP	-0.4 to +7	V	
5	Analog signal range (steady state voltage)	V_{SIG}	-105 to +105	V	
6	Analog signal range (peak overshoot voltage)	V_{SIG_OS}	-150 to +150	V	Max. 500ns pulse width
7	Peak analog signal current per channel	I_{SW}	2.5	A	
8	Operating junction temperature	T_{Jop}	-20 to +150	°C	
9	Storage temperature	T_{STG}	-55 to +150	°C	
10	Maximum power dissipation	P_{Dmax}	4	W	

Remark Stresses beyond the absolute maximum ratings may cause permanent damage to the product.

■ Operating Supply Voltages, Logic Levels, and Application Circuits

1. Operating supply voltages, temperature, and logic levels

Table 2 Operating Supply Voltages and Logic Levels

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	Logic supply voltage	V_{LL}	1.7	1.8 to 5	V_{DD}	V	
2	Positive supply voltage	V_{DD}	4.75	5	5.25	V	
3	IC substrate voltage *1	V_{SUB}	-	0	-	V	
4	Operating free-air temperature	T_A	0	-	75	°C	
5	High-level logic input voltage	V_{IH}	$0.8V_{LL}$	-	V_{LL}	V	
6	Low-level logic input voltage	V_{IL}	0	-	$0.2V_{LL}$	V	
7	High-level logic output voltage	V_{oH}	$0.8V_{LL}$	-	-	V	I_{SOURCE} = 1mA
8	Low-level logic output voltage	V_{oL}	-	-	$0.2V_{LL}$	V	I_{SINK} = 1mA
9	Logic input high current *2	I_{IH}	-10	-	10	μA	DIN, LEB, CLK, CLR_BSEL, BANK_EN
10	Logic input low current	I_{IL}	-10	-	10	μA	
11	Logic input capacitance	C_{IN}	-	2	-	pF	
12	Set up time before LEB rises	t_{SD}	25	-	-	ns	
13	Time width of LEB	t_{WLEB}	12	-	-	ns	
14	Clock delay time to data out	t_{DO}	7	10	24	ns	
15	Time width of CLR_BSEL	t_{OLR}	55	-	-	ns	
16	Clock frequency	f_{CLK}	-	-	50	MHz	V_{LL}=1.8V
			-	-	80	MHz	V_{LL}=2.5V
			-	-	95	MHz	V_{LL}=3.3V
17	Clock rise and fall times	t_R, t_F	-	-	50	ns	
18	Setup time data to clock	t_{SU}	4	-	-	ns	
19	Hold time data from clock	t_{HLD}	4	-	-	ns	
20	Bank interface setup time	t_{SD_BNK}	100	-	-	ns	
21	BANKx minimum pulse width	t_{WBANK}	4	-	-	μs	

***1.** Thermal pad on the bottom of the package must be soldered to the ground.
***2.** BANK_EN has 100μA leakage at V_{LL}=5V due to 50kΩ internal pull-down resistor.

2. Power supply sequencing

No power supply sequencing is required even if V_{LL} is different from V_{DD}.
Please apply the V_{DD} voltage to the V_{LL} when operating with a single 5V.

■ Electrical Characteristics

1. DC characteristics

Table 3 DC Characteristics

V_{LL}=3.3V, V_{DD}=5V, LEB=0, BANK_EN=0/1, T_A=25ºC, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Analog signal range (steady state voltage)	V_{SIG}	-100	-	+100	V	
2	Analog signal range (peak overshoot voltage)	V_{SIG_OS}	-150	-	+150	V	Max. 500ns pulse width
3	V_{LL} quiescent current	I_{LLQ}	-	0.2	-	μA	Quiescent current-1 All switches off
4	V_{DD} quiescent current	I_{DDQ}	-	1.5	-	mA	
5	V_{LL} quiescent current	I_{LLQ}	-	0.2	-	μA	Quiescent current-2 All switches on
6	V_{DD} quiescent current	I_{DDQ}	-	1.5	-	mA	
7	V_{LL} dynamic current	I_{LL}	-	2	10	μA	Dynamic current All channels switching simultaneously at f_{SW}=50kHz
8	V_{DD} dynamic current	I_{DD}	-	3.4	4.6	mA	
9	DC offset switch off	V_{OS}	-	0	-	mV	
10	Small signal switch on-resistance	R_{ONS}	-	8	10	Ω	V_{SIG}=0.1Vpp to 5Vpp @5MHz, R_S=10Ω
11	Small signal switch on-resistance matching	ΔR_{ONS}	-	2	5	%	V_{SIG}=0V, I_{SIG}=5mA
12	Large signal switch on-resistance	R_{ONL}	-	8	-	Ω	V_{SIG}=20Vpp@5MHz, R_S=10Ω
13	Shunt resistance	R_{BLD}	30	40	50	kΩ	On probe side
14	Switch output peak current	I_{SW}	-	2	-	A	100ns pulse, 0.1% duty cycle

2. Thermal protection

Table 4 Thermal Protection Characteristics

V_{LL}=3.3V, V_{DD}=5V, LEB=0, BANK_EN=0/1, T_A=25ºC, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	THP pull-up voltage	V_{PUTHP}	-	-	5.25	V	Open drain
2	THP output current	I_{THP}	-	1.0	-	mA	
3	THP output low voltage	V_{OLTHP}	-	-	0.5	V	THP active, V_{LL}=3.3V, I_{THP}=1mA
4	THP temperature threshold	T_{THP}	90	110	130	ºC	Thermal protection flag indicator by THP pin (open N-MOS drain, Low=THP activating)
5	THP reset hysteresis	T_{HYSTHP}	-	10	-	ºC	

3. AC Characteristics

Table 5 AC Characteristics

V_{LL}=3.3V, V_{DD}=5V, LEB=0, BANK_EN=0/1, T_A=25°C, unless otherwise specified.

No.	Items		Symbol	Spec			Units	Conditions
				Min	Typ	Max		
1	Turn-on time		t_{ON}	-	2	4	μs	
			t_{ON_BNK}	-	2	4	μs	
2	Turn-off time		t_{OFF}	-	2	4	μs	
			t_{OFF_BNK}	-	2	4	μs	
3	Output switching frequency		f_{SW}	-	-	50	kHz	Duty cycle=50%
4	Small signal frequency		f_{SIG}	0.01	-	85	MHz	C_L=220pF
5	Off isolation	small signal	$V_{ISO(RX)}$	-	-75	-	dB	f_{SIG}=5MHz, R_L=50Ω
		large signal	$V_{ISO(TX)}$	-	-67	-	dB	f_{SIG}=5MHz, R_L=50Ω
6	Crosstalk		V_{CT}	-	-60	-	dB	f_{SIG}=5MHz, R_L=50Ω
7	On capacitance	small signal	$C_{ON(RX)}$	-	25	-	pF	V_{SIG}=0V, f_{SIG}=1MHz
		large signal	$C_{ON(TX)}$	-	15	-	pF	V_{SIG}=10Vpp, f_{SIG}=1MHz
8	Off capacitance SW_P to GND	small signal	$C_{OFF(SWP\_RX)}$	-	20	-	pF	V_{SIG}=0V, f_{SIG}=1MHz
9	Off capacitance SW_A to GND	small signal	$C_{OFF(SWA\_RX)}$	-	18	-	pF	V_{SIG}=0V, f_{SIG}=1MHz
		large signal	$C_{OFF(SWA\_TX)}$	-	10	-	pF	V_{SIG}=10Vpp, f_{SIG}=1MHz
10	Output spike voltage (SW_P)		$V_{SPK\_ON(SWP)}$	-	50	-	mV	50Ω load @switch on
			$V_{SPK\_OFF(SWP)}$	-	50	-	mV	50Ω load @switch off
11	Output spike voltage (SW_A)		$V_{SPK\_ON(SWA)}$	-	50	-	mV	50Ω load @switch on
			$V_{SPK\_OFF(SWA)}$	-	50	-	mV	50Ω load @switch off
12	Charge injection		QC	-	10	-	pC	

■ Test Circuits

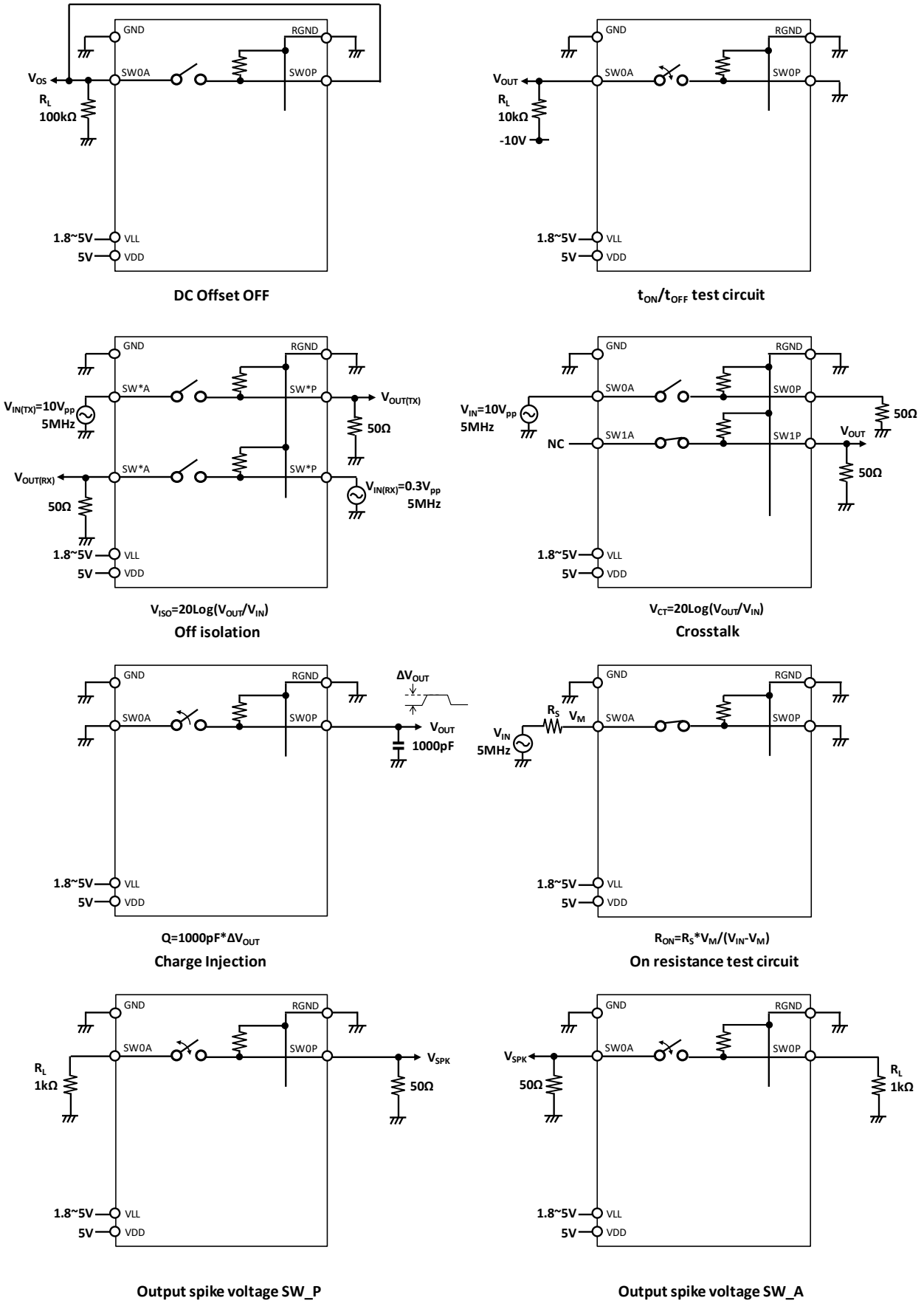


Figure 2 Test Circuits

■ Truth Table

Table 6 Truth Table

Logic Inputs								Analog Switch State				
LEB	CLR	BANK_EN	DIN									
			D0	D1	···	D30	D31	SW0	SW1	···	SW30	SW31
L	L	L	L	-		-	-	OFF	-		-	-
L	L	L	H	-		-	-	ON	-		-	-
L	L	L	-	L		-	-	-	OFF		-	-
L	L	L	-	H		-	-	-	ON		-	-
L	L	L	-	-		-	-	-	-		-	-
L	L	L	-	-		-	-	-	-		-	-
L	L	L	-	-		-	-	-	-		-	-
L	L	L	-	-		-	-	-	-		-	-
L	L	L	-	-	···	-	-	-	-	···	-	-
L	L	L	-	-		-	-	-	-		-	-
L	L	L	-	-		-	-	-	-		-	-
L	L	L	-	-		-	-	-	-		-	-
L	L	L	-	-		-	-	-	-		-	-
L	L	L	-	-		L	-	-	-		OFF	-
L	L	L	-	-		H	-	-	-		ON	-
L	L	L	-	-		-	L	-	-		-	OFF
L	L	L	-	-		-	H	-	-		-	ON
H	L	L	X	X	X	X	X	Hold Previous State				
X	H	L	X	X	X	X	X	ALL SWs OFF				
X	X	H	L					ALL SWs OFF				
X	X	H	H					ALL SWs ON				

■ Logic Timing

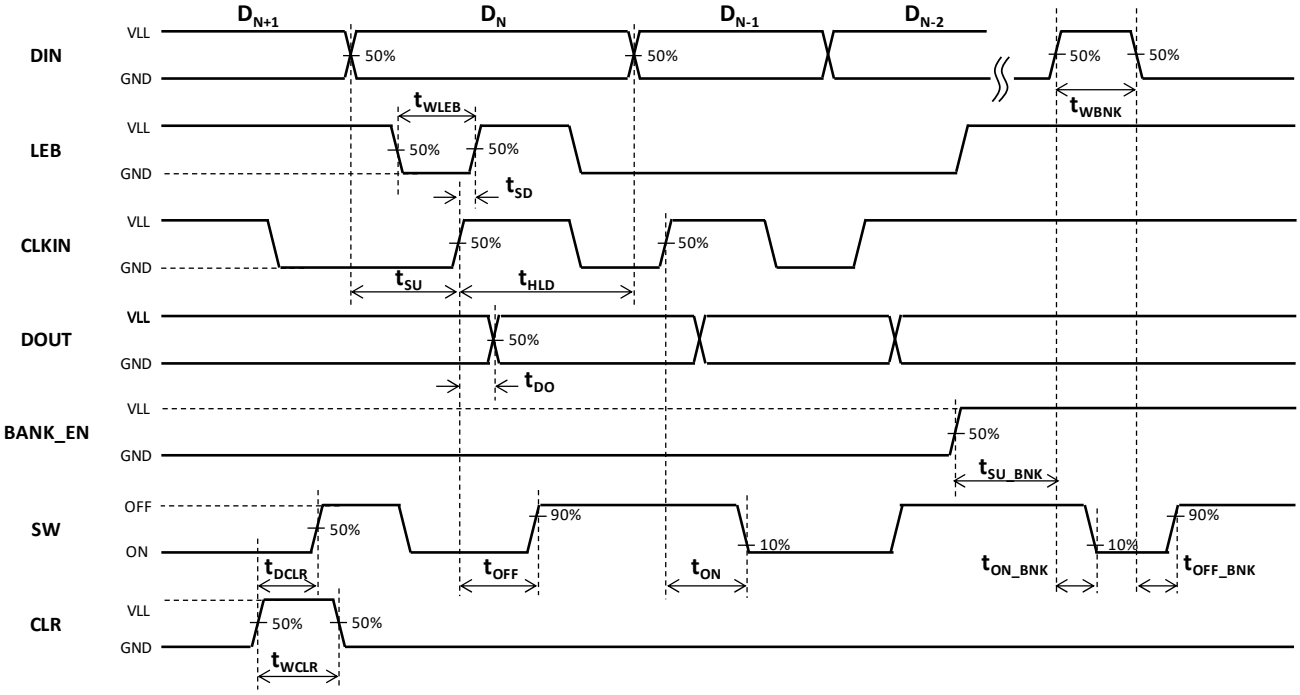


Figure 3 Logic Timing

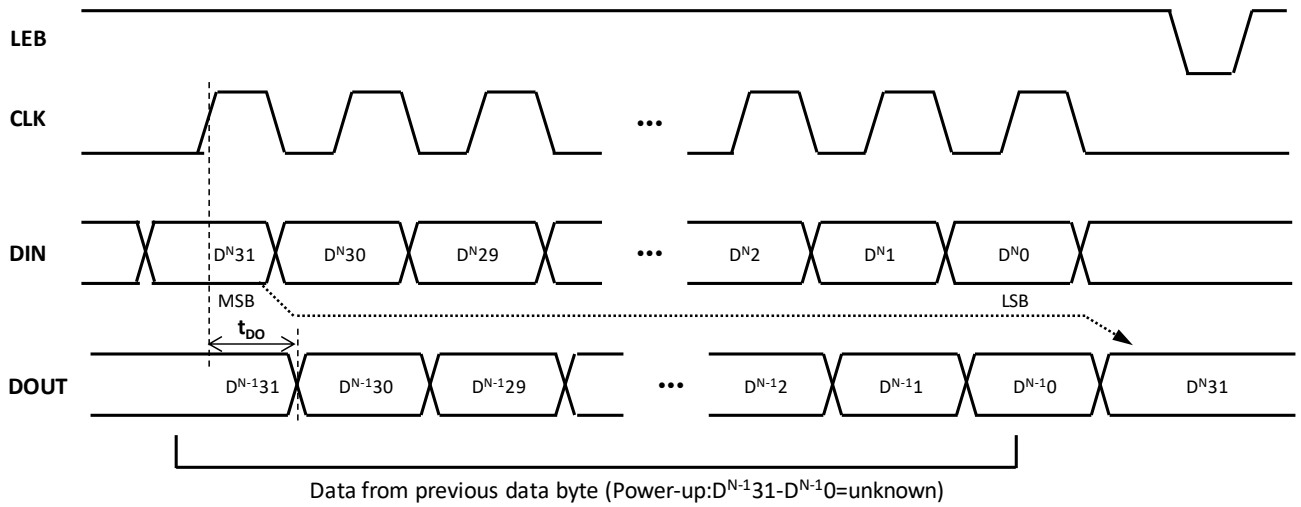


Figure 4 Latch Enable Interface Timing

■ Pin Configuration

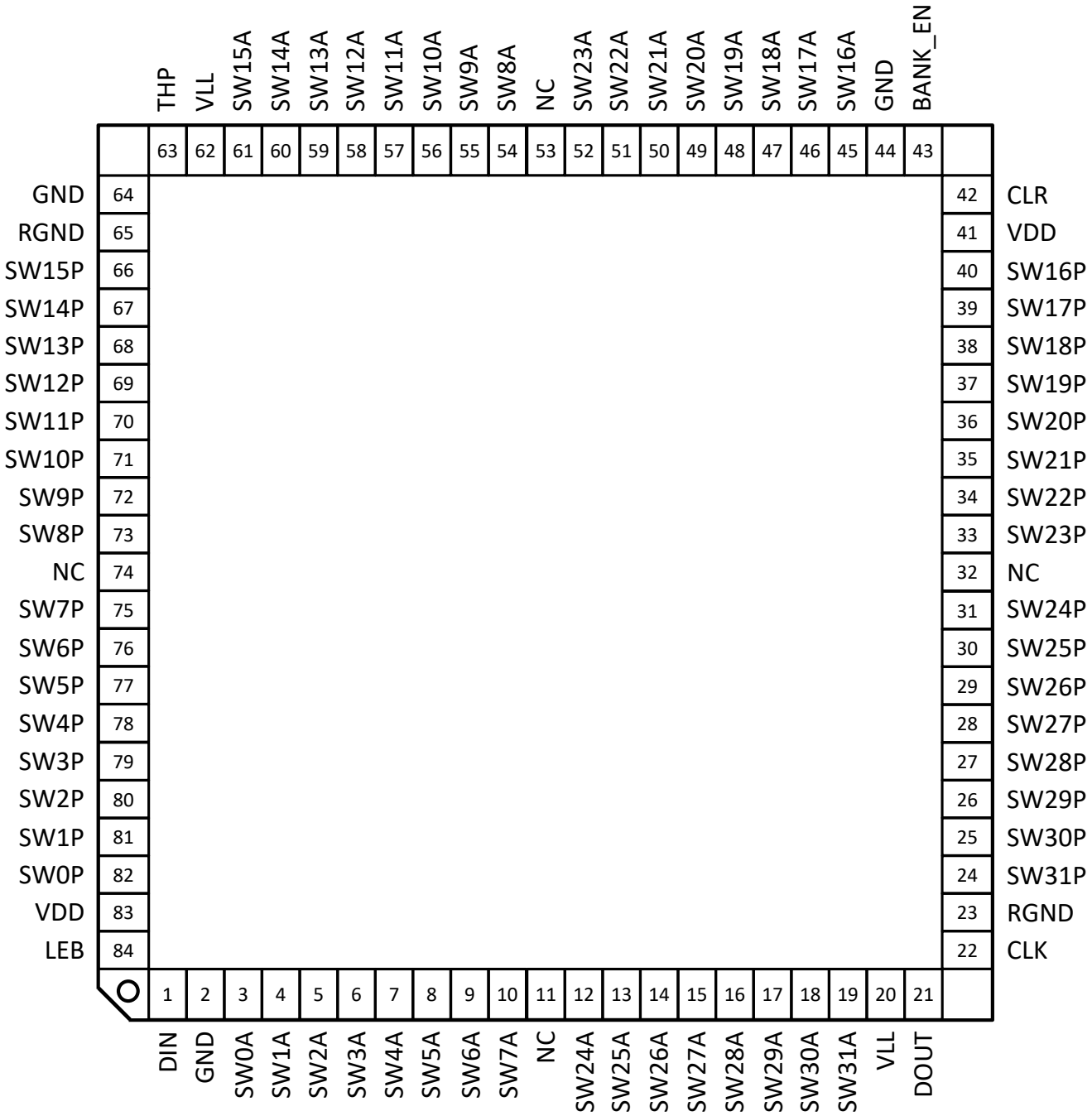


Figure 5 Pin Configuration

Table 7 Pin Configuration (1 / 2)

Pin#	Pin Name	I/O	Function
1	DIN	I	Serial-Data (BANK_EN=0) / Bank-Data (BANK_EN=1) input
2	GND	-	Drive power ground (0V)
3	SW0A	I/O	Analog switch terminal 0 (AFE side)
4	SW1A	I/O	Analog switch terminal 1 (AFE side)
5	SW2A	I/O	Analog switch terminal 2 (AFE side)
6	SW3A	I/O	Analog switch terminal 3 (AFE side)
7	SW4A	I/O	Analog switch terminal 4 (AFE side)
8	SW5A	I/O	Analog switch terminal 5 (AFE side)
9	SW6A	I/O	Analog switch terminal 6 (AFE side)
10	SW7A	I/O	Analog switch terminal 7 (AFE side)
11	NC	-	No connection (Not internally connected)
12	SW24A	I/O	Analog switch terminal 24 (AFE side)
13	SW25A	I/O	Analog switch terminal 25 (AFE side)
14	SW26A	I/O	Analog switch terminal 26 (AFE side)
15	SW27A	I/O	Analog switch terminal 27 (AFE side)
16	SW28A	I/O	Analog switch terminal 28 (AFE side)
17	SW29A	I/O	Analog switch terminal 29 (AFE side)
18	SW30A	I/O	Analog switch terminal 30 (AFE side)
19	SW31A	I/O	Analog switch terminal 31 (AFE side)
20	VLL	-	Positive voltage supply of low voltage interface (+1.8V~+5V)
21	DOUT	O	Serial-Data output
22	CLK	I	Serial-Clock input
23	RGND	-	Bleed resistor ground (0V)
24	SW31P	I/O	Analog switch terminal 31 (Probe side)
25	SW30P	I/O	Analog switch terminal 30 (Probe side)
26	SW29P	I/O	Analog switch terminal 29 (Probe side)
27	SW28P	I/O	Analog switch terminal 28 (Probe side)
28	SW27P	I/O	Analog switch terminal 27 (Probe side)
29	SW26P	I/O	Analog switch terminal 26 (Probe side)
30	SW25P	I/O	Analog switch terminal 25 (Probe side)
31	SW24P	I/O	Analog switch terminal 24 (Probe side)
32	NC	-	No connection (Not internally connected)
33	SW23P	I/O	Analog switch terminal 23 (Probe side)
34	SW22P	I/O	Analog switch terminal 22 (Probe side)
35	SW21P	I/O	Analog switch terminal 21 (Probe side)
36	SW20P	I/O	Analog switch terminal 20 (Probe side)
37	SW19P	I/O	Analog switch terminal 19 (Probe side)
38	SW18P	I/O	Analog switch terminal 18 (Probe side)
39	SW17P	I/O	Analog switch terminal 17 (Probe side)
40	SW16P	I/O	Analog switch terminal 16 (Probe side)
41	VDD	-	Positive low voltage power supply (+5V)
42	CLR	I	Shift register and latch clear input

Table 7 Pin Configuration (2 / 2)

Pin#	Pin Name	I/O	Function
43	BANK_EN	I	Logic interface control, Hi=Bank interface, Low=Serial data interface
44	GND	-	Drive power ground (0V)
45	SW16A	I/O	Analog switch terminal 16 (AFE side)
46	SW17A	I/O	Analog switch terminal 17 (AFE side)
47	SW18A	I/O	Analog switch terminal 18 (AFE side)
48	SW19A	I/O	Analog switch terminal 19 (AFE side)
49	SW20A	I/O	Analog switch terminal 20 (AFE side)
50	SW21A	I/O	Analog switch terminal 21 (AFE side)
51	SW22A	I/O	Analog switch terminal 22 (AFE side)
52	SW23A	I/O	Analog switch terminal 23 (AFE side)
53	NC	-	No connection (Not internally connected)
54	SW8A	I/O	Analog switch terminal 8 (AFE side)
55	SW9A	I/O	Analog switch terminal 9 (AFE side)
56	SW10A	I/O	Analog switch terminal 10 (AFE side)
57	SW11A	I/O	Analog switch terminal 11 (AFE side)
58	SW12A	I/O	Analog switch terminal 12 (AFE side)
59	SW13A	I/O	Analog switch terminal 13 (AFE side)
60	SW14A	I/O	Analog switch terminal 14 (AFE side)
61	SW15A	I/O	Analog switch terminal 15 (AFE side)
62	VLL	-	Positive voltage supply of low voltage interface (+1.8V~+5V)
63	THP	O	Thermal protection output flag, open N-MOS drain
64	GND	-	Drive power ground (0V)
65	RGND	-	Bleed resistor ground (0V)
66	SW15P	I/O	Analog switch terminal 15 (Probe side)
67	SW14P	I/O	Analog switch terminal 14 (Probe side)
68	SW13P	I/O	Analog switch terminal 13 (Probe side)
69	SW12P	I/O	Analog switch terminal 12 (Probe side)
70	SW11P	I/O	Analog switch terminal 11 (Probe side)
71	SW10P	I/O	Analog switch terminal 10 (Probe side)
72	SW9P	I/O	Analog switch terminal 9 (Probe side)
73	SW8P	I/O	Analog switch terminal 8 (Probe side)
74	NC	-	No connection (Not internally connected)
75	SW7P	I/O	Analog switch terminal 7 (Probe side)
76	SW6P	I/O	Analog switch terminal 6 (Probe side)
77	SW5P	I/O	Analog switch terminal 5 (Probe side)
78	SW4P	I/O	Analog switch terminal 4 (Probe side)
79	SW3P	I/O	Analog switch terminal 3 (Probe side)
80	SW2P	I/O	Analog switch terminal 2 (Probe side)
81	SW1P	I/O	Analog switch terminal 1 (Probe side)
82	SW0P	I/O	Analog switch terminal 0 (Probe side)
83	VDD	-	Positive low voltage power supply (+5V)
84	LEB	I	Active-Low latch enable input, Hi=Hold data, Low=Latch data input

■ Package

Table 8 Package Drawing Codes

Package Name	Dimension	Tray	Marking	Land	Packing
QFN-84(1010)B	QN084-B-P-SD	QN084-B-T-SD	QN084-B-M-SD	QN084-B-L-SD	QN084-B-K-SD

■ Storage, Mounting

1. Storage conditions

1. 1 The storage location should be kept at 5 to 35°C and 40 to 70% relative humidity. Keeping in a dry box is recommended. Moisture-proof property is assured for 12 months from delivery date for sealed moisture-proof packing, while it is guaranteed for 7 days from unpacked date under the condition above.

1. 2 When the storage conditions do not conform to those above or other conditions occur indicating moisture exposure, the ICs should be dried to avoid package cracks. A baking process at 125°C lasting for 24 hours results in sufficient dehumidification. The baking is not allowed more than twice, and the ICs should be mounted within 7 days after initial baking or within 10 days of total exposure after the second dehumidification.

2. Reflow soldering

The temperature rise may be different in the resin and a terminal part due to the reflow soldering.
It is necessary to check the package surface temperature (resin) before setting the temperature profile.
Figure 6 shows the resistance to soldering heat condition for package (Reflow method).
Confirm the heat resistance of the package shown below. (Based on JEDEC J-STD-020).

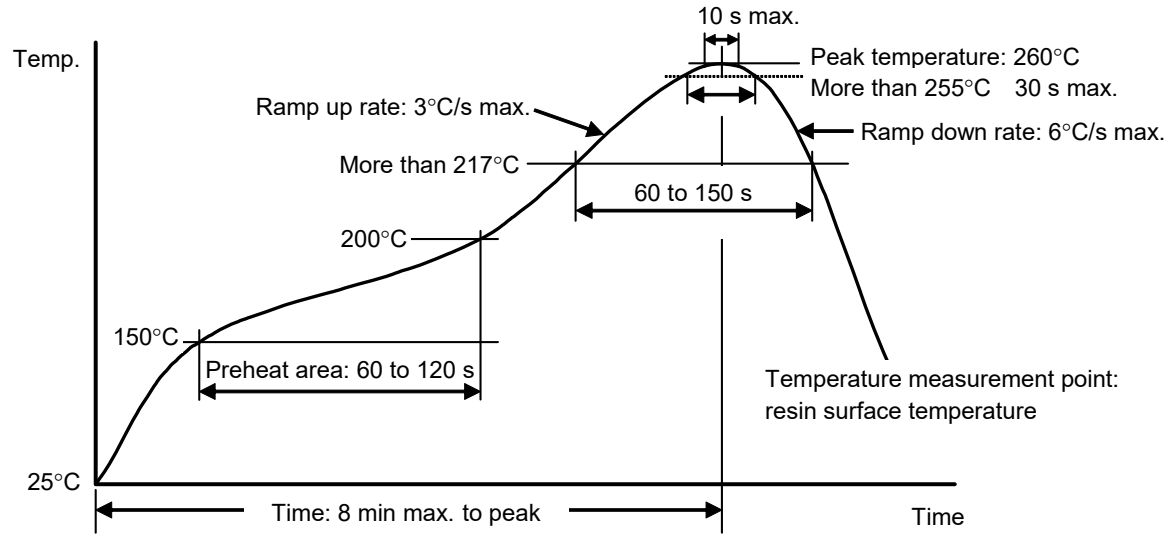


Figure 6 Resistance to Soldering Heat Condition for Package (Reflow Method)

■ Important Notice

1. ABLIC Inc. warrants performance of its hardware products (hereinafter called “products”) to the specifications applicable at the time of sale in accordance with the Product Specification. Testing and other quality control techniques are utilized to the extent ABLIC Inc. needs to meet specifications described in the Product Specification. Specific testing of all parameters of each device is not necessarily performed, except those mandated by related laws and/or regulations.

2. Should any claim be made within one month of product delivery about products’ failure to meet performance described in the Product Specification, all the products in relevant lot(s) shall be re-tested and re-delivered. Products delivered more than one month before such claim shall not be counted for such response.

3. ABLIC Inc. assumes no obligation or any way of compensation should any fault about customer products and applications using ABLIC Inc. products be found in marketplace. Only in such a case fault of ABLIC Inc. is evident and products concerned do not meet the Product Specification, compensation shall be conducted if claimed within one year of product delivery up to in the way of product replacement or payment of equivalent amount.

4. ABLIC Inc. reserves the right to make changes to the Product Specification at any time and to discontinue mass production of the relevant products without notice. Customers are advised before placing orders to confirm that the Product Specification of inquiry is the latest version and that the relevant product is currently on mass production status.

5. In no event shall ABLIC Inc. be liable for any damage that may result from an accident or any other cause during operation of the user’s units according to the Product Specification. ABLIC Inc. assumes no responsibility for any intellectual property claims or any other problems that may result from applications of information, products or circuits described in the Product Specification.

6. No license is granted by the Product Specification under any patents or other rights of any third party or ABLIC Inc.

7. The Product Specification may not be reproduced or duplicated, in any form, in whole or in part, without the expressed written permission of ABLIC Inc.

8. Resale of ABLIC Inc. products with statements different from or beyond the parameters described in the Product Specification voids all express and any implied warranties for the products, and is an unfair and deceptive business practice. ABLIC Inc. is not responsible or liable for any such statements.

9. Products (technologies) described in the Product Specification are not to be provided to any party whose purpose in their application will hinder maintenance of international peace and safety nor are they to be applied to that purpose by their direct purchasers or any third party. When exporting those products (technologies), the necessary procedures are to be taken in accordance with related laws and regulations.

■ Cautions

1. Customers are advised to follow the cautions below to protect products from damage caused by electrical static discharge (ESD).

1. 1 Material of container or any device to carry products should be free from ESD, which may be caused by vibration while transportation. It is recommended that electric-conductive container or aluminum sheet be used as an effective countermeasure.

1. 2 Those that touch products, such as work platform, machine, or measurement/test equipment, should be grounded.

1. 3 Those who deal with products should be grounded through a large series impedance around 100kΩ to 1MΩ.

1. 4 Prevent friction with other materials made with high polymer.

1. 5 Prevent vibration or friction when carrying the printed circuit board (PCB) where products are mounted. To short circuit terminals is a recommended countermeasure to keep the same electric potential on the PCB.

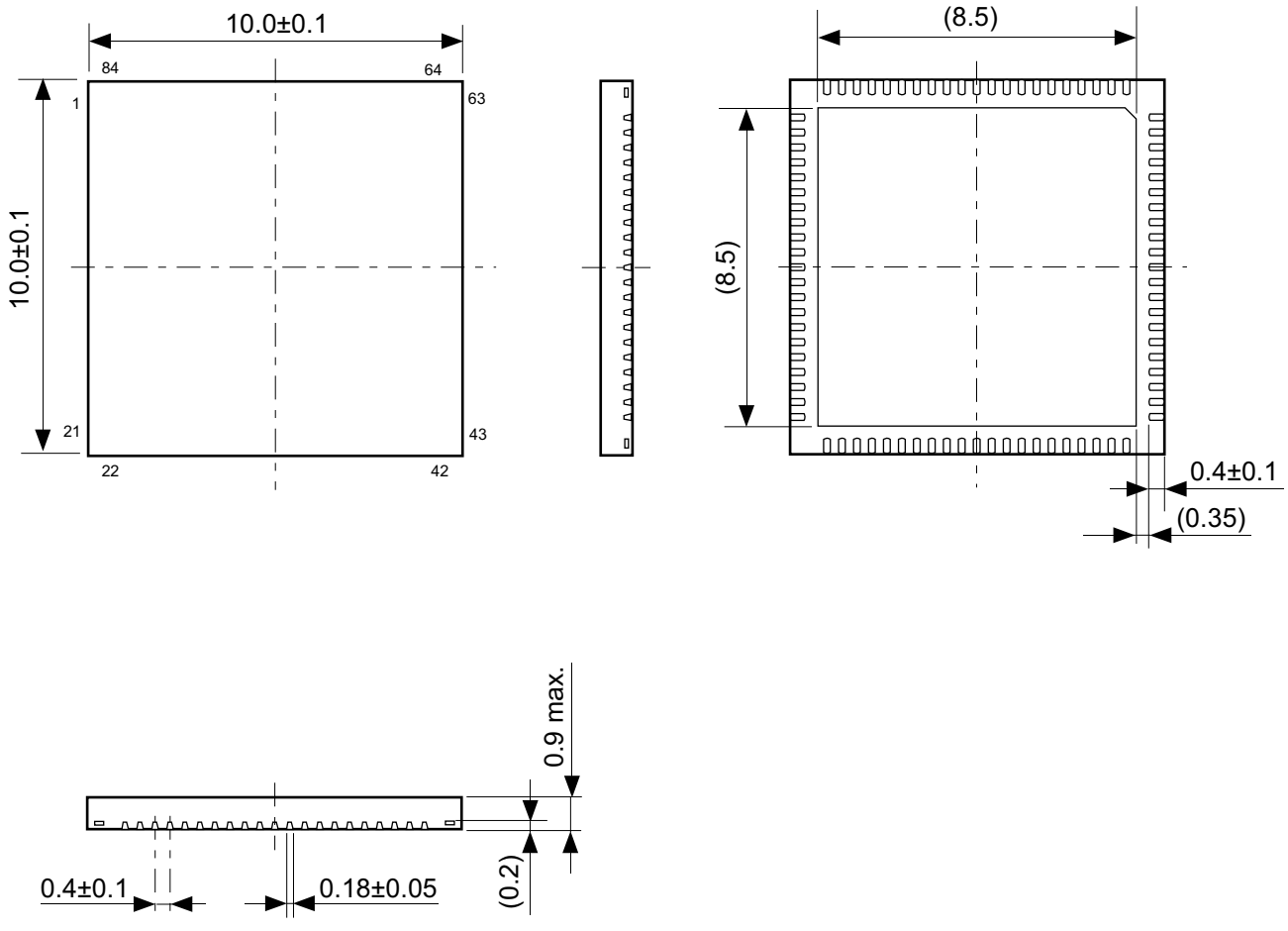
1. 6 Avoid dealing with or storing products in an extremely arid environment.

2. "Absolute maximum ratings" should never be exceeded during use regardless of any change in external conditions. Otherwise, products may be damaged or destroyed. In no event shall ABLIC Inc. be liable for any failure in products or any secondary damage resulting from use at a value exceeding the absolute maximum ratings.

3. Products may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of a failure. (If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)

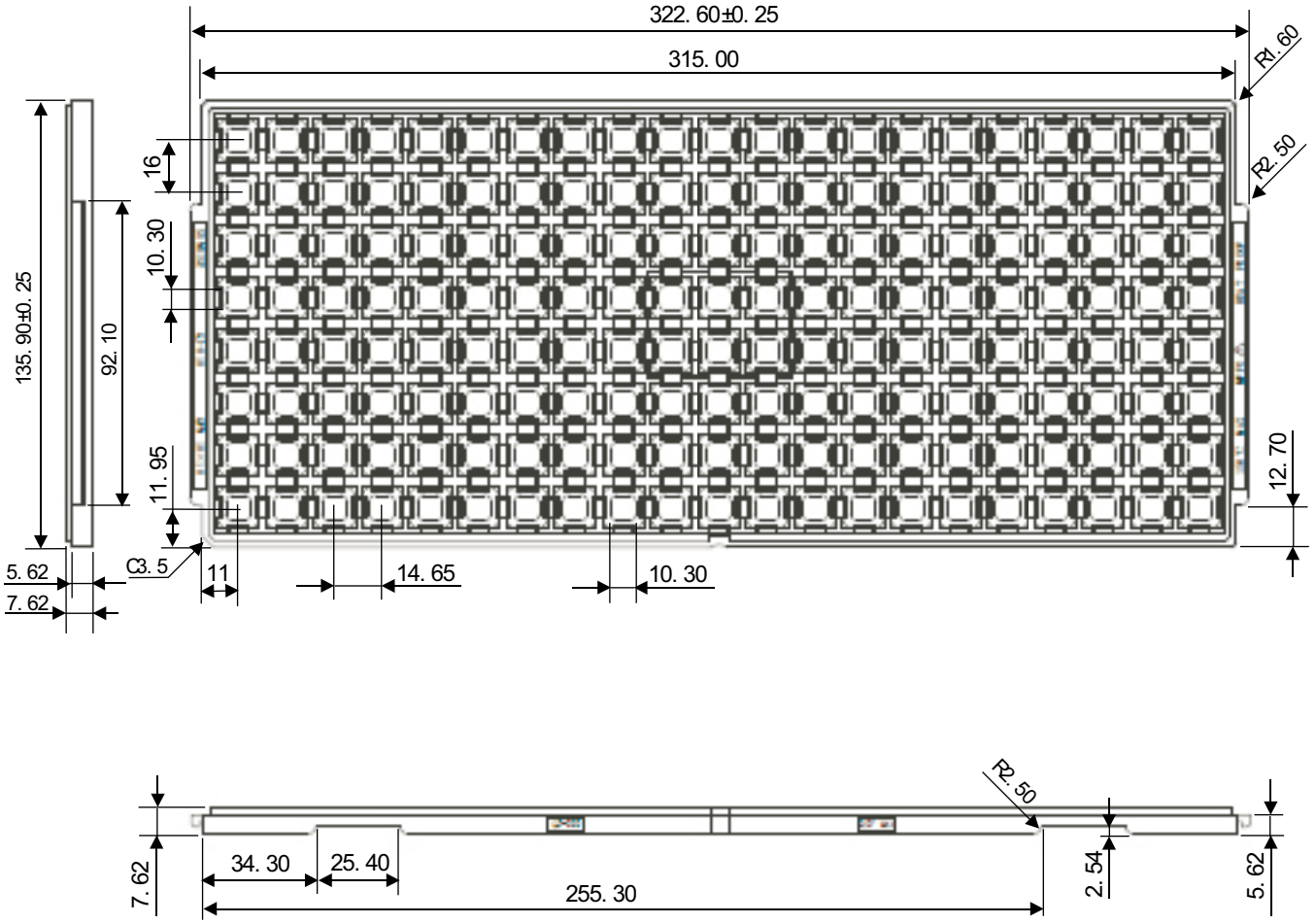
4. Products may experience failures or malfunction in poor surroundings, such as electrical leakage in products due to long-term use in high humidity, malfunctioning or permanent damage due to chemical reaction of products in corrosive environment or due to discharge by strongly charged object near products or due to excessive mechanical shock. To use products in radiation environment is not assumed. To use products near material easy to ignite may cause a fire due to its flammable package. Avoid using products in such environment or take appropriate countermeasures depending on the environment.

5. Products are not designed, manufactured, or warranted to be suitable for use where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment). Inclusion of products in such application shall be fully at the risk of customers. ABLIC Inc. assumes no liability for applications assistance, customer product design, or performance.

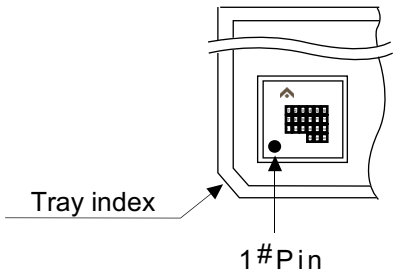


No. QN084-B-P-SD-1.0

TITLE	QFN84-B-PKG Dimensions
No.	QN084-B-P-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	



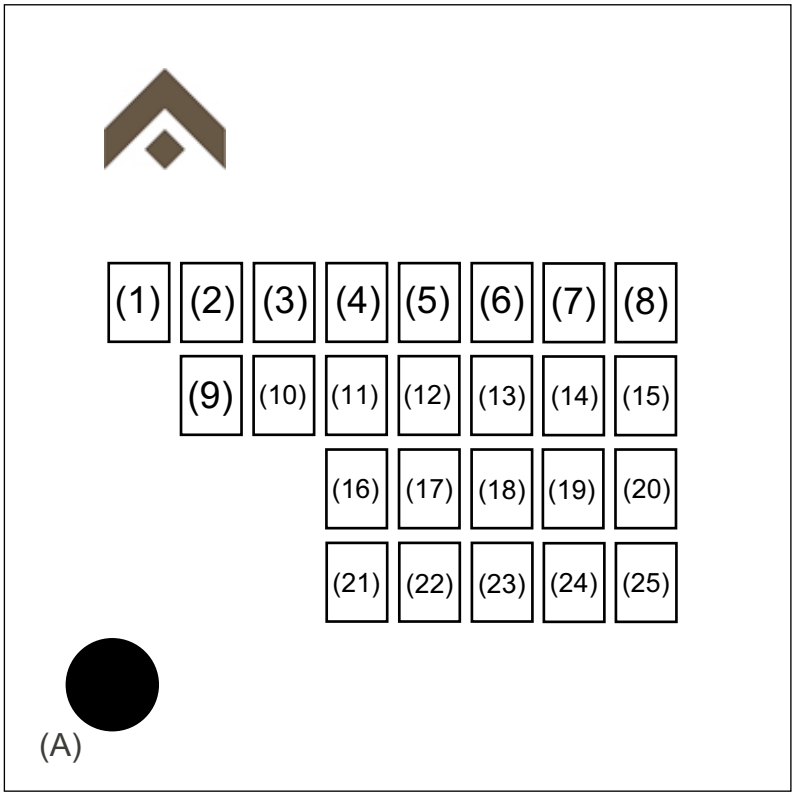
(Direction of IC in tray)



No. QFN84-B-T-SD-1.0

TITLE	QFN84-B-Tray		
No.	QN084-B-T-SD-1.0		
ANGLE		QTY.	168
UNIT	mm		

ABLIC Inc.



(1) to (10) : Product code

(11) , (12) : Quality control code

(13) : Year of assembly

(14) : Month of assembly

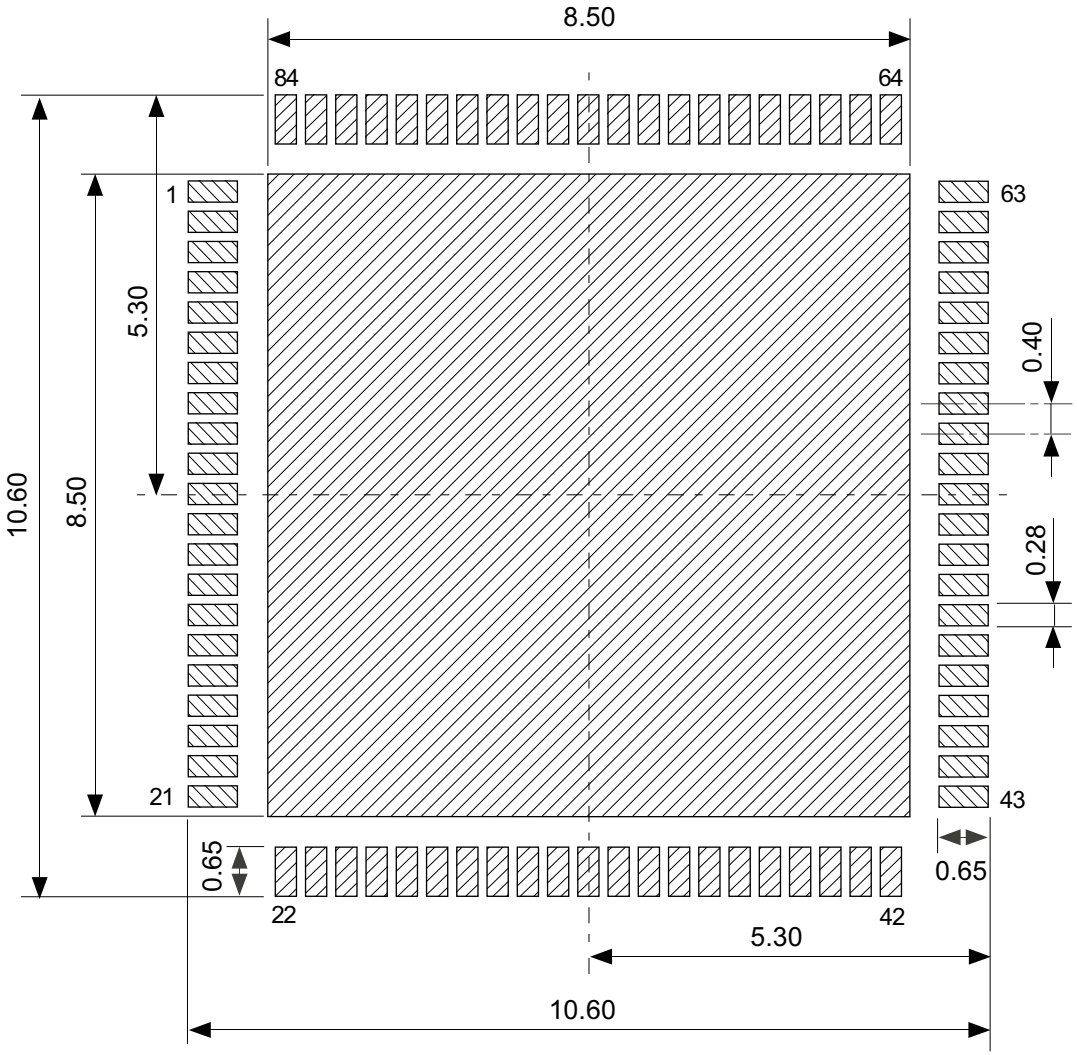
(15) : Week of assembly

(16) to (25) : Quality control code

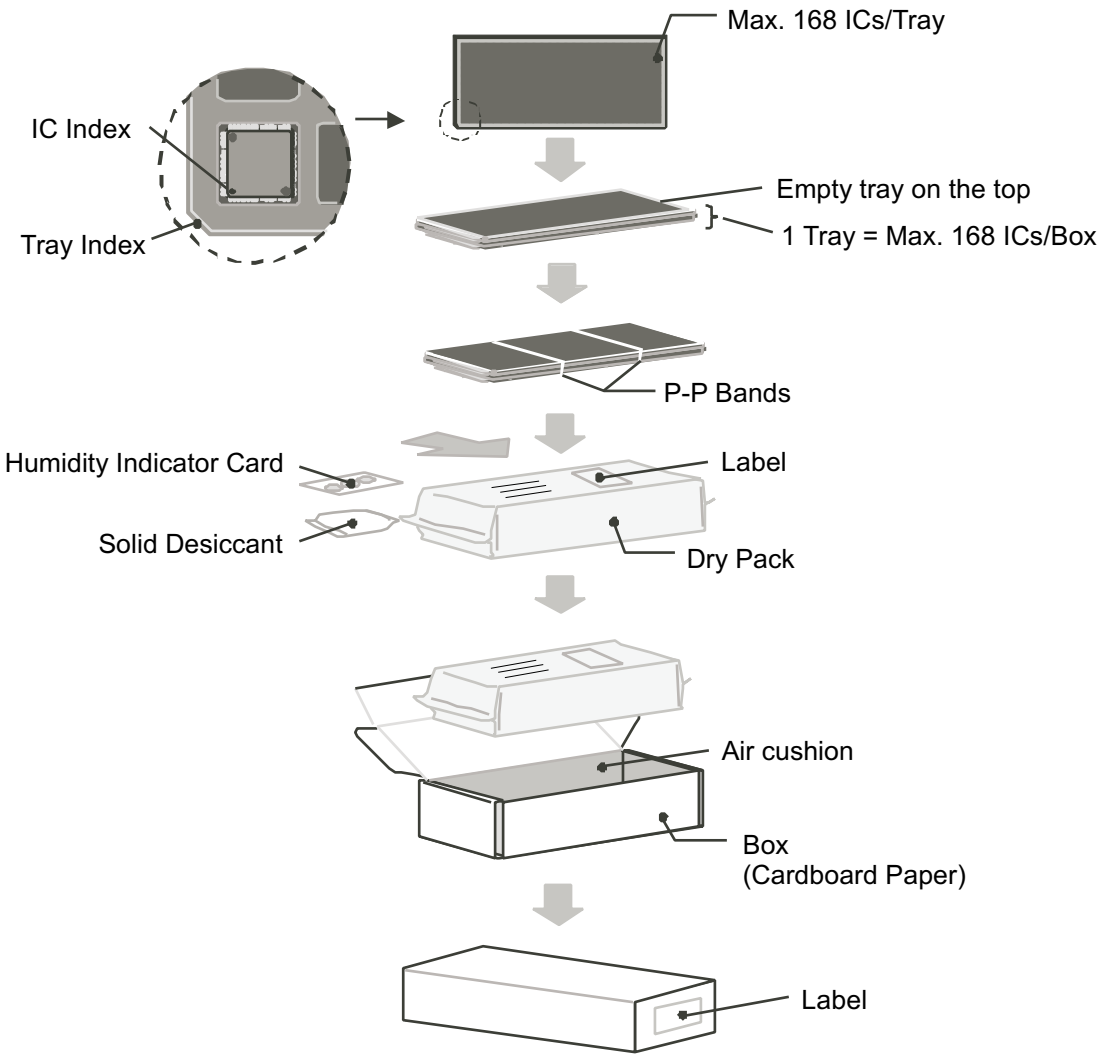
(A) : 1-pin mark

No. QFN84-B-M-SD-1.0

TITLE	QFN84-B-Markings		
No.	QN084-B-M-SD-1.0		
ANGLE			
UNIT		TYPE	LASER
ABLIC Inc.			



TITLE	QFN84-B -Land Recommendation
No.	QN084-B-L-SD-1.0
ANGLE	
UNIT	mm
	ABLIC Inc.



TITLE	QFN84-B -Packing Procedure
No.	QN084-B-K-SD-1.0
ANGLE	
UNIT	
ABLIC Inc.	

Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the reasons other than the products described herein (hereinafter "the products") or infringement of third-party intellectual property right and any other right due to the use of the information described herein.
3. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the incorrect information described herein.
4. Be careful to use the products within their ranges described herein. Pay special attention for use to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by failures and / or accidents, etc. due to the use of the products outside their specified ranges.
5. Before using the products, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products are strictly prohibited from using, providing or exporting for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by any provision or export to the person or entity who intends to develop, manufacture, use or store nuclear, biological or chemical weapons or missiles, or use any other military purposes.
8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses by ABLIC, Inc. Do not apply the products to the above listed devices and equipments.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by unauthorized or unspecified use of the products.
9. In general, semiconductor products may fail or malfunction with some probability. The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.
   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of ABLIC Inc. The information described herein does not convey any license under any intellectual property rights or any other rights belonging to ABLIC Inc. or a third party. Reproduction or copying of the information from this document or any part of this document described herein for the purpose of disclosing it to a third-party is strictly prohibited without the express permission of ABLIC Inc.
14. For more details on the information described herein or any other questions, please contact ABLIC Inc.'s sales representative.
15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.

2.4-2019.07