The MUZE Family of Z8 Microcontrollers

MAXIMUM MEMORY WITH UART AND ZiLOG EXPANDABLE EPROM

Product Specification

PRELIMINARY

PS004005-1100

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Architectural Overview

ZiLOG's large Z8® family of 8-bit microcontrollers now includes the MUZE product line, featuring 4 KB to 64 KB of In-Circuit Serially-Programmable (ICSP) OTP memory, an industry-standard Universal Asynchronous Receiver/Transmitter (UART), enhanced wake-up circuitry, programmable Watch-Dog Timers (WDT), and low-noise/EMI options. Each of the new enhancements to the Z8 offers a more efficient, cost-effective design and provides the user with increased design flexibility over the standard Z8 microcontroller core. The low-power-consumption OTP microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

The MUZE family features an Expanded Register File (ERF) to allow access to register-mapped peripheral and I/O circuits. Four basic address spaces are available to support this wide range of configurations: Program Memory, Register File, Data Memory, and ERF. The Register File is composed of 236 bytes contained within one general-purpose register (GPR), 4 I/O port registers, 15 control registers, and status registers. The ERF consists of 12 control registers.

For applications demanding powerful I/O capabilities, the Z86E122/E123/E124/E125/E126 offers 16 pins, the Z86E132/E133/E134/E135/E136 offers 24 pins, and the Z86E142/E143/144/E145/E146 offers 32 pins dedicated to input and output. These lines are configurable under software control to provide timing, status signals, parallel I/O with or without handshake, and address/data bus for interfacing external memory.

The MUZE family operates at 16 MHz with a voltage range of 4.5 to 5.5 V_{DC} and up to 12 MHz with a voltage range of 3.0 to 5.5 V_{DC}.

To unburden the system from coping with real-time tasks such as counting/timing and data communication, the Z8 offers two on-chip counter/timers with a large number of user-selectable modes and a hardware UART.

With ROM/ROMless selectivity, the Z86E142/E143/E144/E145/E146 provides both external memory and ICSP, which enables this Z8® MCU to be used in high-volume applications, or where code flexibility is required.

Note: All signals with an overline are active Low. For example, B/$\overline{W}$, for which WORD is active Low, and $\overline{B}$/W, for which BYTE is active Low.

Power connections follow these conventional descriptions:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

MUZE Features

Table 1. MUZE Family Features

Device	OTP (KB)	RAM* (Bytes)	Speed 4.5V to 5.5V (MHz—Standard and Extended Temperature)	Speed 3.0V to 5.5V (MHz—Standard Temperature Only)
Z86E122	4	236	16	12
Z86E123	8	236	16	12
Z86E124	16	236	16	12
Z86E125	32	236	16	12
Z86E126	64	236	16	12
Z86E132	4	236	16	12
Z86E133	8	236	16	12
Z86E134	16	236	16	12
Z86E135	32	236	16	12
Z86E136	64	236	16	12
Z86E142	4	236	16	12
Z86E143	8	236	16	12
Z86E144	16	236	16	12
Z86E145	32	236	16	12
Z86E146	64	236	16	12

Note: *General-Purpose.

- 4 KB to 64 KB OTP Memory
- Full-Duplex UART Asynchronous Serial Communications Interface (ASCI)
- Dedicated 16-Bit Baud Rate Generator (BRG)
- In-Circuit Serial Programming Interface
- 20-Pin DIP and 20-Pin SOIC (E122, E123, E124, E125, E126)
- 28-Pin DIP and 28-Pin SOIC (E132, E133, E134, E135, E136)
- 40-Pin DIP and 44-Pin PQFP Packages (E142, E143, E144, E145, E146)
- 3.0- to 5.5-Volt Operating Range

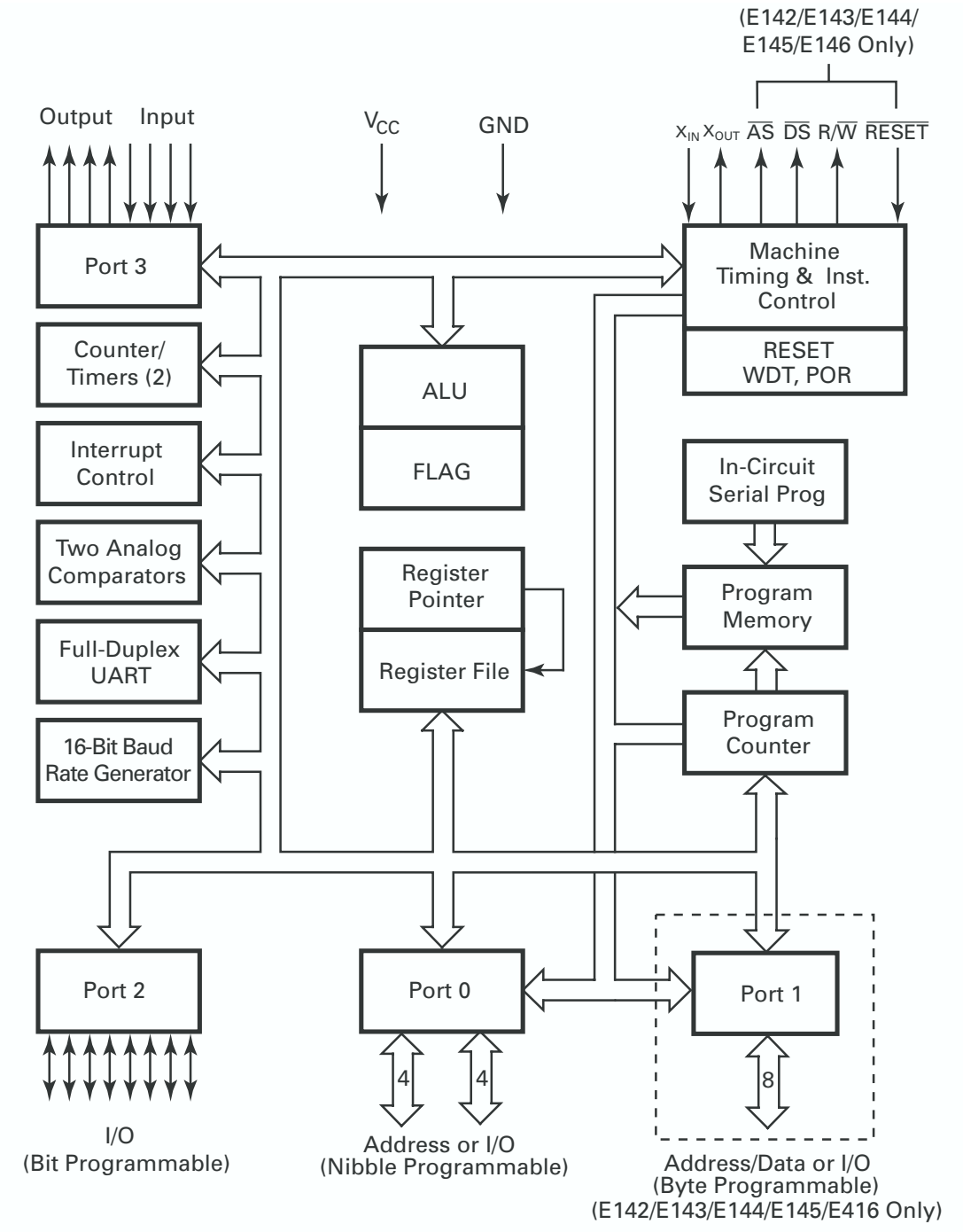
- Operating Temperature Ranges:
  Standard: 0ºC to 70ºC
  Extended: –40ºC to +105ºC

Note: The extended temperature range is only for the 4.5- to 5.5-volt part, at 16-MHz max. operation.

- Expanded Register File (ERF)
- 16 Input/Output Lines (E122, E123, E124, E125, E126)
  24 Input/Output Lines (E132, E133, E134, E135, E136)
  32 Input/Output Lines (E142, E143, E144, E145, E146)
- Vectored, Prioritized Interrupts with Programmable Polarity
- Two Analog Comparators
- Two Programmable 8-Bit Counter/Timers, each with a 6-Bit Programmable Prescaler
- VBO/Power-On Reset (POR)
- Clock-Free Watch-Dog Timer (WDT) Reset
- On-Chip Oscillator that accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock
- RAM and EPROM Protect
- Optional 32-kHz Oscillator

Functional Block Diagram

Figure 1. MUZE Functional Block Diagram



Pin Description

Figure 2. 20-Pin DIP/SOIC Pin Configuration

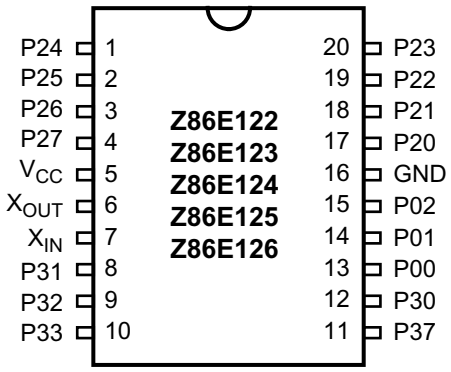


Table 2. 20-Pin DIP/SOIC Pin Identification

Pin #	Symbol	Function	Direction
1–4	P24–P27	Port 2, Bits 4,5,6,7	Input/Output
5	V_{CC}	Power Supply	
6	X_{OUT}	Crystal Oscillator	Output
7	X_{IN}	Crystal Oscillator	Input
8–10	P31–P33	Port 3, Bits 1,2,3	Fixed Input
11	P37	Port 3, Bit 7	Fixed Output
12	P30	Port 3, Bit 0	Fixed Input
13–15	P00–P02	Port 0, Bits 0,1,2	Input/Output
16	GND	Ground	
17–20	P20–P23	Port 2, Bits 0,1,2,3	Input/Output

Figure 3. 20-Pin DIP/SOIC Pin Configuration—ICSP Mode

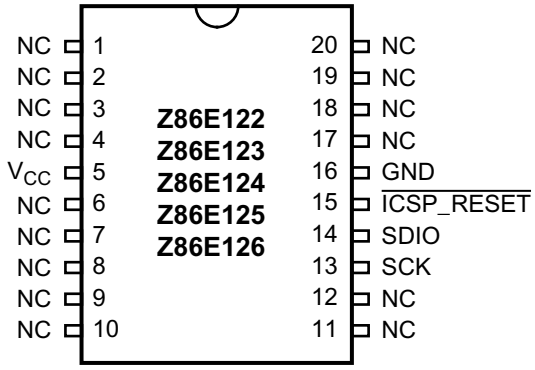


Table 3. 20-Pin DIP/SOIC Pin Identification—ICSP Mode

Pin #	Symbol	Function	Direction
1–4	NC	No Connection	
5	V_{CC}	Power Supply	
6–12	NC	No Connection	
13	SCK	Serial ICSP Clock	Input
14	SDIO	Serial Data	Input/Output
15	$\overline{\text{ICSP\_RESET}}$	ICSP Reset	Input
16	GND	Ground	
17–20	NC	No Connection	

Figure 4. 28-Pin DIP/SOIC Pin Configuration

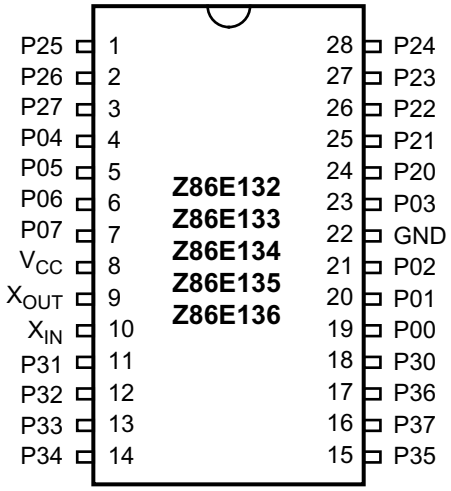


Table 4. 28-Pin DIP/SOIC Pin Identification

Pin #	Symbol	Function	Direction
1–3	P25	Port 2, Bit 5	Input/Output
2	P26	Port 2, Bit 6	Input/Output
3	P27	Port 2, Bit 7	Input/Output
4	P04	Port 0, Bit 4	Input/Output
5	P05	Port 0, Bit 5	Input/Output
6	P06	Port 0, Bit 6	Input/Output
7	P07	Port 0, Bit 7	Input/Output
8	V_{CC}	Power Supply	
9	X_{OUT}	Crystal Oscillator	Output
10	X_{IN}	Crystal Oscillator	Input
11	P31	Port 3, Bit 1	Fixed Input
12	P32	Port 3, Bit 2	Fixed Input
13	P33	Port 3, Bit 3	Fixed Input
14	P34	Port 3, Bit 4	Fixed Output
15	P35	Port 3, Bit 5	Fixed Output
16	P37	Port 3, Bit 7	Fixed Output

Table 4. 28-Pin DIP/SOIC Pin Identification (Continued)

Pin #	Symbol	Function	Direction
17	P36	Port 3, Bit 6	Fixed Output
18	P30	Port 3, Bit 0	Fixed Input
19	P00	Port 0, Bit 0	Input/Output
20	P01	Port 0, Bit 0	Input/Output
21	P02	Port 0, Bit 2	Input/Output
22	GND	Ground	
23	P03	Port 0, Bit 3	Input/Output
24	P20	Port 2, Bit 0	Input/Output
25	P21	Port 2, Bit 1	Input/Output
26	P22	Port 2, Bit 2	Input/Output
27	P33	Port 2, Bit 3	Input/Output
28	P24	Port 2, Bit 4	Input/Output

Figure 5. 28-Pin DIP/SOIC Pin Configuration—ICSP Mode

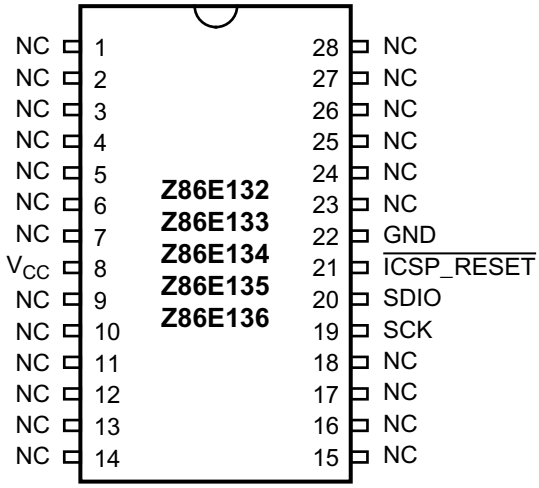


Table 5. 28-Pin DIP/SOIC Pin Identification—ICSP Mode

Pin #	Symbol	Function	Direction
1	NC	No Connection	
2	NC	No Connection	
3	NC	No Connection	
4	NC	No Connection	
5	NC	No Connection	
6	NC	No Connection	
7	NC	No Connection	
8	V_{CC}	Power Supply	
9	NC	No Connection	
10	NC	No Connection	
11	NC	No Connection	
12	NC	No Connection	
13	NC	No Connection	
14	NC	No Connection	
15	NC	No Connection	
16	NC	No Connection	
17	NC	No Connection	

Table 5. 28-Pin DIP/SOIC Pin Identification—ICSP Mode (Continued)

Pin #	Symbol	Function	Direction
18	NC	No Connection	
19	$\overline{\text{SCK}}$	Serial ICSP Clock	Input
20	$\overline{\text{SDIO}}$	Serial Data	Input/Output
21	$\overline{\text{ICSP\_RESET}}$	ICSP Reset	Input
22	GND	Ground	
23	NC	No Connection	
24	NC	No Connection	
25	NC	No Connection	
26	NC	No Connection	
27	NC	No Connection	
28	NC	No Connection	

Figure 6. 40-Pin DIP/SOIC Pin Configuration

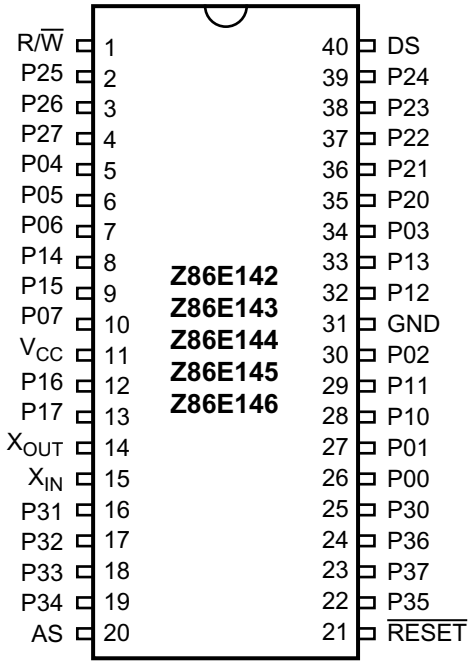


Table 6. 40-Pin DIP/SOIC Pin Identification

Pin #	Symbol	Function	Direction
1	R/$\overline{W}$	READ/WRITE	Output
2	P25	Port 2, Bit 5	Input/Output
3	P26	Port 2, Bit 6	Input/Output
4	P27	Port 2, Bit 7	Input/Output
5	P04	Port 0, Bit 4	Input/Output
6	P05	Port 0, Bit 5	Input/Output
7	P06	Port 0, Bit 6	Input/Output
8	P14	Port 1, Bit 4	Input/Output
9	P15	Port 1, Bit 5	Input/Output
10	P07	Port 0, Bit 7	Input/Output
11	V_{CC}	Power Supply	
12	P16	Port 1, Bit 6	Input/Output
13	P17	Port 1, Bit 7	Input/Output

Table 6. 40-Pin DIP/SOIC Pin Identification (Continued)

Pin #	Symbol	Function	Direction
14	X_{OUT}	Crystal Oscillator	Output
15	X_{IN}	Crystal Oscillator	Input
16	P31	Port 3, Bit 1	Input
17	P32	Port 3, Bit 2	Input
18	P33	Port 3, Bit 3	Input
19	P34	Port 3, Bit 4	Output
20	$\overline{AS}$	Address Strobe	Output
21	$\overline{RESET}$	Reset	Input
22	P35	Port 3, Bit 5	Output
23	P37	Port 3, Bit 7	Output
24	P36	Port 3, Bit 6	Output
25	P30	Port 3, Bit 0	Input
26	P00	Port 0, Bit 0	Input/Output
27	P01	Port 0, Bit 1	Input/Output
28	P10	Port 1, Bit 0	Input/Output
29	P11	Port 1, Bit 1	Input/Output
30	P02	Port 0, Bit 2	Input/Output
31	GND	Ground	
32	P12	Port 1, Bit 2	Input/Output
33	P13	Port 1, Bit 3	Input/Output
34	P03	Port 0, Bit 3	Input/Output
35	P20	Port 2, Bit 0	Input/Output
36	P21	Port 2, Bit 1	Input/Output
37	P22	Port 2, Bit 2	Input/Output
38	P23	Port 2, Bit 3	Input/Output
39	P24	Port 2, Bit 4	Input/Output
40	$\overline{DS}$	Data Strobe	Output

Figure 7. 40-Pin DIP/SOIC Pin Configuration—ICSP Mode

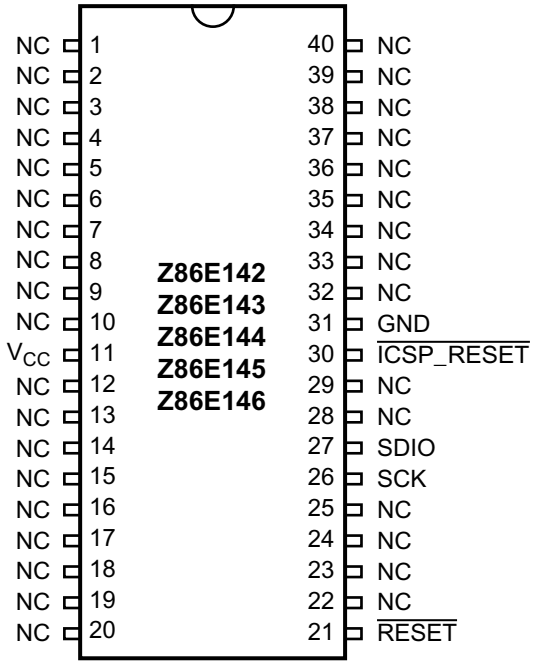


Table 7. 40-Pin DIP/SOIC Pin Identification—ICSP Mode

Pin #	Symbol	Function	Direction
1	NC	No connection	
2	NC	No connection	
3	NC	No connection	
4	NC	No connection	
5	NC	No connection	
6	NC	No connection	
7	NC	No connection	
8	NC	No connection	
9	NC	No connection	
10	NC	No connection	
11	V_{CC}	Power Supply	
12	NC	No connection	
13	NC	No connection	

Table 7. 40-Pin DIP/SOIC Pin Identification—ICSP Mode (Continued)

Pin #	Symbol	Function	Direction
14	NC	No connection	
15	NC	No connection	
16	NC	No connection	
17	NC	No connection	
18	NC	No connection	
19	NC	No connection	
20	NC	No connection	
21	$\overline{\text{RESET}}$	Reset	Input
22	NC	No connection	
23	NC	No connection	
24	NC	No connection	
25	NC	No connection	
26	$\overline{\text{SCK}}$	Serial ICSP Clock	Input
27	$\overline{\text{SDIO}}$	Serial Data	Input/Output
28	NC	No Connection	
29	NC	No Connection	
30	$\overline{\text{ICSP\_RESET}}$	ICSP Reset	Input
31	GND	Ground	
32	NC	No Connection	
33	NC	No Connection	
34	NC	No Connection	
35	NC	No Connection	
36	NC	No Connection	
37	NC	No Connection	
38	NC	No Connection	
39	NC	No Connection	
40	NC	No Connection	

Figure 8. 44-Pin PQFP Pin Configuration

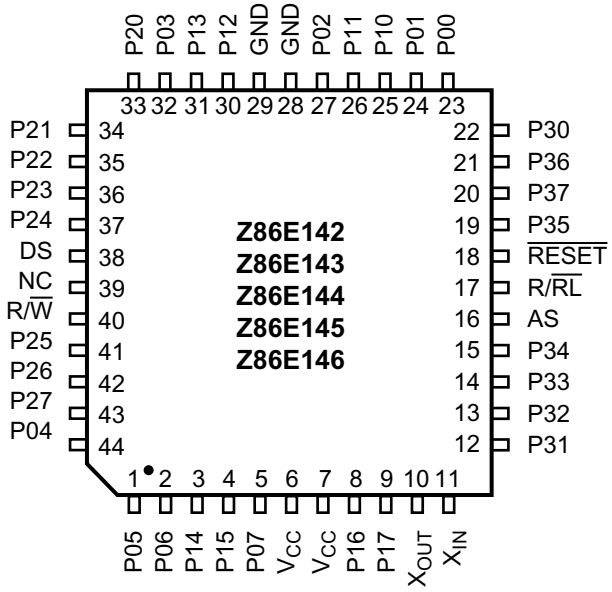


Table 8. 44-Pin PQFP Pin Identification

Pin #	Symbol	Function	Direction
1	P05	Port 0, Bit 5	Input/Output
2	P06	Port 0, Bit 5	Input/Output
3	P14	Port 1, Bit 4	Input/Output
4	P15	Port 1, Bit 5	Input/Output
5	P07	Port 0, Bit 7	Input/Output
6	V_{CC}	Power Supply	
7	V_{CC}	Power Supply	
8	P16	Port 1 Bit 6	Input/Output
9	P17	Port 1 Bit 7	Input/Output
10	X_{OUT}	Crystal Oscillator	Output
11	X_{IN}	Crystal Oscillator	Input
12	P31	Port 3, Bit 1	Input
13	P32	Port 3, Bit 2	Input
14	P33	Port 3, Bit 3	Input

Table 8. 44-Pin PQFP Pin Identification (Continued)

Pin #	Symbol	Function	Direction
15	P34	Port 3, Bit 4	Output
16	$\overline{AS}$	Address Strobe	Output
17	R/$\overline{RL}$	ROM/ROMless Control	Input
18	$\overline{RESET}$	Reset	Input
19	P35	Port 3, Bit 5	Output
20	P37	Port 3, Bit 7	Output
21	P36	Port 3, Bit 6	Output
22	P30	Port 3, Bit 0	Input
23	P00	Port 0, Bit 0	Input/Output
24	P01	Port 0, Bit 0	Input/Output
25	P10	Port 1, Bit 0	Input/Output
26	P11	Port 1, Bit 1	Input/Output
27	P02	Port 0, Bit 2	Input/Output
28	GND	Ground	
29	GND	Ground	
30	P12	Port 1, Bit 2	Input/Output
31	P13	Port 1, Bit 3	Input/Output
32	P03	Port 0, Bit 3	Input/Output
33	P20	Port 2, Bit 0	Input/Output
34	P21	Port 2, Bit 1	Input/Output
35	P22	Port 2, Bit 2	Input/Output
36	P23	Port 2, Bit 3	Input/Output
37	P24	Port 2, Bit 4	Input/Output
38	$\overline{DS}$	Data Strobe	Output
39	NC	Not Connected	
40	R/$\overline{W}$	READ/WRITE	Output
41	P25	Port 2, Bit 5	Input/Output
42	P26	Port 2, Bit 6	Input/Output
43	P27	Port 2, Bit 7	Input/Output
44	P04	Port 0, Bit 4	Input/Output

Figure 9. 44-Pin PQFP Pin Configuration—ICSP Mode

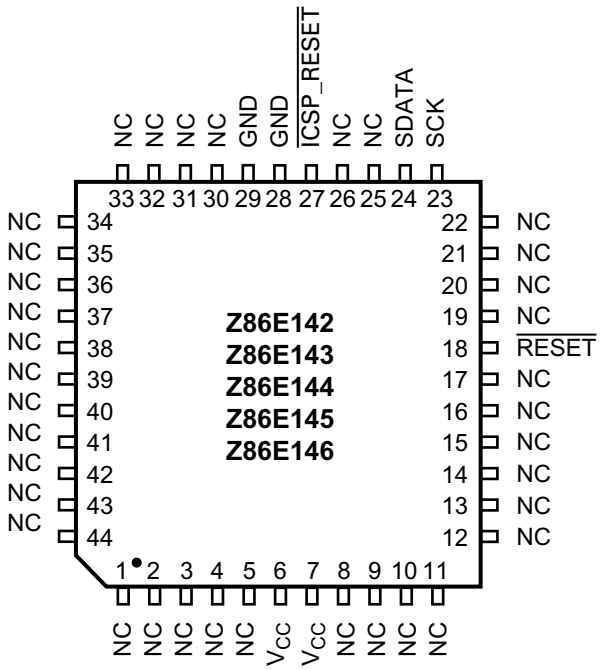


Table 9. 44-Pin PQFP Pin Identification—ICSP Mode

Pin #	Symbol	Function	Direction
1	NC	No Connection	
2	NC	No Connection	
3	NC	No Connection	
4	NC	No Connection	
5	NC	No Connection	
6	V_{CC}	Power Supply	
7	V_{CC}	Power Supply	
8	NC	No Connection	
9	NC	No Connection	
10	NC	No Connection	
11	NC	No Connection	
12	NC	No Connection	
13	NC	No Connection	

Table 9. 44-Pin PQFP Pin Identification—ICSP Mode (Continued)

Pin #	Symbol	Function	Direction
14	NC	No Connection	
15	NC	No Connection	
16	NC	No Connection	
17	NC	No Connection	
18	$\overline{\text{RESET}}$	Reset	Input
19	NC	No Connection	
20	NC	No Connection	
21	NC	No Connection	
22	NC	No Connection	
23	SCK	Serial Clock	Input
24	SDIO	Serial Data	Input/Output
25	NC	No Connection	
26	NC	No Connection	
27	$\overline{\text{ICSP\_RESET}}$	Programming Mode	Input
28	GND	Ground	
29	GND	Ground	
30	NC	No Connection	
31	NC	No Connection	
32	NC	No Connection	
33	NC	No Connection	
34	NC	No Connection	
35	NC	No Connection	
36	NC	No Connection	
37	NC	No Connection	
38	NC	No Connection	
39	NC	No Connection	
40	NC	No Connection	
41	NC	No Connection	

Table 9. 44-Pin PQFP Pin Identification—ICSP Mode (Continued)

Pin #	Symbol	Function	Direction
42	NC	No Connection	
43	NC	No Connection	
44	NC	No Connection	

Pin Functions

The following pages describe the function of each available MUZE family pin.

R/$\overline{RL}$ (input). The ROM/ROMless pin, when connected to GND, disables the internal ROM and forces the device to function as a ROMless Z8. (Available for devices in the 44-pin PQFP package only.)

Notes: When left unconnected or pulled High to V_{CC}, the device functions normally as a Z8 ROM version. When using the device in ROM mode in a high-EMI (noisy) environment, the ROMless pins must be connected directly to V_{CC}.

$\overline{DS}$ (output, active Low). The Data Strobe is activated one time for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of $\overline{DS}$. For WRITE operations, the falling edge of $\overline{DS}$ indicates that output data is valid. (Not available for devices in the 28-pin package.)

$\overline{AS}$ (output, active Low). The Address Strobe is pulsed one time at the beginning of each machine cycle for external memory transfer. Address output is from Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of $\overline{AS}$. Under program control, $\overline{AS}$ is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and READ/WRITE. (Not available for devices in the 28-pin package.)

X_{IN} Crystal Input. This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network, or an external single-phase clock to the on-chip oscillator input.

X_{OUT} Crystal Output. This pin connects a parallel-resonant crystal, ceramic resonant, LC, or RC network to the on-chip oscillator output.

R/$\overline{W}$ (output, WRITE Low). The READ/WRITE signal is High when the Z8 reads from external program or data memory. The signal is Low when the Z8 writes to external data memory. (Not available for devices in the 28-pin package.)

Port 0 (P00–P07). Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port (P03–P00 input/output and P07–P04 input/output), or as an address port for interfacing external memory. The input buffers are Schmitt-triggered and nibble-programmed as outputs and can be globally programmed as either push-pull or open-drain. Low-EMI output buffers are globally programmed by the software. Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control $\overline{DAV0}$ and RDY0. Handshake signal direction is dictated by the I/O direction (input or output) of Port 0 of the upper nibble P04–P07. The lower nibble must indicate the same direction as the upper nibble.

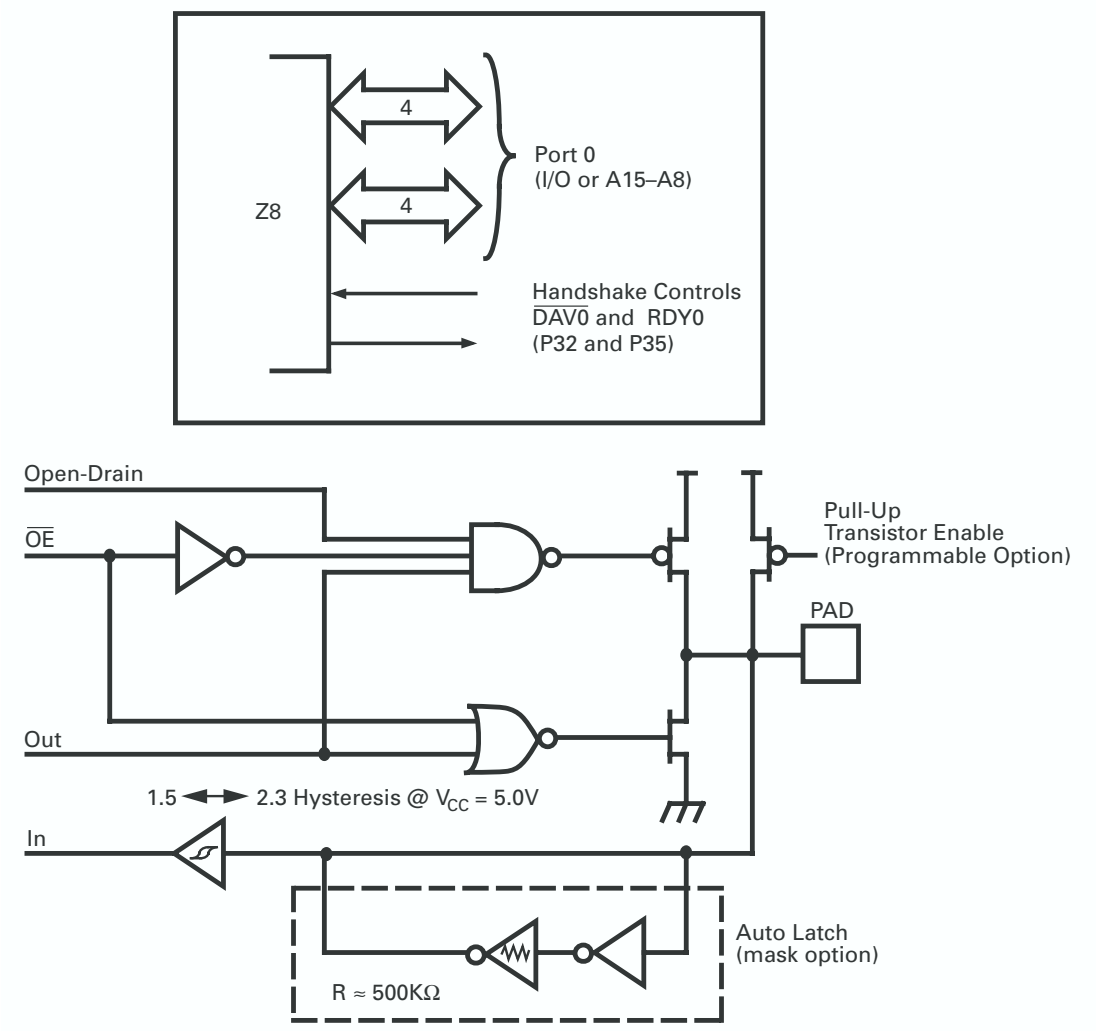
For external memory references, Port 0 provides address bits A11–A8 (lower nibble) and A15–A8 (lower and upper nibble) depending on the required address

space. If the address range requires 12 bits or less, the upper nibble of Port 0 is programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are required for I/O operation, they are configured by writing to the Port 0 mode register.

In ROMless mode, after a hardware RESET, Port 0 is configured as address lines A15–A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode. (In ROM mode, Port 0 is defined as input after RESET.)

Port 0 can be placed in a high-impedance state along with Port 1, $\overline{AS}$, $\overline{DS}$ and R/$\overline{W}$, allowing the Z8 to share common resources in multiprocessor and DMA applications (Figure 10).

Figure 10. Port 0 Configuration



Port 1 (P17–P10). Port 1 is an 8-bit, bidirectional, CMOS- compatible port (Figure 11), with multiplexed Address (A7–A0) and Data (D7–D0) ports. These 8 I/O lines are programmed as inputs or outputs, or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt-triggered and byte-programmed as outputs and can be globally programmed as either push-pull or open-drain. Low-EMI output buffers are globally programmed by the software.

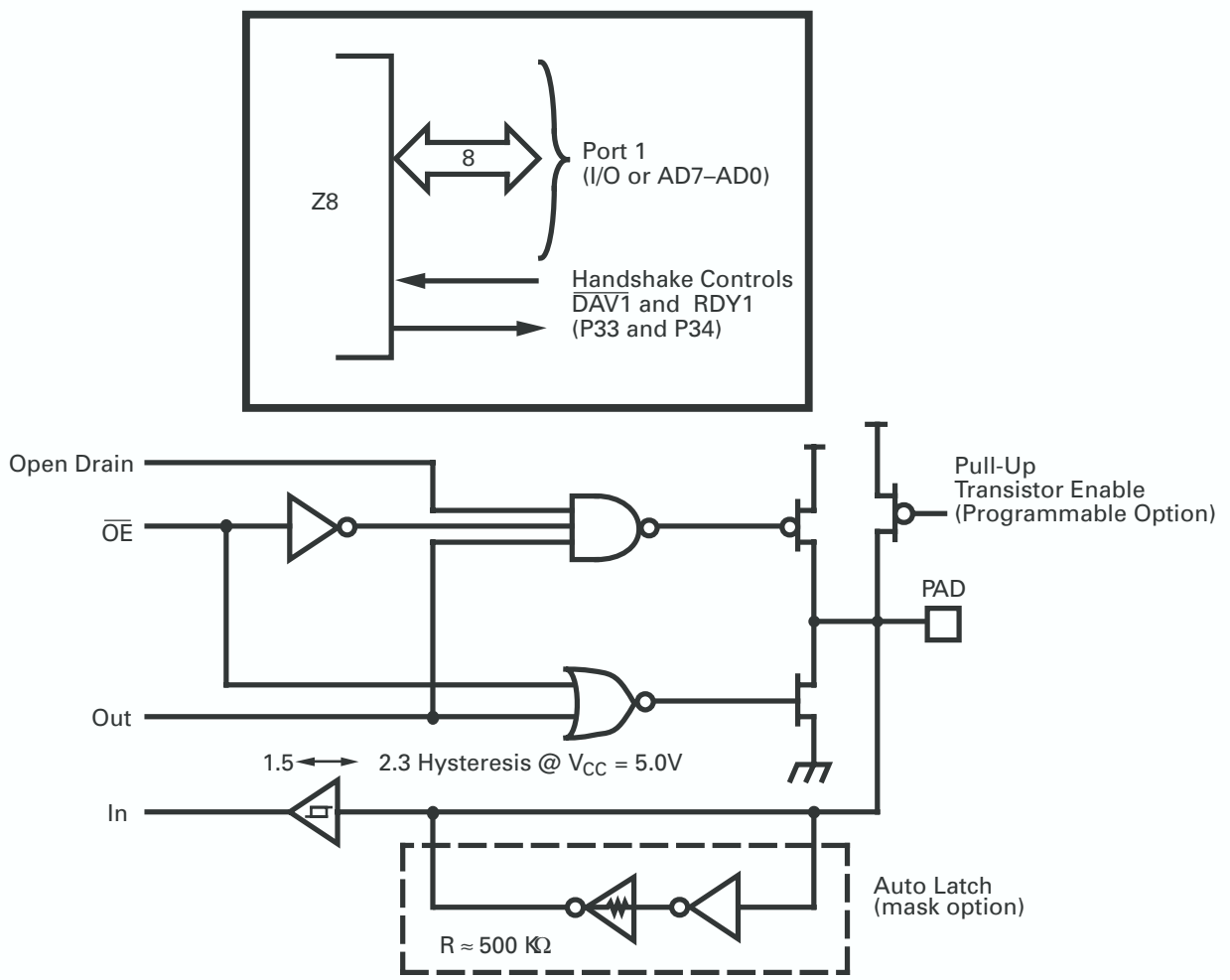
Note: Port 1 is not available on the devices in the 28-pin package, and P01M Register must set bit D4,D3 as 00. Low-EMI mode is not supported on the emulator for Port1. PCON register D4 must be 1.

Port 1 may be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls RDY1 and $\overline{\text{DAV1}}$ (Ready and Data Available).

Memory locations greater than the internal ROM address are referenced through Port 1, except for the Z86E146 (due to its 64 KB of internal memory). To interface external memory, Port 1 must be programmed for multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0, $\overline{\text{AS}}$, $\overline{\text{DS}}$, and R/$\overline{\text{W}}$, allowing the Z8 to share common resources in multiprocessor and DMA applications.

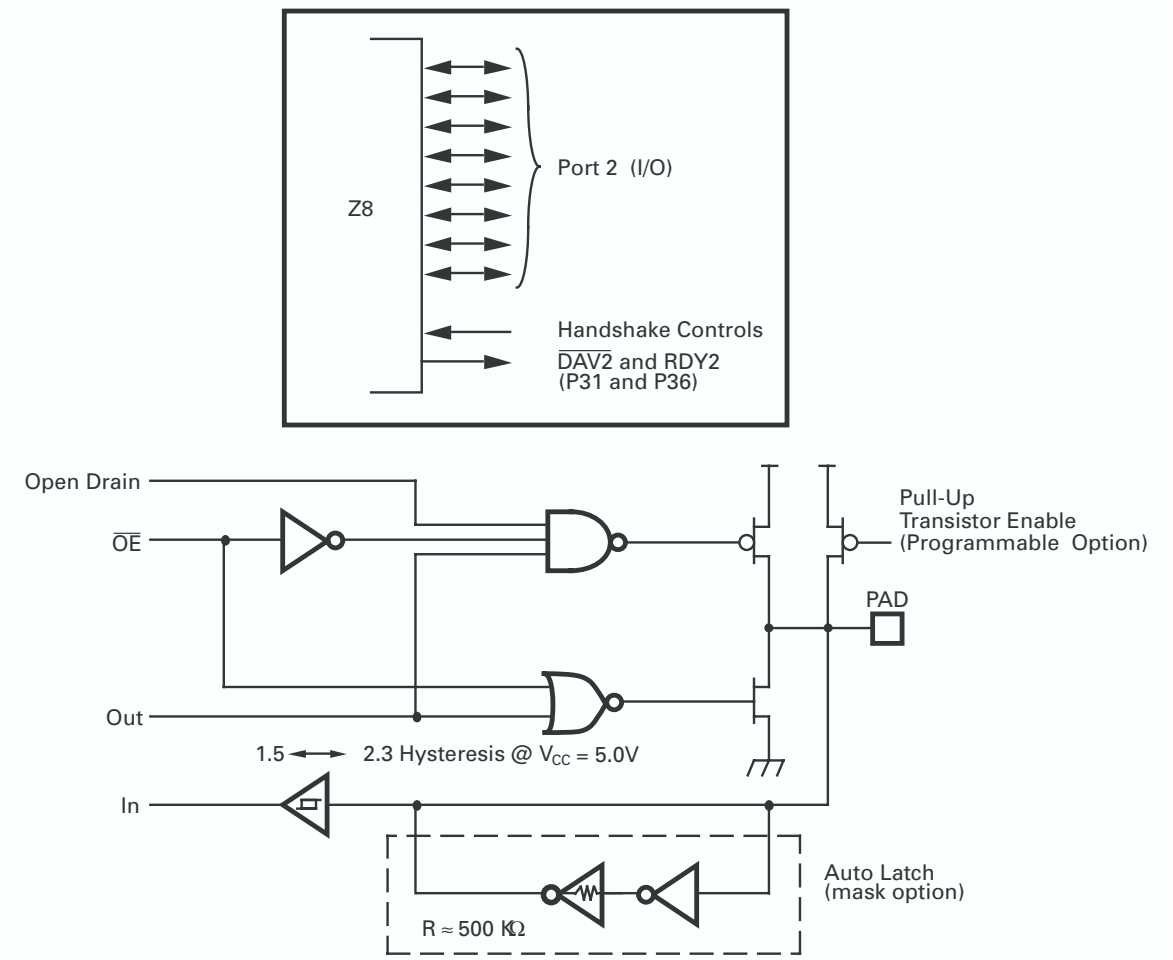
Figure 11. Port 1 Configuration



Port 2 (P27–P20). Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines are configured under software control as an input or output, independently. Port 2 is always available for I/O operation. The input buffers are Schmitt-triggered. Bits programmed as outputs may be globally programmed as either push-pull or open-drain. Low-EMI output buffers are globally programmed by the software.

Port 2 may be placed under handshake control. In HANDSHAKE mode, Port 3 lines P31 and P36 are used as the handshake control lines DAV2 and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to bit 7, Port 2 (Figure 12).

Figure 12. Port 2 Configuration



Port 3 (P37–P30). Port 3 is an 8-bit, CMOS-compatible port, with four fixed inputs (P33–P30) and four fixed outputs (P34–P37). Port 3 is configured under software control for Input/Output, Counter/Timers, interrupt, UART, port handshake, and Data Memory functions. Port 3, bit 0 input is Schmitt-triggered, and pins P31, P32, and P33 are standard CMOS inputs (no autolatches). Pins P34, P35, P36, P37 are push-pull output lines. Low-EMI output buffers are globally programmed by the software.

Two onboard comparators process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming Port 3 Mode Register (P3M bit 1). For interrupt functions, Port 3, bit 0 and pin 3 are falling-edge interrupt inputs. P31 and P32 are programmable as rising, falling, or both edge-triggered interrupts (IRQ register bits 6 and 7). P33 is the comparator reference voltage input when in Analog mode. Access to Counter/Timer 1 is made

through P31 (T_{IN}) and P36 (T_{OUT}). Handshake lines for Ports 0, 1, and 2 are available on P31 through P36.

Port 3 also provides the following control functions: handshake for Ports 0, 1, and 2 ($\overline{DAV}$ and RDY); four external interrupt request signals (IRQ3–IRQ0); timer input and output signals (T_{IN} and T_{OUT}); Data Memory Select ($\overline{DM}$, see Table 10 and Figure 13).

P34 output is software-programmed to function as a Data Memory Select ($\overline{DM}$). The Port 3 Mode Register (P3M) bit D3,D4 selects this function. When accessing external data memory, P34 goes active Low; when accessing external program memory, P34 goes High.

An onboard UART (ASCI) is enabled by software by setting the RE and TE bits of the ASCI Control Register A (CNTLA). When enabled, P30 is the receive input and P37 is the transmit output.

Table 10. Port 3 Pin Assignments

Pin	I/O	Control Timer	Analog	Interrupt	P0 HS	P1 HS	P2 HS	Ext	UART
P30	IN			IRQ3					RX
P31	IN	T_{IN}	AN1	IRQ2			D/R		
P32	IN		AN2	IRQ0	D/R				
P33	IN		REF	IRQ1		D/R			
P34	OUT		AN1–OUT			R/D		DM	
P35	OUT				R/D				
P36	OUT	T_{OUT}					R/D		
P37	OUT		AN2–OUT						TX

Notes:
HS = Handshake Signals
D = $\overline{DAV}$
R = RDY

Comparator Inputs and Outputs. Port 3, pins P31 and P32 each feature a comparator front end. The comparator reference voltage, pin P33, is common to both comparators. In ANALOG mode, the P31 and P32 are the positive inputs to the comparators, and P33 is the reference voltage supplied to both comparators. In DIGITAL mode, pin P33 is used as a P33 register input or IRQ1 source. P34 and P37 can provide the comparator output directly by software-programming the PCON register bit D0 to 1 (see Figure 14).

Note: The user must add a two-NOP delay after setting the P3M bit D1 to 1 before the comparator output is valid. IRQ0, IRQ1, and IRQ2 must be cleared in the IRQ register when the comparator is enabled or disabled.

Figure 13. Port 3 Configuration

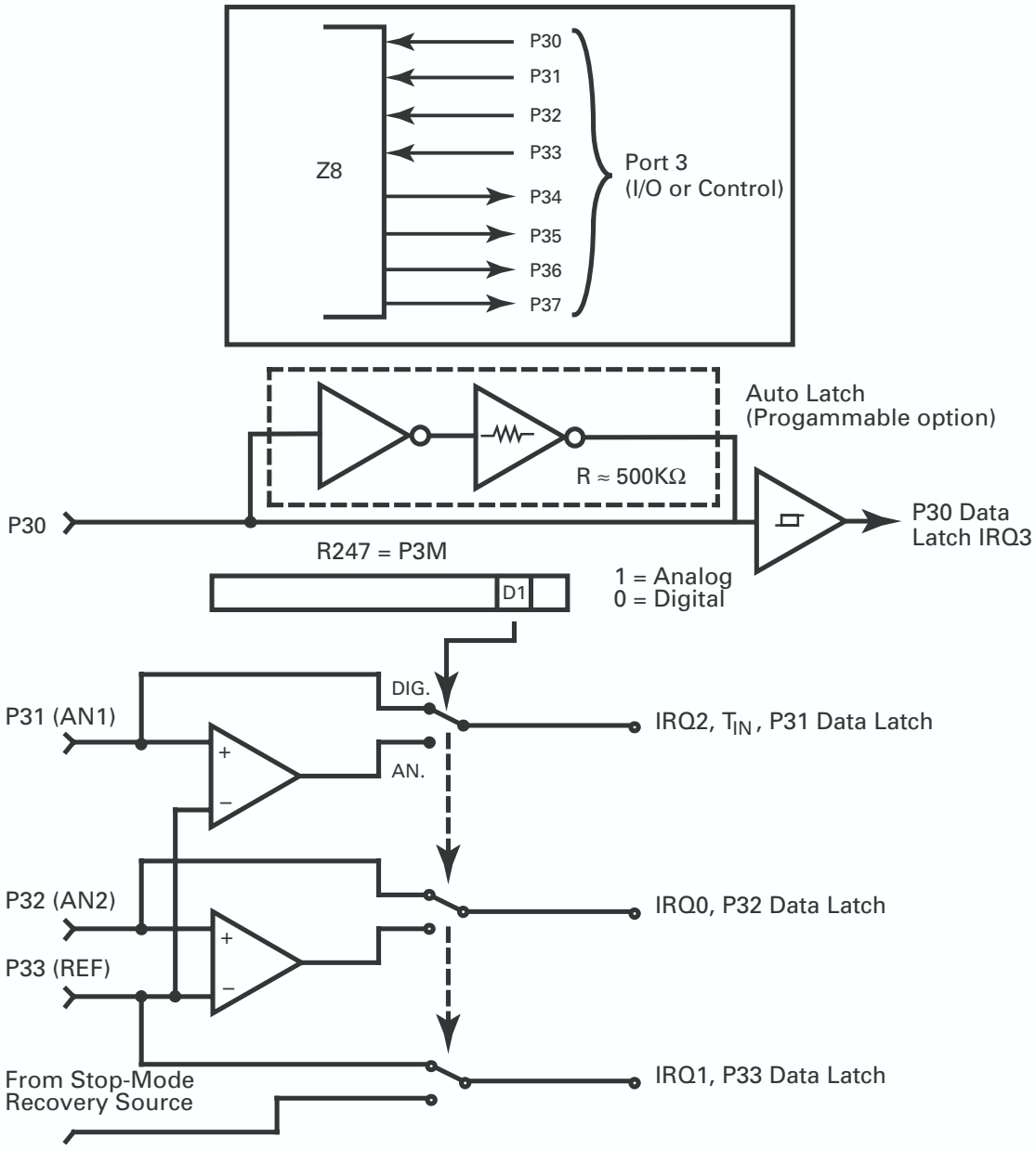
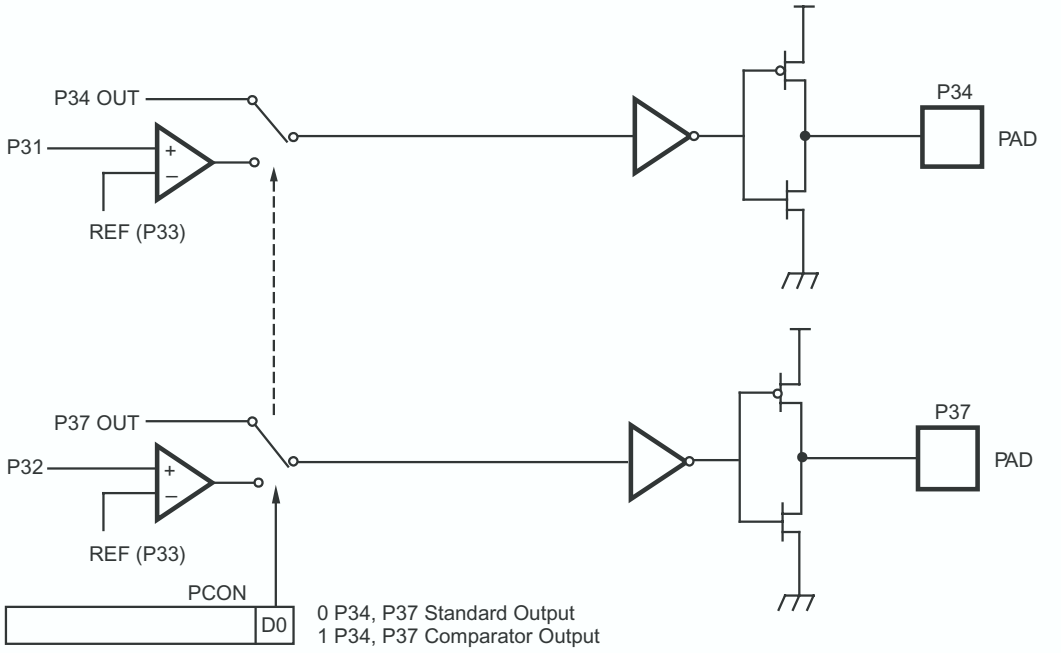


Figure 14. Port 3 Configuration—PCON Register Detail



Autolatch. The autolatch places valid CMOS levels on all CMOS inputs (except P33–P31) that are not externally driven. Whether this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. Autolatches are available on Port 0, Port 1, Port 2, and P30. There are no autolatches on P31, P32, and P33.

Note: Deletion of all port autolatches is available as an option when the device is programmed. The AUTOLATCH DISABLE option is selected by the customer when the device is programmed.

$\overline{\text{RESET}}$ (input/output, active Low). Initializes the MCU. $\overline{\text{RESET}}$ occurs through Power-On Reset, Watch-Dog Timer reset, Stop-Mode Recovery, or external reset. During Power-On Reset and Watch-Dog Reset, the internally-generated reset drives the $\overline{\text{RESET}}$ pin Low for the POR time. Pull-up is provided internally.

Caution: Any devices driving the reset line must be open-drain to avoid damage from a possible conflict during reset conditions. $\overline{\text{RESET}}$ depends on oscillator operation to achieve full reset conditions, except for conditions wherein the reset is caused by a WDT time-out.

Note: The $\overline{\text{RESET}}$ pin is not available on devices in the 28-pin package.

After the POR time, $\overline{\text{RESET}}$ is a Schmitt-triggered input. During the RESET cycle, $\overline{\text{DS}}$ is held active Low while $\overline{\text{AS}}$ cycles at a rate of $T_PC \div 2$. Program execution begins at location 000Ch, after the $\overline{\text{RESET}}$ is released. For Power-On Reset, the reset output time is T_{POR} ms.

When program execution begins, $\overline{\text{AS}}$ and $\overline{\text{DS}}$ toggles only for external memory accesses. The Z8 does not reset WDTMR, SMR, P2M, PCON, and P3M registers on a Stop-Mode Recovery operation or from a WDT reset out of STOP mode.

Functional Description

The Z8 MCU incorporates the following functions that enhance the standard Z8® architecture and provide the user with increased design flexibility:

- Reset
- Program Memory
- Data Memory
- EPROM Protect
- RAM Protect
- Working Register File
- Expanded Register File
- General-Purpose Registers
- Stack Pointer
- Counter/Timers
- Interrupts
- Clock
- Power-On Reset
- HALT and STOP Modes
- Port Configuration Register
- Comparator
- Stop-Mode Recovery
- Watch-Dog Timer
- Voltage Comparator

$\overline{\text{RESET}}$. The device is reset in one of the following conditions:

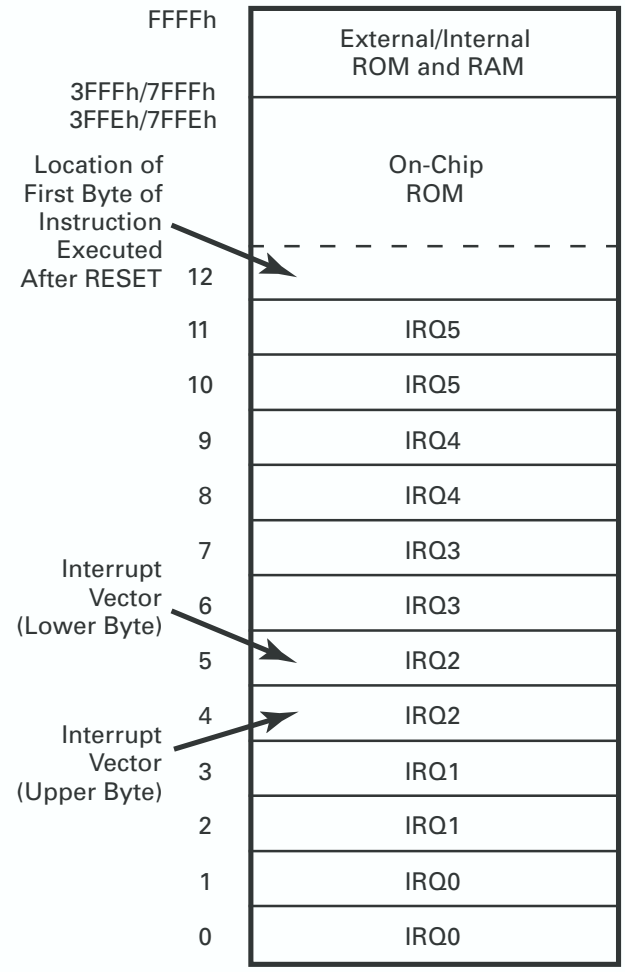
- Power-On Reset
- Watch-Dog Timer
- Stop-Mode Recovery Source
- External Reset
- Low Voltage Recovery

Automatic Power-On Reset circuitry is built into the Z8, eliminating the requirement for an external reset circuit to reset upon power-up. The internal pull-up resistor is on the $\overline{\text{RESET}}$ pin, so a pull-up resistor is not required; however, in a high-EMI (noisy) environment, it is recommended that a low-value pull-up resistor be used.

Note: The $\overline{\text{RESET}}$ pin is not available on devices in the 28-pin package.

Program Memory. The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For ROM mode, address 12 to address FFFFh (E136/E146)/7FFFh (E135/E145)/3FFF (E134/E144) consists of programmable EPROM. The Z86E142/E143/E144/E145 can access external program and data memory from addresses 4000h/8000h to FFFFh. See Figure 15.

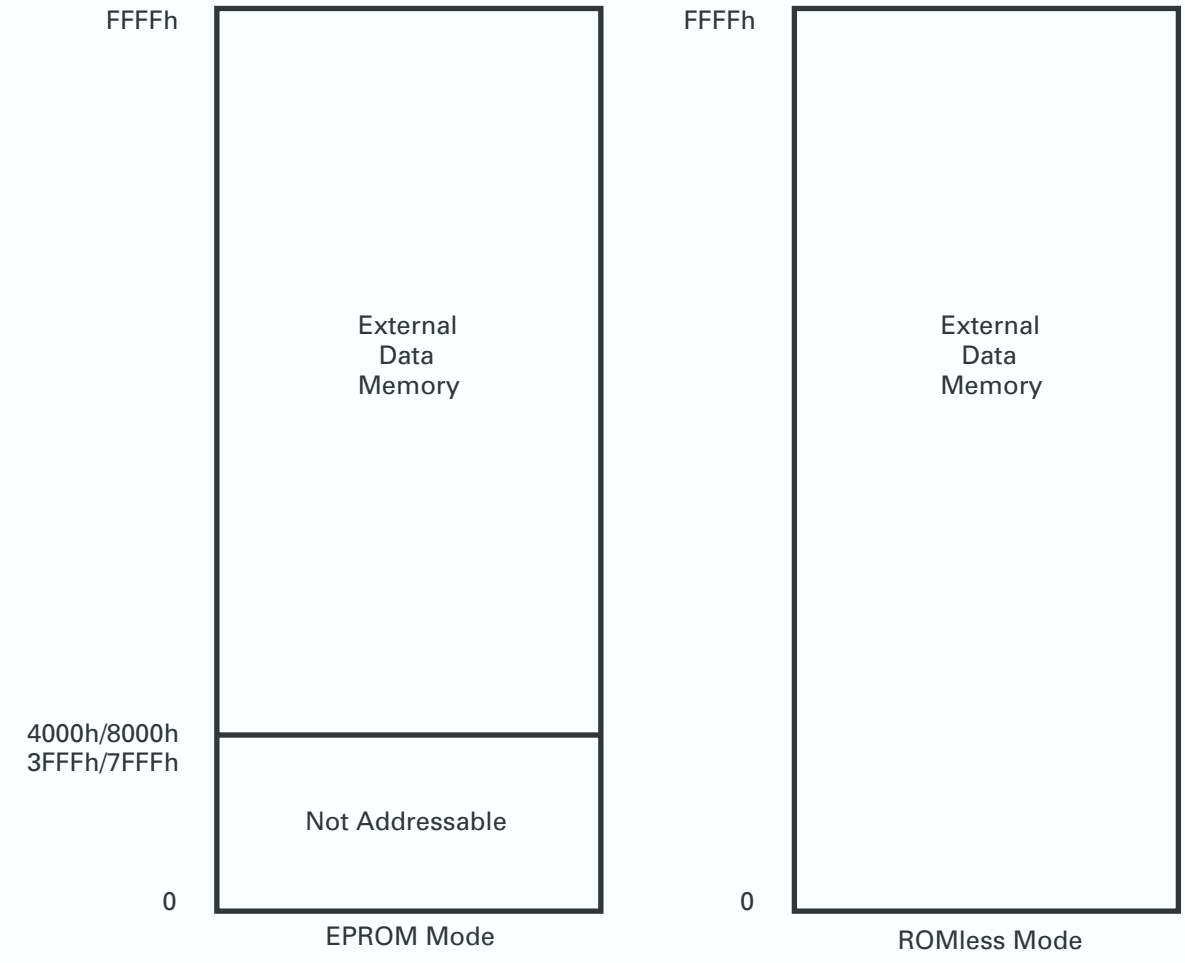
Figure 15. Program Memory Map for the MUZE Family



Data Memory ($\overline{DM}$). The ROMless version addresses up to 64 KB of external data memory. External data memory may be included with, or separated from, the external program memory space. $\overline{DM}$, an optional I/O function that is programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 16). The state of the $\overline{DM}$ signal is controlled by the type of instruction being executed. An LDC Op Code references PROGRAM ($\overline{DM}$ inactive) memory, and an LDE instruction references data ($\overline{DM}$ active Low) memory. The user must configure Port 3 Mode Register (P3M) bits D3 and D4 for this mode. This feature is not usable for devices in 28-pin package.

Note: When used in ROM mode, the Z86E146 cannot access any external data or program memory. The Z86E14X series of Z8 MCUs can access external program and data memory from addresses 4000h/8000h to FFFFh.

Figure 16. Data Memory Map



EPROM Protect. EPROM PROTECT provides an additional security function. When the device is programmed with the EPROM PROTECT option bit selected, and it is executing out of External Program Memory, instructions LDC, LDCI, LDE, and LDEI cannot read Internal Program Memory.

When the EPROM PROTECT option bit is selected, and executing out of Internal Program Memory, instructions LDC, LDCI, LDE, and LDEI can read Internal Program Memory.

RAM Protect. The upper portion of the RAM's address spaces 80h to EFh (excluding the control registers) can be protected from writing. The RAM Protect option bit can be selected when the device is programmed. After the mask option is selected, the user activates this feature from the internal ROM code to turn off/on the RAM Protect by loading either a 0 or a 1 into the IMR register, bit D6. A 1 in bit D6 enables the RAM Protect option.

Working Register File. The Z8 standard register file contains 4 I/O port registers, 236 general-purpose registers, and 15 control and status registers. Expanded register file Fh contains 3 system-configuration registers. Expanded register file Ah contains 8 ASCI control registers. The working registers are accessed directly or indirectly via an 8-bit address field. As a result, a short 4-bit register address can use the Register Pointer (Table 11 and Figure 17). In the 4-bit mode, the working register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

Throughout this document, the Z8 Standard Register File is referred to as a Bank.

Table 11. Register Pointer Register—RP FDh/R253 Bank 0h: READ/WRITE

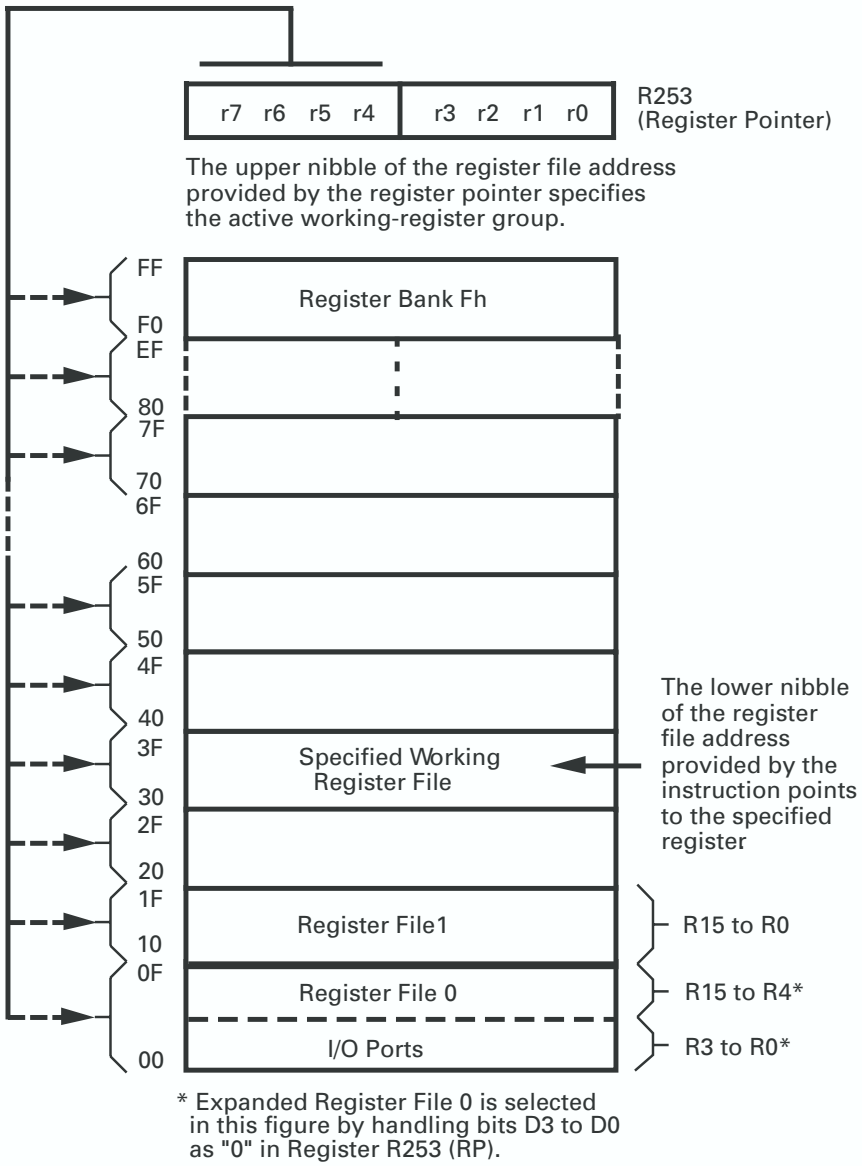
Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Note: R = Read, W = Write, X = Indeterminate.								

Bit Position	Bit Field	R/W	State	Description
D7–D4	Working Registers	R/W	0	Working Register Group Pointer
D3–D0	ERF	R/W	0	Expanded Register File

Expanded Register File (ERF). The Z8 register file is expanded to allow for additional system control registers, and for mapping of additional peripheral devices, along with the I/O ports, into the register address area. The Z8 register address space R0 through R15 is implemented as 16 groups of 16 registers per bank (Fig-

ures 17 and 18). These register groups are known as the Expanded Register File (ERF). Bits 7–4 of register RP select the Working Register Group. Bits 3–0 of register RP select the Expanded Register File. Five system configuration registers reside in the Expanded Register File at Bank Fh—PCON, VFY, SMR, SMR2, and WDTMR. The 8 control registers for the ASCI are located in the Expanded Register File Bank Ah. The remainder of the Expanded Register is not physically implemented, and is open for future expansion.

Figure 17. Register Pointer—Detail



General-Purpose Registers (GPR). General-purpose registers are undefined after the device is powered up. These registers keep the most recent value after any RESET, as long as the RESET occurs in the V_{CC} voltage-specified operating range. General-purpose registers are not guaranteed to keep their most recent state from a Low-Voltage Protection (V_{LV}) RESET if V_{CC} drops below 1.8V.

Note: Register Bank E0–EF is only accessed via working register and indirect addressing modes.

Stack Pointer. The Z8 internal register file is used for the stack. The 16-bit Stack Pointer (SPH and SPL) is used for the external stack, which can reside anywhere in the data memory for ROMless mode. An 8-bit Stack Pointer (SPL) is used for the internal stack that resides within the 236 general-purpose registers. Stack Pointer High (SPH) is used as a general-purpose register only when using an internal stack. The devices in the 28-pin and 40-pin packages can only use the 8-bit stack pointer (SPL) for the internal stack.

Note: SPH and SPL are set to 00h after any RESET or Stop-Mode Recovery.

Counter/Timers. There are two 8-bit programmable counter/timers (T0–T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 19).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 2to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that is loaded into the counter. When the counter reaches the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters are programmed to START, STOP, restart to CONTINUE, or restart from the initial value. The counters can also be programmed to STOP upon reaching 0 (SINGLE-PASS mode) or to automatically reload the initial value and continue counting (MODULO–N CONTINUOUS mode).

The counters, *but not the prescalers*, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divide-by-four, or an external signal input through Port 3. The Timer Mode Register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or nonretriggerable, or as a gate input for the internal clock. The counter/timers are cascaded by connecting the T0 output to the input of T1. T_{IN} mode is enabled by setting PRE1 bit D1 to 0.

Figure 18. Expanded Register File Architecture

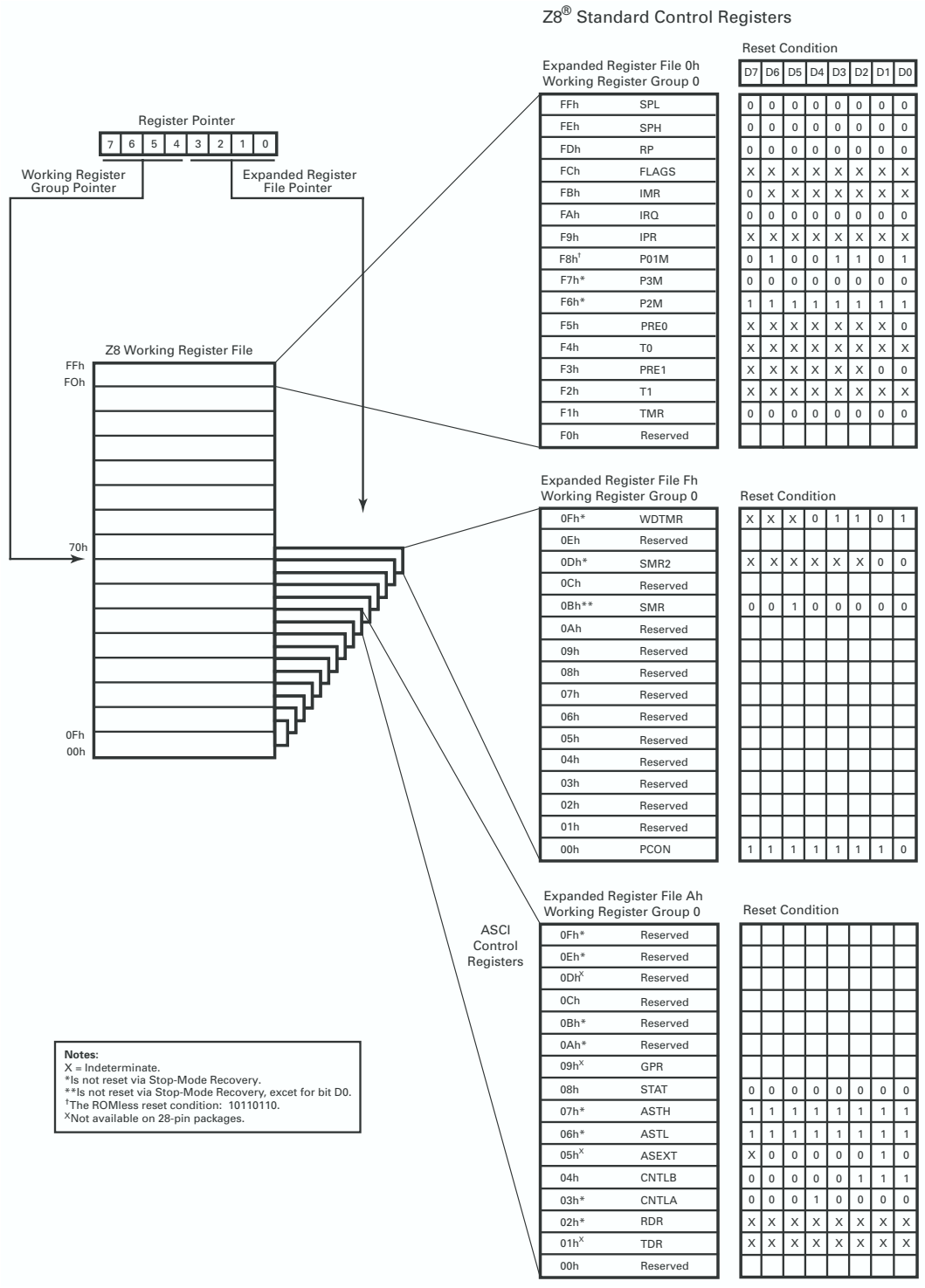
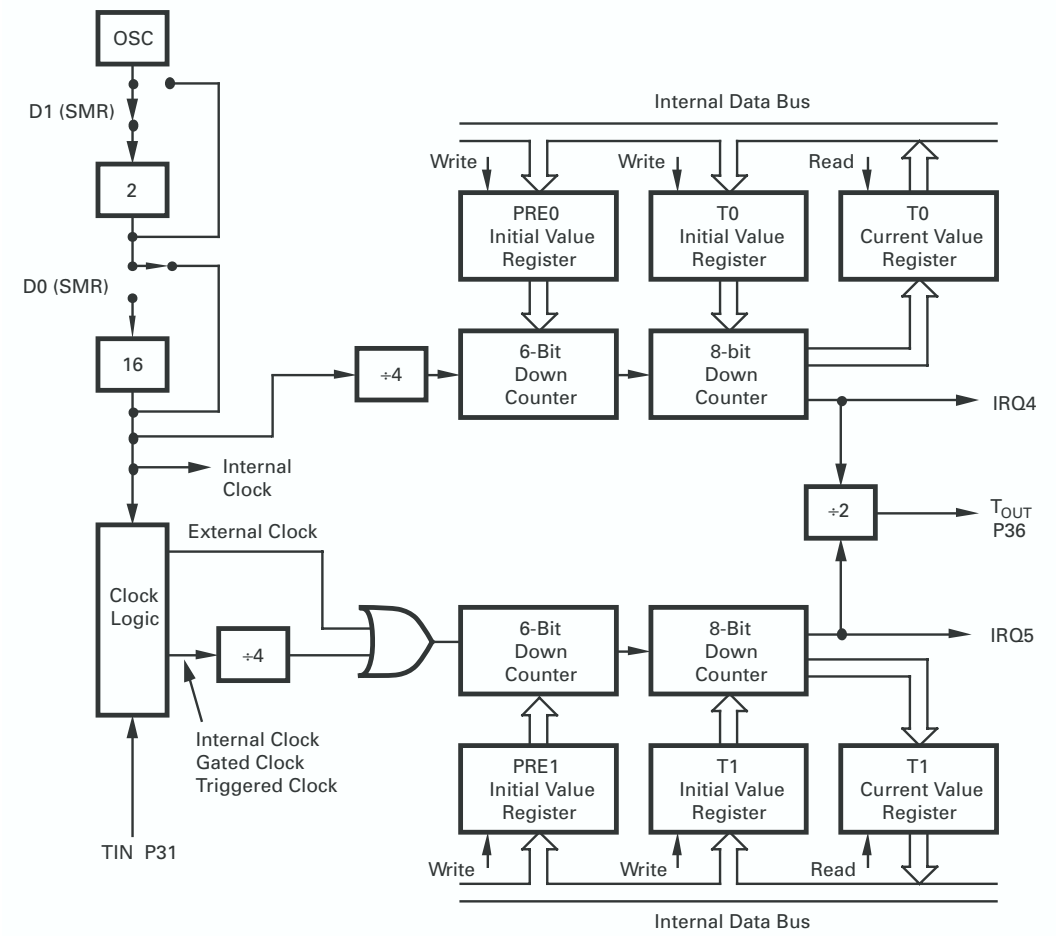


Figure 19. Counter/Timer Block Diagram



Interrupts. The Z8 features six different interrupts from six different sources. These interrupts are maskable and prioritized (Figure 24). The 6 sources are divided as follows: 4 sources are claimed by Port 3 lines P33–P30, and 2 are claimed by counter/timers (Table 12). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests.

Table 12. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	$\overline{DAV0}$, IRQ0	0,1	External (P32), Rising and Falling Edges Triggered
IRQ1,	IRQ1	2,3	External (P33), Falling Edge Triggered
IRQ2	$\overline{DAV2}$, IRQ2, T_{IN}	4,5	External (P31), Rising and Falling Edges Triggered

Table 12. Interrupt Types, Sources, and Vectors (Continued)

Name	Source	Vector Location	Comments
IRQ3	UART (ASCI)	6,7	External (P30), Falling Edge Triggered
IRQ4	T0	8,9	Internal
IRQ5	T1	10,11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle activates when an interrupt request is granted. This action disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt.

All Z8 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests require service.

When in ANALOG mode, an interrupt resulting from COMPARATOR1 maps to IRQ2, and an interrupt from COMPARATOR2 maps to IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge-triggered, and are programmed in the IRQ register. The software polls to identify the state of the pin. When in ANALOG mode, IRQ1 is generated by the Stop-Mode Recovery source selected by SMR Register bits D4, D3, D2, or SMR2 D1 or D0.

Programming bits for the Interrupt Edge Select are located in the IRQ register, bits D7 and D6. The configuration is indicated in Table 13.

Table 13. IRQ Register*

IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

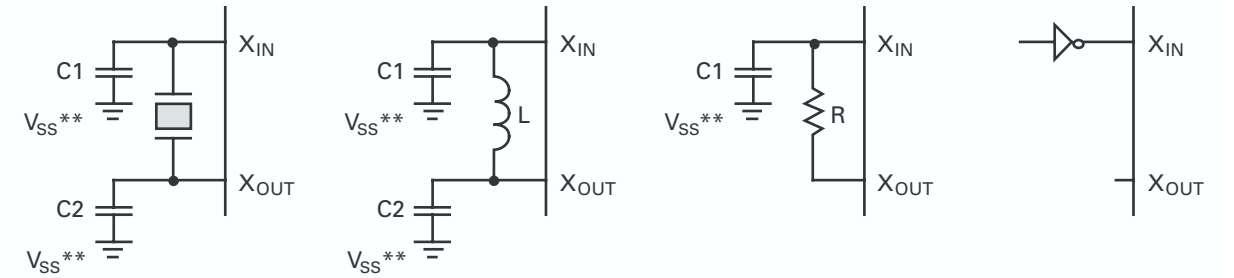
Notes:
F = Falling Edge
R = Rising Edge

Clock. The Z8 on-chip oscillator features a high-gain, parallel-resonant amplifier for connection to a crystal, LC, RC, ceramic resonator, or any suitable external clock source (X_{IN} = INPUT, X_{OUT} = OUTPUT). The crystal should be AT-cut, 16 MHz maximum, with a series resistance (RS) of less than or equal to 100 Ω when oscillating from 1 MHz to 16 MHz.

The crystal should be connected across X_{IN} and X_{OUT} using the vendor's recommended capacitor values from each pin directly to the device Ground pin to reduce ground-noise injection into the oscillator. The RC oscillator option can be selected when the device is programmed.

Note: The RC option is available up to 8 MHz. The RC oscillator configuration must be an external resistor connected from X_{IN} to X_{OUT}, with a frequency-setting capacitor from X_{IN} to Ground (Figure 20).
For better noise immunity, the capacitors should be tied directly to the device Ground pin (V_{SS}).

Figure 20. Oscillator Configuration



*Preliminary value, including pin parasitics.
**Device ground pin.

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power fail to Power OK status.
2. Stop-Mode Recovery (if D5 of SMR = 1).
3. WDT time-out.

The POR time is specified as TPOR. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock, RC/LC oscillators).

HALT. HALT turns off the internal CPU clock, but not the CRYSTAL oscillation. The counter/timers, UART, and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts and are either externally or internally generated. An interrupt request must be enabled and executed to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. Therefore, the user must execute a NOP (Op Code = FFh) immediately before the appropriate sleep instruction. For example:

```
FF    NOP    ; clear the pipeline
6F    STOP   ; enter STOP mode
```

or

```
FF    NOP    ; clear the pipeline
7F    HALT   ; enter HALT mode
```

STOP. This instruction turns off the internal clock and external crystal oscillation. The STOP instruction also reduces the standby current to 10 µA or less. STOP mode is terminated by a RESET only, either by WDT time-out, POR, Stop-Mode Recovery, or external reset. As a result, the processor restarts the application program at address 000Ch. A WDT time-out in STOP mode affects all registers the same as if a Stop-Mode Recovery occurred via a selected Stop-Mode Recovery source except that the POR delay is enabled even if the delay is selected for disable.

Note: If a permanent WDT is selected, the WDT runs in all modes and cannot be stopped or disabled if the onboard RC oscillator is selected to drive the WDT.

Port Configuration Register (PCON). The PCON register configures the ports individually; comparator output on Port 3, open-drain on Port 0 and Port 1, low EMI on Ports 0, 1, 2, and 3, and low-EMI oscillator. The PCON register is located in the expanded register file at Bank F, location 00h (Table 14).

Table 14. Port Configuration Register—PCON 00h/R0 Bank Fh: WRITE ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset	1	1	1	1	1	1	1	0
Note: R = Read, W = Write, X = Indeterminate.								

Bit Position	Bit Field	R/W	State	Description
D7	Oscillator	W	1	**Low-EMI Oscillator** 0: Low EMI 1: Standard
D6	Port 3 I/O	W	1	**Port 3** 0: Low EMI 1: Standard
D5	Port 2 I/O	W	1	**Port 2** 0: Low EMI 1: Standard
D4	Port 1 I/O	W	1	**Port 1** 0: Low EMI 1: Standard
D3	Port 0 I/O	W	1	**Port 0*** 0: Low EMI 1: Standard
D2	Port 0 I/O	W	1	**Port 0** 0: Open-Drain 1: Push-Pull Active
D1	Port 1 I/O	W	1	**Port 1*** 0: Open-Drain 1: Push-Pull Active
D0	Port 3	W	0	**Port 3 Comparator Output** 0: P34, P37 Standard Output 1: P34, P37 Comparator Output
Note: Must be set to 1 for devices in 28-pin packages.				

Comparator

Comparator Output Port 3 (D0). Bit 0 controls the comparator use in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration. The default value is 0.

Port 1 Open-Drain (D1). Port 1 is configured as an open-drain by resetting this bit (D1 = 0) or configured as push-pull active by setting this bit (D1 = 1). The default value is 1. The user must set D1 = 1 for devices in 28-pin packages.

Port 0 Open-Drain (D2). Port 0 is configured as an open-drain by resetting this bit (D2 = 0) or configured as push-pull active by setting this bit (D2 = 1). The default value is 1.

Low-EMI Port 0 (D3). Port 0 is configured as a low-EMI port by resetting this bit (D3 = 0) or configured as a Standard Port by setting this bit (D3 = 1). The default value is 1.

Low-EMI Port 1 (D4). Port 1 is configured as a low-EMI port by resetting this bit (D4 = 0) or configured as a Standard Port by setting this bit (D4 = 1). The default value is 1. The user must set D4 = 1 for devices in 28-pin packages.

Note: For emulator, this bit must be set to 1.

Low-EMI Port 2 (D5). Port 2 is configured as a low-EMI port by resetting this bit (D5 = 0) or configured as a Standard Port by setting this bit (D5 = 1). The default value is 1.

Low-EMI Port 3 (D6). Port 3 is configured as a low-EMI port by resetting this bit (D6 = 0) or configured as a Standard Port by setting this bit (D6 = 1). The default value is 1.

Low-EMI OSC (D7). This bit of the PCON register controls the low-EMI noise oscillator. A 1 in this location configures the oscillator, $\overline{DS}$, $\overline{AS}$ and R/$\overline{W}$ with standard drive, while a 0 configures the oscillator, $\overline{DS}$, $\overline{AS}$ and R/$\overline{W}$ with low noise drive. LOW-EMI mode reduces the drive of the oscillator (OSC). The default value is 1.

Note: Maximum external clock frequency of 4 MHz when running in LOW-EMI OSCILLATOR mode.

Low-EMI Emission. The Z8 is programmed to operate in a low-EMI emission mode in the PCON register. The oscillator and all I/O ports is programmed as LOW-EMI EMISSION mode independently. Use of this feature results in:

- The pre-drivers slew rate reduced to 10 ns (typical)
- Low-EMI output drivers exhibit resistance of 200Ω (typical)
- Low-EMI Oscillator
- Internal SCLK = CRYSTAL operation limited to a maximum of 4 MHz–250 ns cycle time, when LOW EMI OSCILLATOR is selected and system clock (SMR Register Bit D1 = 1)

Stop-Mode Recovery

Stop-Mode Recovery Registers (SMR1 and SMR2). These registers select the clock divide value and determine the mode of Stop-Mode Recovery (Tables 15 and 18). All bits are WRITE ONLY, except bit 7 of SMR1, which is READ ONLY. SMR1 bit 7 is a flag bit that is set by hardware on a Stop-Mode Recovery condition and

reset by a power-on cycle. For SMR1, bit 6 controls whether a Low level or a High level is required from the recovery source. Bit 5 controls the reset delay after Stop-Mode Recovery. Bits 2, 3, and 4 of the SMR1 register specify the source of the Stop-Mode Recovery signal. Bits 0 and 1 determine the time-out period of the WDT. The SMR registers are located in Bank F of the Expanded Register File at addresses 0Bh and 0Dh, respectively.

For SMR2, bits 7 to 2 are reserved. Bits 1 and 0 of the SMR2 register specify the source of the Stop-Mode Recovery signal.

Table 15. Stop-Mode Recovery Register 1—SMR1 0Bh/R11 Bank Fh: WRITE ONLY, except Bit D7, which is READ ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	W	W	W	W	W	W	W
Reset	0	0	1	0	0	0	0	0
Note: R = Read, W = Write, X = Indeterminate.								

Bit Position	Bit Field	R/W	State	Description
D7	STP	R	0	**Stop Flag** 0: POR 1: Stop-Mode Recovery
D6	SMR	W	0	**Stop-Mode Recovery Level** 0: Low 1: High
D5	STPDLY	W	1	**Stop Delay** 0: Off 1: On
D0	CLK	W	0	**SCLK ÷ TCLK Divide-by-16** 0: Off[1] 1: On

Notes:
1. Do not use in conjunction with SMR2 Source.
2. Cleared by $\overline{\text{RESET}}$ and SMR.

D4–D2	SMRSRC	W	000	**Stop-Mode Recovery Source2** 000: POR only and/or external $\overline{\text{RESET}}$ 001: P30 010: P31 011: P32 100: P33 101: P27 110: P2 NOR 0–3 111: P2 NOR 0–7
D1	EXTCLK	W	0	**External Clock Divide-by-2** 0: SCLK ÷ TCLK = Crystal ÷ 2 1: SCLK = Crystal
D0	CLK	W	0	**SCLK ÷ TCLK Divide-by-16** 0: Off[1] 1: On

Notes:
1. Do not use in conjunction with SMR2 Source.
2. Cleared by $\overline{\text{RESET}}$ and SMR.

SCLK ÷ TCLK Divide-by-16 Select (D0). Bit D0 of the SMR controls a divide-by-16 prescaler of SCLK ÷ TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic). This bit is reset to D0 = 0 after a Stop-Mode Recovery.

External Clock Divide-by-Two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, the system clock (SCLK) and timer clock (TCLK) are equal to the external clock frequency divided by 2. The SCLK is equal to the external clock frequency when this bit is set (D1 = 1). Using this bit together with D7 of PCON further helps lower EMI (that is, D7 (PCON) = 0, D1 (SMR) = 1). The default setting is 0. Maximum external clock frequency is 4 MHz when SMR bit D1 = 1 where SCLK ÷ TCLK = Crystal.

Stop-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR specify the wake-up source of the Stop-Mode Recovery (Figure 21 and Table 16). When the Stop-Mode Recovery Sources are selected in this register, then SMR2 register bits D0,D1 must be set to 0.

Note: If the Port 2 pin is configured as an output, this output level is read by the SMR circuitry.

Figure 21. Stop-Mode Recovery Source

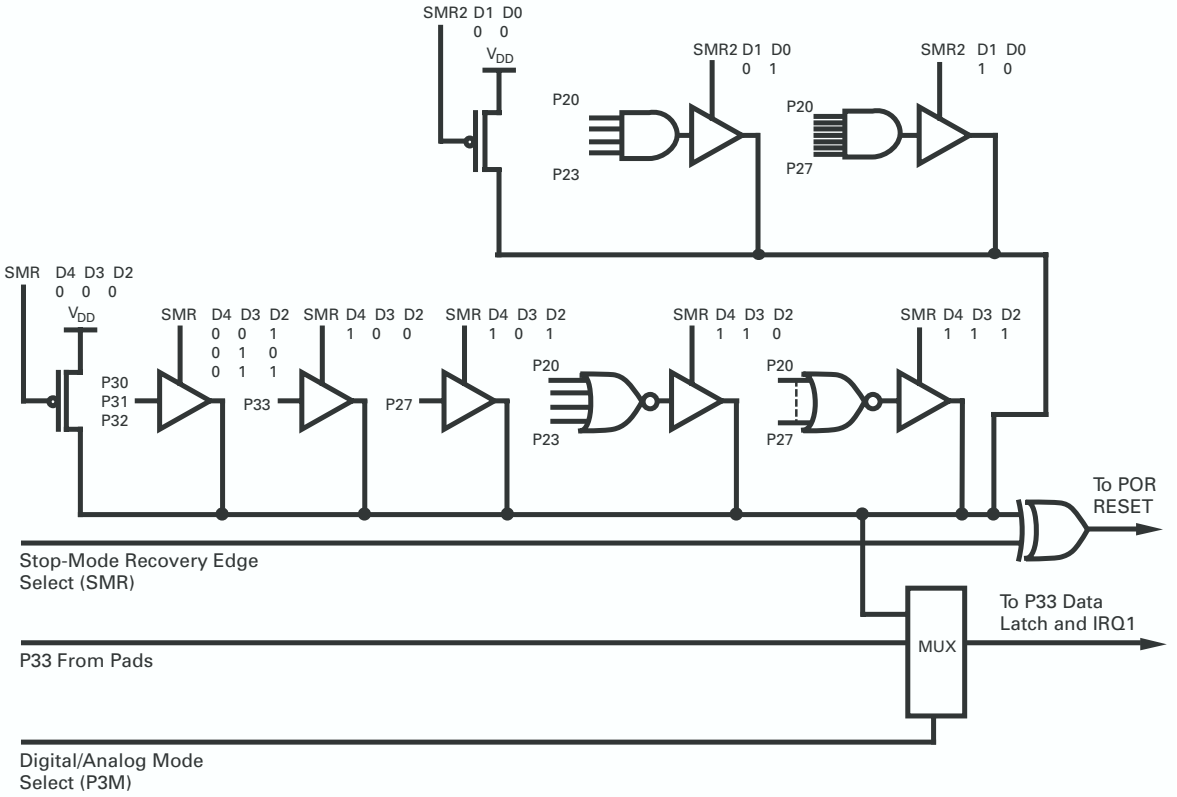


Table 16. Stop-Mode Recovery Source

SMR[4–2]			
D4	**D3**	**D2**	**Operation/Description of Action**
0	0	0	POR and/or external reset recovery
0	0	1	P30 transition
0	1	0	P31 transition (not in ANALOG mode)
0	1	1	P32 transition (not in ANALOG mode)
1	0	0	P33 transition (not in ANALOG mode)
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

Stop-Mode Recovery Delay Select (D5). This bit, if High, enables the T_{POR} $\overline{\text{RESET}}$ delay after Stop-Mode Recovery. The default configuration of this bit is 1. If the *fast* wake up is selected, the Stop-Mode Recovery source must be kept active for at least 5 T_PC. Code execution begins after T_{EDELAY} (see Tables 58 and 59).

Stop-Mode Recovery Edge Select (D6). A 1 in this bit position indicates that a high level on any one of the recovery sources wakes the Z8 from STOP mode. A 0 indicates low-level recovery. The default is 0 on POR (Table 17). This bit is used for either SMR or SMR2.

Cold or Warm Start (D7). This bit is set by the device upon entering STOP mode. A 0 in this bit (cold) indicates that the device resets by POR/WDT RESET. A 1 in this bit (warm) indicates that the device awakens by a Stop-Mode Recovery source.

Note: If the Port 2 pin is configured as an output, this output level is read by the SMR2 circuitry.

Stop-Mode Recovery Register 2 (SMR2). This register contains additional Stop-Mode Recovery sources. When the Stop-Mode Recovery sources are selected in this register then SMR register bits D2, D3, and D4 must be 0.

Table 17. Stop-Mode Recovery Register 2

SMR1–0		
D1	**D0**	**Operation/Description of Action**
0	0	POR and/or external reset recovery
0	1	Logical AND of P20 through P23
1	0	Logical AND of P20 through P27

Table 18. Stop-Mode Recovery Register 2—SMR2 0Dh/R13 Bank Fh: WRITE ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	X	X	X	0	0

Note: R = Read, W = Write, X = Indeterminate.

Bit/ Field	Bit Position	R/W	State	Description
D7–D2	Reserved	W	X	Reserved—must be 0
D1–D0	STOP Mode	W	00	**Stop-Mode Recovery Source 2*** 00: POR only 01: AND P20, P21, P22, P23 10: AND P20, P21, P22, P23, P24, P25, P26, P27

Note: *Do not use in conjunction with SMR Source.

Watch-Dog Timer

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an onboard RC oscillator or external oscillator from the X_{IN} pin. The POR clock source is selected with bit 4 of the WDT register (Table 19).

WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags. The WDTMR must be written to within the first 64 internal system clocks. After that, the WDTMR is WRITE-protected.

Note: WDT time-out while in STOP mode does not reset SMR, PCON, WDTMR, P2M, P3M, Ports 2 & 3 Data Registers, but the POR delay counter is still enabled even though the SMR stop delay is disabled.

Table 19. Watch-Dog Timer Mode Register—WDTMR 0Fh/R15: WRITE ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	0	1	1	0	1

Note: R = Read, W = Write, X = Indeterminate.

Bit/ Field	Bit Position	R/W	State	Description
D7–D5	Reserved	W	X	Reserved—must be 0
D4	X_{IN}	W	0	**XIN/INT RC Select for WDT** 0: On-Board RC 1: Crystal
D3	WDT	W	1	WDT During STOP
D2	WDT	W	1	WDT During HALT
D1–D0	WDT Tap	W	01	**WDT Tap — Int RC OSC — System Clock** 00: 3.5 ms — 128 SCLK 01: 10.0 ms — 256 SCLK 10: 14.0 ms — 512 SCLK 11: 56.0 ms — 2048 SCLK

Note: Not used in conjunction with SMR Source.

WDT Time Select (D0,D1). Selects the WDT time period and is configured as indicated in Table 20.

Table 20. WDT Time Select

D1	D0	Timeout of Internal RC OSC	Timeout of System Clock
0	0	3.5 ms min	128 SCLK
0	1	7 ms min	256 SCLK
1	0	14 ms min	512 SCLK
1	1	56 ms min	2048 SCLK

Note: SCLK = system bus clock cycle. The default on RESET is 7 ms. Values provided are for V_{CC} = 5.0V.

WDTMR During HALT (D2). This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1.

WDTMR During STOP (D3). This bit determines whether or not the WDT is active during STOP mode. Because the CRYSTAL clock is stopped during STOP mode, the on-board RC must be selected as the clock source to the POR counter. A 1 indicates active during STOP. The default is 1.

Note: If the permanent WDT programming option is selected, the WDT runs in all modes and cannot be stopped or disabled if the on board RC oscillator is selected as the clock source for WDT.

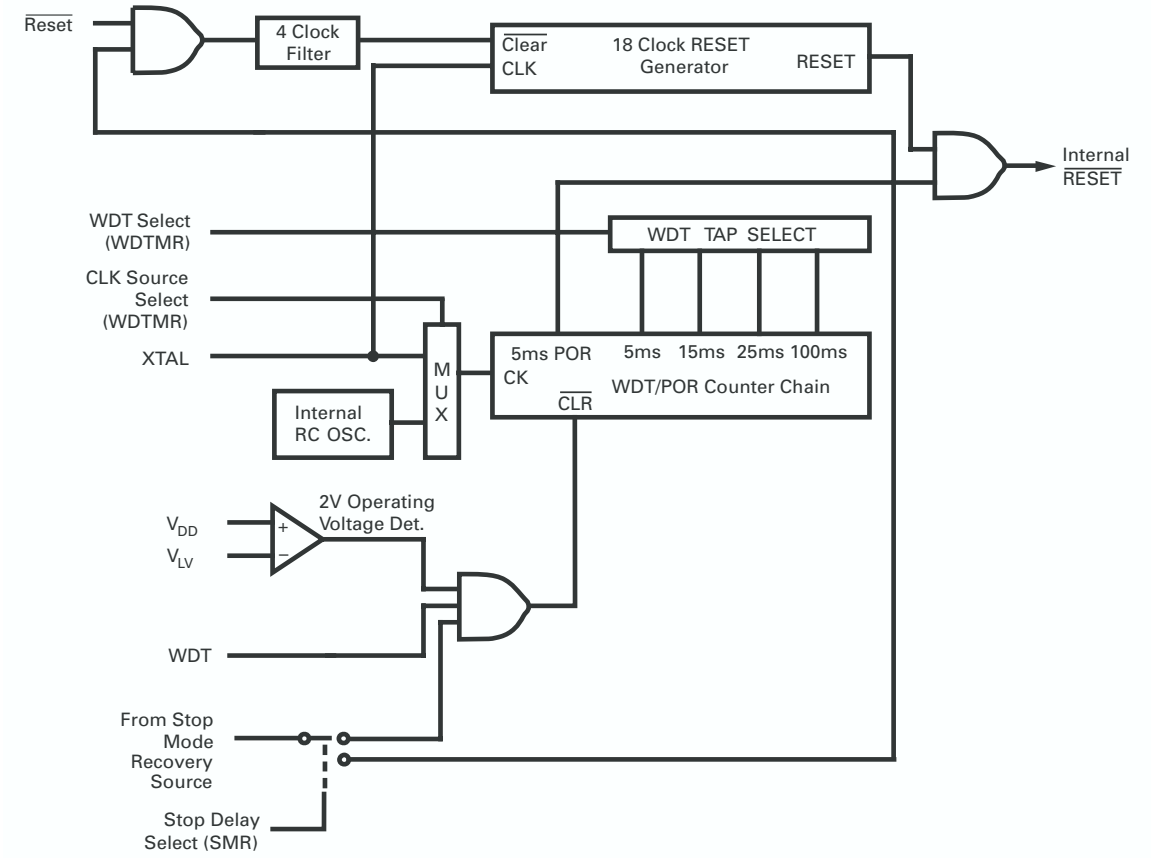
Clock Source for WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, X_{IN}. The default configuration of this bit is 0 which selects the internal RC oscillator.

WDTMR Register Accessibility. The WDTMR register is accessible only during the first 64 internal system clock cycles from the execution of the first instruction after Power-On Reset, Watch-Dog Reset, or Stop-Mode Recovery. After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank Fh of the Expanded Register File at address location 0Fh (Figure 22).

Note: The WDT is permanently enabled (automatically enabled after RESET) through a programmable option. The option is selected when the device is programmed. In this mode, WDT is always activated when the device comes out of RESET. Execution of the WDT instruction serves to refresh the WDT time-out period. WDT operation in the HALT and STOP modes is controlled by WDTMR programming. If this option is not selected when the

device is programmed, the WDT must be activated by the user through the WDT instruction and is always disabled by any reset to the device.

Figure 22. Resets and Watch-Dog Timer Example



Voltage Comparator

Low-Voltage Protection. An onboard Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. RESET is globally driven if V_{CC} is below the specified voltage (Low-Voltage Protection). The minimum operating voltage varies with the temperature and operating frequency, while the Low-Voltage Protection (V_{LV}) varies with temperature only.

The Low-Voltage Protection trip voltage (V_{LV}) is less than 3V and more than 1.4V under the following conditions.

The device functions normally at or above 4.5V under all conditions. Below 4.5V, the device functions normally until the Low-Voltage Protection trip point (V_{LV}) is reached, for the temperatures and operating frequencies in Case 1 and Case 2, in Table 21. The device is guaranteed to function normally at supply voltages above

the Low-Voltage Protection trip point. The actual Low-Voltage Protection trip point is a function of temperature and process parameters (Figure 23).

Figure 23. Typical Low-Voltage Protection vs. Temperature

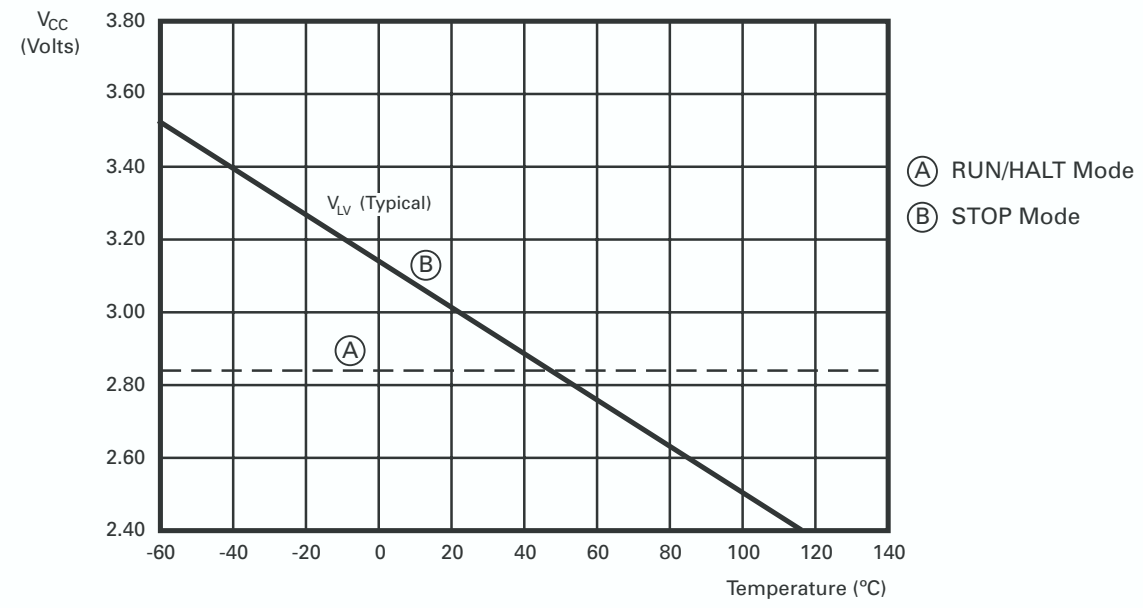


Table 21. Maximum (V_{LV}) Conditions:

Case 1:	T_A = –40ºC, +105ºC, Internal Clock Frequency equal or less than 4 MHz
Case 2:	T_A = –40ºC, +85ºC, Internal Clock Frequency equal or less than 6 MHz

Note: The internal clock frequency relationship to the CRYSTAL clock is dependent on SMR Bit 0 1 setting.

Control Registers

The MUZE family of Z8 parts offers 3 banks of registers, including eight ASCI registers in Bank Ah, as detailed in the following pages.

Expanded Register File, Bank 0h

Bank 0h of the Expanded Register File contains 15 registers that perform the Timer, Prescaler, Port, Interrupt, Flag, and Pointer functions, as shown in Tables 23 through 37. These 15 registers are not reset by a Stop-Mode Recovery. Table 22 lists the reset states of all 15 Bank 0h registers.

Table 22. Expanded Register File Registers—Reset States

		D7	D6	D5	D4	D3	D2	D1	D0
F0h	Reserved								
F1h	TMR*	0	0	0	0	0	0	0	0
F2h	T1*	X	X	X	X	X	X	X	X
F3h	PRE1*	X	X	X	X	X	X	0	0
F4h	T0*	X	X	X	X	X	X	X	X
F5h	PRE0*	X	X	X	X	X	X	X	0
F6h	P2M*	1	1	1	1	1	1	1	1
F7h	P3M*	0	0	0	0	0	0	0	0
F8h	P01M*	0	1	0	0	1	1	0	1
F9h	IPR*	X	X	X	X	X	X	X	X
FAh	IRQ*	0	0	0	0	0	0	0	0
FBh	IMR*	0	X	X	X	X	X	X	X
FCh	FLAGS*	X	X	X	X	X	X	X	X
FDh	RP*	0	0	0	0	0	0	0	0
FEh	SPH*	0	0	0	0	0	0	0	0
FFh	SPL*	0	0	0	0	0	0	0	0

Note: *Not reset with a Stop-Mode Recovery.

Timer Mode Register

The Timer Mode Register, TMR, controls timing and counter functions. READ/WRITE and reset states for bits D7–D0 are listed in Table 23.

Table 23. Timer Mode Register—TMR F1h/R241 Bank 0h: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset State	0	0	0	0	0	0	0	0
Note: R = Read, W = Write.								

Bit Position	Bit Field	R/W	State	Description
D7–D6	T_{OUT} Mode	R/W	00	**T_{OUT} Mode** 00: Off 01: T0 Output 10: T1 Output 11: Internal Clock Output
D5–D4	T_{IN} Mode	R/W	00	**T_{IN} Mode** 00: External Clock Input 01: Gate Input 10: Trigger Input (nonretriggerable) 11: Trigger Input (retriggerable)
D3	T1 Count	R/W	0	**T1 Count** 0: Disable 1: Enable
D2	T1	R/W	0	**T1** 0: No Function 1: Load T1
D1	T0 Count	R/W	0	**T0 Count** 0: Disable 1: Enable
D0	T0	R/W	0	**T0** 0: No Function 1: Load T0

Counter/Timer 1 Register

The Counter/Timer 1 Register, T1, controls timing and counter functions. READ/WRITE and reset states for bits D7–D0 are listed in Table 24.

Table 24. Counter/Timer 1 Register—T1 F2h/R242 Bank 0h: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset State	X	X	X	X	X	X	X	X
Note: R = Read, W = Write, X = Indeterminate.								

Bit Position	Bit Field	R/W	State	Description
D7–D0	T1	R	X	T1 Current Value
		W	X	T1 Automatic Reload Value Range = 1–256 decimal; 01h–00h

Prescaler 1 Register

The Prescaler 1 Register, PRE1, controls clocking functions. READ/WRITE and reset states for bits D7–D0 are listed in Table 25.

Table 25. Prescaler 1 Register—PRE1 F3h/R243 Bank 0h: WRITE ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset State	X	X	X	X	X	X	0	0
Note: W = Write, X = Indeterminate.								

Bit Position	Bit Field	R/W	State	Description
D7–D2	Prescaler	W	X	**Prescaler Modulo** Range = 1–64 decimal; 01h–00h
D1	Clock	W	0	**Clock Source** 0: T1 External Timing Input (T_{IN}) Mode 1: T1 Internal
D0	Count	W	0	**Count Mode** 0: T1 Single Pass 1: T1 Modulo N

Counter/Timer 0 Register

The Counter/Timer 0 Register, T0, controls timing and counter functions. READ/WRITE and reset states for bits D7–D0 are listed in Table 26.

Table 26. Counter/Timer 0 Register—T0 F4h/R244 Bank 0h: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset State	X	X	X	X	X	X	X	X
Note: R = Read, W = Write, X = Indeterminate.								

Bit Position	Bit Field	R/W	State	Description
D7–D0	T0	R	X	T0 Current Value
		W	X	T0 automatic Reload Value Range = 1–256 decimal

Prescaler 0 Register

The Prescaler 0 Register PRE0 controls clocking functions. WRITE and reset states for bits D7–D0 are listed in Table 27.

Table 27. Prescaler 0 Register—PRE0 F5h/R245 Bank 0h: WRITE ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset State	X	X	X	X	X	X	X	0
Note: W = Write, X = Indeterminate.								

Bit Position	Bit Field	R/W	State	Description
D7–D2	Prescaler	W	X	**Prescaler Modulo** Range = 1–64 decimal; 01h–00h
D1	Reserved	W	X	Reserved—must be 0
D0	Count	W	0	**Count Mode** 0: T0 Single Pass 1: T0 Modulo N

Port 2 Mode Register

The Port 2 Mode Register, P2M, controls Port 2 I/O functions. WRITE and reset states for bits D7–D0 are listed in Table 28.

Table 28. Port 2 Mode Register—P2M F6h/R246 Bank 0h: WRITE ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset State	1	1	1	1	1	1	1	1
Note: W = Write.								

Bit Position	Bit Field	R/W	State	Description
D7–D0	P20–P27	W	1	**P20–P27 I/O Definition** 0: Defines bit as Output 1: Defines bit as Input

Port 3 Mode Register

The Port 3 Mode Register P3M controls Port 3 I/O functions. WRITE and reset states for bits D7–D0 are listed in Table 29.

Table 29. Port 3 Mode Register—P3M F7h/R247 Bank 0h: WRITE ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset State	0	0	0	0	0	0	0	0
Note: W = Write.								

Bit Position	Bit Field	R/W	State	Description
D7–D6	Reserved	W	00	Reserved—must be 00
D5	Port 3	W	0	**Port 3** 0: P31 = Input (T_{IN}) P36 = Output (T_{OUT}) 1: P31 = $\overline{DAV2}$/RDY2 P36 = RDY2/$\overline{DAV2}$
D4–D3	Port 3	W	00	**Port 3** 00: P33 = Input; P34 = Output 01: P33 = Input; P34 = $\overline{DM}$ 10: P33 = Input; P34 = $\overline{DM}$ 11: P33 = $\overline{DAV1}$/RDY1; P34 = RDY1/$\overline{DAV1}$

Bit Position	Bit Field	R/W	State	Description
D2	Port 3	W	0	**Port 3** 0: P32 = Input; P35 = Output 1: P32 = $\overline{\text{DAV0}}$/$\overline{\text{RDY0}}$; P35 = RDY0/$\overline{\text{DAV0}}$
D1	Port 3	W	0	**Port 3** 0: P31, P32 DIGITAL mode 1: P31, P32 ANALOG mode
D0	Port 2	W	0	**Port 2** 0: Open-Drain 1: Push-Pull

Ports 0 and 1 Mode Register

The Ports 0 and 1 Mode Register, P01M, controls port and timing functions for Ports 0 and 1. WRITE and reset states for bits D7–D0 are listed in Table 30.

Table 30. Ports 0 and 1 Mode Register—P01M F8h/R248 Bank 0h: WRITE ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset State	0	1	0	0	1	1	0	1
Note: W = Write.								

Bit Position	Bit Field	R/W	State	Description
D7–D6	P04–P07	W	01	**P04–P07 Mode*** 00: Output 01: Input 1X: A15–A12 (Z86E14x only)
D5	Timing	W	0	**External Memory Timing** 0: Normal 1: Extended
D4–D3	P10–P17	W	01	**P10–P17 Mode*** 00: Byte Output 01: Byte Input 10: AD7–AD0 11: High-Impedance AD7–AD0, $\overline{\text{AS}}$, $\overline{\text{DS}}$, R/$\overline{\text{W}}$, A11–A8, A15–A12, if selected

Note: *For 20- and 28-pin devices, the user must set D7=0, D4=0, D2=1, and D1=0.

Bit Position	Bit Field	R/W	State	Description
D2	Stack	W	1	**Stack Selection*** 0: External 1: Internal
D1–D0	P00–P03	W	01	**P00–P03 Mode*** 00: Output 01: Input 1X: A11–A8 (Z86E14x only)
Note: *For 20- and 28-pin devices, the user must set D7=0, D4=0, D2=1, and D1=0.				

Interrupt Priority Register

The Interrupt Priority Register, IPR, prioritizes interrupt functions. WRITE and reset states for bits D7–D0 are listed in Table 31.

Table 31. Interrupt Priority Register—IPR F9h/R249 Bank 0h: WRITE ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset State	X	X	X	X	X	X	X	X
Note: W = Write, X = Indeterminate.								

Bit Position	Bit Field	R/W	State	Description
D7–D6	Reserved	W	XX	Reserved—must be 0
D5	IRQ3, IRQ5	W	X	**IRQ3, IRQ5 Priority (Group A)** 0: IRQ5 > IRQ3 1: IRQ3 > IRQ5
D4,D3,D0	Interrupt	W	XXX	**Interrupt Group Priority** 000: Reserved 001: C > A > B 010: A > B > C 011: A > C > B 100: B > C > A 101: C > B > A 110: B > A > C 111: Reserved
D2	IRQ0, IRQ2	W	X	**IRQ0, IRQ2 Priority (Group B)** 0: IRQ2 > IRQ0 1: IRQ0 > IRQ2

Bit Position	Bit Field	R/W	State	Description
D1	IRQ1, IRQ4	W	X	**IRQ1, IRQ4 Priority (Group C)** 0: IRQ1 > IRQ4 1: IRQ4 > IRQ1

Interrupt Request Register

The Interrupt Request Register, IRQ, controls interrupt functions. READ/WRITE and reset states for bits D7–D0 are listed in Table 32.

Table 32. Interrupt Request Register—IRQ FAh/R250 Bank 0h: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Note: R = Read, W = Write.								

Bit Position	Bit Field	R/W	State	Description
D7–D6	Interrupt Edge	R/W	00	**Interrupt Edge** 00: P31 ↓ P32 ↓ 01: P31 ↓ P32 ↑ 10: P31 ↑ P32 ↓ 11: P31 ↑↓ P32 ↑↓
D5	IRQ5	R/W	0	**Interrupt** IRQ5 = T1 0: No Interrupt pending 1: Interrupt pending
D4	IRQ4	R/W	0	**Interrupt** IRQ4 = T0 0: No Interrupt pending 1: Interrupt pending
D3	IRQ3	R/W	0	**Interrupt** IRQ3 = P30 Input/UART 0: No Interrupt pending 1: Interrupt pending
D2	IRQ2	R/W	0	**Interrupt** IRQ2 = P31 Input 0: No Interrupt pending 1: Interrupt pending

Bit Position	Bit Field	R/W	State	Description
D1	IRQ1	R/W	0	**Interrupt** IRQ1 = P33 Input 0: No Interrupt pending 1: Interrupt pending
D0	IRQ0	R/W	0	**Interrupt** IRQ0 = P32 Input 0: No Interrupt pending 1: Interrupt pending

Interrupt Mask Register

The Interrupt Mask Register, IMR, controls interrupt functions. READ/WRITE and reset states for bits D7–D0 are listed in Table 33.

Table 33. Interrupt Mask Register—IMR FBh/R251 Bank 0h: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	X	X	X	X	X	X	X
Note: R = Read, W = Write, X = Indeterminate.								

Bit Position	Bit Field	R/W	State	Description
D7	MIE	R/W	0	**Master Interrupt Enable** 1: Enable interrupts 0: Disable interrupts
D6	RAM Protect	R/W	X	**RAM Protect** 1: Enable RAM Protect 0: Disable RAM Protect
D5–D0	IRQ5–IRQ0	R/W	X	**Interrupt Request** 1: Enable IRQ0–IRQ5 0: Disable IRQ0–IRQ5

Flags Register

The CPU sets flags in the Flags Register, FLAGS, to allow the user to perform tests based on differing logical states. READ/WRITE and reset states for bits D7–D0 are listed in Table 34.

Table 34. Flags Register—FLAGS FCh/R252 Bank 0h: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	X	X	X	X	X	X	X	X
Note: R = Read, W = Write, X = Indeterminate.								

Bit Position	Bit Field	R/W	State	Description
D7	Carry	R/W	X	Carry Flag
D6	Zero	R/W	X	Zero Flag
D5	Sign	R/W	X	Sign Flag
D4	Overflow	R/W	X	Overflow Flag
D3	Decimal Adjust	R/W	X	Decimal Adjust Flag
D2	Half Carry	R/W	X	Half Carry Flag
D1	User	R/W	X	User Flag F2*
D0	User	R/W	X	User Flag F1*
Note: *Not affected by $\overline{\text{RESET}}$.				

Register Pointer Register

The Register Pointer Register, RP, controls pointer functions in the working registers. READ/WRITE and reset states for bits D7–D0 are listed in Table 35.

Table 35. Register Pointer—RP FDh/R253 Bank 0h: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Note: R = Read, W = Write.								

Bit Position	Bit Field	R/W	State	Description
D7–D4	Working Register Pointer	R/W	0	Working Register Pointer

Bit Position	Bit Field	R/W	State	Description
D3–D0	Expanded Register File Bank	R/W	0	Expanded Register File Bank

Stack Pointer High Register

The Stack Pointer High Register, SPH, controls pointer functions in the upper byte. READ/WRITE and reset states for bits D7–D0 are listed in Table 36.

Table 36. Stack Pointer High—SPH FEh/R254 Bank 0h: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Note: R = Read, W = Write.								

Bit Position	Bit Field	R/W	State	Description
D7–D0	SPH	R/W	0	Stack Pointer Upper Byte* (SP15–SP8)
Note: *This register can be employed as a GPR for 20- and 28-pin devices.				

Stack Pointer Low Register

The Stack Pointer Low Register, SPL, controls pointer functions in the lower byte. READ/WRITE and reset states for bits D7–D0 are listed in Table 37.

Table 37. Stack Pointer Low—SPL FFh/R255 Bank 0h: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Note: R = Read, W = Write.								

Bit Position	Bit Field	R/W	State	Description
D7–D0	SPL	R/W	0	Stack Pointer Lower Byte (SP7–SP0)

ASCI Registers—Expanded Register File, Bank Ah

Bank Ah of the Expanded Register File includes registers that perform ASCI functions. The 8 available registers are the Transmit Data, Receive Data, Multiprocessor Control, Extension, Time Constant, and Status registers, as shown in Tables 39 through 46. These eight registers are not reset by a Stop-Mode Recovery. An additional register, 09h, is available for general purposes. Table 38 lists the reset states of all 16 ASCI registers.

Table 38. Expanded Register File Registers—Reset States

		D7	D6	D5	D4	D3	D2	D1	D0
00h	Reserved								
01h*	TDR	X	X	X	X	X	X	X	X
02h*	RDR	X	X	X	X	X	X	X	X
03h*	CNTLA	0	0	0	1	0	0	0	0
04h*	CNTLB	0	0	0	0	0	1	1	1
05h*	ASEXT	P30	0	0	0	0	0	1	0
06h*	ASTL	1	1	1	1	1	1	1	1
07h*	ASTH	1	1	1	1	1	1	1	1
08h*	STAT	0	0	0	0	0	0	0	0
09h	General-Purpose								
0Ah	Reserved								
0Bh	Reserved								
0Ch	Reserved								
0Dh	Reserved								
0Eh	Reserved								
0Fh	Reserved								

Note: *Not reset with a Stop-Mode Recovery.

Transmit Data Register

The Transmit Data Register, TDR, monitors data transmission functions in the FIFO. READ/WRITE and reset states for bits D7–D0 are listed in Table 39.

Table 39. Transmit Data Register—TDR 01h/R1 Bank Ah: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	X	X	X	X	X	X	X	X
Note: R = Read, W = Write, X = Indeterminate.								

Bit Position	Bit Field	R/W	State	Description
D7–D0	TDR	R/W	X	Transmit Data Register

Receive Data Register

The Receive Data Register, RDR, monitors data receive functions in the FIFO. READ/WRITE and reset states for bits D7–D0 are listed in Table 40.

Table 40. Receive Data Register—RDR 02h/R2 Bank Ah : READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	X	X	X	X	X	X	X	X
Note: R = Read, W = Write, X = Indeterminate.								

Bit Position	Bit Field	R/W	State	Description
D7–D0	RDR	R/W	X	Receive Data Register

Control Register A

Control Register A, CNTLA, controls data transmit, receive, and clocking functions. READ/WRITE and reset states for bits D7–D0 are listed in Table 41.

Table 41. Control Register A—CNTLA 03h/R3 Bank Ah: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	1	0	0	0	0
Note: R = Read, W = Write.								

Bit Position	Bit Field	R/W	State	Description
D7	MPE	R/W	0	**Multiprocessor Enable** 0: Receive all bytes 1: Filter bytes with MPB = 0
D6	RE	R/W	0	**Receiver Enable** 0: ASCI Receiver Disabled (P30 = Input) 1: ASCI Receiver Enabled (P30 = RX)
D5	TE	R/W	0	**Transmitter Enable** 0: ASCI Transmitter Disabled (P37 = Output) 1: ASCI Transmitter Enabled (P37 = TX)
D4	Reserved	R/W	1	Reserved
D3	MPBR	R	0	Multiprocessor Bit Received
	EFR	W		**Error Flag Reset** 0: Clear Error Latches 1: No Effect
D2–D0	MOD2–0	R	0	**Mode Select** MOD2—Number of Data Bits 0: 7 Data Bits 1: 8 Data Bits
				Mode Select MOD1—Parity Enabled 0: No Parity 1: With Parity
				Mode Select MOD0—Number of Stop Bits 0: 1 Stop Bit 1: 2 Stop Bits

Control Register B

Control Register B, CNTLB, controls multiprocessor, parity, and clock sourcing functions. READ/WRITE and reset states for bits D7–D0 are listed in Table 42.

Table 42. Control Register B—CNTLB 04h/R4 Bank Ah: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	1	1	1
Note: R = Read, W = Write.								

Bit Position	Bit Field	R/W	State	Description
D7	MPBT	R/W	0	**Multiprocessor Bit Transmitter** 0: Transmit 0 in MPB 1: Transmit 1 in MPB
D6	MP	R/W	0	**Multiprocessor Mode** 0: MULTIPROCESSOR mode disabled 1: MULTIPROCESSOR mode enabled (no parity)
D5	PR	W	0	**Prescale** 0: BRG ÷ 10 1: BRG ÷ 30
D4	PEO	R/W	0	**Parity Even/Odd** 0: Even Parity 1: Odd Parity
D3	DR	R/W	0	**Divide Ratio** 0: Divide by 16 1: Divide by 64
D2	SS2	R	1	**Clock Source and Speed Bits** SS2 0: ÷1, ÷2, ÷4, ÷8 1: ÷16, ÷32, ÷64, Reserved
D1	SS1	R	1	**Clock Source and Speed Bits** SS1 0: ÷1, ÷2, ÷16, ÷32 1: ÷4, ÷8, ÷64, Reserved
D0	SS0	R	1	**Clock Source and Speed Bits** SS0 0: ÷1, ÷4, ÷16, ÷64 1: ÷2, ÷8, ÷32, Reserved

ASCI Extension Control Register

The ASCI Extension Control Register, ASEXT, controls ASCI transmission functions. READ/WRITE and reset states for bits D7–D0 are listed in Table 43.

Table 43. Extension Control Register—ASEXT 05h/R5 Bank Ah: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	R/W	R/W	R/W	R/W	R/W	R	R/W
Reset	X	0	0	0	0	0	1	0
Note: R = Read, W = Write.								

Bit Position	Bit Field	R/W	State	Description
D7	RX	R	X	RX Data State
D6	Reserved	R/W	0	Reserved
D5	Reserved	R/W	0	Reserved
D4	Reserved	R/W	0	Reserved (must be 0)
D3	BRG	R/W	0	**Baud Rate Generator Mode** 0: Use SS Selection 1: Use ASTH or ASTL Value
D2	RIS	R/W	0	**RX Interrupt on Start Bit** 0: No IRQ on Start Bit 1: IRQ3 on Start Bit
D1	BD	R	1	**Break Detect** 0: Valid Data Byte 1: Break Detected
D0	SB	R/W	0	**Send Break** 0: Normal Operation 1: Send Break

ASCI Time Constant Low Register

The ASCI Time Constant Low Register, ASTL, controls transmission functions in the lower byte. READ/WRITE and reset states for bits D7–D0 are listed in Table 44.

Table 44. Time Constant Low Register—ASTL 06h/R6 Bank Ah: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1
Note: R = Read, W = Write.								

Bit Position	Bit Field	R/W	State	Description
D7–D0	ASTL	R/W	1	ASCI Time Constant Low

ASCI Time Constant High Register

The ASCI Time Constant High Register, ASTH, controls transmission functions in the upper byte. READ/WRITE and reset states for bits D7–D0 are listed in Table 45.

Table 45. Time Constant Register High—ASTH 07h/R7 Bank Ah: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1
Note: R = Read, W = Write.								

Bit Position	Bit Field	R/W	State	Description
D7–D0	ASTH	R/W	1	ASCI Time Constant High

ASCI Status Register

The ASCI Status Register, STAT, controls status functions. READ/WRITE and reset states for bits D7–D0 are listed in Table 46.

Table 46. Status Register—STAT 08h/R8 Bank Ah: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	R	R	R	R/W	R/W	R	R/W
Reset	0	0	0	0	0	0	0	0
Note: R = Read, W = Write.								

Bit Position	Bit Field	R/W	State	Description
D7	RDRNE	R	0	**Receive Data Register Not Empty** 0: Receive FIFO Empty 1: Receive FIFO contains 1 or more bytes
D6	OE	R	0	**Overrun Error** 0: Receive OK 1: Next byte is a FIFO overrun
D5	PE	R	0	**Parity Error** 0: Parity OK 1: Parity Error
D4	FE	R	0	**Framing Error** 0: Receive OK 1: Framing Error
D3	RIE	R/W	0	**Receive Interrupt Enable** 0: No IRQ on Receive 1: Enable Receiver Interrupt
D2	Reserved	R/W	0	Reserved
D1	TDRE	R	0	**Transmit Data Register Empty** 0: Transmitter Working 1: Transmit Buffer Empty
D0	TIE	R/W	0	**Transmit Interrupt Enable** 0: No IRQ on Transmit 1: IRQ3 on TDRE↑

Expanded Register File, Bank Fh

Expanded Register File Fh Bank 0h contains 5 registers that perform the Port Configuration, Verify, Stop-Mode Recovery, and Watch-Dog Timer Mode functions, as shown in Tables 49 through 52. These 5 registers are not reset by a Stop-Mode Recovery. Table 47 lists the reset states of all 5 Bank 0h registers.

Table 47. Expanded Register File Registers—Reset States

		D7	D6	D5	D4	D3	D2	D1	D0
00h	PCON*	1	1	1	1	1	1	1	0
01h	Reserved								
02h	Reserved								
03h	Reserved								
04h	Reserved								
05h	Reserved								
06h	Reserved								
07h	Reserved								
08h	Reserved								
09h	Reserved								
0Ah	Reserved								
0Bh	SMR*	0	0	1	0	0	0	0	0
0Ch	Reserved								
0Dh	SMR2*	X	X	X	X	X	X	0	0
0Eh	Reserved								
0Fh	WDTMR*	X	X	X	0	1	1	0	1

Note: *Not reset with a Stop-Mode Recovery.

Port Configuration Register

The Port Configuration Register, PCON, controls the configurations of Ports 0, 1, 2, and 3. WRITE and reset states for bits D7–D0 are listed in Table 48.

Table 48. Port Configuration Register—PCON 00h/R0 Bank Fh: WRITE ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset	1	1	1	1	1	1	1	0
Note: W = Write.								

Bit Position	Bit Field	R/W	State	Description
D7	Oscillator	W	1	**Low-EMI Oscillator** 0: Low EMI 1: Standard
D6	Port 3 I/O	W	1	**Port 3** 0: Low EMI 1: Standard
D5	Port 2 I/O	W	1	**Port 2** 0: Low EMI 1: Standard
D4	Port 1 I/O	W	1	**Port 1*** 0: Low EMI 1: Standard
D3	Port 0 I/O	W	1	**Port 0†** 0: Low EMI 1: Standard
D2	Port 0 I/O	W	1	**Port 0** 0: Open-Drain 1: Push-Pull Active
D1	Port 1 I/O	W	1	**Port 1***† 0: Open-Drain 1: Push-Pull Active
D0	Port 3	W	0	**Port 3 Comparator Output** 0: P34, P37 Standard Output 1: P34, P37 Comparator Output

Notes:
1. Must be set to 1 when using an emulator.
2. Must be set to 1 for both 20- and 28-pin devices.

Verify Register

The Verify Register, VFY, is only available after the ICSP unlock sequence executes. READ and reset states for bits D7–D0 are listed in Table 49. For more information on the VFY register, please see the MUZE Programming Specification.

Table 49. Verify Register—VFY 09h/R09 Bank Fh: READ ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	R	R	R	R	R	R	R
Reset	X	X	X	X	X	X	X	X
Note: R = Read, X = Indeterminate.								

Bit Position	Bit Field	R/W	State	Description
D7–D2	Reserved	R	X	Reserved
D1	VFY1	R	X	**Verify 1** Programming verification result is output at this register
D0	VFY0	R	X	**Verify 0** Programming verification result is output at this register

Stop-Mode Recovery Register

The Stop-Mode Recovery Register, SMR, controls clocking functions. READ/WRITE and reset states for bits D7–D0 are listed in Table 50.

Table 50. Stop-Mode Recovery Register—SMR 0Bh/R11 Bank Fh:READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	W	W	W	W	W	W	W
Reset	0	0	1	0	0	0	0	0
Note: R = Read, W = Write.								

Bit Position	Bit Field	R/W	State	Description
D7	Stop	R	0	**Stop Flag** 0: POR 1: Stop Recovery

Notes:
1. For the Stop-Mode Recovery Source, either SMR or SMR2 can be selected. If SMR is used to select the Stop-Mode Recovery Source, bits D1–D0 of SMR2 must be 0.
2. Cleared by $\overline{\text{RESET}}$ and SMR.

Bit Position	Bit Field	R/W	State	Description
D6	Stop-Mode Recovery	W	0	**Stop-Mode Recovery Level** 0: Low 1: High
D5	Stop Delay	W	1	**Stop Delay** 0: Off 1: On
D4–D2	Stop Mode	W	000	**Stop-Mode Recovery Source*** 000: POR only and/or external $\overline{\text{RESET}}$ 001: P30 010: P31 011: P32 100: P33 101: P27 110: P2 NOR 0–3 111: P2 NOR 0–7
D1	Clock	W	0	**External Clock Divide-by-2** 0: SCLK ÷ TCLK = Crystal ÷ 2 1: SCLK = Crystal
D0	SCLK/TCLK	W	0	**SCLK/TCLK Divide-by-16** 0: Off 1: On

Notes:
1. For the Stop-Mode Recovery Source, either SMR or SMR2 can be selected. If SMR is used to select the Stop-Mode Recovery Source, bits D1–D0 of SMR2 must be 0.
2. Cleared by $\overline{\text{RESET}}$ and SMR.

Stop-Mode Recovery Register 2

The Stop-Mode Recovery Register, SMR2, controls additional Port 2 clocking functions. WRITE and reset states for bits D7–D0 are listed in Table 51.

Table 51. Stop-Mode Recovery Register 2—SMR2 0Dh/R13 Bank Fh: WRITE ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	X	X	X	0	0
Note: W = Write, X = Indeterminate.								

Bit Position	Bit Field	R/W	State	Description
D7–D2	Reserved	W	X	Reserved—must be 0
D1–D0	STOP Mode	W	00	**Stop-Mode Recovery Source 2*** 00: POR only 01: AND P20, P21, P22, P23 10: AND P20, P21, P22, P23, P24, P25, P26, P27

Note: For the Stop-Mode Recovery Source, either SMR or SMR2 can be selected. If SMR2 is used to select the Stop-Mode Recovery Source, bits D4–D2 of SMR must be 0.

Watch-Dog Timer Mode Register

The Watch-Dog Timer Mode Register, WDTMR, controls Watch-Dog Timer functions. WRITE and reset states for bits D7–D0 are listed in Table 52.

Table 52. Watch-Dog Timer Mode Register—WDTMR 0Fh/R15 Bank Fh: WRITE ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	0	1	1	0	1
Note: W = Write, X = Indeterminate.								

Bit Position	Bit Field	R/W	State	Description
D7–D5	Reserved	W	X	Reserved—must be 0
D4	X_{IN}	W	0	Crystal Input/**Internal RC Select for WDT** 0: On-Board RC 1: Crystal

Note: Not used in conjunction with SMR Source.

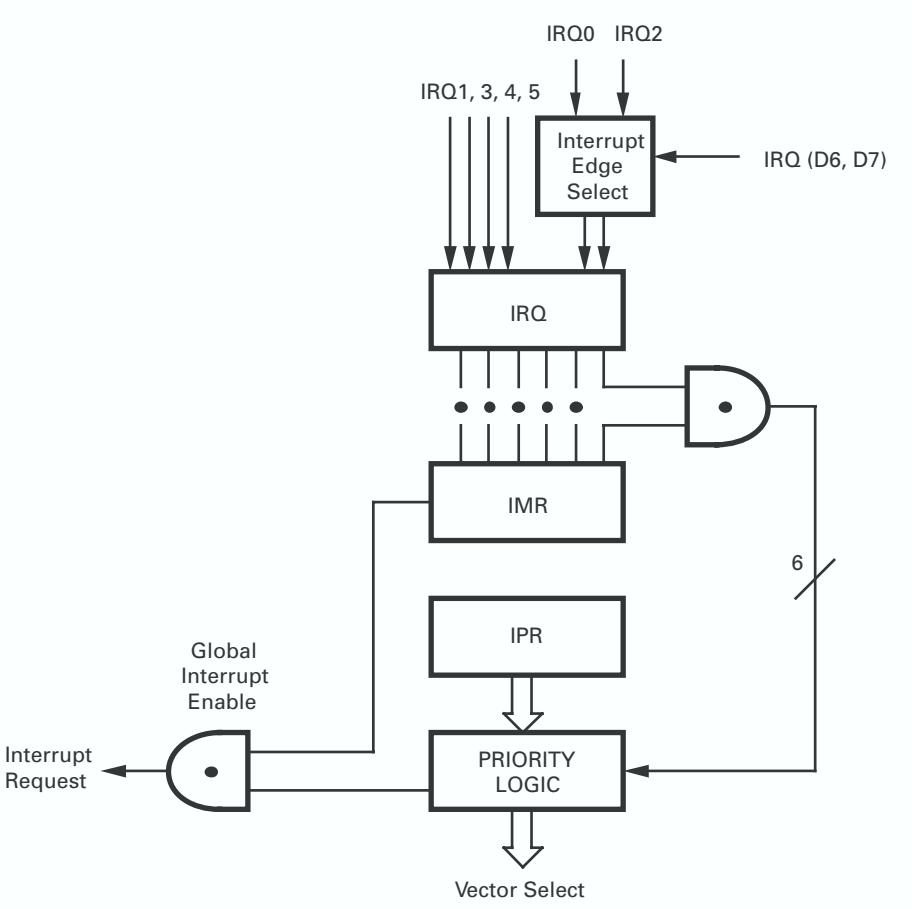
Bit Position	Bit Field	R/W	State	Description
D3	WDT	W	1	**WDT During STOP** 0: WDT disabled during STOP mode 1: WDT enabled during STOP mode
D2	WDT	W	1	**WDT During HALT** 0: WDT disabled during HALT mode 1: WDT enabled during HALT mode
D1–D0	WDT Tap	W	01	**WDT Tap — Int. RC Osc. — System Clock** 00: 3.5 ms 128 SCLK 01: 7 ms 256 SCLK 10: 14 ms 512 SCLK 11: 56 ms 2048 SCLK

Note: Not used in conjunction with SMR Source.

Interrupts

Interrupt Block Diagram

Figure 24. Interrupt Block Diagram



Electrical Characteristics

Absolute Maximum Ratings

Stresses greater than the Absolute Maximum Ratings listed in Table 53 may cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Table 53. Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on X_{IN} and $\overline{RESET}$ Pins with Respect to V_{SS}	–0.6	V_{DD}+1	V	2
Total Power Dissipation		1.21	W	
Maximum Allowable Current out of V_{SS}		220	mA	
Maximum Allowable Current into V_{DD}		180	mA	
Maximum Allowable Current into an Input Pin	–600	+600	µA	3
Maximum Allowable Current into an Open-Drain Pin	–600	+600	µA	4
Maximum Allowable Output Current Sunk by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA	

Notes:
1. Applies to all pins except Crystal pins and where otherwise noted.
2. There is no input protection diode from pin to V_{DD} and current into pin is limited to ±600 µA.
3. Excludes Crystal pins.
4. Device pin is not at an output Low state.

Total power dissipation should not exceed 1.21 W for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [I_{DD} - (\text{sum of } I_{OH}), + \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{OL} \times I_{OL})$$

DC Electrical Characteristics

Standard Temperature Range

Table 54. DC Electrical Characteristics at Standard Temperature

Sym	Parameter	V_{CC1}	T_A = 0°C to +70°C Min	T_A = 0°C to +70°C Max	Typical[2] @25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	1.8	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.6	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	4.5V	GND–0.3	0.2 V_{CC}	1.2	V	Driven by External Clock Generator	
		5.5V	GND–0.3	0.2 V_{CC}	2.1	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	1.8	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.6	V		
V_{IL}	Input Low Voltage	4.5V	GND–0.3	0.2 V_{CC}	1.1	V		
		5.5V	GND–0.3	0.2 V_{CC}	1.6	V		

Notes:
1. The V_{CC} voltage specification of 4.5V guarantees 3.3V ±0.3V with typicals at V_{CC} = 3.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V with typicals at V_{CC} = 5.0V.
2. Typical voltage is V_{CC} = 5.0V and 3.3V.
3. STANDARD Mode (not Low-EMI Mode).
4. Not applicable to devices in 28-pin packages.
5. For analog comparator, inputs when analog comparators are enabled.
6. All outputs unloaded, I/O pins floating, inputs at rail.
7. Same as note 6, except inputs at V_{CC}.
8. Clock must be forced Low, when X_{IN} is clock-driven and X_{OUT} is floating.
9. 0ºC to 70ºC (standard temperature).
10. Autolatch (Mask Option) selected.
11. The V_{LV} voltage increases as the temperature decreases and overlaps lower V_{CC} operating region. See Figure 23 on page 49
12. –40˚C to 150˚C (extended temperature).

Table 54. DC Electrical Characteristics at Standard Temperature (Continued)

Sym	Parameter	V_{CC1}	T_A = 0°C to +70°C Min	T_A = 0°C to +70°C Max	Typical[2] @25°C	Units	Conditions	Notes
V_{OH}	Output High Voltage (Low-EMI Mode)	4.5V	V_{CC}–0.4		3.1	V	I_{OH} = –0.5 mA	
		5.0V	V_{CC}–0.4		4.8	V	I_{OH} = –0.5 mA	
V_{OH1}	Output High Voltage	4.5V	V_{CC}–0.4		3.1	V	I_{OH} = –2.0 mA	3
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	3
V_{OL}	Output Low Voltage (Low-EMI Mode)	4.5V		0.6	0.2	V	I_{OL} = 1.0 mA	
		5.0V		0.4	0.1	V	I_{OL} = 1.0 mA	
V_{OL1}	Output Low Voltage	4.5V		0.6	0.2	V	I_{OL} = +4.0 mA	3
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	3
V_{OL2}	Output Low Voltage	4.5V		1.2	0.3	V	I_{OL} = +6 mA	3
		5.5V		1.2	0.4	V	I_{OL} = +12 mA	3
V_{RH}	Reset Input High Voltage	4.5V	0.8 V_{CC}	V_{CC}	1.8	V		4
		5.5V	0.8 V_{CC}	V_{CC}	2.6	V		4
V_{RI}	Reset Input Low Voltage	4.5V	GND–0.3	0.2 V_{CC}	1.1	V		4
		5.5V	GND–0.3	0.2 V_{CC}	1.6	V		4
V_{OLR}	Reset Output Low Voltage	4.5V		0.6	0.3	V	I_{OL} = +1.0 mA	4
		5.5V		0.6	0.3	V	I_{OL} = +1.0 mA	4

Notes:
1. The V_{CC} voltage specification of 4.5V guarantees 3.3V ±0.3V with typicals at V_{CC} = 3.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V with typicals at V_{CC} = 5.0V.
2. Typical voltage is V_{CC} = 5.0V and 3.3V.
3. STANDARD Mode (not Low-EMI Mode).
4. Not applicable to devices in 28-pin packages.
5. For analog comparator, inputs when analog comparators are enabled.
6. All outputs unloaded, I/O pins floating, inputs at rail.
7. Same as note 6, except inputs at V_{CC}.
8. Clock must be forced Low, when X_{IN} is clock-driven and X_{OUT} is floating.
9. 0ºC to 70ºC (standard temperature).
10. Autolatch (Mask Option) selected.
11. The V_{LV} voltage increases as the temperature decreases and overlaps lower V_{CC} operating region. See Figure 23 on page 49
12. –40˚C to 150˚C (extended temperature).

Table 54. DC Electrical Characteristics at Standard Temperature (Continued)

Sym	Parameter	V_{CC1}	T_A = 0°C to +70°C Min	T_A = 0°C to +70°C Max	Typical[2] @25°C	Units	Conditions	Notes
V_{OFFSET}	Comparator Input Offset Voltage	4.5V		25	10	mV		5
		5.5V		25	10	mV		5
I_{IL}	Input Leakage	4.5V	–1	2	0.004	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1	2	0.004	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	4.5V	–1	1	0.004	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1	1	0.004	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	4.5V	–20	–130	–60	µA		
		5.5V	–20	–180	–85	µA		
I_{CC}	Supply Current	4.5V		20	7	mA	@ 16 MHz	6
		5.5V		25	20	mA	@ 16 MHz	6
		4.5V		15	5	mA	@ 12 MHz	6
		5.5V		20	15	mA	@ 12 MHz	6

Notes:
1. The V_{CC} voltage specification of 4.5V guarantees 3.3V ±0.3V with typicals at V_{CC} = 3.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V with typicals at V_{CC} = 5.0V.
2. Typical voltage is V_{CC} = 5.0V and 3.3V.
3. STANDARD Mode (not Low-EMI Mode).
4. Not applicable to devices in 28-pin packages.
5. For analog comparator, inputs when analog comparators are enabled.
6. All outputs unloaded, I/O pins floating, inputs at rail.
7. Same as note 6, except inputs at V_{CC}.
8. Clock must be forced Low, when X_{IN} is clock-driven and X_{OUT} is floating.
9. 0ºC to 70ºC (standard temperature).
10. Autolatch (Mask Option) selected.
11. The V_{LV} voltage increases as the temperature decreases and overlaps lower V_{CC} operating region. See Figure 23 on page 49
12. –40˚C to 150˚C (extended temperature).

Table 54. DC Electrical Characteristics at Standard Temperature (Continued)

Sym	Parameter	V_{CC1}	T_A = 0°C to +70°C Min	T_A = 0°C to +70°C Max	Typical[2] @25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (HALT mode)	4.5V		4.5	2.0	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	6
		5.5V		8	3.7	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	6
		4.5V		3.4	1.5	mA	Clock Divide-by-16 @ 16 MHz	6
		5.5V		7.0	2.9	mA	Clock Divide-by-16 @ 16 MHz	6
I_{CC2}	Standby Current (STOP Mode)	4.5V		8	2	µA	V_{IN} = 0V, V_{CC} WDT is not Running	7,8
		5.5V		10	4	µA	V_{IN} = 0V, V_{CC} WDT is not Running	7,8
		4.5V		500	310	µA	V_{IN} = 0V, V_{CC} WDT is Running	7,8,9
		5.5V		800	600	µA	V_{IN} = 0V, V_{CC} WDT is Running	7,8,9

Notes:
1. The V_{CC} voltage specification of 4.5V guarantees 3.3V ±0.3V with typicals at V_{CC} = 3.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V with typicals at V_{CC} = 5.0V.
2. Typical voltage is V_{CC} = 5.0V and 3.3V.
3. STANDARD Mode (not Low-EMI Mode).
4. Not applicable to devices in 28-pin packages.
5. For analog comparator, inputs when analog comparators are enabled.
6. All outputs unloaded, I/O pins floating, inputs at rail.
7. Same as note 6, except inputs at V_{CC}.
8. Clock must be forced Low, when X_{IN} is clock-driven and X_{OUT} is floating.
9. 0ºC to 70ºC (standard temperature).
10. Autolatch (Mask Option) selected.
11. The V_{LV} voltage increases as the temperature decreases and overlaps lower V_{CC} operating region. See Figure 23 on page 49
12. –40˚C to 150˚C (extended temperature).

Table 54. DC Electrical Characteristics at Standard Temperature (Continued)

Sym	Parameter	V_{CC1}	T_A = 0°C to +70°C Min	T_A = 0°C to +70°C Max	Typical[2] @25°C	Units	Conditions	Notes
V_{ICR}	Input Common Mode Voltage Range	4.5V	0	V_{CC}–1.0V		V		5
		5.5V	0	V_{CC}–1.0V		V		5
I_{ALL}	Autolatch Low Current	4.5V	0.7	8	3	µA	$0V<V_{IN}<V_{CC}$	10
		5.5V	1.4	15	5	µA	$0V<V_{IN}<V_{CC}$	10
I_{ALH}	Autolatch High Current	4.5V	–0.6	–5	–3	µA	$0V<V_{IN}<V_{CC}$	10
		5.5V	–1.0	–8	–6	µA	$0V<V_{IN}<V_{CC}$	10
V_{LV}	V_{CC} Low Voltage Protection Voltage	4.5V			2.8	V	4 MHz max Interrupt CLK Freq.	11,12
		5.5V	2.2	3.1	2.8	V	6 MHz max Interrupt CLK Freq.	9,11

Notes:
1. The V_{CC} voltage specification of 4.5V guarantees 3.3V ±0.3V with typicals at V_{CC} = 3.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V with typicals at V_{CC} = 5.0V.
2. Typical voltage is V_{CC} = 5.0V and 3.3V.
3. STANDARD Mode (not Low-EMI Mode).
4. Not applicable to devices in 28-pin packages.
5. For analog comparator, inputs when analog comparators are enabled.
6. All outputs unloaded, I/O pins floating, inputs at rail.
7. Same as note 6, except inputs at V_{CC}.
8. Clock must be forced Low, when X_{IN} is clock-driven and X_{OUT} is floating.
9. 0ºC to 70ºC (standard temperature).
10. Autolatch (Mask Option) selected.
11. The V_{LV} voltage increases as the temperature decreases and overlaps lower V_{CC} operating region. See Figure 23 on page 49
12. –40˚C to 150˚C (extended temperature).

Extended Temperature Range

Table 55. DC Electrical Characteristics at Extended Temperature

Sym	Parameter	V_{CC1}	T_A = –40°C to +105°C Min	T_A = –40°C to +105°C Max	Typical[2] @25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	1.8	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.6	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	4.5V	GND–0.3	0.2 V_{CC}	1.2	V	Driven by External Clock Generator	
		5.5V	GND–0.3	0.2 V_{CC}	2.1	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	1.8	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.6	V		
V_{IL}	Input Low Voltage	4.5V	GND–0.3	0.2 V_{CC}	1.1	V		
		5.5V	GND–0.3	0.2 V_{CC}	1.6	V		
V_{OH}	Output High Voltage (Low-EMI Mode)	4.5V	V_{CC}–0.4		3.1	V	I_{OH} = –0.5 mA	
		5.0V	V_{CC}–0.4		4.8	V	I_{OH} = –0.5 mA	
V_{OH1}	Output High Voltage	4.5V	V_{CC}–0.4		3.1	V	I_{OH} = –2.0 mA	3
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	3

Notes:
1. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V with typicals at V_{CC} = 5.0V.
2. Typicals are at V_{CC} = 5.0V and 3.3V.
3. STANDARD Mode (not Low EMI).
4. Not applicable to devices in 28-pin packages.
5. For analog comparator, inputs when analog comparators are enabled.
6. All outputs unloaded, I/O pins floating, inputs at rail.
7. Same as note 6, except inputs at V_{CC}.
8. Clock must be forced Low, when X_{IN} is clock-driven and X_{OUT} is floating.
9. 0ºC to 70ºC (standard temperature).
10. Autolatch (Mask Option) selected.
11. The V_{LV} voltage increases as the temperature decreases and overlaps lower V_{CC} operating region.
12. –40˚C to 150˚C (extended temperature).

Table 55. DC Electrical Characteristics at Extended Temperature (Continued)

Sym	Parameter	V_{CC1}	T_A = –40°C to +105°C Min	Max	Typical[2] @25°C	Units	Conditions	Notes
V_{OL}	Output Low Voltage (Low-EMI Mode)	4.5V		0.6	0.2	V	I_{OL} = 1.0 mA	
		5.0V		0.4	0.1	V	I_{OL} = 1.0 mA	
V_{OL1}	Output Low Voltage	4.5V		0.6	0.2	V	I_{OL} = +4.0 mA	3
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	3
V_{OL2}	Output Low Voltage	4.5V		1.2	0.3	V	I_{OL} = +6 mA	3
		5.5V		1.2	0.4	V	I_{OL} = +12 mA	3
V_{RH}	Reset Input High Voltage	4.5V	0.8 V_{CC}	V_{CC}	1.8	V		4
		5.5V	0.8 V_{CC}	V_{CC}	2.6	V		4
V_{RI}	Reset Input Low Voltage	4.5V	GND–0.3	0.2 V_{CC}	1.1	V		4
		5.5V	GND–0.3	0.2 V_{CC}	1.6	V		4
V_{OLR}	Reset Output Low Voltage	4.5V		0.6	0.3	V	I_{OL} = +1.0 mA	4
		5.5V		0.6	0.3	V	I_{OL} = +1.0 mA	4
V_{OFFSET}	Comparator Input Offset Voltage	4.5V		25	10	mV		5
		5.5V		25	10	mV		5
I_{IL}	Input Leakage	4.5V	–1	2	0.004	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1	2	0.004	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	4.5V	–1	2	0.004	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1	2	0.004	µA	V_{IN} = 0V, V_{CC}	

Notes:
1. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V with typicals at V_{CC} = 5.0V.
2. Typicals are at V_{CC} = 5.0V and 3.3V.
3. STANDARD Mode (not Low EMI).
4. Not applicable to devices in 28-pin packages.
5. For analog comparator, inputs when analog comparators are enabled.
6. All outputs unloaded, I/O pins floating, inputs at rail.
7. Same as note 6, except inputs at V_{CC}.
8. Clock must be forced Low, when X_{IN} is clock-driven and X_{OUT} is floating.
9. 0ºC to 70ºC (standard temperature).
10. Autolatch (Mask Option) selected.
11. The V_{LV} voltage increases as the temperature decreases and overlaps lower V_{CC} operating region.
12. –40˚C to 150˚C (extended temperature).

Table 55. DC Electrical Characteristics at Extended Temperature (Continued)

Sym	Parameter	V_{CC1}	T_A = –40°C to +105°C Min	T_A = –40°C to +105°C Max	Typical[2] @25°C	Units	Conditions	Notes
I_{IR}	Reset Input Current	4.5V	–18	–130	–60	µA		
		5.5V	–18	–180	–85	µA		
I_{CC}	Supply Current	4.5V		20	7	mA	@ 16 MHz	6
		5.5V		25	20	mA	@ 16 MHz	6
		4.5V		15	5	mA	@ 12 MHz	6
		5.5V		20	15	mA	@ 12 MHz	6
I_{CC1}	Standby Current (HALT mode)	4.5V		4.5	2.0	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	6
		5.5V		8	3.7	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	6
		4.5V		3.4	1.5	mA	Clock Divide-by-16 @ 16 MHz	6
		5.5V		7.0	2.9	mA	Clock Divide-by-16 @ 16 MHz	6

Notes:
1. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V with typicals at V_{CC} = 5.0V.
2. Typicals are at V_{CC} = 5.0V and 3.3V.
3. STANDARD Mode (not Low EMI).
4. Not applicable to devices in 28-pin packages.
5. For analog comparator, inputs when analog comparators are enabled.
6. All outputs unloaded, I/O pins floating, inputs at rail.
7. Same as note 6, except inputs at V_{CC}.
8. Clock must be forced Low, when X_{IN} is clock-driven and X_{OUT} is floating.
9. 0ºC to 70ºC (standard temperature).
10. Autolatch (Mask Option) selected.
11. The V_{LV} voltage increases as the temperature decreases and overlaps lower V_{CC} operating region.
12. –40˚C to 150˚C (extended temperature).

Table 55. DC Electrical Characteristics at Extended Temperature (Continued)

Sym	Parameter	V_{CC1}	T_A = –40°C to +105°C Min	T_A = –40°C to +105°C Max	Typical[2] @25°C	Units	Conditions	Notes
I_{CC2}	Standby Current (STOP Mode)	4.5V		8	2	µA	V_{IN} = 0V, V_{CC} WDT is not Running	7,8
		5.5V		10	4	µA	V_{IN} = 0V, V_{CC} WDT is not Running	7,8
		4.5V		600	310	µA	V_{IN} = 0V, V_{CC} WDT is Running	7,8,9
		5.5V		1000	600	µA	V_{IN} = 0V, V_{CC} WDT is Running	7,8,9
V_{ICR}	Input Common Mode Voltage Range	4.5V	0	V_{CC}–1.5V		V		5
		5.5V	0	V_{CC}–1.5V		V		5
I_{ALL}	Autolatch Low Current	4.5V	0.7	10	3	µA	0V<V_{IN}<V_{CC}	10
		5.5V	1.4	20	5	µA	0V<V_{IN}<V_{CC}	10

Notes:
1. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V with typicals at V_{CC} = 5.0V.
2. Typicals are at V_{CC} = 5.0V and 3.3V.
3. STANDARD Mode (not Low EMI).
4. Not applicable to devices in 28-pin packages.
5. For analog comparator, inputs when analog comparators are enabled.
6. All outputs unloaded, I/O pins floating, inputs at rail.
7. Same as note 6, except inputs at V_{CC}.
8. Clock must be forced Low, when X_{IN} is clock-driven and X_{OUT} is floating.
9. 0ºC to 70ºC (standard temperature).
10. Autolatch (Mask Option) selected.
11. The V_{LV} voltage increases as the temperature decreases and overlaps lower V_{CC} operating region.
12. –40˚C to 150˚C (extended temperature).

Table 55. DC Electrical Characteristics at Extended Temperature (Continued)

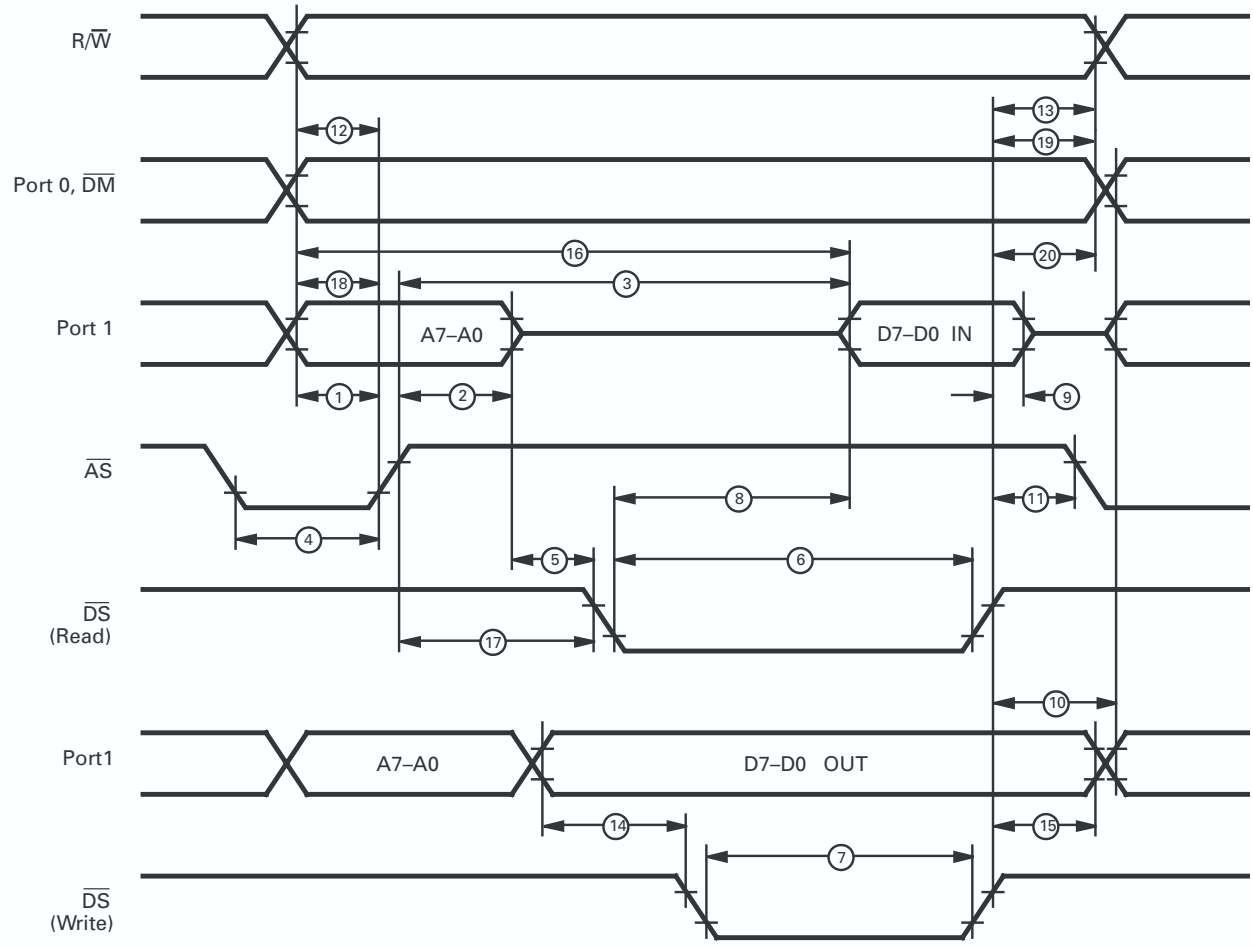
Sym	Parameter	V_{CC1}	T_A = –40°C to +105°C Min	Max	Typical[2] @25°C	Units	Conditions	Notes
I_{ALH}	Autolatch High Current	4.5V	–0.6	–7	–3	µA	$0V<V_{IN}<V_{CC}$	10
		5.5V	–1.0	–10	–6	µA	$0V<V_{IN}<V_{CC}$	10
V_{LV}	V_{CC} Low Voltage Protection Voltage	4.5V	2.0	3.3	2.8	V	4 MHz max Interrupt CLK Freq.	11,12
		5.5V			2.8		6 MHz max Interrupt CLK Freq.	9,11

Notes:
1. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V with typicals at V_{CC} = 5.0V.
2. Typicals are at V_{CC} = 5.0V and 3.3V.
3. STANDARD Mode (not Low EMI).
4. Not applicable to devices in 28-pin packages.
5. For analog comparator, inputs when analog comparators are enabled.
6. All outputs unloaded, I/O pins floating, inputs at rail.
7. Same as note 6, except inputs at V_{CC}.
8. Clock must be forced Low, when X_{IN} is clock-driven and X_{OUT} is floating.
9. 0ºC to 70ºC (standard temperature).
10. Autolatch (Mask Option) selected.
11. The V_{LV} voltage increases as the temperature decreases and overlaps lower V_{CC} operating region.
12. –40˚C to 150˚C (extended temperature).

AC Electrical Characteristics

Figure 25 illustrates the timing characteristics of the MUZE Family of parts with respect to external input/output sources. See Tables 56 and 57 for descriptions of the numbered timing parameters in the figure.

Figure 25. External I/O or Memory READ and WRITE Timing



Standard Temperature Range

Table 56. External I/O or Memory READ and WRITE Timing—Standard Temperature

				T_A = –0ºC to 70ºC @ 12 MHz			
No	**Symbol**	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Units**	**Notes**
1	T_DA(AS)	Address Valid to $\overline{AS}$ Rise Delay	4.5V	35		ns	2
			5.5V	35		ns	2
2	T_DAS(A)	$\overline{AS}$ Rise to Address Float Delay	4.5V	45		ns	2
			5.5V	45		ns	2
3	T_DAS(DR)	$\overline{AS}$ Rise to Read Data Req'd Valid	4.5V		250	ns	2,3
			5.5V		250	ns	2
4	T_WAS	$\overline{AS}$ Low Width	4.5V	55		ns	2
			5.5V	55		ns	2
5	T_DAS(DS)	Address Float to $\overline{DS}$ Fall	4.5V	0		ns	
			5.5V	0		ns	
6	T_WDSR	$\overline{DS}$ (Read) Low Width	4.5V	200		ns	2,3
			5.5V	200		ns	2,3
7	T_WDSW	$\overline{DS}$ (WRITE) Low Width	4.5V	110		ns	2,3
			5.5V	110		ns	2,3
8	T_DDSR(DR)	$\overline{DS}$ Fall to Read Data Req'd Valid	4.5V		150	ns	2,3
			5.5V		150	ns	2,3
9	T_HDR(DS)	Read Data to $\overline{DS}$ Rise Hold Time	4.5V	0		ns	2
			5.5V	0		ns	2
10	T_DDS(A)	$\overline{DS}$ Rise to Address Active Delay	4.5V	45		ns	2
			5.5V	55		ns	2
11	T_DDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	4.5V	30		ns	2
			5.5V	45		ns	2
12	T_DR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay	4.5V	45		ns	2
			5.5V	45		ns	2

Notes:
1. Z86E142/E143/E144/E145/E146 only; SCLK ÷ TCLK = Crystal ÷ 2.
2. The V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V.
3. Timing numbers provided are for minimum T_PC.

Table 56. External I/O or Memory READ and WRITE Timing—Standard Temperature (Continued)

			T_A = –0ºC to 70ºC @ 12 MHz				
No	**Symbol**	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Units**	**Notes**
13	T_DDS(R/W)	$\overline{DS}$ Rise to R/$\overline{W}$ Not Valid	4.5V	45		ns	2
			5.5V	45		ns	2
14	T_DDW(DSW)	WRITE Data Valid to $\overline{DS}$ Fall (WRITE) Delay	4.5V	55		ns	2
			5.5V	55		ns	2
15	T_DDS(DW)	$\overline{DS}$ Rise to WRITE Data Not Valid Delay	4.5V	45		ns	2
			5.5V	45		ns	2
16	T_DA(DR)	Address Valid to Read Data Req'd Valid	4.5V		310	ns	2,3
			5.5V		310	ns	2,3
17	T_DAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay	4.5V	65		ns	2
			5.5V	65		ns	2
18	T_DDM(AS)	$\overline{DM}$ Valid to $\overline{AS}$ Fall Delay	4.5V	35		ns	2
			5.5V	35		ns	2
19	T_DDS(DM)	$\overline{DS}$ Rise to DM Valid Delay	4.5V	45		ns	2
			5.5V	45		ns	2
20	T_HDS(AS)	$\overline{DS}$ Valid to Address Valid Hold Time	4.5V	45		ns	2
			5.5V	45		ns	2

Notes:
1. Z86E142/E143/E144/E145/E146 only; SCLK ÷ TCLK = Crystal ÷ 2.
2. The V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V.
3. Timing numbers provided are for minimum T_PC.

Extended Temperature Range

Table 57. External I/O or Memory READ and WRITE Timing—Extended Temperature

			T_A = –40ºC to +105ºC @ 12 MHz				
No	**Symbol**	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Units**	**Notes**
1	T_DA(AS)	Address Valid to $\overline{AS}$ Rise Delay	4.5V	35		ns	2
			5.5V	35		ns	2
2	T_DAS(A)	$\overline{AS}$ Rise to Address Float Delay	4.5V	45		ns	2
			5.5V	45		ns	2
3	T_DAS(DR)	$\overline{AS}$ Rise to Read Data Req'd Valid	4.5V		250	ns	2,3
			5.5V		250	ns	2
4	T_WAS	$\overline{AS}$ Low Width	4.5V	55		ns	2
			5.5V	55		ns	2
5	T_DAS(DS)	Address Float to $\overline{DS}$ Fall	4.5V	0		ns	
			5.5V	0		ns	
6	T_WDSR	$\overline{DS}$ (Read) Low Width	4.5V	200		ns	2,3
			5.5V	200		ns	2,3
7	T_WDSW	$\overline{DS}$ (WRITE) Low Width	4.5V	110		ns	2,3
			5.5V	110		ns	2,3
8	T_DDSR(DR)	$\overline{DS}$ Fall to Read Data Req'd Valid	4.5V		150	ns	2,3
			5.5V		150	ns	2,3
9	T_HDR(DS)	Read Data to $\overline{DS}$ Rise Hold Time	4.5V	0		ns	2
			5.5V	0		ns	2
10	T_DDS(A)	$\overline{DS}$ Rise to Address Active Delay	4.5V	45		ns	2
			5.5V	55		ns	2
11	T_DDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	4.5V	30		ns	2
			5.5V	45		ns	2

Notes:
1. E142/E143/E144/E145/E146 only; SCLK ÷ TCLK = Crystal ÷ 2.
2. The V_{CC} voltage specification of 4.5V guarantees 3.3V ± 0.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V.
3. Timing numbers provided are for minimum T_PC.

Table 57. External I/O or Memory READ and WRITE Timing—Extended Temperature (Continued)

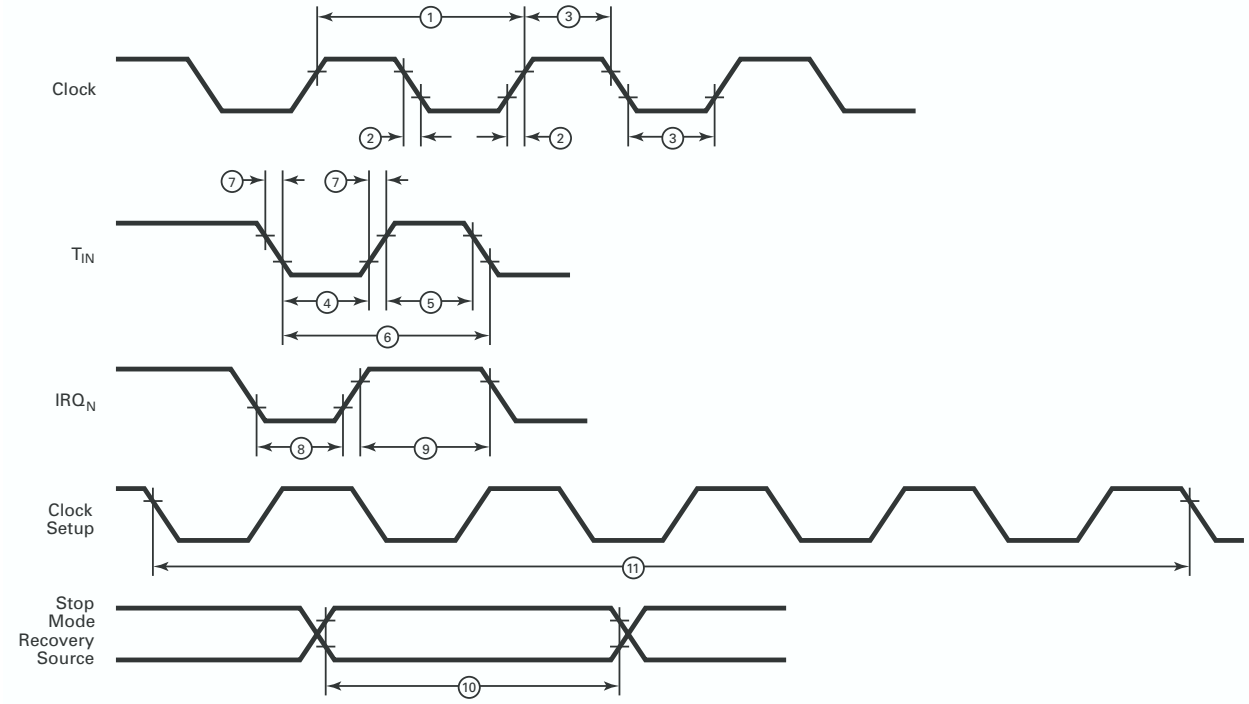
				T_A = –40ºC to +105ºC @ 12 MHz			
No	**Symbol**	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Units**	**Notes**
12	T_DR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay	4.5V	45		ns	2
			5.5V	45		ns	2
13	T_DDS(R/W)	$\overline{DS}$ Rise to R/$\overline{W}$ Not Valid	4.5V	45		ns	2
			5.5V	45		ns	2
14	T_DDW(DSW)	WRITE Data Valid to $\overline{DS}$ Fall (WRITE) Delay	4.5V	55		ns	2
			5.5V	55		ns	2
15	T_DDS(DW)	$\overline{DS}$ Rise to WRITE Data Not Valid Delay	4.5V	45		ns	2
			5.5V	45		ns	2
16	T_DA(DR)	Address Valid to Read Data Req'd Valid	4.5V		310	ns	2,3
			5.5V		310	ns	2,3
17	T_DAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay	4.5V	65		ns	2
			5.5V	65		ns	2
18	T_DDM(AS)	$\overline{DM}$ Valid to $\overline{AS}$ Fall Delay	4.5V	35		ns	2
			5.5V	35		ns	2
19	T_DDs(DM)	$\overline{DS}$ Rise to DM Valid Delay	4.5V	45		ns	2
			5.5V	45		ns	2
20	T_HDS(AS)	$\overline{DS}$ Valid to Address Valid Hold Time	4.5V	45		ns	2
			5.5V	45		ns	2

Notes:
1. E142/E143/E144/E145/E146 only; SCLK ÷ TCLK = Crystal ÷ 2.
2. The V_{CC} voltage specification of 4.5V guarantees 3.3V ± 0.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V.
3. Timing numbers provided are for minimum T_PC.

Additional Timing

Figure 26 illustrates the timing characteristics of the MUZE Family of parts with respect to system clock functions. See Tables 58 and 59 for descriptions of the numbered timing parameters in the figure.

Figure 26. Additional Timing



For the values in Table 58, SCLK ÷ TCLK = Crystal ÷ 2, within a standard temperature range of 0ºC to 70ºC.

Table 58. Additional Timing at Standard Temperature

				T_A = 0ºC to +70ºC						
				8 MHz		12 MHz				
No	Sym	Parameter	V_{CC}[1]	Min	Max	Min	Max	Units	Notes	D1,D0
1	T_PC	Input Clock Period	4.5V	250	DC	83	DC	ns	2,3,4	
			5.5V	250	DC	83	DC	ns	2,3,4	
			4.5V	125	DC	250	DC	ns	2,3	
			5.5V	125	DC	250	DC	ns	2,3	
2	T_RC, T_FC	Clock Input Rise & Fall Times	4.5V		25		15	ns	2,3	
			5.5V		25		15	ns	2,3	
3	T_WC	Input Clock Width	4.5V	125		41		ns	2,3,4	
			5.5V	125		41		ns	2,3,4	
			4.5V	62		125		ns	2,3	
			5.5V	62		125		ns	2,3	
4	$T_WT_{IN}L$	Timer Input Low Width	4.5V	100		100		ns	2,3	
			5.5V	70		70		ns	2,3	
5	$T_WT_{IN}H$	Timer Input High Width	4.5V	$3T_PC$		$5T_PC$			2,3	
			5.5V	$3T_PC$		$5T_PC$			2,3	
6	T_PT_{IN}	Timer Input Period	4.5V	$4T_PC$		$8T_PC$			2,3	
			5.5V	$4T_PC$		$8T_PC$			2,3	
7	T_RT_{IN}, T_FT_{IN}	Timer Input Rise & Fall Timer	4.5V		100		100	ns	2,3	
			5.5V		100		100	ns	2,3	

Notes:
1. The V_{CC} voltage specification of 4.5V guarantees 3.3V ±0.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
2. Timing reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
3. SMR: D1 = 0.
4. The maximum frequency for the external crystal clock is 4 MHz when using LOW-EMI OSCILLATOR mode.
5. The interrupt request via Port 3 (P31–P33).
6. The interrupt request via Port 3 (P30).
7. SMR: D5 = 1, and the POR Stop-Mode Delay is on.
8. For RC and LC oscillators, and for an oscillator driven by a clock driver.
9. The D1,D0 column applies to the Watch-Dog Timer Mode Register tap selection.
10. 12 µs is the typical delay time; only applies when SMR Register bit D5 is cleared to 0

Table 58. Additional Timing at Standard Temperature (Continued)

				T_A = 0ºC to +70ºC						
				8 MHz		12 MHz				
No	Sym	Parameter	V_{CC}[1]	Min	Max	Min	Max	Units	Notes	D1,D0
8A	T_WIL	Interrupt Request Low Time	4.5V	100		100		ns	2,3,5	
			5.5V	70		70		ns	2,3,5	
8B	T_WIL	Interrupt Request Low Time	4.5V	$3T_PC$		$5T_PC$			2,3,6	
			5.5V	$3T_PC$		$5T_PC$			2,3,6	
9	T_WIH	Interrupt Request Input High Time	4.5V	$3T_PC$		$5T_PC$			2,3,5	
			5.5V	$3T_PC$		$5T_PC$			2,3,5	
10	T_{WSM}	Stop-Mode Recovery Width Spec	4.5V	12		12		ns	7	
			5.5V	12		12		ns	7	
11	T_{OST}	Oscillator Startup Time	4.5V		$5T_PC$		$5T_PC$		7,8	
			5.5V		$5T_PC$		$5T_PC$		7,8	
12	T_{WDT}	Watch-Dog Timer Delay Timer before time-out	4.5V			7		ms	9	0,0
			5.5V			3.5		ms	9	0,0
			4.5V			14		ms	9	0,1
			5.5V			7		ms	9	0,1
			4.5V			28		ms	9	1,0
			5.5V			14		ms	9	1,0
			4.5V			112		ms	9	1,1
			5.5V			56		ms	9	1,1

Notes:
1. The V_{CC} voltage specification of 4.5V guarantees 3.3V ±0.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
2. Timing reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
3. SMR: D1 = 0.
4. The maximum frequency for the external crystal clock is 4 MHz when using LOW-EMI OSCILLATOR mode.
5. The interrupt request via Port 3 (P31–P33).
6. The interrupt request via Port 3 (P30).
7. SMR: D5 = 1, and the POR Stop-Mode Delay is on.
8. For RC and LC oscillators, and for an oscillator driven by a clock driver.
9. The D1,D0 column applies to the Watch-Dog Timer Mode Register tap selection.
10. 12 µs is the typical delay time; only applies when SMR Register bit D5 is cleared to 0

Table 58. Additional Timing at Standard Temperature (Continued)

				T_A = 0ºC to +70ºC						
				8 MHz		12 MHz				
No	Sym	Parameter	V_{CC}[1]	Min	Max	Min	Max	Units	Notes	D1,D0
13	T_{POR}	Power-On Reset Delay	4.5V			3	24	ms		
			5.5V			1.5	13	ms		
14	T_{EDELAY}	POR Delay Time	4.5V				35	µs	10	
			5.5V				35	µs	10	

Notes:
1. The V_{CC} voltage specification of 4.5V guarantees 3.3V ±0.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
2. Timing reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
3. SMR: D1 = 0.
4. The maximum frequency for the external crystal clock is 4 MHz when using LOW-EMI OSCILLATOR mode.
5. The interrupt request via Port 3 (P31–P33).
6. The interrupt request via Port 3 (P30).
7. SMR: D5 = 1, and the POR Stop-Mode Delay is on.
8. For RC and LC oscillators, and for an oscillator driven by a clock driver.
9. The D1,D0 column applies to the Watch-Dog Timer Mode Register tap selection.
10. 12 µs is the typical delay time; only applies when SMR Register bit D5 is cleared to 0

For the values in Table 59, SCLK ÷ TCLK = Crystal ÷ 2, within an extended temperature range of –40ºC to 105ºC.

Table 59. Additional Timing at Extended Temperature

				T_A = –40ºC to +105ºC						
				8 MHz		12 MHz				
No	Sym	Parameter	V_{CC}[1]	Min	Max	Min	Max	Units	Notes	D1,D0
1	T_PC	Input Clock Period	4.5V	250	DC	83	DC	ns	2,3,4	
			5.5V	250	DC	83	DC	ns	2,3,4	
			4.5V	125	DC	250	DC	ns	2,3	
			5.5V	125	DC	250	DC	ns	2,3	
2	T_RC, T_FC	Clock Input Rise & Fall Times	4.5V		25		15	ns	2,3	
			5.5V		25		15	ns	2,3	
3	T_WC	Input Clock Width	4.5V	125		41		ns	2,3,4	
			5.5V	125		41		ns	2,3,4	
			4.5V	62		125		ns	2,3	
			5.5V	62		125		ns	2,3	
4	$T_WT_{IN}L$	Timer Input Low Width	4.5V	100		100		ns	2,3	
			5.5V	70		70		ns	2,3	
5	$T_WT_{IN}H$	Timer Input High Width	4.5V	$3T_PC$		$5T_PC$			2,3	
			5.5V	$3T_PC$		$5T_PC$			2,3	
6	T_PT_{IN}	Timer Input Period	4.5V	$4T_PC$		$8T_PC$			2,3	
			5.5V	$4T_PC$		$8T_PC$			2,3	
7	T_RT_{IN}, T_FT_{IN}	Timer Input Rise & Fall Timer	4.5V		100		100	ns	2,3	
			5.5V		100		100	ns	2,3	

Notes:
1. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
2. The timing reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
3. SMR: D1 = 0.
4. The maximum frequency for the external crystal clock is 4 MHz when using LOW-EMI OSCILLATOR mode.
5. The interrupt request via Port 3 (P31–P33).
6. The interrupt request via Port 3 (P30).
7. SMR: D5 = 1, and the POR Stop-Mode Delay is on.
8. For RC and LC oscillators, and for an oscillator driven by a clock driver.
9. The D1,D0 column applies to the Watch-Dog Timer Mode Register tap selection.
10. 12 µs is the typical delay time.

Table 59. Additional Timing at Extended Temperature (Continued)

				T_A = –40ºC to +105ºC						
				8 MHz		12 MHz				
No	Sym	Parameter	V_{CC}[1]	Min	Max	Min	Max	Units	Notes	D1,D0
8A	T_WIL	Interrupt Request Low Time	4.5V	100		100		ns	2,3,5	
			5.5V	70		70		ns	2,3,5	
8B	T_WIL	Interrupt Request Low Time	4.5V	$3T_PC$		$5T_PC$			2,3,6	
			5.5V	$3T_PC$		$5T_PC$			2,3,6	
9	T_WIH	Interrupt Request Input High Time	4.5V	$3T_PC$		$5T_PC$			2,3,5	
			5.5V	$2T_PC$		$5T_PC$			2,3,5	
10	T_{WSM}	Stop-Mode Recovery Width Spec	4.5V	12		12		ns	7	
			5.5V	12		12		ns	7	
11	T_{OST}	Oscillator Startup Time	4.5V		$5T_PC$		$5T_PC$		7,8	
			5.5V		$5T_PC$		$5T_PC$		7,8	
12	T_{WDT}	Watch-Dog Timer Delay Timer before time-out	4.5V			7		ms	9	0,0
			5.5V			3.5		ms	9	0,0
			4.5V			14		ms	9	0,1
			5.5V			7		ms	9	0,1
			4.5V			28		ms	9	1,0
			5.5V			14		ms	9	1,0
			4.5V			112		ms	9	1,1
			5.5V			56		ms	9	1,1
13	T_{POR}	Power-On Reset Delay	4.5V			3	25	ms		
			5.5V			1	14	ms		

Notes:
1. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
2. The timing reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
3. SMR: D1 = 0.
4. The maximum frequency for the external crystal clock is 4 MHz when using LOW-EMI OSCILLATOR mode.
5. The interrupt request via Port 3 (P31–P33).
6. The interrupt request via Port 3 (P30).
7. SMR: D5 = 1, and the POR Stop-Mode Delay is on.
8. For RC and LC oscillators, and for an oscillator driven by a clock driver.
9. The D1,D0 column applies to the Watch-Dog Timer Mode Register tap selection.
10. 12 µs is the typical delay time.

Table 59. Additional Timing at Extended Temperature (Continued)

				T_A = –40ºC to +105ºC						
				8 MHz		12 MHz				
No	Sym	Parameter	V_{CC}[1]	Min	Max	Min	Max	Units	Notes	D1,D0
14	T_{EDELAY}	POR Delay Time	4.5V				35	µs	10	
			5.5V				35	µs	10	

Notes:
1. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
2. The timing reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
3. SMR: D1 = 0.
4. The maximum frequency for the external crystal clock is 4 MHz when using LOW-EMI OSCILLATOR mode.
5. The interrupt request via Port 3 (P31–P33).
6. The interrupt request via Port 3 (P30).
7. SMR: D5 = 1, and the POR Stop-Mode Delay is on.
8. For RC and LC oscillators, and for an oscillator driven by a clock driver.
9. The D1,D0 column applies to the Watch-Dog Timer Mode Register tap selection.
10. 12 µs is the typical delay time.

Figure 27. Input Handshake Timing

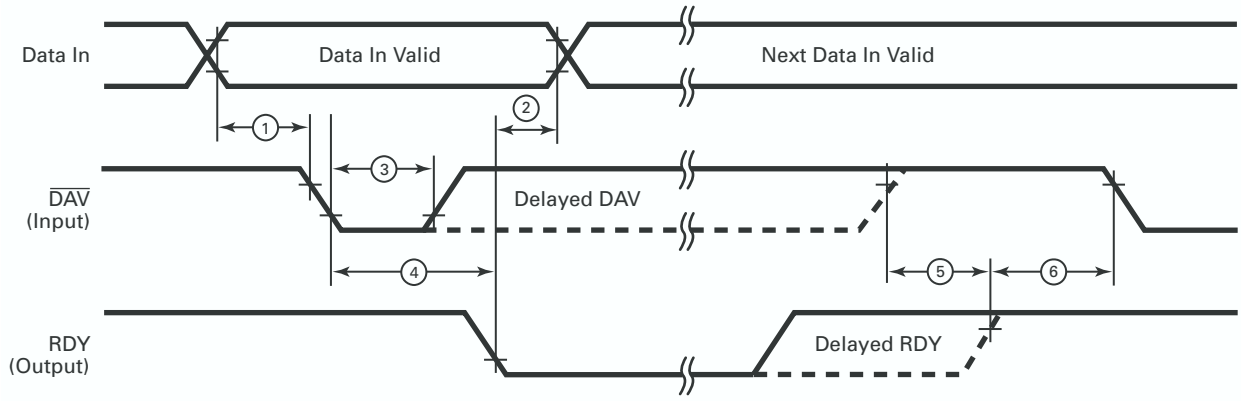


Figure 28. Output Handshake Timing

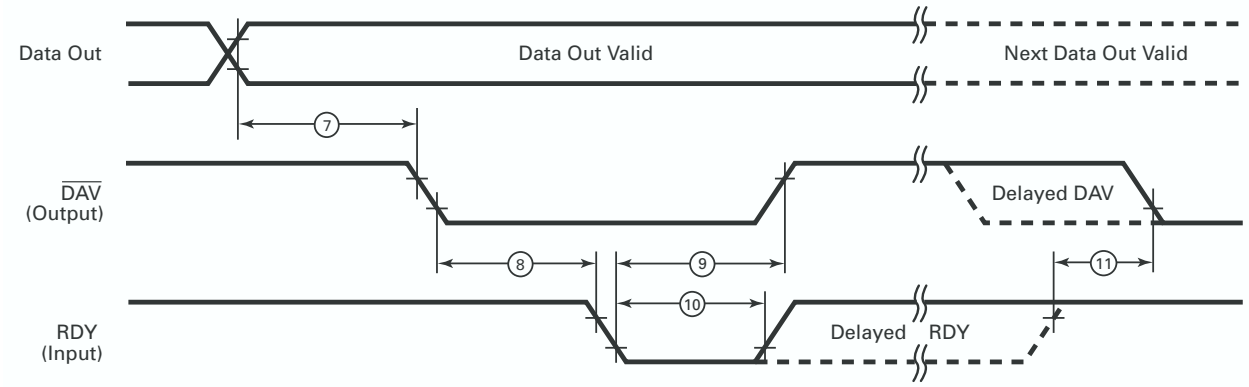


Table 60. Handshake Timing[1] at Standard Temperature

No	Symbol	Parameter	V_{CC}[2]	12 MHz Min	12 MHz Max	Units	Data Direction
1	T_SDI(DAV)	Data In Setup Time	4.5V	0		ns	Input
			5.5V	0		ns	Input
2	T_HDI(RDY)	Data In Hold Time	4.5V	0		ns	Input
			5.5V	0		ns	Input
3	T_WDAV	Data Available Width	4.5V	155		ns	Input
			5.5V	110		ns	Input
4	T_DDAVI(RDY)	DAV Fall to RDY Fall Delay	4.5V		0	ns	Input
			5.5V		0	ns	Input
5	T_DDAVId(RDY)	DAV Out to DAV Fall Delay	4.5V		120	ns	Input
			5.5V		80	ns	Input
6	RDY0$_D$(DAV)	RDY Rise to DAV Fall Delay	4.5V	0		ns	Input
			5.5V	0		ns	Input
7	T_DD0(DAV)	Data Out to DAV Fall Delay	4.5V	42		ns	Output
			5.5V	42		ns	Output
8	T_DDAV0(RDY)	DAV Fall to RDY Fall Delay	4.5V	0		ns	Output
			5.5V	0		ns	Output

Notes:
1. The Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.

Table 60. Handshake Timing[1] at Standard Temperature (Continued)

No	Symbol	Parameter	V_{CC}[2]	12 MHz Min	12 MHz Max	Units	Data Direction
9	T_DRDY0(DAV)	RDY Fall to DAV Rise Delay	4.5V		160	ns	Output
			5.5V		115	ns	Output
10	T_WRDY	RDY Width	4.5V	110		ns	Output
			5.5V	80		ns	Output
11	T_DRDY0$_D$(DAV)	RDY Rise to DAV Fall Delay	4.5V		110	ns	Output
			5.5V		80	ns	Output

Notes:
1. The Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.

Table 61. Handshake Timing[1] at Extended Temperature

No	Symbol	Parameter	V_{CC}[2]	12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	Units	Data Direction
1	T_SDI(DAV)	Data In Setup Time	4.5V	0		0		ns	Input
			5.5V	0		0		ns	Input
2	T_HDI(RDY)	Data In Hold Time	4.5V	0		0		ns	Input
			5.5V	0		0		ns	Input
3	T_WDAV	Data Available Width	4.5V	155		155		ns	Input
			5.5V	110		110		ns	Input
4	T_DDAVI(RDY)	DAV Fall to RDY Fall Delay	4.5V		0		0	ns	Input
			5.5V		0		0	ns	Input
5	T_DDAVId(RDY)	DAV Out to DAV Fall Delay	4.5V		120		120	ns	Input
			5.5V		80		80	ns	Input
6	RDY0$_D$(DAV)	RDY Rise to DAV Fall Delay	4.5V	0		0		ns	Input
			5.5V	0		0		ns	Input
7	T_DD0(DAV)	Data Out to DAV Fall Delay	4.5V	42		31		ns	Output
			5.5V	42		31		ns	Output

Notes:
1. The Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.

Table 61. Handshake Timing[1] at Extended Temperature (Continued)

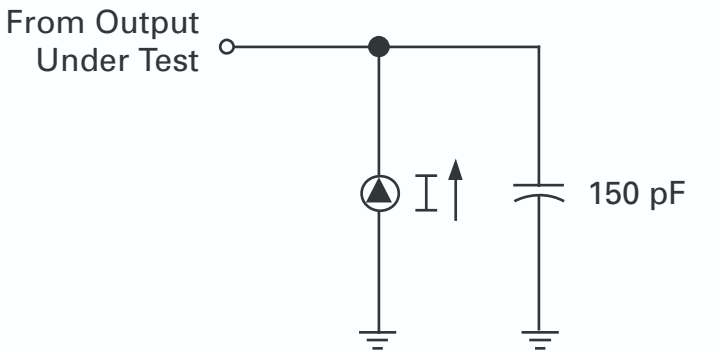
No	Symbol	Parameter	V_{CC}[2]	12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	Units	Data Direction
8	T_DDAV0(RDY)	DAV Fall to RDY Fall Delay	4.5V	0		0		ns	Output
			5.5V	0		0		ns	Output
9	T_DRDY0(DAV)	RDY Fall to DAV Rise Delay	4.5V		160		160	ns	Output
			5.5V		115		115	ns	Output
10	T_WRDY	RDY Width	4.5V	110		110		ns	Output
			5.5V	80		80		ns	Output
11	T_DRDY0$_D$(DAV)	RDY Rise to DAV Fall Delay	4.5V		110		110	ns	Output
			5.5V		80		80	ns	Output

Notes:
1. The Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.

Standard Test Conditions

The characteristics listed in following pages apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 29.)

Figure 29. Test Load Diagram



Capacitance

Table 62. Capacitance*

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

Note: *T_A = 25ºC, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins to GND.

One-Time Programming

Table 63 briefly describes the MUZE Family OTP option bit selection at each bit's default value before programming.

Table 63. Option Bit Description*

Bit	Option	Unprogrammed Default Value
0	EPROM Protect	Disabled
1	RAM Protect	Disabled
2	Autolatches	Enabled
3	P0 Pull-Ups	Disabled
4	P1 Pull-Ups	Disabled
5	P2 Pull-Ups	Disabled
6	RC Oscillator	Disabled
7	32-kHz Oscillator	Disabled
8	Permanent WDT	Disabled
9	VBO	Enabled
10	Reserved	Must not be changed
11	Reserved	Must not be changed
12	Reserved	Must not be changed
13	Reserved	Must not be changed
14	Reserved	Must not be changed
15	Reserved	Must not be changed

Note: *Option bits are 0 when unprogrammed and are 1 when programmed. If bits are not to be programmed, use 0.

EPROM Protect. Selecting the DISABLE EPROM PROTECT option, bit 0, allows the software program that is in the program memory to be read using ZiLOG's internal factory test mode. Selecting the ENABLE EPROM PROTECT option negates the possibility of reading the code out of the part using a tester, programmer, or any other standard method.

The EPROM PROTECT option bit only affects the part's ability to read from an external source and does not affect the operation of the part in an application.

RAM Protect. Selecting the DISABLE RAM PROTECT option, bit 1, does not affect the RAM memory. RAM memory operates as defined in this Product Specification for all address locations. Selecting the ENABLE RAM PROTECT option, allows protection (under software control) of a portion of the RAM's address space from being read or written.

AUTOLATCH Mode. Selecting the DISABLE AUTOLATCHES option, bit 2, disables the autolatches on the Port pins. These pins float, rather than are pulled, to a valid CMOS level when they are inputs and not connected to an external signal. Selecting the ENABLE AUTOLATCHES option enables the autolatches on the Port pins and pulls the pins to a valid CMOS level when they are not connected to an external signal.

Port 0 Pull-Ups. Selecting DISABLE PULL-UPS option, bit 3, disables the input pull-up circuitry on all Port 0 pins. Selecting ENABLE PULL-UPS enables the input pull-up circuitry on all Port 0 pins. This option bit does not affect any of the other port pins on the part.

Port 1 Pull-Ups. Selecting DISABLE PULL-UPS option, bit 4, disables the input pull-up circuitry on all Port 1 pins. Selecting ENABLE PULL-UPS enables the input pull-up circuitry on all Port 1 pins. This option bit does not affect any of the other port pins on the part.

Port 2 Pull-Ups. Selecting DISABLE PULL-UPS option, bit 5, disables the input pull-up circuitry on all Port 2 pins. Selecting ENABLE PULL-UPS enables the input pull-up circuitry on all Port 2 pins. This option bit does not affect any of the other port pins on the part.

System Clock Source. Selecting the RC OSCILLATOR ENABLE option, bit 6, configures the oscillator circuit on the microcontroller to work with an external RC circuit. Selecting the CRYSTAL/OTHER CLOCK SOURCE option configures the oscillator circuit to work with an external crystal, ceramic resonator, or LC oscillator.

Oscillator Operational Mode. Selecting the NORMAL HIGH FREQUENCY OPERATION ENABLED option, bit 7, enables the part to operate using a standard crystal or resonator, but it does not operate using a 32-kHz crystal. Selecting the 32-KHZ OPERATION ENABLED option enables the microcontroller to work with a 32-kHz crystal and an external feedback resistor—these 2 items must be supplied between the X_{IN} and X_{OUT} pins. (If RC OSCILLATOR ENABLED is selected in the SYSTEM CLOCK SOURCE option, this option defaults to the NORMAL HIGH FREQUENCY OPERATION ENABLED bit.)

WDT Mode. Selecting the WDT ENABLED BY SOFTWARE ONLY option, bit 8, operates the Watch-Dog Timer (WDT) when turned on under software control. Selecting the WDT ENABLED AUTOMATICALLY AFTER RESET option starts the WDT automatically at RESET.There is no way to disable or stop this mode, making it necessary in the code to periodically clear the WDT to prevent it from resetting the microcontroller. If the WDT ENABLED AUTOMATICALLY AFTER RESET option and the WDT DRIVEN BY SYSTEM CLOCK option (if offered) are selected, the WDT *never* operates in STOP mode, and cannot be enabled, by any means, to operate in STOP mode.

VBO. Selecting the VBO option, bit 9, enables low-voltage protection circuitry. The device resets if V_{CC} goes below V_{LV} when VBO is selected. If it is disabled, the device does not reset if V_{CC} falls below V_{LV}. See Low-Voltage Protection for more details.

The remainder of the OTP options, bits 10–15, are reserved by ZiLOG and must not be changed from their default values.

Universal Asynchronous Receiver/Transmitter

ASCI Key Features

Key features of the UART Asynchronous Serial Communications Interface (ASCI) include:

- Full-duplex operation
- Programmable data format
- 7 or 8 data bits with optional ninth bit for multiprocessor communication
- P30 and P37 are used as general-purpose I/O as long as the ASCI channels are disabled
- One or two STOP bits
- Odd, even or no parity
- Programmable interrupt conditions
- Four level data/status FIFOs for the receiver
- Receive parity, framing and overrun error detection
- Break detection and generation

Transmit Data Register. Data written to the ASCI Transmit Data Register (TDR) is transferred to the Transmit Shift Register (TSR) as soon as the TSR is empty. Data is written while the TSR shifts the previous byte of data, thereby providing a double buffer for the transmit data. The TDR is READ- and WRITE-accessible. Reading from the TDR does not affect the ASCI data transmit operation currently in progress.

Transmit Shift Register. When the Transmit Shift Register (TSR) receives data from the ASCI Transmit Data Register, the data shifts to the TX (P37) pin. When transmission is completed, the next byte, if available, is automatically loaded from the TDR into the TSR. The next transmission then starts. If no data is available for transmission, the TSR idles at a continuous High level. This register is not program-accessible.

Receive Shift Register. When the Receive Enable (RE) bit is set in the CNTLA register, the RX (P30) pin is monitored for a Low. One-half bit-time after a Low is sensed at RX, the ASCI samples RX again. If RX goes back to High, the ASCI ignores the previous Low and resumes looking for a new Low. However, if RX is still Low, it considers RX a START bit and proceeds to clock in the data based upon the selected baud rate. The number of data bits, parity, multiprocessor and STOP bits are selected by the MOD2, MOD1, MOD0 and MULTIPROCESSOR mode (MP) bits in the CNTLA and CNTLB registers.

After the data is received, the appropriate MP, parity and STOP bits are checked. Data and any errors are clocked into the receive data and status FIFO during the STOP bit if there is an empty position available. Interrupts and Receive Data Register Full Flag also goes active during this time. If there is no space in the FIFO at the time that the RSR attempts to transfer the received data into it, an overrun error occurs.

Receive Data FIFO. When a complete incoming data byte is assembled in the RSR, it is automatically transferred to the 4-byte FIFO, which serves to reduce the incidence of overrun errors. The top (oldest) character in the FIFO (if any) is read via the Receive Data Register (RDR).

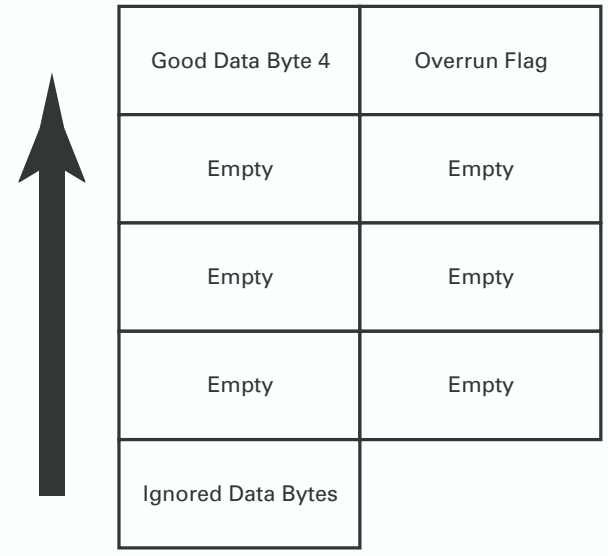
Figure 30. Receive Data Register FIFO

The next incoming data byte can shift into the RSR while the FIFO is full, thus providing an additional level of buffering. However, an overrun occurs if the receive FIFO is still full when the receiver completes assembly of that character and is ready to transfer it to the FIFO. If this situation occurs, the overrun error bit is set in the previous byte of the FIFO stack.

Figure 31. FIFO Overrun Example

The latest data byte is not transferred from the shift register to the FIFO in this case, and is lost. When an overrun occurs, the receiver does not place any further data in the FIFO until the most recent good byte received arrives at the top of the FIFO and sets the Overrun latch, and software then clears the Overrun latch by a WRITE of 0 to the EFR bit.

Figure 32. Clear FIFO Overrun Example



Assembly of bytes continues in the shift register, but this data is ignored until the byte with the overrun error reaches the top of the FIFO and the status is cleared.

When a break occurs (defined as a framing error with the data equal to all zeros), the all-zero byte, with its associated error bits, are transferred to the FIFO if it is not full. As a result, the Break Detect bit (bit 1) is set in the ASEXT register. If the FIFO is full, an overrun is generated, but the break, framing error and data are not transferred to the FIFO. Any time a break is detected, the receiver does not receive any more data until the RX pin returns to a high state.

If the channel is set in MULTIPROCESSOR mode and the MPE bit (bit 7) of the CNTLA register is set to 1, then break, errors and data are ignored unless the MP bit in the received character is 1. The two conditions listed above could cause the missing of a break condition if the FIFO is full and the break occurs or if the MP bit in the transmission is not a one with the conditions specified above.

ASCI Status FIFO/Registers This FIFO contains Parity Error, Framing Error, RX Overrun, and Break status bits associated with each character in the receive data FIFO. The status of the oldest character (if any) is read from the ASCI status register, which also provides several other, non-FIFOed status conditions.

The outputs of the error FIFO set the inputs of the software-accessible error latches in the status register. Writing a 0 to the EFR bit (bit 3) in CNTLA is the only way to clear these latches. In other words, when an error bit reaches the top of the FIFO, it sets an error latch. If the FIFO contains more data and the software reads the next byte out of the FIFO, the error latch remains set until the software writes a 0 to the EFR bit. The error bits are cumulative, so if additional errors are in the FIFO they set any unset error latches as they reach the top.

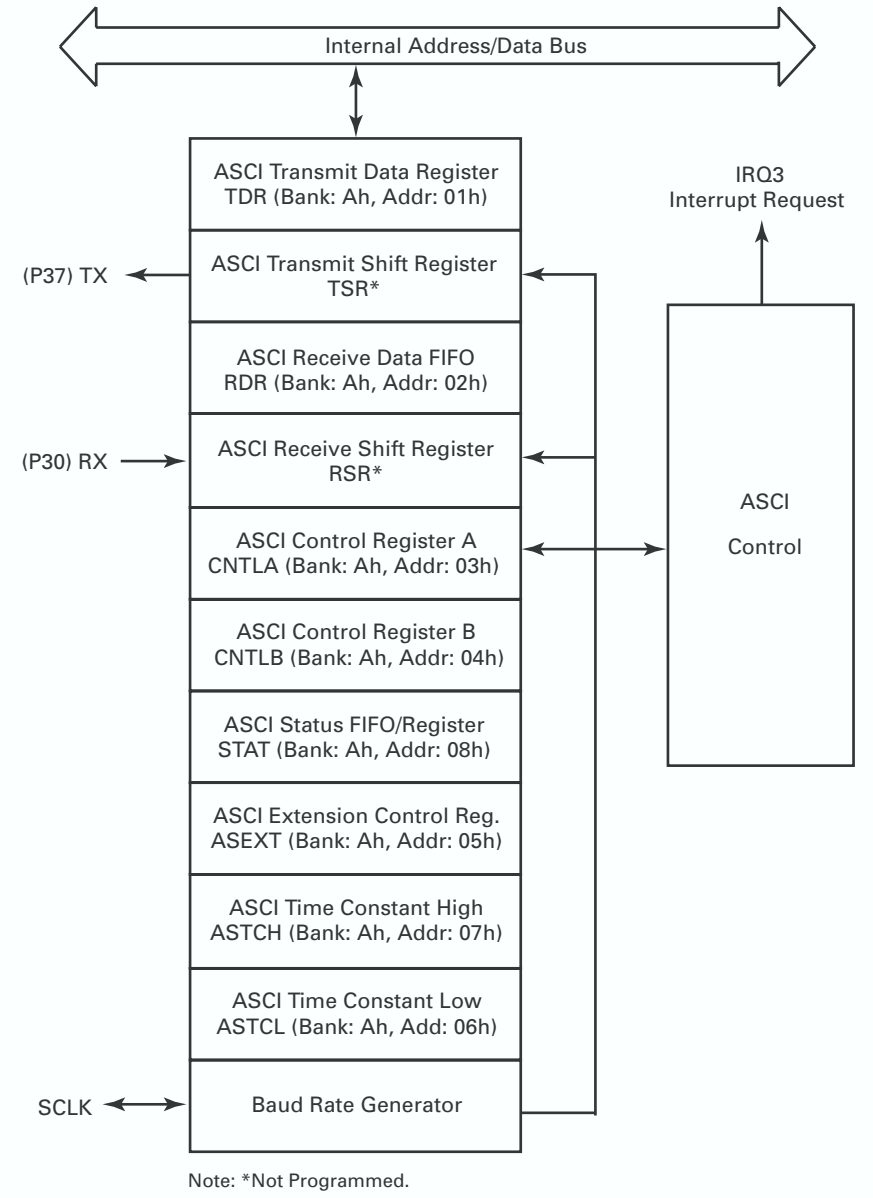
Baud Rate Generator (BRG) The baud rate generator features two modes. The first provides a dual set of fixed clock divide ratios as defined in CNTLB. In the second mode, the BRG is configured as a sixteen-bit down counter that divides the processor clock by the value in a software accessible, sixteen-bit, time-constant register. As a result, virtually any frequency is created by appropriately selecting the main processor clock frequency. The BRG can also be disabled in favor of the SCLK.

The Receiver and Transmitter subsequently divide the output of the Baud rate Generator (or the signal from the CLK pin) by 1, 16 or 64 under the control of the DR bit (bit 3) in the CNTLB register and the X1 bit in the ASCI Extension Control Register (ASEXT).

ResetDuring RESET, the ASCI is forced to the following conditions:

- FIFO Empty
- All Error Bits Cleared (including those in the FIFO)
- Receive Enable Cleared (CNTLA Bit 6 = 0)
- Transmit Enable Cleared (CNTLA Bit 5 = 0)

Figure 33. ASCI Interface Diagram

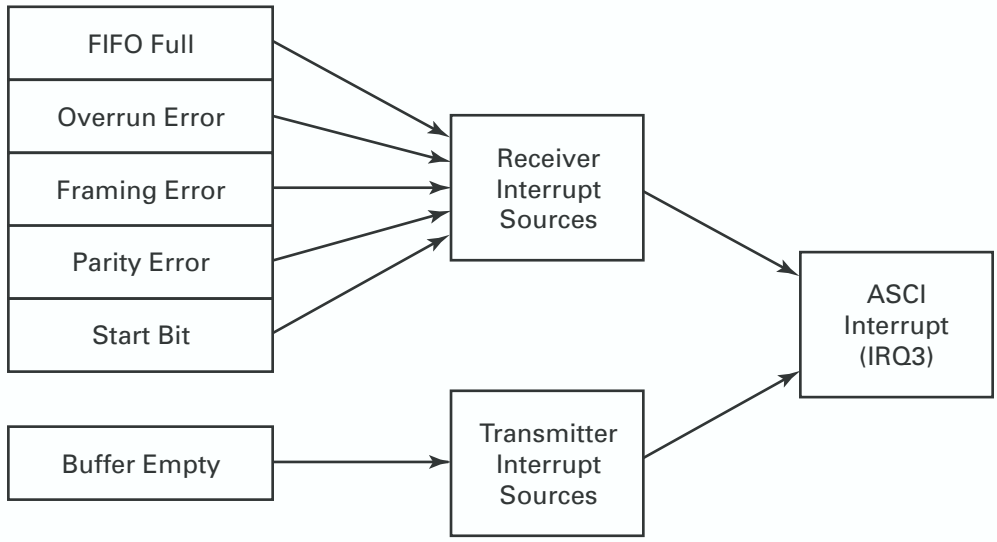


Note: *Not Programmed.

ASCI Interrupts

The ASCI channel generates one interrupt, IRQ3, from two sources of interrupts: a receiver and a transmitter. In addition, there are several conditions that may cause these interrupts to trigger. Figure 64 illustrates the different conditions for each interrupt source enabled under program control.

Table 64. ASCI Interrupt Conditions and Sources



ASCI Transmit Data Register

Data written to the ASCI Transmit Data Register (TDR) is transferred to the Transmit Shift Register (TSR) as soon as the TSR is empty. The TSR is not software-accessible. The ASCI transmitter is double-buffered so data can be written to the TDR while the TSR is shifting out the previous byte. Data can be written into and read out of the TDR. When the TDR is read, the data transmit operation is not affected.

READ/WRITE and reset states for bits D7–D0 of the TDR are listed in Table 65.

Table 65. Transmit Data Register—TDR 01h/R1 Bank Ah: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	X	X	X	X	X	X	X	X
Note: R = Read, W = Write, X = Indeterminate.								

Bit/ Field	Bit Position	R/W	State	Description
D7–D0	TDR	R/W	X	Transmit Data Register

ASCI Receive Data Register

When a complete incoming data byte is assembled in the Receive Shift Register (RSR), it is automatically transferred to the highest available location in the

Receive Data FIFO. The Receive Data Register (RDR) is the highest location in the Receive Data FIFO. The Receive Data Register Not Empty bit (RDRNE—bit 7) in the STAT register is set when one or more bytes is available from the FIFO. The FIFO status for the character in the RDR is available in the STAT register via bits 6, 5 and 4. STAT should be read before reading the RDR. The data in both FIFO locations is *popped* when the character is read from the RDR.

READ/WRITE and reset states for bits D7–D0 of the RDR are listed in Table 66.

Table 66. Receive Data Register—RDR 02h/R2 Bank Ah: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	X	X	X	X	X	X	X	X
Note: R = Read, W = Write, X = Indeterminate.								

Bit/ Field	Bit Position	R/W	State	Description
D7–D0	RDR	R/W	X	Receive Data Register

ASCI Control Register A

ASCI Control Register A, CNTLA, controls data transmit, receive, and clocking functions. READ/WRITE and reset states for bits D7–D0 are listed in Table 67.

Table 67. Control Register A—CNTLA 03h/R3 Bank Ah: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	1	0	0	0	0
Note: R = Read, W = Write, X = Indeterminate.								

Bit/Field	Bit Position	R/W	State	Description
D7	MPE	R/W	0	**Multiprocessor Enable** 0: Receive all bytes 1: Filter bytes with MPB = 0
D6	RE	R/W	0	**Receiver Enable** 0: ASCI Receiver Disabled (P30 = Input) 1: ASCI Receiver Enabled (P30 = RX)

Bit/Field	Bit Position	R/W	State	Description
D5	TE	R/W	0	**Transmitter Enable** 0: ASCI Transmitter Disabled (P37 = Output) 1: ASCI Transmitter Enabled (P37 = TX)
D4	Reserved	R/W	1	Reserved
D3	MPBR	R	0	Multiprocessor Bit Received
	EFR	W	0	**Error Flag Reset** 0: Clear Error Latches 1: No Effect
D2–D0	MOD2–0	R	0	**MOD2—Number of Data Bits** 0: 7 Data Bits 1: 8 Data Bits
				MOD1—Parity Enabled 0: No Parity 1: With Parity
				MOD0—Number of Stop Bits 0: 1 Stop Bit 1: 2 Stop Bits

Multiprocessor Enable. The ASCI features a multiprocessor communication mode that utilizes an extra data bit for selective communication when a number of processors share a common serial bus. Multiprocessor data format is selected when the MP in the corresponding register is set to 1. If MULTIPROCESSOR mode is not selected (MP bit in CNTLB = 0), MULTIPROCESSOR ENABLE (MPE, bit 7) exhibits no effect. If MULTIPROCESSOR mode is selected (MPE bit in CNTLB = 1), MPE enables or disables the *wake-up* feature as follows. If MPE is set to 1, only received bytes in which the multiprocessor bit (MPB) = 1 are treated as valid data characters and loaded into the receiver FIFO with corresponding error flags in the status FIFO. Bytes with MPB = 0 are ignored by the ASCI. If MPE is reset to 0, all bytes are received by the ASCI, regardless of the state of the MPB data bit.

Receiver Enable. When Receiver Enable (RE, bit 6) is set to 1, the ASCI receiver is enabled. When RE is reset to 0, the receiver is disabled and any receive operation in progress is aborted. However, the previous contents of the receiver data and status FIFO are not affected.

Transmitter Enable. When Transmitter Enable (TE, bit 5) is set to 1, the ASCI transmitter is enabled. When TE is reset to 0, the transmitter is disabled and any transmit operation in progress is aborted. However, the previous contents of the

transmitter data register and the TDRE flag (bit 1 of the STAT register) are not affected.

Bit 4 is reserved.

Multiprocessor Bit Receive. When MULTIPROCESSOR mode is enabled (MP in CNTLB = 1), this READ-ONLY bit, when read, contains the value of the MPB bit for the data byte currently available at the Receive Data Register (the *top* of the receiver FIFO). The Multiprocessor Bit Receive bit, MPBR, is bit 3.

Error Flag Reset. When the WRITE-ONLY Error Flag Reset (EFR), bit 3, is written to 0, the error flags (OVRN, FE; PE in STAT and BRK in ASEXT) are cleared to 0. This command self-resets, and as a result, writing EFR to a 1 is not required.

ASCI Data Format Mode. Bits 2–0 program the ASCI data format, as indicated in Table 68.

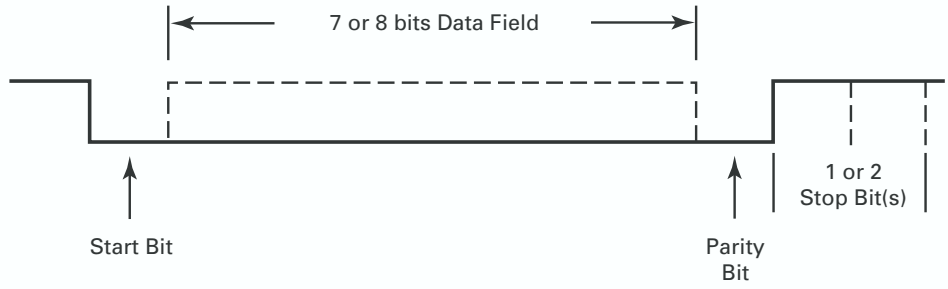
Table 68. ASCI Data Format Mode Control Bits

Bit	Name	Function	Bit = 0	Bit = 1
2	MOD2	Number of Data Bits	7	8
1	MOD1	Parity Enabled	No Parity	With Parity
0	MOD0	Number of Stop Bits	1	2

If MOD1 = 1, parity is checked on received data and a parity bit is appended to the data bits in the transmitted data. Parity Even/Odd (PEO) in CNTLB selects even or odd parity.

The ASCI serial data format is illustrated in Figure 34.

Figure 34. ASCI Serial Data Format



ASCI Control Register B

Control Register B, CNTLB, controls multiprocessor, parity, and clock sourcing functions. READ/WRITE and reset states for bits D7–D0 are listed in Table 69.

Table 69. Control Register B—CNTLB 04h/R4 Bank Ah: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	1	1	1
Note: R = Read, W = Write, X = Indeterminate.								

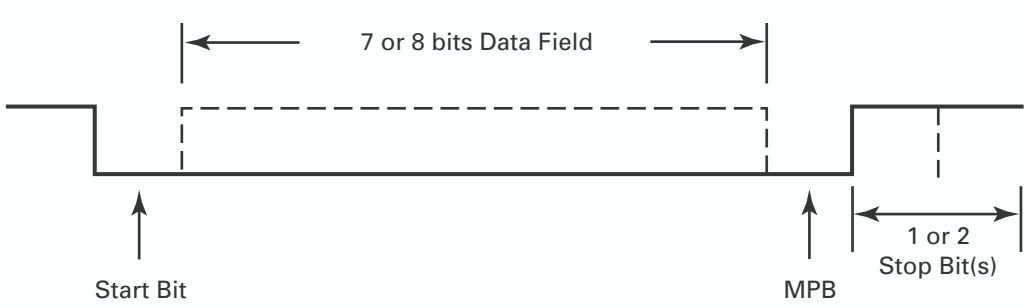
Bit/ Field	Bit Position	R/W	State	Description
D7	MPBT	R/W	0	**Multiprocessor Bit Transmitter** 0: Transmit 0 in MPB 1: Transmit 1 in MPB
D6	MP	R/W	0	**Multiprocessor Mode** 0: MULTIPROCESSOR mode disabled 1: MULTIPROCESSOR mode enabled (no parity)
D5	PR	W	0	**Prescale** 0: BRG ÷ 10 1: BRG ÷ 30
D4	PEO	R/W	0	**Parity Even/Odd** 0: Even Parity 1: Odd Parity
D3	DR	R/W	0	**Divide Ratio** 0: Divide by 16 1: Divide by 64
D2	SS2	R	1	**Clock Source and Speed Bits—**SS2 0: ÷1, ÷2, ÷4, ÷8 1: ÷16, ÷32, ÷64, Reserved
D1	SS1	R	1	**Clock Source and Speed Bits—**SS1 0: ÷1, ÷2, ÷16, ÷32 1: ÷4, ÷8, ÷64, Reserved
D0	SS0	R	1	**Clock Source and Speed Bits—**SS0 0: ÷1, ÷4, ÷16, ÷64 1: ÷2, ÷8, ÷32, Reserved

Multiprocessor Bit Transmit. When multiprocessor format is selected (MP bit = 1), Multiprocessor Bit Transmit (MPBT, bit 7) is used to specify the MPB data bit for transmission. If MPBT = 1, then a 1 is transmitted in the MPB bit position. If MPBT = 0, a 0 is transmitted.

MULTIPROCESSOR Mode. When MULTIPROCESSOR mode is set to 1, the serial data format is configured for MULTIPROCESSOR mode (MP, bit 6), adding a bit position whose value is specified in MPBT immediately after the specified number of data bits and preceding the specified number of STOP bits.

Note: The multiprocessor format does not provide parity. The serial data format while in MP mode is illustrated in Figure 35.

Figure 35. Multiprocessor Mode Serial Data Format



If MP = 0, the data format is based on MOD2–0 in CNTLA and may include parity.

BRG Prescaler. The Prescale bit specifies the baud rate generator (BRG, bit 5) prescale factor when using the SS2–0 bits to define the ASCI baud rate (BRG mode = 0). Writing a 0 to this bit sets the BRG Prescaler to divide by 10. Setting this bit to a 1 sets the BRG Prescaler to divide by 30. See the Baud Rate Generation Summary for more information on setting the ASCI baud rate.

Parity Even/Odd. Parity Even/Odd (PEO, bit 4) controls the parity bit transmitted on the serial output and the parity check on the serial input. If PEO is cleared to 0, even parity is transmitted and checked. If PEO is set to 1, odd parity is transmitted and checked.

Divide Ratio. The Divide Ratio bit (DR, bit 3) specifies the divider used to obtain the baud rate from the data sampling clock when using the SS2–0 bits to define the ASCI baud rate (BRG mode = 0). If DR is 0, then DIVIDE-BY-16 is used. If DR is set to 1, then DIVIDE-BY-64 is used. See the Baud Rate Generation Summary for more information on setting the ASCI baud rate.

DR	Sampling Clock
0	Divide by 16
1	Divide by 64

Clock Source and Speed Select. When the BRG mode bit (bit 3) in the ASEXT register is set to 0, these 3 bits, along with DR and PR in this register define the ASCI baud rate. Bits 2, 1 and 0 specify a power-of-two divider of the SCLK as defined in Table 70. These bits should never be set to all 1s or erratic results may occur. See the Baud Rate Generation Summary for more information on setting the ASCI baud rate.

Table 70. Clock Source and Speed Bits

SS2	SS1	SS0	Divider (DIV)
0	0	0	÷1
0	0	1	÷2
0	1	0	÷4
0	1	1	÷8
1	0	0	÷16
1	0	1	÷32
1	1	0	÷64
1	1	1	Reserved

ASCI Extension Control Register

Following are the bit functions for the ASCI Extension Control Register (ASEXT).

Table 71. Extension Control Register—ASEXT 05h/R5 Bank Ah: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	R/W	R/W	R/W	R/W	R/W	R	R/W
Reset	P30	0	0	0	0	0	0	0
Note: R = Read, W = Write, X = Indeterminate.								

Bit/ Field	Bit Position	R/W	State	Description
D7	RX	R	P30	RX Data State
D6	Reserved	R/W	0	Reserved
D5	Reserved	R/W	0	Reserved

D4	Reserved	R/W	0	Reserved (must be 0)
D3	BRG	R/W	0	**Baud Rate Generator Mode** 0: Use SS Selection 1: Use ASTH or ASTL Value
D2	RIS	R/W	0	**RX Interrupt on Start Bit** 0: No IRQ on Start Bit 1: IRQ3 on Start Bit
D1	BD	R	0	**Break Detect** 0: Valid Data Byte 1: Break Detected
D0	SB	R/W	0	**Send Break** 0: Normal Operation 1: Send Break

RX State. This bit provides the real-time state of the channel's receive data input pin (RX, bit 7), which is P30.

Reserved bits 6, 5, and 4. When read, bits 6 and 5 reflect the default value 0. When written, these bits are ignored. Bit 4 must be set to 0 or erratic results may occur.

BRG Mode. When the Baud Rate Generator (BRG, bit 3) bit is set to 1, the ASCI's baud rate is set by the 16-bit programmable divider programmed in ASCI Time Constant High (ASTH) and ASCI Time Constant Low (ASTL). If this bit is set to 0, the baud rate is defined by the PR bit, the DR bit, and the SS2–0 bits in the CNTLB register. In either case, the source for the baud rate generator is the SCLK. See the Baud Rate Generation Summary for more information on setting the ASCI baud rate.

RX Interrupt on Start. If software sets RX (bit 2) to 1, a receive interrupt is requested (in a combinatorial fashion) when a START bit is detected on RX. Such a receive interrupt is always followed by setting RDRNE (bit 7) in the middle of the STOP bit. Upon receiving the interrupt service request, the RX Interrupt on Start (RIS) bit must be set to 0, then immediately set to 1 to continue operation with a start bit interrupt. One function of this feature is to wake the part from HALT mode when a character arrives, so that the ASCI receives clocking to process the character. Another function is to ensure that the associated interrupt service routine is activated in time to sense the setting of RDRNE in the status register, and to start a timer for baud rate measurement at that time.

Break Detect. This READ-ONLY status bit (BD, bit 1)is set to 1 when a break is detected. A break is defined as a framing error with the data bits all equal to 0. The all-zero byte with its associated error bits are transferred to the FIFO if it is not full. If the FIFO is full, an overrun is generated, but the break, framing error and data are not transferred to the FIFO. Any time a break is detected, the receiver does not receive any more data until the RX pin returns to a High state. When set,

this bit remains set until it is cleared by writing a 0 to the EFR bit in the CNTLA register.

Send Break. Setting the SB bit (bit 0) to a 1 forces the channel's transmitter data output pin, TX, to a Low for as long as it remains set. Before starting the break, any character(s) in the TSR and in the TDR are transmitted completely. If a character is loaded into the TDR while a break is being generated, that character is held until the break is terminated and then transmitted.

ASCI Time Constant Registers

The ASTL and ASTH registers are only used when the BRG mode bit in the ASEXT register is set to 1. These two 8-bit registers form a 16-bit counter with a flip-flop logic circuit (DIVIDE-BY-2) on the output so that the final BRG output is symmetrical. The values written to these registers determine the time constant from which the baud rate is generated.

READ/WRITE and reset states for bits D7–D0 of the ASTL and ASTH registers are listed in Tables 72 and 73, respectively.

Table 72. Time Constant Register Low—ASTL 06h/R6 Bank Ah: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1
Note: R = Read, W = Write, X = Indeterminate.								

Bit/ Field	Bit Position	R/W	State	Description
D7–D0	ASTL	R/W	1	ASCI Time Constant Low

Table 73. Time Constant Register High—ASTH 07h/R7 Bank Ah: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1
Note: R = Read, W = Write, X = Indeterminate.								

Bit/ Field	Bit Position	R/W	State	Description
D7–D0	ASTH	R/W	1	ASCI Time Constant High

ASCI Status Register

The ASCI Status Register, STAT, controls status functions. READ/WRITE and reset states for bits D7–D0 are listed in Table 74.

Table 74. Status Register—STAT 08h/R8 Bank Ah: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	R	R	R	R/W	R/W	R	R/W
Reset	0	0	0	0	0	0	1	0
Note: R = Read, W = Write, X = Indeterminate.								

Bit/ Field	Bit Position	R/W	State	Description
D7	RDRNE	R	0	**Receive Data Register Not Empty** 0: Receive FIFO Empty 1: Receive FIFO contains 1 or more bytes
D6	OE	R	0	**Overrun Error** 0: Receive OK 1: Next byte is a FIFO overrun
D5	PE	R	0	**Parity Error** 0: Parity OK 1: Parity Error
D4	FE	R	0	**Framing Error** 0: Receive OK 1: Framing Error
D3	RIE	R/W	0	**Receive Interrupt Enable** 0: No IRQ on Receive 1: IRQ3 on RDRNE↑ or Start Bit
D2	Reserved	R/W	0	Reserved
D1	TDRE	R	1	**Transmit Data Register Empty** 0: Transmitter Working 1: Transmit Buffer Empty
D0	TIE	R/W	0	**Transmit Interrupt Enable** 0: No IRQ on Transmit 1: IRQ3 on TDRE↑

Receive Data Register Not Empty. RDRNE (RDRNE, bit 7)is set to 1 when the receiver transfers a character from the RSR into an empty RX FIFO.

Note: If a framing or parity error occurs, RDRNE is still set and the receive data (which generated the error) is still loaded into the FIFO.

When there is more than one byte in the FIFO and software reads a byte, RDRNE is not cleared to 0. The bit is cleared when the last byte is read from the FIFO.

Overrun Error. An overrun error (OE, bit 6) occurs if the receive FIFO is still full when the receiver completes assembly of a character and is ready to transfer it to the FIFO. If this situation occurs, the overrun error bit associated with the previous byte in the FIFO is set. In this case, the latest data byte is not transferred from the shift register to the FIFO and is lost.

When an overrun occurs, the receiver does not place any further data in the FIFO until the most recent good byte received (the byte with the associated overrun error bit set) moves to the top of the FIFO and sets the Overrun latch, and software then clears the Overrun latch. Assembly of bytes continues in the shift register, but this data is ignored until the byte with the overrun error reaches the top of the FIFO and the status is cleared. When set, the bit remains set until it is cleared by writing a 0 to the EFR bit in the CNTLA register. The bit is also cleared during Power-On Reset.

Parity Error. A parity error (PE, bit 5) is detected when parity generation and checking is enabled by the MOD1 bit (bit 1) in the CNTLA register and a character is assembled in which the parity does not match that specified by the PEO bit (bit 4) in CNTLB.

Note: PE is FIFOed and the error bit is not actually set until the associated data becomes available for reading in the RDR.

When set, the bit remains set until it is cleared by writing a 0 to the EFR bit (bit 3) in the CNTLA register. The bit is cleared at Power-On Reset.

Framing Error. A framing error (FE, bit 4) is detected when the stop bit of a character is sampled as a 0 (space). Like PE, FE is FIFOed and the error bit is not actually set until the associated data becomes available for reading in the RDR. When set, the bit remains set until it is cleared by writing a 0 to the EFR bit (bit 3) in the CNTLA register. The bit is cleared at Power-On Reset.

Receive Interrupt Enable. RIE, bit 3, must be set to 1 to enable ASCI receive interrupt requests. The Z8 edge-triggered interrupt (IRQ3) is generated when RDRNE (bit 7 of the STAT Register) is transitioned from 0 to 1. IRQ3 is also generated if a start bit is detected; the RIE bit is set to 1, and bit 2 of the ASEXT register is set to 1.

Reserved Bit 2. When read, bit 2 reflects the default value 0. When written, bit 2 is ignored.

Transmit Data Register Empty. TDRE = 1 indicates that the Transmit Data Register (TDR) is empty and that the next data byte to be transmitted can be written into the TDR. TDRE, bit 1, is cleared to 0 after the byte is written to TDR, until the ASCI transfers the byte from the TDR to the Transmit Shift Register (TSR), and then TDRE is again set to 1. TDRE is set to 1 at Power-On Reset.

Transmit Interrupt Enable. TIE, bit 0, should be set to 1 to enable ASCI transmit interrupt requests. An interrupt (IRQ3) is generated when TDRE (bit 1 of the STAT register) transitions from 0 to 1. TIE is cleared to 0 at Power-On Reset.

Note: If both TIE and RIE are set to 1, a receive interrupt is not generated on the incoming (RDR) data. To generate a receive interrupt:

1. The user must set only RIE to 1.
2. If both TIE and RIE have been previously set to 1, ZiLOG recommends that the EFR flag also be cleared to 0. If the EFR flag is not cleared to 0, the receive interrupt may not occur. Clear the EFR flag bit with the following instruction:

```
        push    rp              ;save the register pointer
        srp     #%1A            ;switch to the ASCI control register
                                ;bank
Loop1:ld        temp,RDR        ;clean up the RDR register
        tm      STAT,#10000000b ;make sure no data exists
                                ;in the RDR FIFO
        jr      nz,Loop1
        and     CNTLA,#11110111b :clear EFR
        pop     rp              ;restore the register pointer
```

Baud Rate Generation Summary

The application can select between one of two baud rate generators for the ASCI. If the BRG mode bit in the ASEXT register is set to 0, the SS2,1,0 bits, the DR bit, and the PR bit in CNTLB are used to select the baud rate. If the BRG mode bit is set to 1, the ASTL and ASTH registers are used to select the baud rate.

The following formulas are used to calculate the baud rate from the two baud rate generators:

If BRG mode = 0:

$$\text{Baud Rate} = \frac{\text{SCLK}}{(10 + 20 \times \text{PS}) \times \text{DIV} \times \text{DIVIDE RATIO}}$$

Where:

1. SCLK is the system clock.
2. PS = 1 or 0 and is bit 5 of CNTLB.
3. DIV = 1, 2, 4, 8, 16, 32 or 64 as reflected by SS2–0 in CNTLB.
4. DIVIDE RATIO = 16 or 64, as defined by DR (bit 3) in CNTLB.

If BRG mode = 1:

$$\text{Baud Rate} = \frac{\text{SCLK}}{(2 \times (TC + 2) \times \text{DIVIDE RATIO}}$$

or

$$TC = \frac{\text{SCLK}}{2 \times \text{BAUD RATE} \times \text{DIVIDE RATIO}} - 2$$

Where:

1. SCLK is the system clock.
2. TC is the 16-bit value programmed in ASTL and ASTH. A minimum TC value of 0 is valid.
3. DIVIDE RATIO = 16 or 64, as defined by DR in CNTLB.
4. BAUD RATE is the desired baud rate.
5. A maximum baud rate of 115Kbps can be obtained by using a 16-MHz Crystal, when TC = 0 and the DIVIDE RATIO = 16.

Table 75. Baud Rate List—BRG Mode = 0

Prescaler		Sampling Rate		Baud Rate					Example Baud Rate (bps)		
PS	Divide Ratio	DR	Rate	SS2	SS1	SS0	Divide Ratio	General Divide Ratio	SCLK = 6.144 MHz	SCLK = 4.608 MHz	SCLK = 3.072 MHz
0	SCLK ÷ 10	0	16	0	0	0	÷1	SCLK ÷ 160	38400		19200
				0	0	1	÷2	SCLK ÷ 320	19200		9600
				0	1	0	÷4	SCLK ÷ 640	9600		4800
				0	1	1	÷8	SCLK ÷ 1280	4800		2400
				1	0	0	÷16	SCLK ÷ 2560	2400		1200
				1	0	1	÷32	SCLK ÷ 5120	1200		600
				1	1	0	÷64	SCLK ÷ 10240	600		300
		1	64	0	0	0	÷1	SCLK ÷ 640	9600		4800
				0	0	1	÷2	SCLK ÷ 1280	4800		2400
				0	1	0	÷4	SCLK ÷ 2560	2400		1200
				0	1	1	÷8	SCLK ÷ 5120	1200		600
				1	0	0	÷16	SCLK ÷ 10240	600		300
				1	0	1	÷32	SCLK ÷ 20480	300		150
				1	1	0	÷64	SCLK ÷ 40960	150		75

Table 75. Baud Rate List—BRG Mode = 0 (Continued)

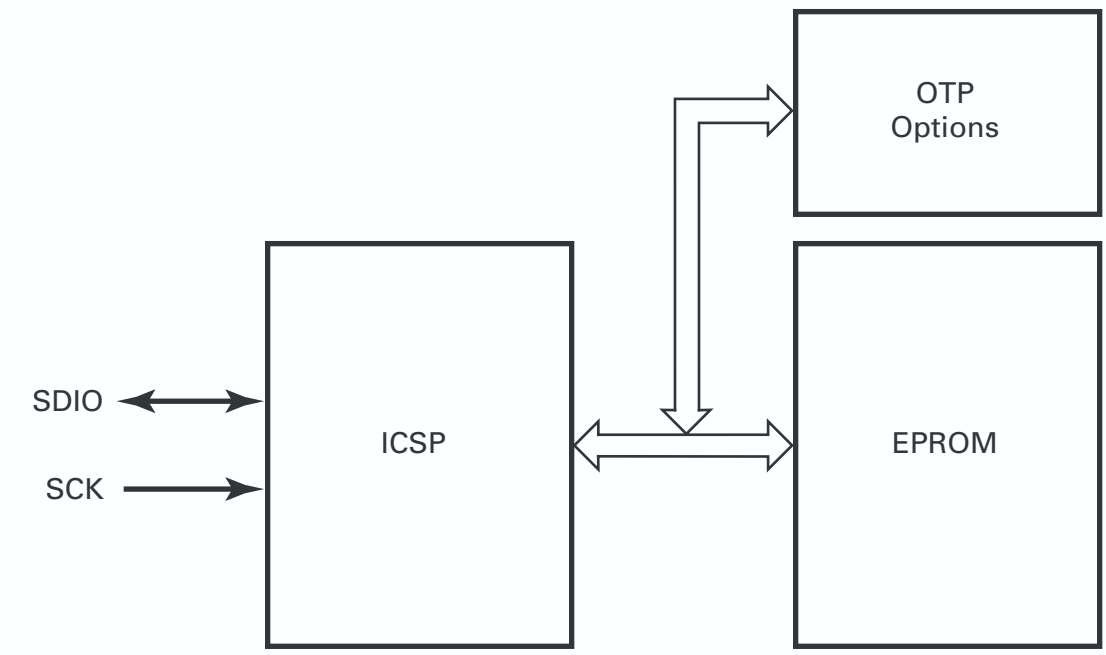
Prescaler		Sampling Rate		Baud Rate					Example Baud Rate (bps)		
PS	Divide Ratio	DR	Rate	SS2	SS1	SS0	Divide Ratio	General Divide Ratio	SCLK = 6.144 MHz	SCLK = 4.608 MHz	SCLK = 3.072 MHz
1	SCLK ÷ 30	0	16	0	0	0	÷1	SCLK ÷ 480		4800	
				0	0	1	÷2	SCLK ÷ 960		2400	
				0	1	0	÷4	SCLK ÷ 1920		1200	
				0	1	1	÷8	SCLK ÷ 3840		600	
				1	0	0	÷16	SCLK ÷ 7680		300	
				1	0	1	÷32	SCLK ÷ 15360		150	
				1	1	0	÷64	SCLK ÷ 30720		75	
		1	64	0	0	0	÷1	SCLK ÷ 1920		2400	
				0	0	1	÷2	SCLK ÷ 3840		1200	
				0	1	0	÷4	SCLK ÷ 7680		600	
				0	1	1	÷8	SCLK ÷ 15360		300	
				1	0	0	÷16	SCLK ÷ 30720		150	
				1	0	1	÷32	SCLK ÷ 61440		75	
				1	1	0	÷64	SCLK ÷ 122880		37.5	

In-Circuit Serial Programming

In-Circuit Serial Programming Block Diagram

Figure 36 shows the basic functionality of the In-Circuit Serial Programming Interface (ICSP). The ICSP interface receives and transmits data via the SDIO line in conjunction with an ICSP clock on the SCK line. Please refer to the MUZE Programming Specification for more details.

Figure 36. ICSP Block Diagram



The ICSP interface is a five-wire connection. The connections for the MUZE are:

V_{CC}. Power Supply.

SDIO. Serial Data Input/Output (SDIO)—data input and output pin, open-drain.

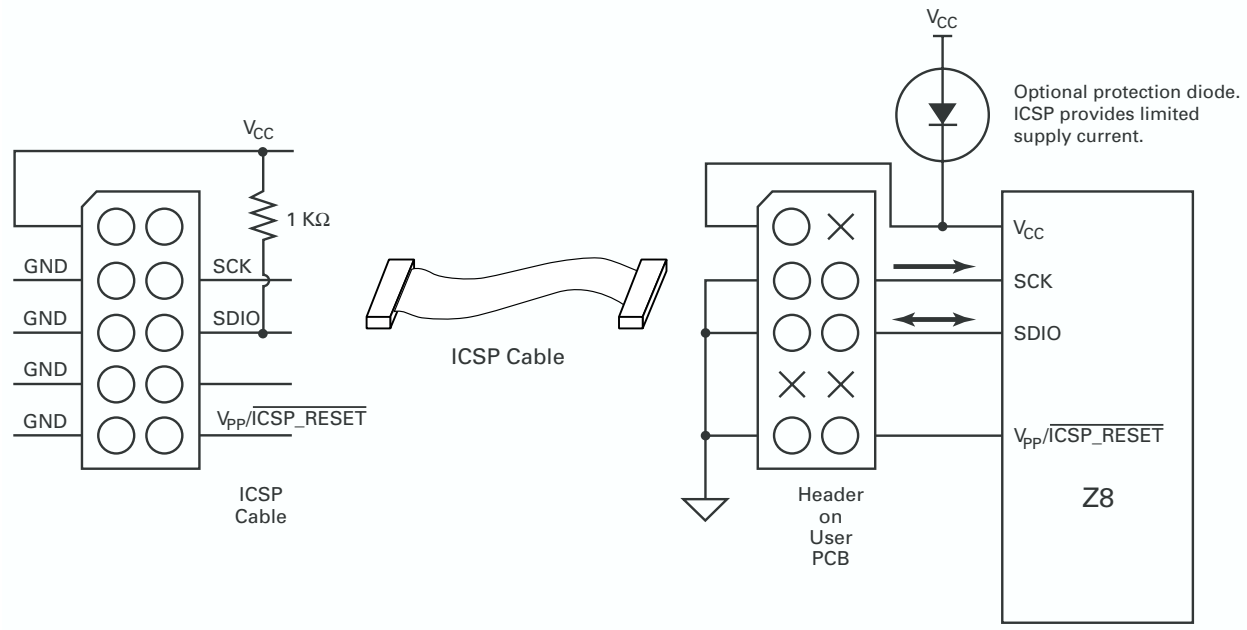
SCK. Serial ICSP Clock (SCK)—data input and output clock.

$\overline{\text{ICSP\_RESET}}$. Active Low (ICSP) Reset. $\overline{\text{ICSP\_RESET}}$ is an internal serial programming reset, not a complete Z8 reset, as is the case with POR.

GND. Ground.

The recommended circuit is illustrated in Figure 37.

Figure 37. ICSP Connectivity



Note: The diode shown in Figure 37 is an optional protection diode. ICSP provides limited supply current.

The following operations are specific to programming in ICSP mode:

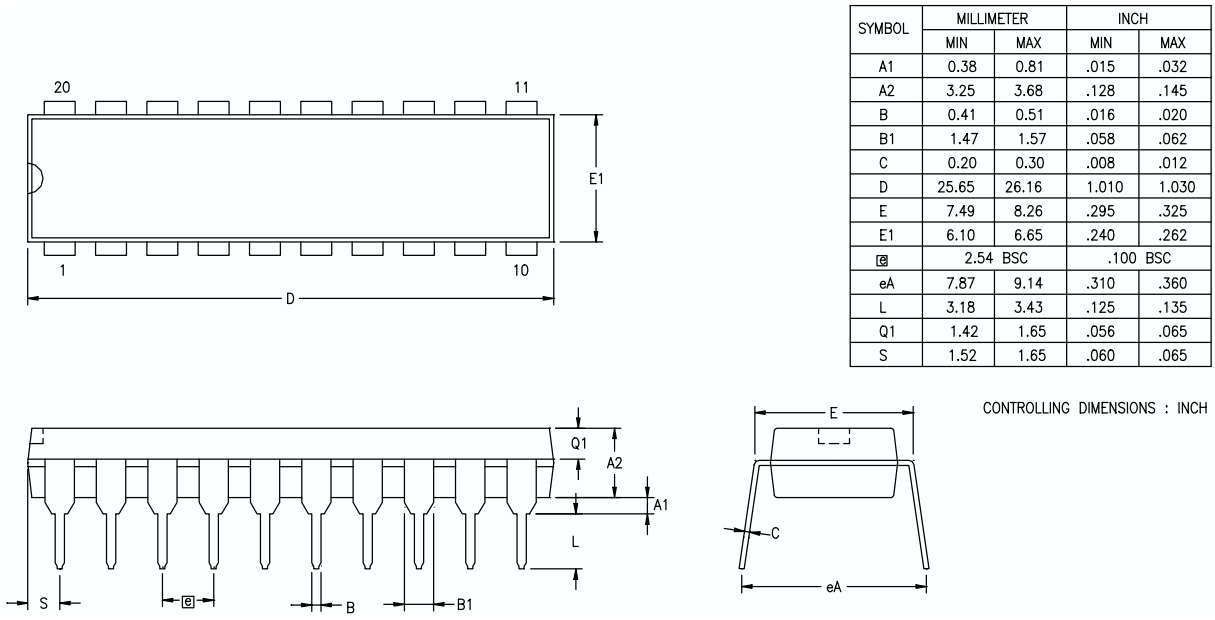
- Serial Operations—Unlock
- Serial Programming Option Bits—WORD Mode
- Serial Programming Option Bits—BYTE Mode
- Serial Operations—Reading
- Data Verify
- Device-Specific Options

For a complete description of these operations, please refer to the MUZE Programming Specification.

Packaging

Figure 38 illustrates the 20-pin DIP package for the Z86E122, Z86E123, Z86E124, Z86E125, and Z86E126 microcontroller devices.

Figure 38. 20-Pin DIP Package Diagram

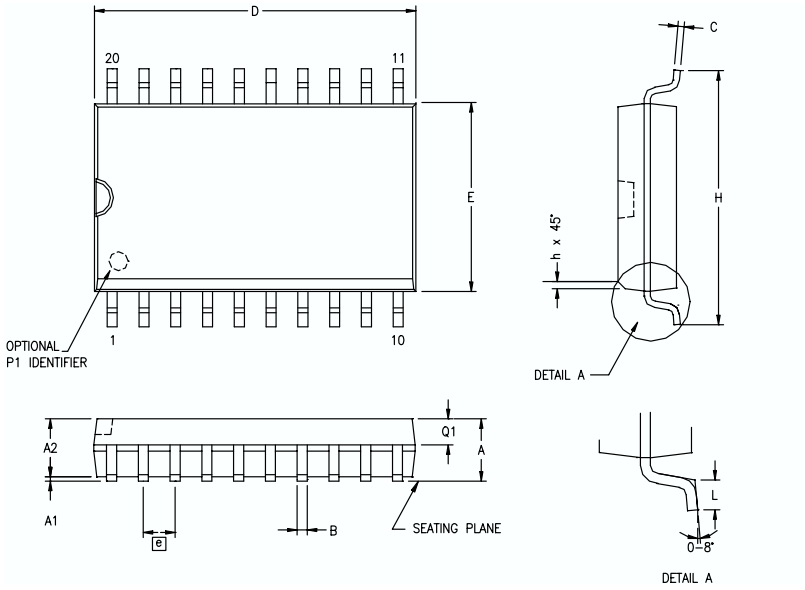


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.38	0.81	.015	.032
A2	3.25	3.68	.128	.145
B	0.41	0.51	.016	.020
B1	1.47	1.57	.058	.062
C	0.20	0.30	.008	.012
D	25.65	26.16	1.010	1.030
E	7.49	8.26	.295	.325
E1	6.10	6.65	.240	.262
e	2.54 BSC		.100 BSC	
eA	7.87	9.14	.310	.360
L	3.18	3.43	.125	.135
Q1	1.42	1.65	.056	.065
S	1.52	1.65	.060	.065

CONTROLLING DIMENSIONS : INCH

Figure 39 illustrates the 20-pin SOIC package for the Z86E122, Z86E123, Z86E124, Z86E125, and Z86E126 microcontroller devices.

Figure 39. 20-Pin SOIC Package Diagram

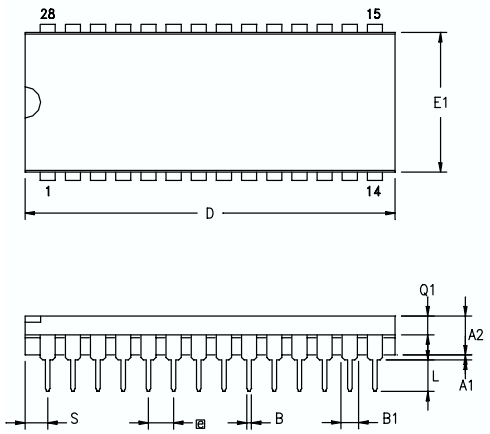


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	12.60	12.95	**.496**	.510
E	7.40	7.60	.291	.299
e	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 40 illustrates the 28-pin DIP package for the Z86E132, Z86E133, Z86E134, Z86E135, and Z86E136 microcontroller devices.

Figure 40. 28-Pin DIP Package Diagram



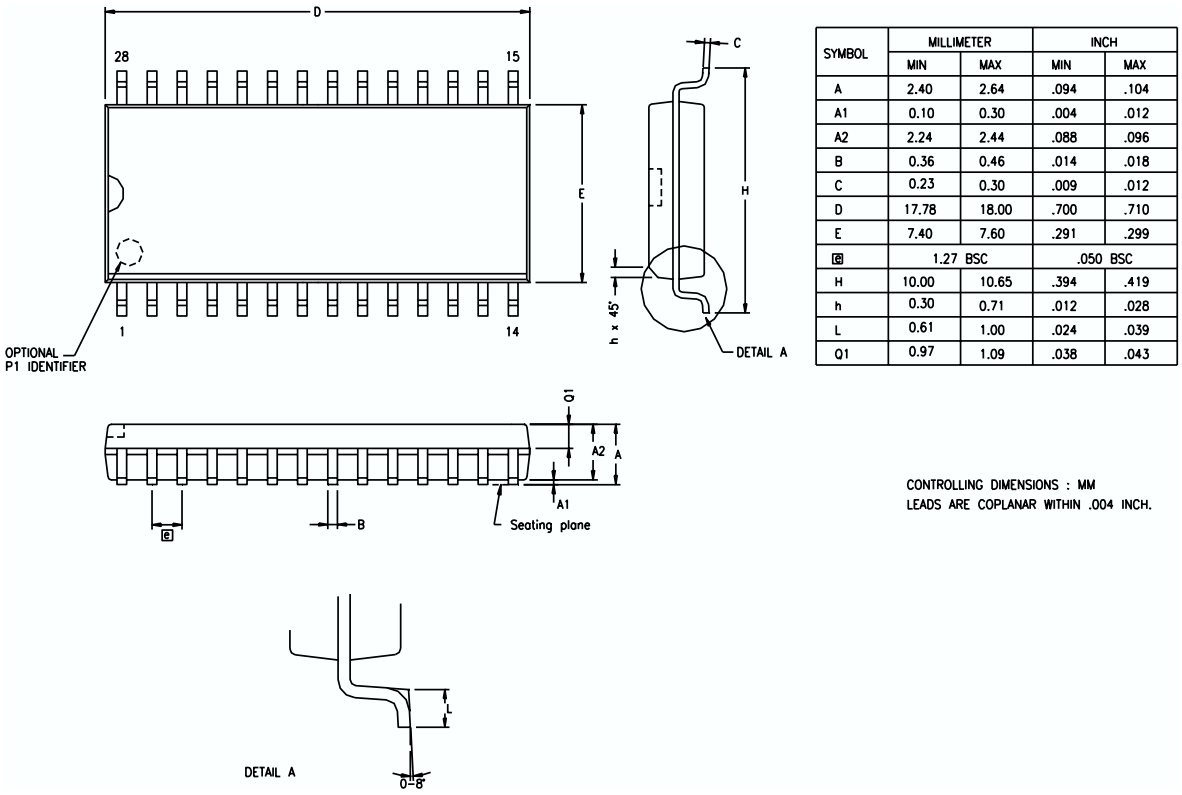
SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.38	1.02	.015	.040
A2		3.18	4.19	.125	.165
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 TYP	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.40	1.91	.055	.075
	02	1.40	1.78	.055	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

CONTROLLING DIMENSIONS : INCH

OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

Figure 41 illustrates the 28-pin SOIC package for the Z86E132, Z86E133, Z86E134, Z86E135, and Z86E136 microcontroller devices.

Figure 41. 28-Pin SOIC Package Diagram

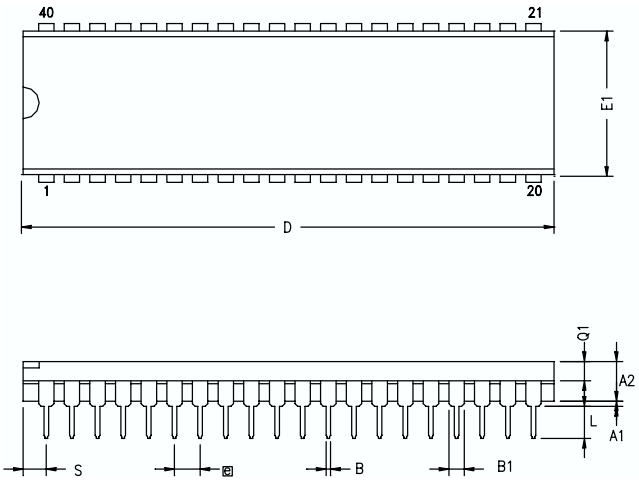


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
e	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.09	.038	.043

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 42 illustrates the 40-pin DIP package for the Z86E142, Z86E143, Z86E144, Z86E145, and Z86E146 microcontroller devices.

Figure 42. 40-Pin DIP Package Diagram

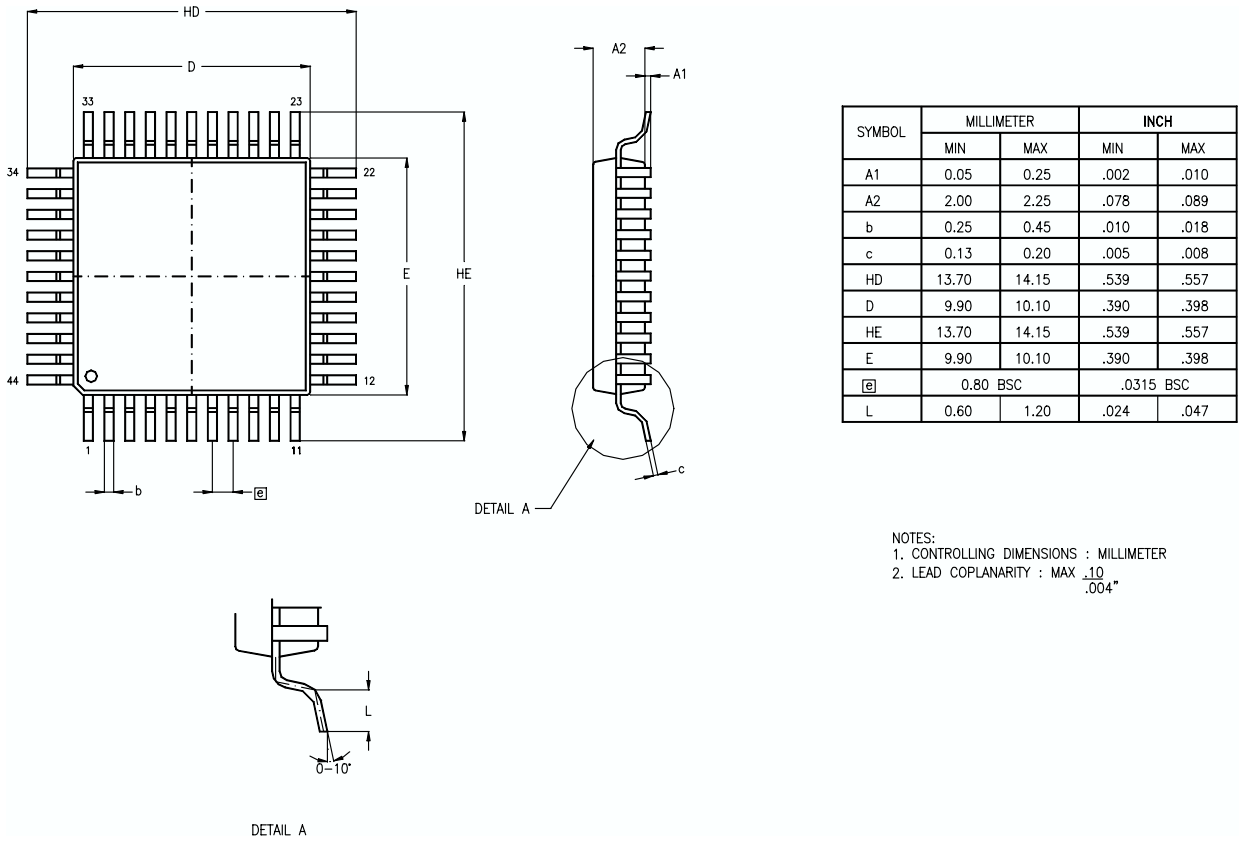


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.40	1.91	.055	.075
S	1.52	2.29	.060	.090

CONTROLLING DIMENSIONS : INCH

Figure 43 illustrates the 44-pin PQFP package for the Z86E142, Z86E143, Z86E144, Z86E145, and Z86E146 microcontroller devices.

Figure 43. 44-Pin PQFP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.15	.539	.557
D	9.90	10.10	.390	.398
HE	13.70	14.15	.539	.557
E	9.90	10.10	.390	.398
e	0.80 BSC		.0315 BSC	
L	0.60	1.20	.024	.047

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 / .004"

Ordering Information

Table 76. Ordering Information

Size	Pin Count	Package	Order Number*
64 KB	28	DIP	Z86E136PZ016SC
		SOIC	Z86E136SZ016SC
	40	DIP	Z86E146PZ016SC
	44	PQFP	Z86E146FZ016SC
32 KB	28	DIP	Z86E135PZ016SC
		SOIC	Z86E135SZ016SC
	40	DIP	Z86E145PZ016SC
	44	PQFP	Z86E145FZ016SC
16 KB	28	DIP	Z86E134PZ016SC
		SOIC	Z86E134SZ016SC
	40	DIP	Z86E144PZ016SC
	44	PQFP	Z86E144FZ016SC
8 KB	28	DIP	Z86E133PZ016SC
		SOIC	Z86E133SZ016SC
	40	DIP	Z86E143FZ016SC
	44	PQFP	Z86E143SZ016SC
4 KB	28	DIP	Z86E132PZ016SC
		SOIC	Z86E132SZ016SC
	40	DIP	Z86E142PZ016SC
	44	PQFP	Z86E142FZ016SC

Note: *The Standard temperature range is 0ºC to 70ºC. For parts that operate in the Extended temperature range of –40ºC to 105ºC, substitute the letter E for the letter S. For example, the Order Number for a 28-pin DIP operating at 64 KB in the Extended temperature range is Z86E136PZ016EC.

For fast results, contact your local ZiLOG sale office for assistance in ordering the part(s) desired.

Part Number Description

ZiLOG part numbers consist of a number of components. For example, part number Z86E136PZ016SC is a 16-MHz 28-pin DIP that operates in the –0ºC to +70ºC temperature range, with Plastic Standard Flow. The Z86E136PZ016SC part number corresponds to the code segments indicated in the following table.

Z	ZiLOG Prefix
86	Z8 Product
E	OTP Product
136	Product Number
PZ	Package
016	Speed (MHz)
S	Temperature
C	Environmental Flow

For fast results, contact your local ZiLOG sales office for assistance in ordering the part required.

Precharacterization Product

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or non-conformance with some aspects of the document may be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery may be uncertain at times, due to start-up yield issues.

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Document Information

Document Number Description

The Document Control Number that appears in the footer of each page of this document contains unique identifying attributes, as indicated in the following table:

PS	Product Specification
0040	Unique Document Number
05	Revision Number
1100	Month and Year Published

Change Log

Rev	Date	Purpose	By
01	02/00	Original issue	K. Johnston, R. Beebe
02	03/00	Corrections	K. Johnston, R. Beebe
03	03/00	Corrections	K. Johnston, R. Beebe
04	06/00	Corrections	K. Johnston, R. Beebe
05	11/00	Additions and Corrections	K. Johnston, R. Beebe

Customer Feedback Form

MUZE Product Specification

If you experience any problems while operating this product, or if you note any inaccuracies while reading this Product Specification, please copy and complete this form, then mail or fax it to ZiLOG (see *Return Information*, below). We also welcome your suggestions!

Customer Information

Name	Country
Company	Phone
Address	Fax
City/State/Zip	E-Mail

Product Information

Serial # or Board Fab #/Rev. #
Software Version
Document Number
Host Computer Description/Type

Return Information

ZiLOG
System Test/Customer Support
910 E. Hamilton Avenue, Suite 110, MS 4–3
Campbell, CA 95008
Fax: (408) 558-8536
Email: tools@zilog.com

Problem Description or Suggestion

Provide a complete description of the problem or your suggestion. If you are reporting a specific problem, include all steps leading up to the occurrence of the problem. Attach additional pages as necessary.

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