SN74LVC1G132 Series

SINGLE 2-INPUT NAND GATE WITH SCHMITT-TRIGGER INPUTS

Features

- Operate from 1.65V to 5.5V
- Inputs accept voltages to 5.5V
- ±24mA output drive at 3.3V
- Low power consumption, I_{CC}=10μA (Max)
- ESD Protection Exceeds JESD 22
  -2000-V Human-Body Model (A114-A)
  -1000-V Charged-Device Model (C101)

Applications

- AV Receiver
- Audio Dock:Portable
- Blu-ray Player and Home Theater
- Embedded PC
- Personal Digital Assistant(PDA)
- Power:Telecom/Server AC/DC Supply:Single Controller:Analog and Digital
- Solid State Drive(SSD):Client and Enterprise
- Wireless Headset,Keyboard,and Mouse

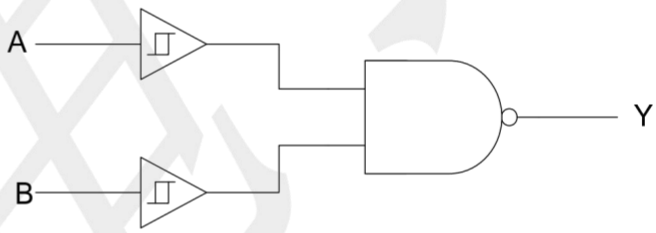
General Description

The S N 74LVC1G132 contains one 2-input NAND gate with Schmitt-trigger inputs designed for 1.65-V to 5.5V VCC operation and performs the Boolean function Y=A · B or Y =A+ B in positive logic.

Because of Schmitt action, this device has different input threshold levels for positive-going (VT+) and negative-going (VT-) signals.

This device can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

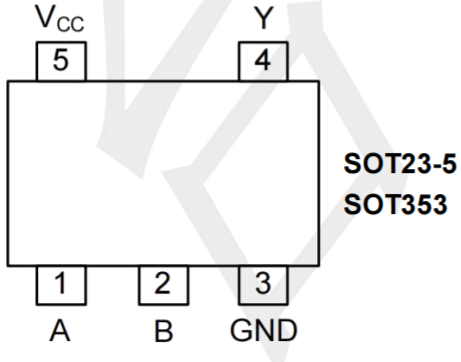
Logic Diagram



Ordering Information

ORDER NUMBER	PACKAGE DESCRIPTION	PACKAGE OPTION
SN74LVC1G132DBVR-TP	SOT23-5	Tape and Reel,3000
SN74LVC1G132DCKR-TP	SOT353	Tape and Reel,3000

Pin Configuratio



Function Table

INPUT(A)	INPUT(B)	OUTPUT(Y)
L	L	H
L	H	H
H	L	H
H	H	L

Note:H: HIGH voltage level;L: LOW voltage level.

Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ +6.5	V
Input Voltage	V_{IN}		-0.5 ~ +6.5	V
Output Voltage	V_{OUT}	Output in the Power-off state	-0.5 ~ +6.5	V
		Output in the High or Low state	-0.5 ~ $V_{CC+0.5}$	V
VCC or GND Current	I_{CC}	Output in the Power-off state	±100	mA
Continuous Output Current	I_{OUT}	V_{OUT}=0~V_{CC}	±50	mA
Input Clamp Current	I_{IK}	V_{IN}<0	-50	mA
Output Clamp Current	I_{OK}	V_{OUT}<0	-50	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	℃
Junction to Ambient	θ_{JA}	SOT23-5	230	℃/W
		SOT353	280	℃/W

Recommended Operating Conditions

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	1.65	--	5.5	V
		Data retention only	1.5	--	--	V
Input Voltage	V_{IN}		0	--	5.5	V
Output Voltage	V_{OUT}	High or low state	0	--	VCC	V
Operating Temperature	T_A		-40	--	125	℃

Electrical Characteristics (TA =25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Positive-going input threshold voltage	V_{T+}	V_{CC}=1.65V	0.79	--	1.16	V
		V_{CC}=2.3V	1.11	--	1.56	V
		V_{CC}=3V	1.5	--	1.87	V
		V_{CC}=4.5V	2.16	--	2.74	V
		V_{CC}=5.5V	2.61	--	3.33	V
Negative-going input threshold voltage	V_{T-}	V_{CC}=1.65V	0.39	--	0.62	V
		V_{CC}=2.3V	0.58	--	0.87	V
		V_{CC}=3V	0.84	--	1.14	V
		V_{CC}=4.5V	1.41	--	1.79	V
		V_{CC}=5.5V	1.87	--	2.29	V
Hysteresis (V_{T+} - V_{T-})	ΔV_T	V_{CC}=1.65V	0.37	--	0.62	V
		V_{CC}=2.3V	0.48	--	0.77	V
		V_{CC}=3V	0.56	--	0.87	V
		V_{CC}=4.5V	0.71	--	1.04	V
		V_{CC}=5.5V	0.71	--	1.11	V
High-Level Output Voltage	V_{OH}	V_{CC}=1.65 ~ 5.5V, I_{OH}=-100μA	V_{CC}-0.1	--	--	V
		V_{CC}=1.65V, I_{OH}=-4mA	1.2	--	--	V
		V_{CC}=2.3V, I_{OH}=-8mA	1.9	--	--	V
		V_{CC}=3.0V, I_{OH}=-16mA	2.4	--	--	V
		V_{CC}=3.0V, I_{OH}=-24mA	2.3	--	--	V
		V_{CC}=4.5V, I_{OH}=-32mA	3.8	--	--	--
Low-Level Output Voltage	V_{OL}	V_{CC}=1.65 ~ 5.5V, I_{OL}=100μA	--	--	0.1	V
		V_{CC}=1.65V, I_{OL}=4mA	--	--	0.45	V
		V_{CC}=2.3V, I_{OL}=8mA	--	--	0.30	V
		V_{CC}=3.0V, I_{OL}=16mA	--	--	0.40	V
		V_{CC}=3.0V, I_{OL}=24mA	--	--	0.55	V
		V_{CC}=4.5V, I_{OL}=32mA	--	--	0.55	V
Input Leakage Current	$I_{I(LEAK)}$	V_{IN}=5.5V or GND, V_{CC}=1.65V ~ 5.5V	--	--	±1	μA
Power OFF Leakage Current	I_{off}	V_{IN} or V_{OUT}=5.5V, V_{CC}=0V	--	--	±10	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND, I_{OUT}=0 V_{CC}=1.65 ~ 5.5V	--	--	10	μA
Additional Quiescent Supply Current Per Input Pin	ΔI_{CC}	V_{CC}=3 V~ 5.5V, One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND	--	--	500	μA
Input Capacitance	C_I	V_{CC}=3.3V, V_{IN}=V_{CC} or GND	--	3.5	--	pF

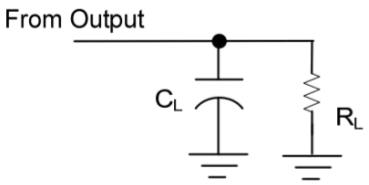
SWITCHING CHARACTERISTICS (TA =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Propagation delay from input (A or B) to output(Y)	t_{PLH}/t_{PHL}	V_{CC}=1.8V±0.15V	C_L=15pF	4	--	16	ns
			C_L=30pF	4	--	16	ns
		V_{CC}=2.5V±0.2V	C_L=15pF	2.5	--	7	ns
			C_L=30pF	3	--	7.5	ns
		V_{CC}=3.3V±0.3V	C_L=15pF	2	--	5.3	ns
			C_L=50pF	2	--	6	ns
		V_{CC}=5V±0.5V	C_L=15pF	1.5	--	4.4	ns
			C_L=50pF	2	--	5	ns

OPERATING CHARACTERISTICS (f=10MHz, TA =25°C , unless otherwise specified)

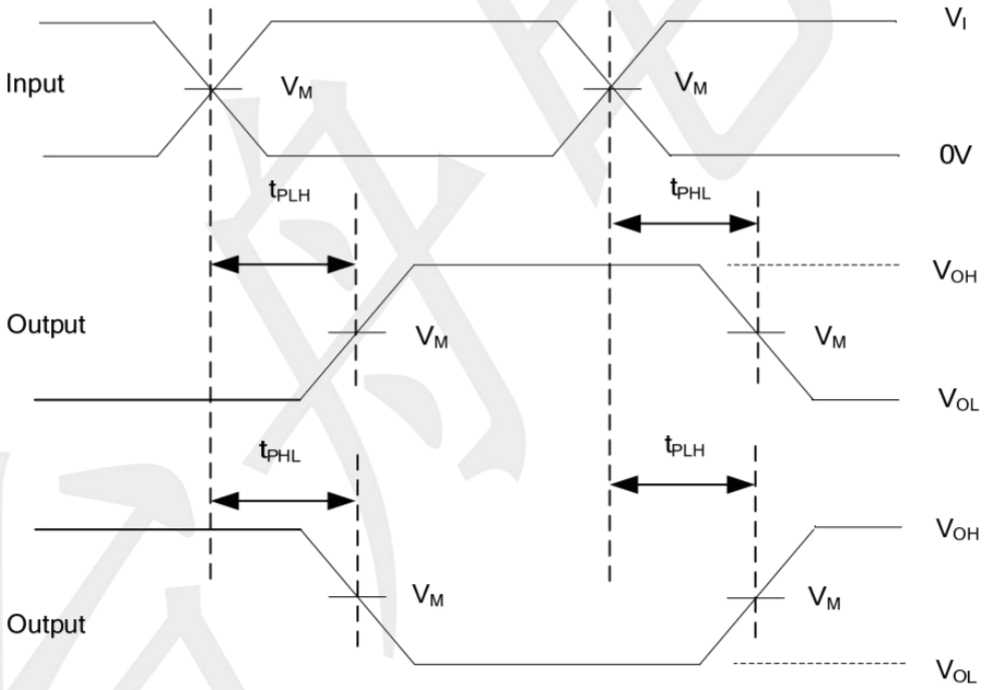
PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	f=10MHZ	V_{CC}=1.8V	--	17	--	pF
			V_{CC}=2.5V	--	18	--	pF
			V_{CC}=3.3V	--	18	--	pF
			V_{CC}=5.0V	--	20	--	pF

TEST CIRCUIT AND WAVEFORMS



TEST CIRCUIT

V_{CC}	INPUTS		V_M	C_L	R_L
	V_I	t_r / t_f			
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	15pF	1MΩ
				30pF	1KΩ
2.5V±0.2V	V_{CC}	≤2ns	$V_{CC}/2$	15pF	1MΩ
				30pF	500Ω
3.3V±0.3V	3V	≤2.5ns	1.5V	15pF	1MΩ
				50pF	500Ω
5V±0.5V	V_{CC}	≤2.5ns	$V_{CC}/2$	15pF	1MΩ
				50pF	500Ω



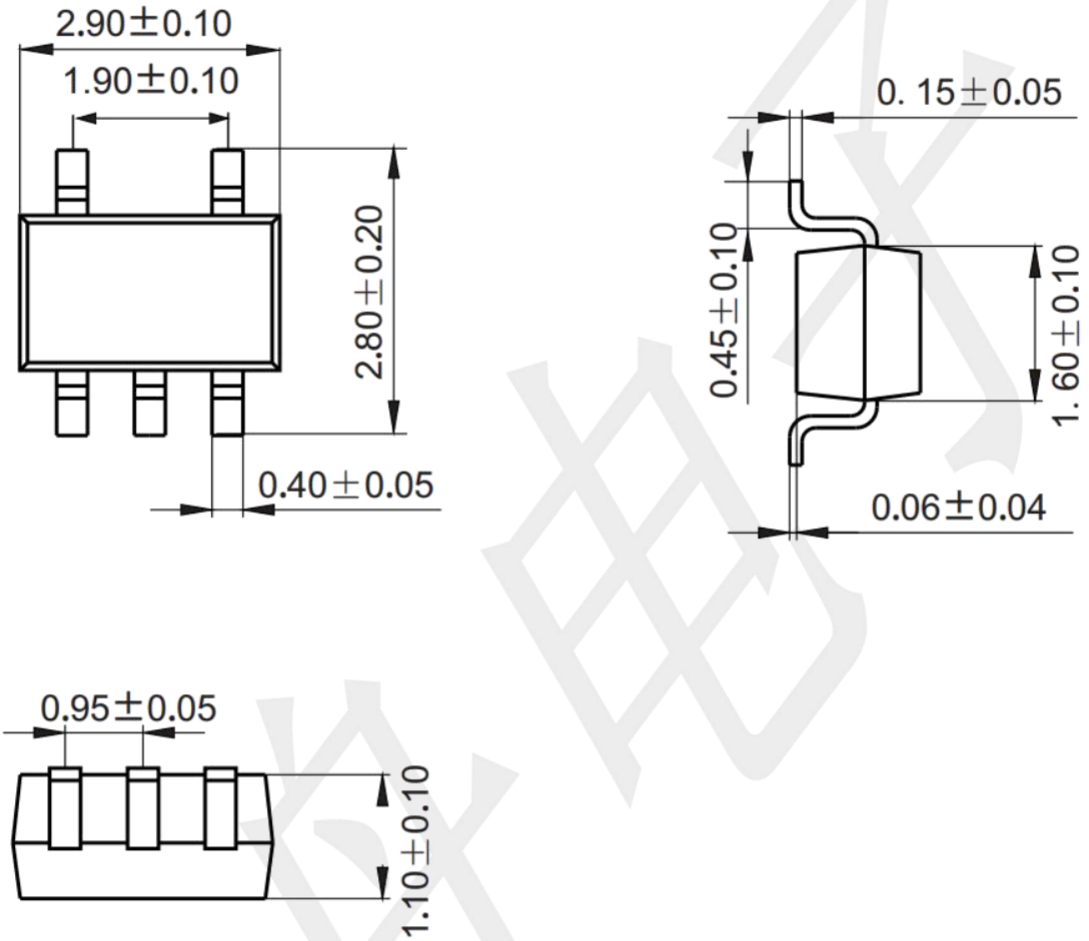
PROPAGATION DELAY TIMES

Figure 1. Test Circuit and Voltage Waveforms

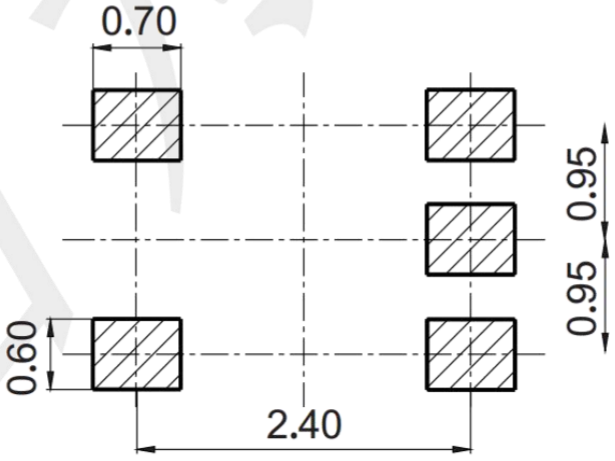
Note: CL includes probe and jig capacitance.
All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, ZO = 50Ω.

Package information

SOT23-5 (Unit: mm)

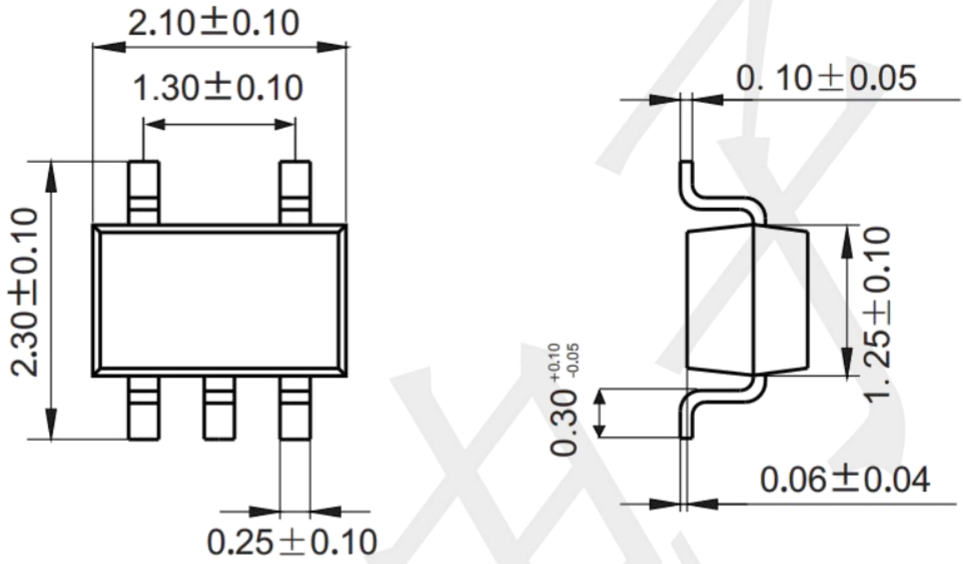


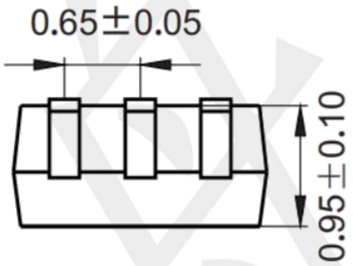
Mounting Pad Layout (Unit: mm)



Package information

SOT353 (Unit: mm)





Mounting Pad Layout (Unit: mm)