

NUP3112UPMU, SZNUP3112UPMU

ESD Protection Diode Array Quad, Ultra–Low Capacitance

The three–line voltage transient suppressor array is designed to protect voltage–sensitive components that require ultra–low capacitance from ESD and transient voltage events. This device features a common anode design which protects three independent high speed data lines and a V_{CC} power line in a single six–lead UDFN low profile package.

Excellent clamping capability, low capacitance, low leakage, and fast response time make these parts ideal for ESD protection on designs where board space is at a premium. Because of its low capacitance, it is suited for use in high frequency designs such as a USB 2.0 high speed.

Features

- Low Capacitance Data Lines (0.7 pF Typical)
- Protects up to Three Data Lines Plus a V_{CC} Pin
- UDFN Package, 1.6 x 1.6 mm
- Low Profile of 0.50 mm for Ultra Slim Design
- ESD Rating: IEC61000–4–2: Level 4
– Contact (14 kV)
- V_{CC} Pin = 15 V Protection
- D_1 , D_2 , and D_3 Pins = 5.2 V Minimum Protection
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q101 Qualified and PPAP Capable
- This is a Pb–Free Device

Typical Applications

- USB 2.0 High–Speed Interface
- Cell Phones
- MP3 Players
- SIM Card Protection

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

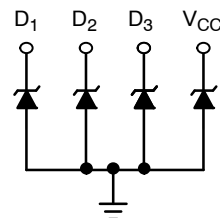
| Symbol | Rating | Value | Unit |
|-----------|--|------------|------------------|
| T_J | Operating Junction Temperature Range | –40 to 125 | $^\circ\text{C}$ |
| T_{STG} | Storage Temperature Range | –55 to 150 | $^\circ\text{C}$ |
| T_L | Lead Solder Temperature – Maximum (10 seconds) | 260 | $^\circ\text{C}$ |
| ESD | IEC 61000–4–2 Contact | 14000 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



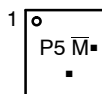
ON Semiconductor®

www.onsemi.com



UDFN6 1.6x1.6
MU SUFFIX
CASE 517AP

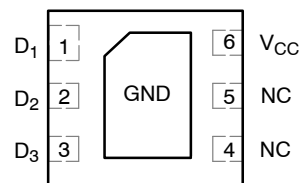
MARKING DIAGRAM



- P5 = Specific Device Code
- M = Date Code
- = Pb–Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

| Device | Package | Shipping† |
|------------------|--------------------|-----------------------|
| NUP3112UPMUTAG | UDFN6 (Pb–Free) | 3000 / Tape & Reel |
| SZNUP3112UPMUTAG | UDFN6 (Pb–Free) | 3000 / Tape & Reel |

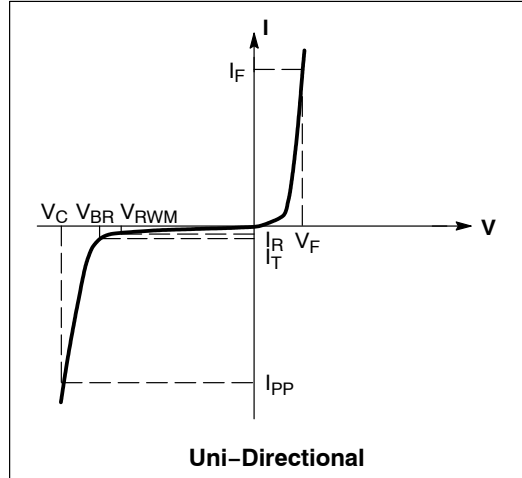
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NUP3112UPMU, SZNUP3112UPMU

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Symbol | Parameter |
|-----------|--|
| I_{PP} | Maximum Reverse Peak Pulse Current |
| V_C | Clamping Voltage @ I_{PP} |
| V_{RWM} | Working Peak Reverse Voltage |
| I_R | Maximum Reverse Leakage Current @ V_{RWM} |
| V_{BR} | Breakdown Voltage @ I_T |
| I_T | Test Current |
| I_F | Forward Current |
| V_F | Forward Voltage @ I_F |
| P_{pk} | Peak Power Dissipation |
| C | Max. Capacitance @ $V_R = 0$ and $f = 1.0$ MHz |



ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

| Parameter | Conditions | Symbol | Min | Typ | Max | Unit |
|---|--|------------|------|-----|------|---------------|
| Reverse Working Voltage ($D_1, D_2,$ and D_3) | (Note 1) | V_{RWM1} | - | - | 4.0 | V |
| Reverse Working Voltage (V_1) | (Note 1) | V_{RWM2} | - | - | 12 | V |
| Breakdown Voltage ($D_1, D_2,$ and D_3) | $I_T = 1$ mA, (Note 2) | V_{BR} | 5.2 | 5.5 | - | V |
| Breakdown Voltage (V_{CC}) | $I_T = 5$ mA, (Note 2) | V_{BR2} | 13.5 | 15 | 15.8 | V |
| Reverse Leakage Current ($D_1, D_2,$ and D_3) | @ V_{RWM} | I_R | - | - | 1.0 | μA |
| Reverse Leakage Current (V_{CC}) | @ V_{RWM2} | I_R | - | - | 1.0 | μA |
| Capacitance ($D_1, D_2,$ and D_3) | $V_R = 0$ V, $f = 1$ MHz (Line to GND) | C_J | - | 0.7 | 0.9 | pF |

- Surge protection devices are normally selected according to the working peak reverse voltage (V_{RWM}), which should be equal or greater than the DC or continuous peak operating voltage level.
- V_{BR} is measured at pulse test current I_T .

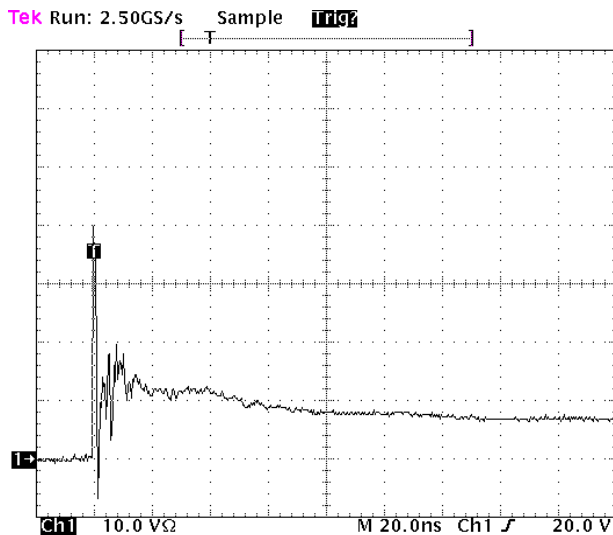


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000-4-2

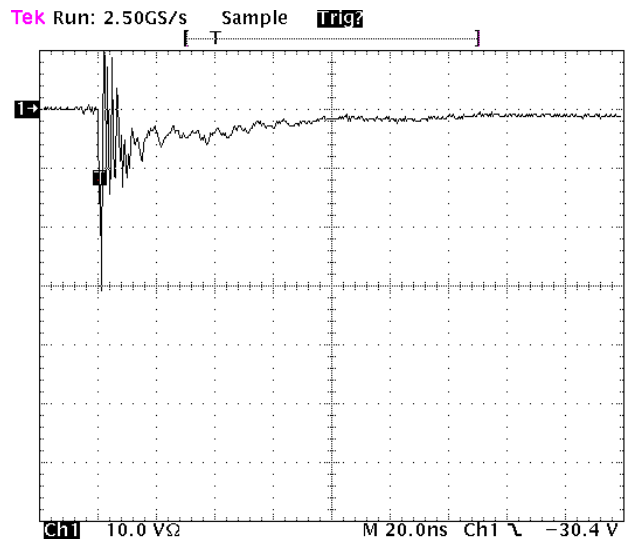


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000-4-2

NUP3112UPMU, SZNUP3112UPMU

IEC 61000-4-2 Spec.

| Level | Test Voltage (kV) | First Peak Current (A) | Current at 30 ns (A) | Current at 60 ns (A) |
|-------|-------------------|------------------------|----------------------|----------------------|
| 1 | 2 | 7.5 | 4 | 2 |
| 2 | 4 | 15 | 8 | 4 |
| 3 | 6 | 22.5 | 12 | 6 |
| 4 | 8 | 30 | 16 | 8 |



Figure 3. IEC61000-4-2 Spec

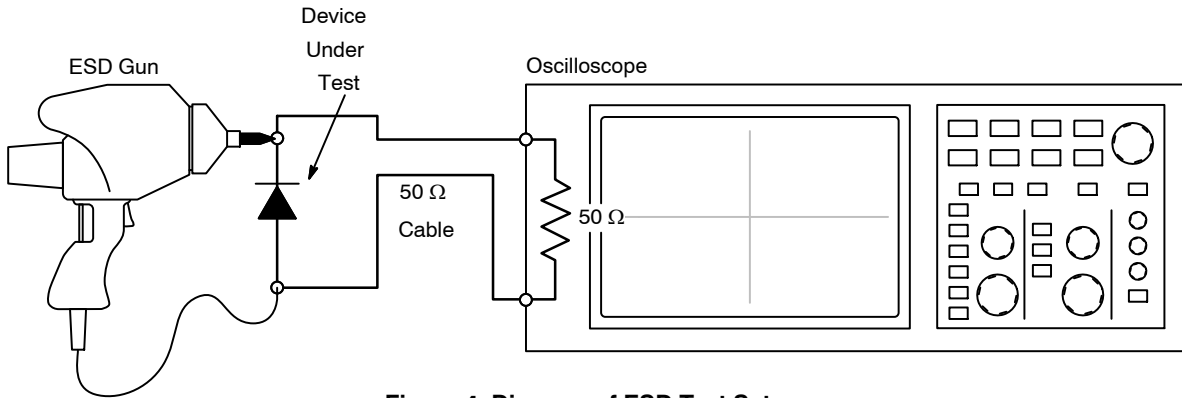


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

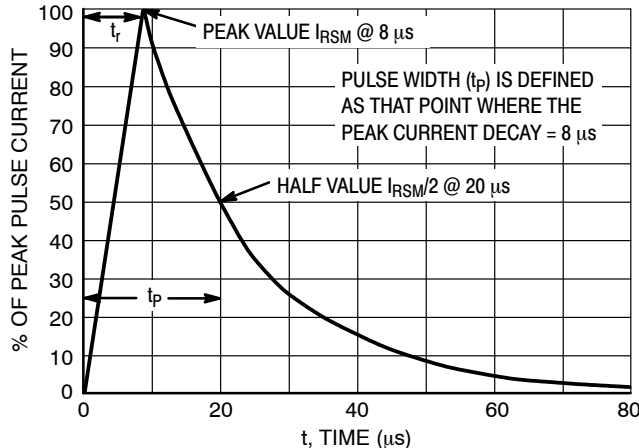
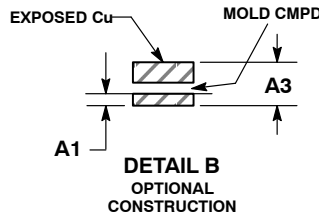
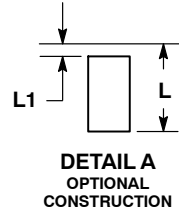
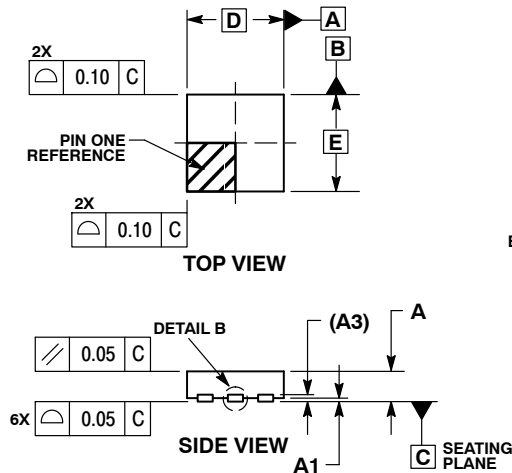
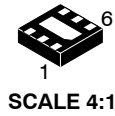


Figure 5. 8 x 20 μs Pulse Waveform



UDFN6 1.6x1.6, 0.5P
CASE 517AP
ISSUE O

DATE 26 OCT 2007

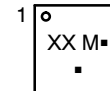


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

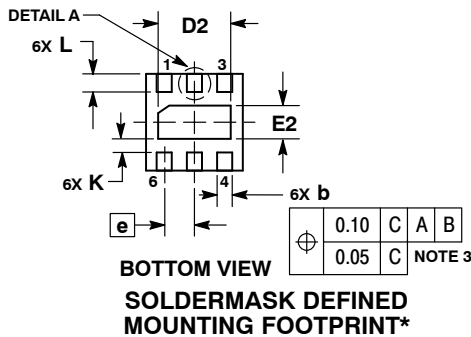
| MILLIMETERS | | |
|-------------|------|------|
| DIM | MIN | MAX |
| A | 0.45 | 0.55 |
| A1 | 0.00 | 0.05 |
| A3 | 0.13 | REF |
| b | 0.20 | 0.30 |
| D | 1.60 | BSC |
| E | 1.60 | BSC |
| e | 0.50 | BSC |
| D2 | 1.10 | 1.30 |
| E2 | 0.45 | 0.65 |
| K | 0.20 | --- |
| L | 0.20 | 0.40 |
| L1 | 0.00 | 0.15 |

GENERIC MARKING DIAGRAM*

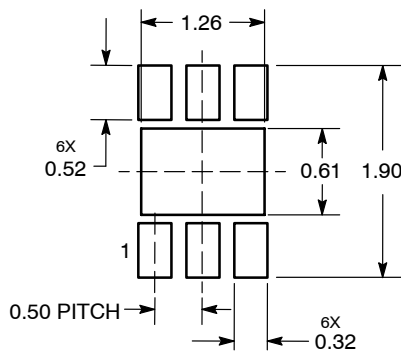


- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)
 *This information is generic. Please refer to device data sheet for actual part marking.
 Pb-Free indicator, "G" or microdot "■", may or may not be present.



SOLDERMASK DEFINED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

| | | |
|-------------------------|----------------------------------|--|
| DOCUMENT NUMBER: | 98AON25711D | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | 6 PIN UDFN, 1.6X1.6, 0.5P | PAGE 1 OF 1 |

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales