

N-Channel Trench Power MOSFET

General Description

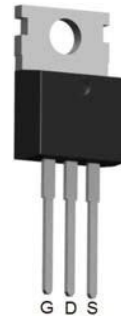
The HP50N10S is N-channel MOS Field Effect Transistor designed for high current switching applications. Rugged EAS capability and ultra low $R_{DS(ON)}$ is suitable for PWM, load switching applications.

Features

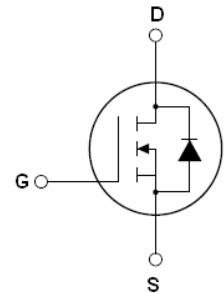
- $V_{DS}=100V$; $I_D=50A @ V_{GS}=10V$;
 $R_{DS(ON)} < 13m\Omega @ V_{GS}=10V$
 $R_{DS(ON)} < 16m\Omega @ V_{GS}=4.5V$
- Ultra Low On-Resistance
- High UIS and UIS 100% Test

Application

- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply



To-220 Top View



Schematic Diagram

$$V_{DS} = 100V$$

$$I_D = 50A$$

$$R_{DS(ON)} = 10m\Omega$$

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HP50N10S	HP50N10S	TO-220	-	-	-

Table 1. Absolute Maximum Ratings (TA=25°C)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage ($V_{GS}=0V$)	100	V
V_{GS}	Gate-Source Voltage ($V_{DS}=0V$)	±20	V
$I_{D(DC)}$	Drain Current (DC) at $T_c=25^\circ C$	50	A
$I_{D(DC)}$	Drain Current (DC) at $T_c=100^\circ C$	35	A
$I_{DM(Pluse)}$	Drain Current-Continuous@ Current-Pulsed (Note 1)	200	A
dv/dt	Peak Diode Recovery Voltage	4.1	V/ns
P_D	Maximum Power Dissipation($T_c=25^\circ C$)	125	W
	Derating Factor	1.03	W/°C
EAS	Single Pulse Avalanche Energy (Note 2)	529	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 175	°C

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2.EAS condition: $T_J=25^\circ C, V_{DD}=50V, V_G=10V, R_G=25\Omega$

Table 2. Thermal Characteristic

Symbol	Parameter	Value	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	---	0.97	$^{\circ}C/W$

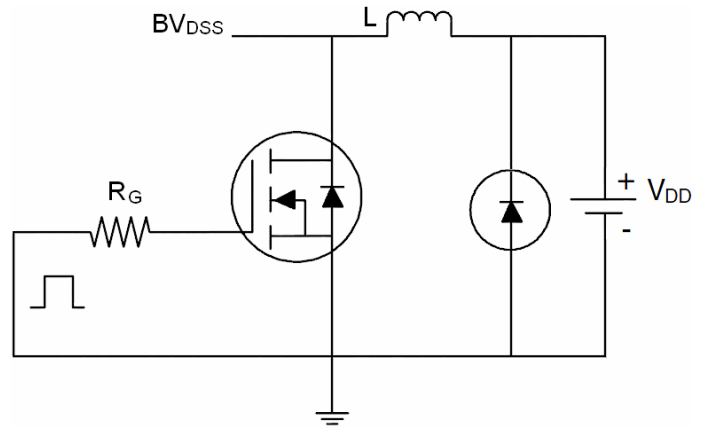
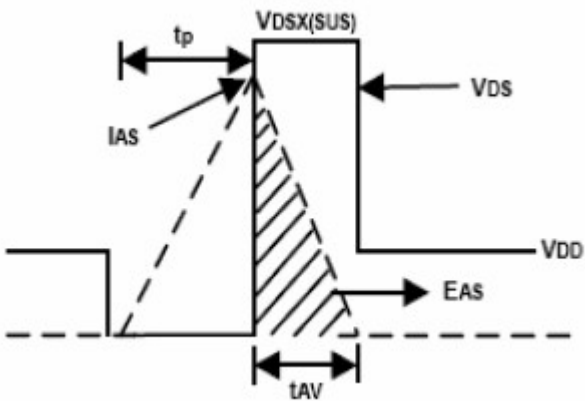
Table 3. Electrical Characteristics (TA=25 $^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	100			V
I_{DSS}	Zero Gate Voltage Drain Current(Tc=25 $^{\circ}C$)	$V_{DS}=100V, V_{GS}=0V$			1	μA
I_{DSS}	Zero Gate Voltage Drain Current(Tc=125 $^{\circ}C$)	$V_{DS}=100V, V_{GS}=0V$			10	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.6	2.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	$V_{GS}=10V, I_D=40A$		10	13	m Ω
		$V_{GS}=4.5, I_D =40A$		13	16	m Ω
Dynamic Characteristics						
g_{FS}	Forward Transconductance	$V_{DS}=10V, I_D=15A$	20			S
C_{iss}	Input Capacitance	$V_{DS}=25V, V_{GS}=0V$ $f=1.0MHz$		4435		PF
C_{oss}	Output Capacitance			336		PF
C_{rss}	Reverse Transfer Capacitance			248		PF
Q_g	Total Gate Charge	$V_{DS}=50V, I_D=40A$ $V_{GS}=10V$		94		nC
Q_{gs}	Gate-Source Charge			19		nC
Q_{gd}	Gate-Drain Charge			31		nC
Switching Times						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=65V, I_D=40A, R_L=15\Omega$ $V_{GS}=10V, R_G=2.5\Omega$		33		nS
t_r	Turn-on Rise Time			59		nS
$t_{d(off)}$	Turn-Off Delay Time			86		nS
t_f	Turn-Off Fall Time			29		nS
Source-Drain Diode Characteristics						
I_{SD}	Source-Drain Current(Body Diode)			60		A
I_{SDM}	Pulsed Source-Drain Current(Body Diode)			240		A
V_{SD}	Forward On Voltage ^(Note 1)	$T_J=25^{\circ}C, I_{SD}=40A, V_{GS}=0V$		0.86	0.99	V
t_{rr}	Reverse Recovery Time ^(Note 1)	$T_J=25^{\circ}C, I_F=40A$ $di/dt=100A/\mu s$		31		nS
Q_{rr}	Reverse Recovery Charge ^(Note 1)			78		nC
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible(turn-on is dominated by L_S+L_D)				

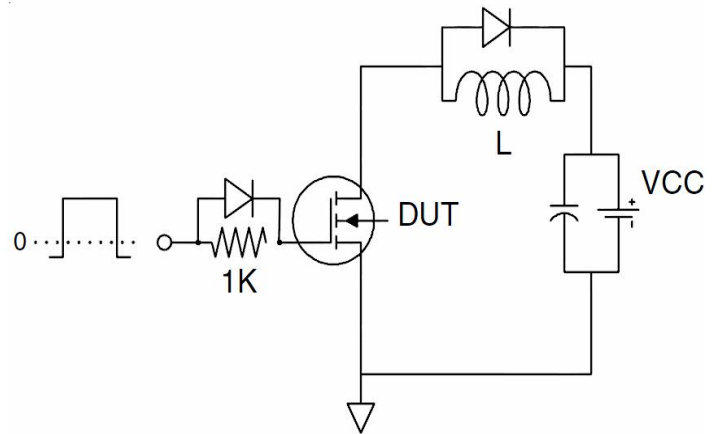
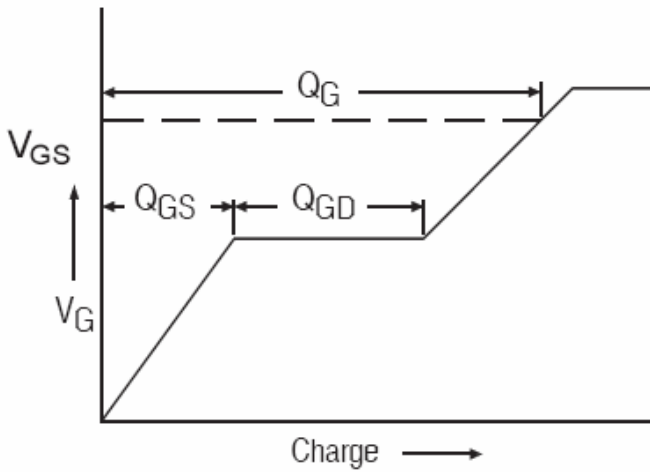
Notes 1. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 1.5\%$, $R_G=25\Omega$, Starting $T_J=25^{\circ}C$

Test Circuit

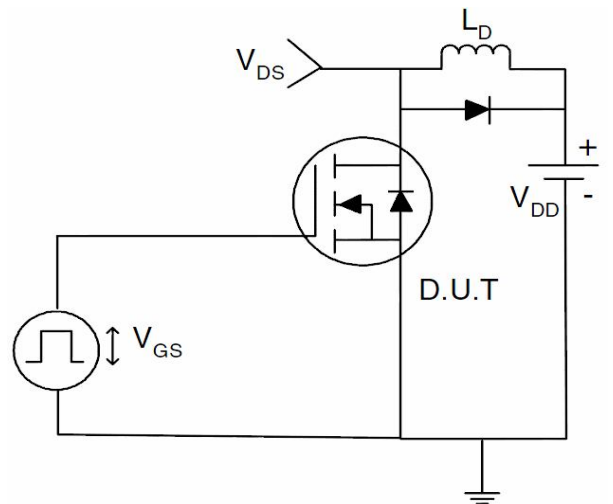
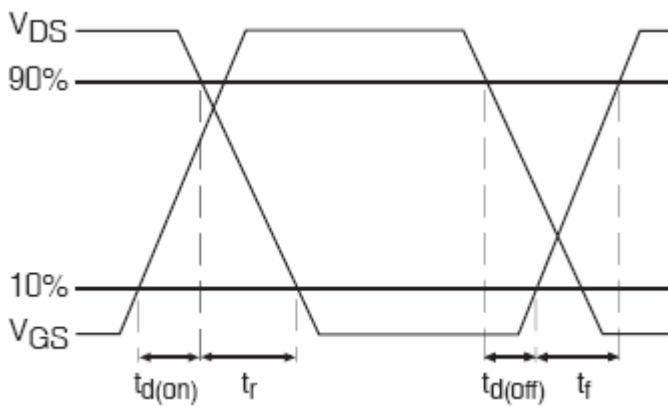
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit:



3) Switch Time Test Circuit:



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

Figure1. Output Characteristics

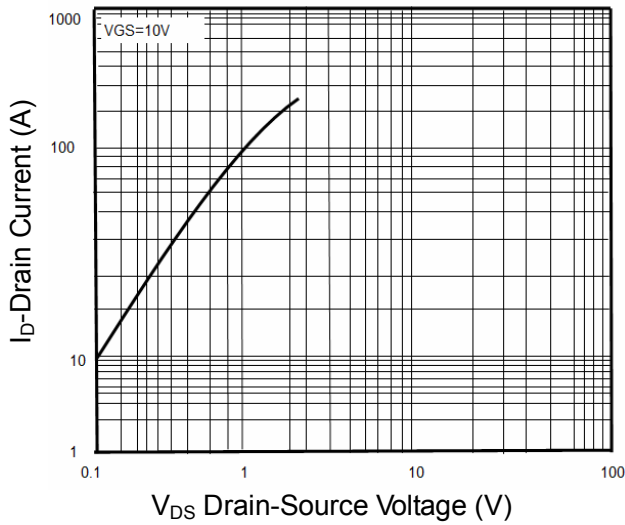


Figure2. Transfer Characteristics

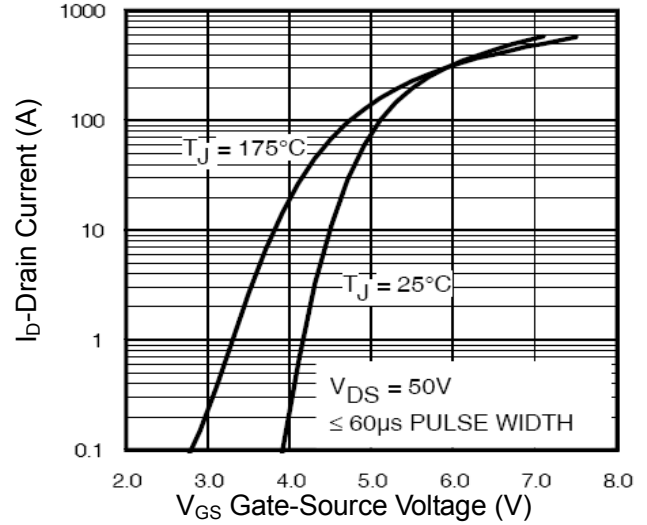


Figure3. ID vs Junction Temperature

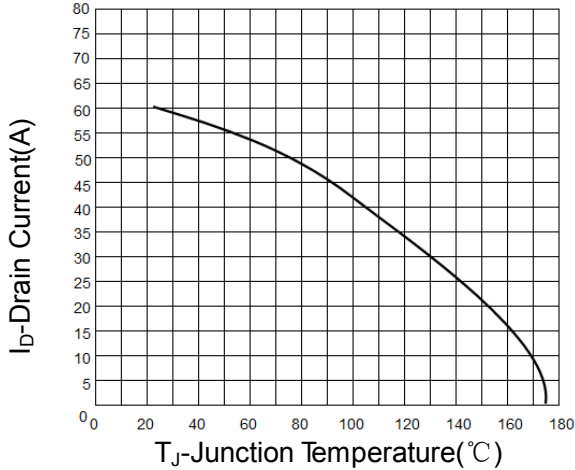


Figure4. RDS(ON)- Junction Temperature

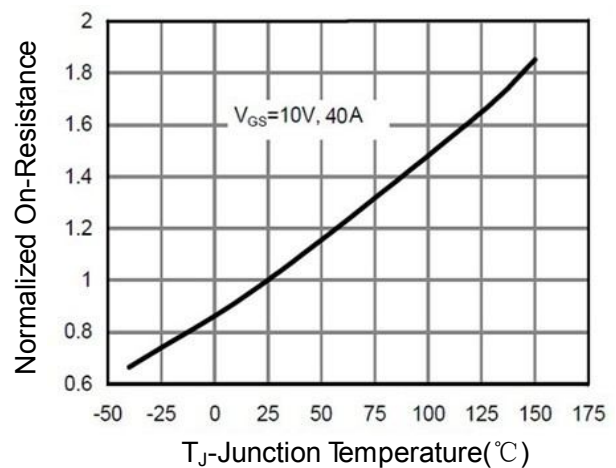


Figure5. BVDS vs Junction Temperature

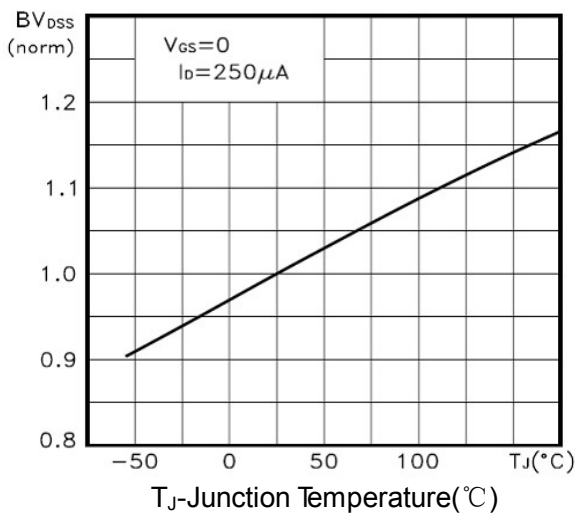


Figure6. VGS(th) vs Junction Temperature

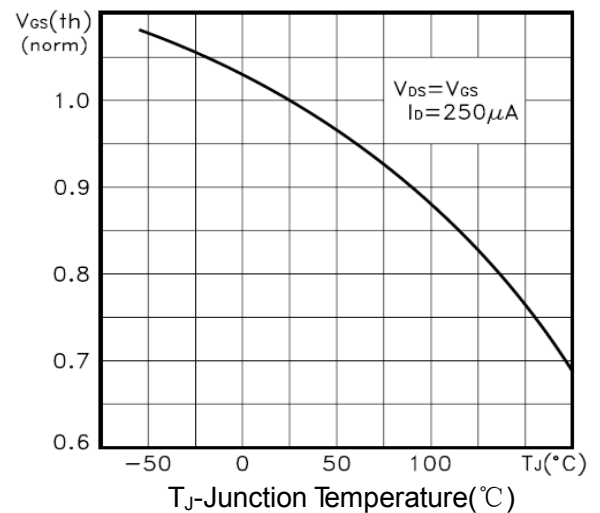


Figure7. Gate Charge

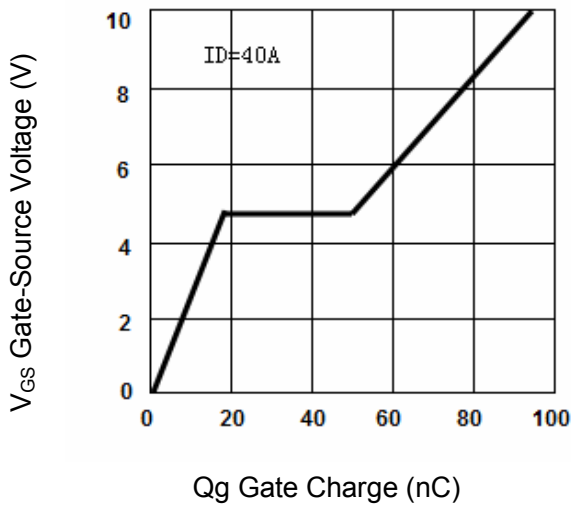


Figure8. Capacitance vs Vds

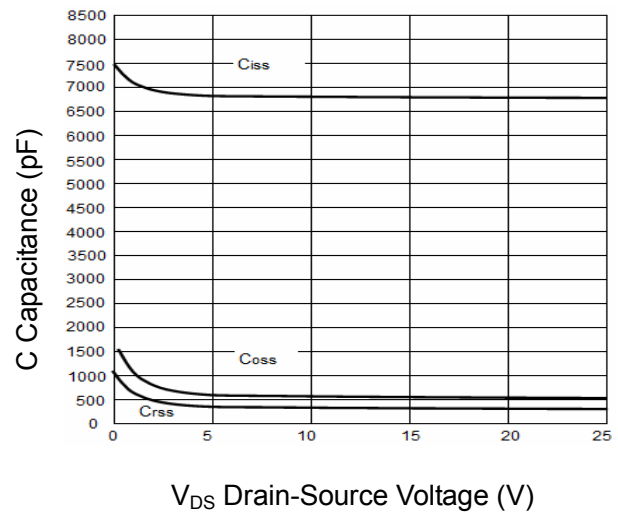


Figure9. Safe Operation Area

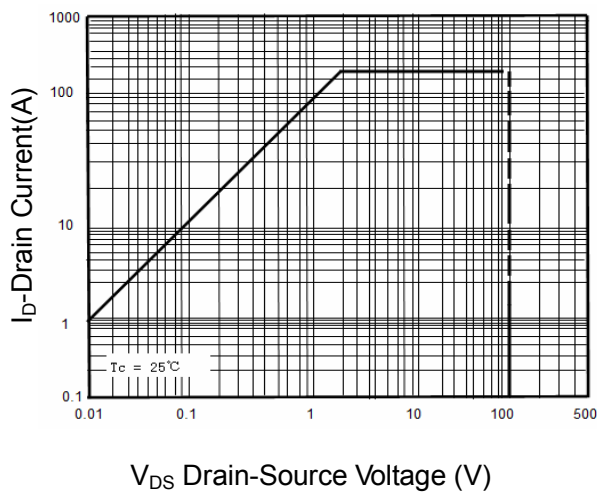


Figure10. Source- Drain Diode Forward

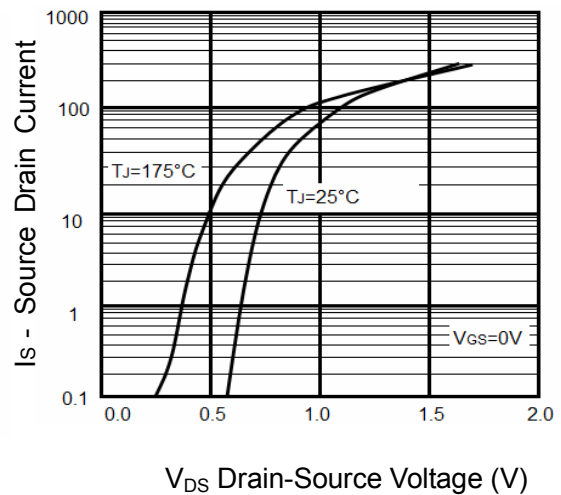
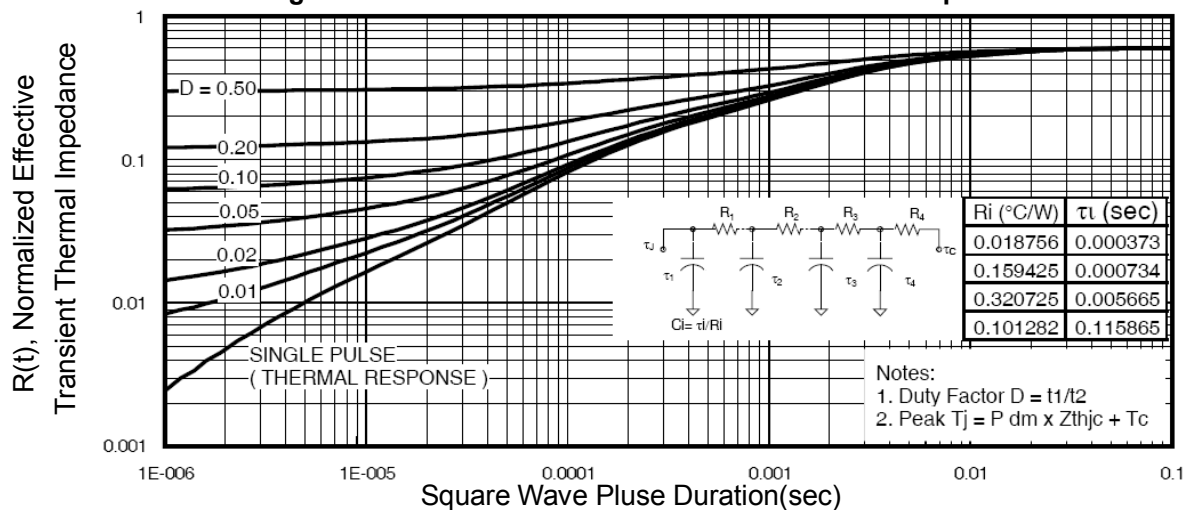
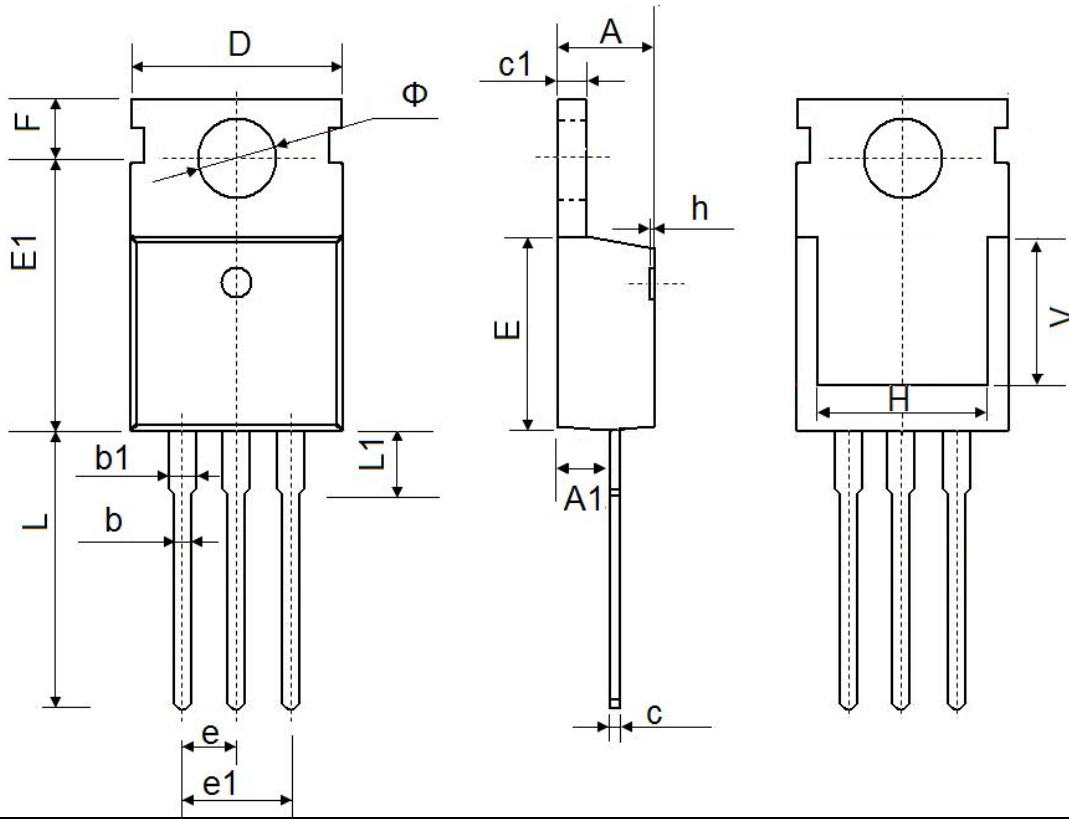


Figure11. Normalized Maximum Transient Thermal Impedance



TO-220 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max
A	4.300	4.700	0.169	0.185
A1	2.200	2.600	0.087	0.102
b	0.700	0.950	0.028	0.037
b1	1.170	1.410	0.046	0.056
c	0.450	0.650	0.018	0.026
c1	1.200	1.400	0.047	0.055
D	9.600	10.400	0.378	0.409
E	8.8500	9.750	0.348	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.750	14.300	0.502	0.563
L1	2.850	3.950	0.112	0.156
V	7.500 REF.		0.295 REF.	
φ	3.400	4.000	0.134	0.157