PT501

Universal NFC card emulation and NFC peer-to-peer solution

Rev. 3.2 — 26 March 2014
224632

Product data sheet
COMPANY PUBLIC

1. Introduction

The PT501 is a highly integrated frontend IC for applications at 13.56 MHz, acting as a card emulator over ISO/IEC 14443-A and FeliCa compliant protocols as well as a passive target IC in the NFC peer-to-peer IP-1 mode.

2. General description

The PT501 is a generic 13.56 MHz communication interface, this transceiver IC can be operated in two operating modes:

- Passive target device for NFC peer-to-peer IP-1 mode communication
- Card emulation mode supporting ISO/IEC 14443-A and FeliCa compliant protocol

In card emulation mode, the PT501 transceiver IC is able to answer to a reader/writer command either according to the ISO/IEC 14443A/MIFARE or FeliCa card interface scheme.

Additionally, the PT501 transceiver IC offers the possibility to communicate directly to an NFCIP-1 device in the NFC peer-to-peer passive target mode. The NFCIP-1 mode offers different communication mode and transfer speeds up to 424 kbit/s according to Ecma 340 and ISO/IEC 18092 NFCIP-1 standards.

Various host controller interfaces are implemented:

- SPI interface
- Serial UART (similar to RS232 with voltage levels according pad voltage supply)
- I^2C interface.

3. Features and benefits

- Highly integrated analog circuitry to demodulate and decode responses
- Buffered output drivers for connecting an antenna with the minimum number of external components
- Integrated RF level detector
- Integrated data mode detector
- ISO/IEC 14443A higher transfer speed communication at 106 kbit/s
- Contactless communication according to the FeliCa scheme at 212 kbit/s and 424 kbit/s
- Integrated RF interface for NFC peer-to-peer passive target NFCIP-1 up to 424 kbit/s
- Additional power supply to directly supply the smart card IC connected via S2C

- Supported host interfaces
  - SPI up to 10 Mbit/s
  - I^2C-bus interface up to 400 kBd in Fast mode, up to 3400 kBd in High-speed mode
  - RS232 Serial UART up to 1228.8 kBd, with voltage levels dependant on pin voltage supply
- FIFO buffer handles 64 byte send and receive
- Flexible interrupt modes
- Hard reset with low power function
- Power-down mode per software
- Programmable timer
- 2.5 V to 3.6 V power supply
- CRC coprocessor
- Programmable I/O pins
- Internal self-test

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	analog supply voltage	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V [1][2]	2.5	-	3.6	V
V_{DDD}	digital supply voltage					
$V_{DD(TVDD)}$	TVDD supply voltage					
$V_{DD(PVDD)}$	PVDD supply voltage	[3]	1.6	-	3.6	V
$V_{DD(SVDD)}$	SVDD supply voltage	$V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	1.6	-	3.6	V
I_{pd}	power-down current	$V_{DDA} = V_{DDD} = V_{DD(TVDD)} = V_{DD(PVDD)} = 3$ V				
		hard power-down; pin NRSTPD set LOW [4]	-	-	5	µA
		soft power-down; RF level detector on [4]	-	-	10	µA
I_{DDD}	digital supply current	pin DVDD; $V_{DDD} = 3$ V	-	6.5	9	mA
I_{DDA}	analog supply current	pin AVDD; $V_{DDA} = 3$ V, CommandReg register's RcvOff bit = 0	-	7	10	mA
		pin AVDD; receiver switched off; $V_{DDA} = 3$ V, CommandReg register's RcvOff bit = 1	-	3	5	mA
$I_{DD(PVDD)}$	PVDD supply current	pin PVDD [5]	-	-	40	mA
T_{amb}	ambient temperature	HVQFN32	−30	-	+85	°C

[1] Supply voltages below 3 V reduce the performance in, for example, the achievable operating distance.

[2] V_{DDA}, V_{DDD} and $V_{DD(TVDD)}$ must always be the same voltage.

[3] $V_{DD(PVDD)}$ must always be the same or lower voltage than V_{DDD}.

[4] I_{pd} is the total current for all supplies.

[5] $I_{DD(PVDD)}$ depends on the overall load at the digital pins.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PT5010A0HN/C1	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm	SOT617-1

6. Block diagram

The analog interface handles the modulation and demodulation of the analog signals according to the Card operation mode and NFCIP-1 mode communication scheme.

The RF level detector detects the presence of an external RF-field delivered by the antenna to the RX pin.

The Data mode detector detects a ISO/IEC 14443-A, FeliCa or NFCIP-1 mode in order to prepare the internal receiver to demodulate signals, which are sent to the PT501.

The communication (S^2C) interface provides digital signals to support communication for transfer speeds above 424 kbit/s and digital signals to communicate to a secure IC.

The contactless UART manages the protocol requirements for the communication protocols in cooperation with the host. The FIFO buffer ensures fast and convenient data transfer to and from the host and the contactless UART and vice versa.

Various host interfaces are implemented to meet different customer requirements.

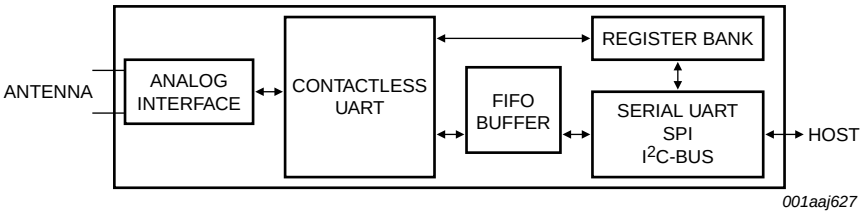


Fig 1. Simplified block diagram of the PT501

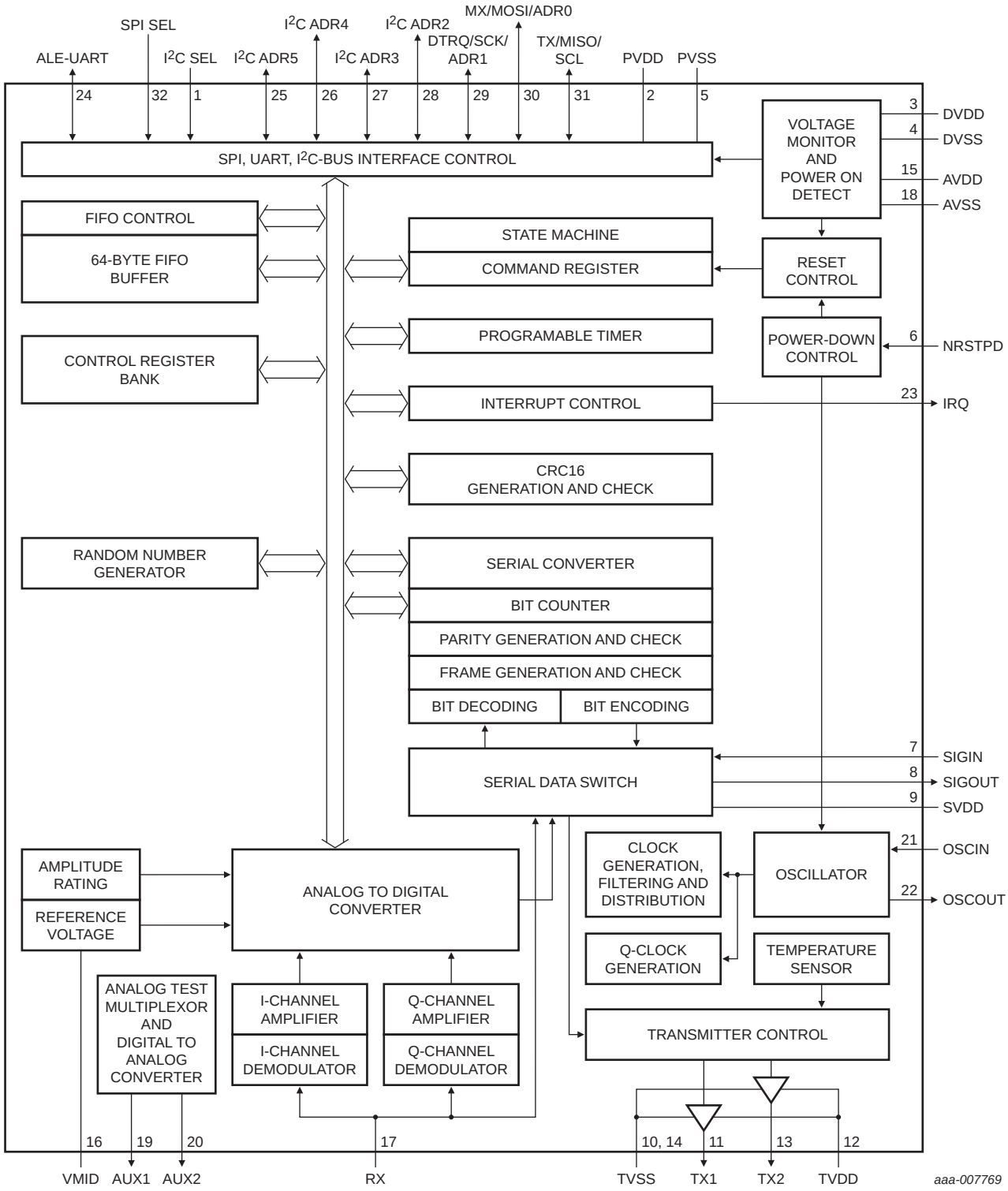


Fig 2. Detailed block diagram of the PT501

7. Pinning information

7.1 Pinning

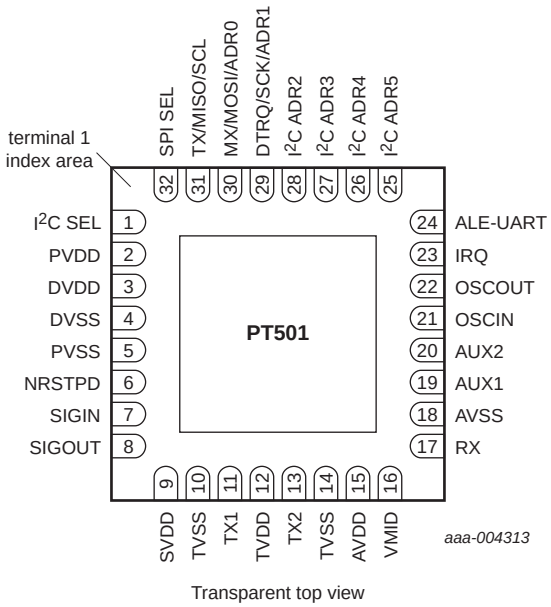


Fig 3. Pinning configuration HVQFN32 (SOT617-1)

7.2 Pin description

Table 3. Pin description HVQFN32

Pin	Symbol	Type	Description
1	I^2CSEL	I	**Address Line**, see Table 110 on page 47
2	PVDD	PWR	**Pad power supply**
3	DVDD	PWR	**Digital Power Supply**
4	DVSS	PWR	**Digital Ground**
5	PVSS	PWR	**Pad power supply ground**
6	NRSTPD	I	**Not Reset and Power Down:** When LOW, internal current sinks are switched off, the oscillator is inhibited, and the input pads are disconnected from the outside world. With a positive edge on this pin the internal reset phase starts.
7	SIGIN	I	**Communication Interface Input:** accepts a digital, serial data stream
8	SIGOUT	O	**Communication Interface Output**: delivers a serial data stream
9	SVDD	PWR	**S2C Pad Power Supply:** provides power to the S^2C pads
10	TVSS	PWR	**Transmitter Ground:** supplies the output stage of TX1 and TX2
11	TX1	O	**Transmitter 1:** modulates the 13.56 MHz energy carrier
12	TVDD	PWR	**Transmitter Power Supply:** supplies the output stage of TX1 and TX2
13	TX2	O	**Transmitter 2:** modulates the 13.56 MHz energy carrier
14	TVSS	PWR	**Transmitter Ground:** supplies the output stage of TX1 and TX2
15	AVDD	PWR	**Analog Power Supply**
16	VMID	PWR	**Internal Reference Voltage:** This pin delivers the internal reference voltage.
17	RX	I	**Receiver Input**
18	AVSS	PWR	**Analog Ground**
19	AUX1	O	**Auxiliary Outputs:** These pins are used for testing.
20	AUX2	O	
21	OSCIN	I	**Crystal Oscillator Input:** input to the inverting amplifier of the oscillator. This pin is also the input for an externally generated clock (27.12 MHz = f_{osc}).
22	OSCOUT	O	**Crystal Oscillator Output:** Output of the inverting amplifier of the oscillator.
23	IRQ	O	**Interrupt Request:** output to signal an interrupt event
24	ALE-UART	I	**Address Latch Enable:** signal to latch AD0 to AD5 into the internal address latch when HIGH.
25	I^2C ADR5	I/O	see Table 110 on page 47
26	I^2C ADR4	I/O	see Table 110 on page 47
27	I^2C ADR3	I/O	see Table 110 on page 47
28	I^2C ADR2	I/O	see Table 110 on page 47
29	DTRQ/SCK/ADR1	I/O	see Table 110 on page 47
30	MX/MOSI/ADR0	I/O	see Table 110 on page 47
31	TX/MISO/SCL	I/O	see Table 110 on page 47
32	SPI SEL	I	**Address Line**

8. Functional description

PT501 transceiver IC supports the following operating modes:

- Card Operation mode supporting ISO/IEC 14443A/MIFARE and FeliCa scheme
- NFCIP-1 mode

The modes support different transfer speeds and modulation schemes. The following chapters will explain the different modes in detail.

All indicated modulation indices and modes in this chapter are system parameters. This means that beside the IC settings a suitable antenna tuning is required to achieve the optimum performance.

8.1 NFCIP-1 mode

The NFCIP-1 communication differentiates between an active and a passive Communication mode.

- Active Communication mode means both the initiator and the target are using their own RF field to transmit data.
- Passive Communication mode means that the target answers to an initiator command in a load modulation scheme. The initiator is active in terms of generating the RF field.
- Initiator: generates RF field at 13.56 MHz and starts the NFCIP-1 communication
- Target: responds to initiator command either in a load modulation scheme in Passive Communication mode or using a self generated and self modulated RF field for Active Communication mode.

The PT501 only supports the Passive Communication Mode as a Target and can use transfer speeds at 106 kbit/s, 212 kbit/s and 424 kbit/s.

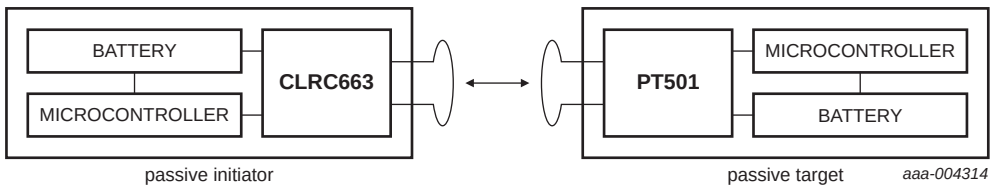


Fig 4. NFCIP-1 mode

Passive Communication mode means that the target (PT501) answers to an initiator command in a load modulation scheme. The initiator (e.g. CLRC663) is generating the RF field.

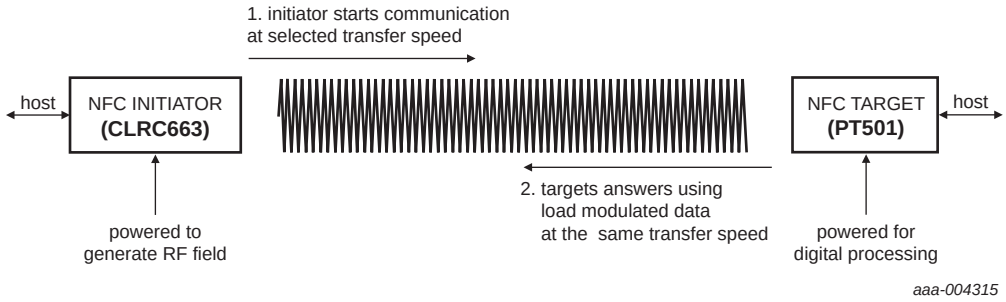


Fig 5. Passive communication mode

Table 4. Communication overview for Passive communication mode

Communication direction	106 kbit/s	212 kbit/s	424 kbit/s
Initiator → Target	According to ISO/IEC 14443A 100 % ASK, Modified Miller Coded	According to FeliCa, 8-30 % ASK Manchester Coded	
Target → Initiator	According to ISO/IEC 14443A subcarrier load modulation, Manchester Coded	According to FeliCa, > 12 % ASK Manchester Coded	

The contactless UART of PT501 and a dedicated host controller are required to handle the NFCIP-1 protocol.

Transfer Speeds above 424 kbit/s are not defined in the NFCIP-1 standard.

8.1.1 NFCIP-1 framing and coding

Table 5. Framing and coding overview

Transfer speed	Framing and Coding
106 kbit/s	According to the ISO/IEC 14443A/MIFARE scheme
212 kbit/s	According to the FeliCa scheme
424 kbit/s	According to the FeliCa scheme

8.1.2 NFCIP-1 protocol support

The NFCIP-1 protocol is not completely described in this document. For detailed explanation of the protocol refer to the NFCIP-1 standard. However the datalink layer is according to the following policy:

- Speed shall not be changed while continuum data exchange in a transaction.
- Transaction includes initialization and anticollision methods and data exchange (in continuous way, meaning no interruption by another transaction).

8.2 Card operation mode

The PT501 offers the possibility to operate as an active card. The card supports the ISO/IEC 14443-A as well as the FeliCa compliant protocol.

8.3 ISO/IEC 14443-A Card operation mode

Table 6. ISO/IEC 14443-A Card operation mode

Communication direction		**ISO/IEC 14443A/ MIFARE**
	transfer speed	**106 kbit/s**
reader/writer → PT501	Modulation on reader side	100 % ASK
	bit coding	Modified Miller
	Bitlength	(128/13.56) μs
PT501 → reader/writer	Modulation on PT501 side	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16
	bit coding	Manchester coding

As the PT501 does not have a UID as defined in ISO/IEC 14443, it is not possible to emulate any cards with Unique Identifier. The product has no CRYPTO1 implemented, as such the emulation of a e.g. MIFARE Classic is not possible.

8.4 FeliCa Card operation mode

Table 7. FeliCa Card operation mode

Communication direction		**FeliCa**	**FeliCa Higher transfer speeds**
	Transfer speed	**212 kbit/s**	**424 kbit/s**
reader/writer → PT501	Modulation on reader side	8-30 % ASK	8-30 % ASK
	bit coding	Manchester Coding	Manchester Coding
	Bitlength	(64/13.56) μs	(32/13.56) μs
PT501 → reader/writer	Load modulation on PT501 side	> 12 % ASK load modulation	> 12 % ASK load modulation
	bit coding	Manchester coding	Manchester coding

9. PT501 register SET

9.1 PT501 registers overview

Table 8. PT501 registers overview

Addr (hex)	Register Name	Function
Command and Status		
00	RFU	Reserved for Future Use
01	CommandReg	Starts and stops command execution
02	CommIEnReg	Controls bits to enable and disable the passing of Interrupt Requests
03	DivlEnReg	Controls bits to enable and disable the passing of Interrupt Requests
04	CommIRqReg	Contains Interrupt Request bits
05	DivIRqReg	Contains Interrupt Request bits
06	ErrorReg	Error bits showing the error status of the last command executed
07	Status1Reg	Contains status bits for communication
08	Status2Reg	Contains status bits of the receiver and transmitter
09	FIFODataReg	In- and output of 64 byte FIFO-buffer
0A	FIFOLevelReg	Indicates the number of bytes stored in the FIFO
0B	WaterLevelReg	Defines the level for FIFO under- and overflow warning
0C	ControlReg	Contains miscellaneous Control Registers
0D	RFU	Reserved for future use
0E	CollReg	Defines the first bit collision detected on the RF interface
0F	RFU	Reserved for future use
Command		
10	RFU	Reserved for Future Use
11	ModeReg	Defines general modes for transmitting and receiving
12	TxModeReg	Defines the data rate and framing during transmission
13	RxModeReg	Defines the data rate and framing during receiving
14	TxControlReg	Controls the logical behavior of the antenna driver pins TX1 and TX2
15	TxAutoReg	Controls the setting of the antenna drivers
16	TxSelReg	Selects the internal sources for the antenna driver
17	RxSelReg	Selects internal receiver settings
18	RxThresholdReg	Selects thresholds for the bit decoder
19	DemodReg	Defines demodulator settings
1A	RFU	Reserved for Future Use
1B	FelNFC2Reg	Defines the length of the valid range for the receive package
1C	MifNFCReg	Controls the communication in ISO/IEC 14443/MIFARE and NFC target mode at 106 kbit
1D	ManualRCVReg	Allows manual fine tuning of the internal receiver
1E	RFU	Reserved for Future Use

Table 8. PT501 registers overview *...continued*

Addr (hex)	Register Name	Function
1F	SerialSpeedReg	Selects the speed of the serial UART interface
Configuration		
20	RFU	Reserved for Future Use
21	CRCResultReg	Shows the actual MSB and LSB values of the CRC calculation
22		
23	GsNOffReg	Selects the conductance of the antenna driver pins TX1 and TX2 for modulation, shall be set to 3F
24	RFU	Reserved for Future Use
25	TxBitPhaseReg	Adjust the TX bit phase at 106 kbit
26	RFCfgReg	Configures the receiver gain and RF level, sets delay of the load maximum carrier modulation
27	RFU	Reserved for Future Use
28	RFU	Reserved for Future Use
29	RFU	Reserved for Future Use
2A	TModeReg TPrescalerReg	Defines settings for the internal timer
2B		
2C	TReloadReg	Describes the 16-bit timer reload value
2D		
2E	TCounterValReg	Shows the 16-bit actual timer value
2F		
TestRegister		
30	RFU	Reserved for Future Use
31	TestSel1Reg	General test signal configuration
32	TestSel2Reg	General test signal configuration and PRBS control
33	TestPinEnReg	
34	RFU	Reserved for Future Use
35	TestBusReg	Shows the status of the internal testbus
36	AutoTestReg	Controls the digital selftest
37	VersionReg	Shows the version
38	AnalogTestReg	Controls the pins AUX1 and AUX2
39	TestDAC1Reg	Defines the test value for the TestDAC1
3A	TestDAC2Reg	Defines the test value for the TestDAC2
3B	TestADCReg	Shows the actual value of ADC I and Q
3C-F	RFTReg	Reserved for production tests

9.1.1 Register bit behavior

Depending on the functionality of a register, the access conditions and value to the register can vary. In principle bits with same behavior are grouped in common registers. In Table 9 the access conditions are described.

Table 9. Behavior of register bits and its designation

Abbreviation	Behavior	Description
r/w	read and write	These bits can be written and read by the μ-Controller. Since they are used only for control means, there content is not influenced by internal state machines, e.g. the PageSelect-Register may be written and read by the μ-Controller. It will also be read by internal state machines, but never changed by them.
dy	dynamic	These bits can be written and read by the μ-Controller. Nevertheless, they may also be written automatically by internal state machines, e.g. the Command-Register changes its value automatically after the execution of the actual command.
r	read only	These registers hold bits, which value is determined by internal states only, e.g. the CRCReady bit can not be written from external but shows internal states.
w	write only	Reading these registers returns always ZERO.
-	not defined	Access is not defined.
RFU	-	These registers are reserved for future use. The value is not fixed.
RFT	-	These registers are reserved for production tests and shall not be changed.

9.2 Register description

9.2.1 Command and status

9.2.1.1 CommandReg

Starts and stops command execution.

Table 10. CommandReg register (address 01h); reset value: 20h, 00100000b

	7	6	5	4	3	2	1	0
	0	0	RcvOff	Power Down	Command			
Access Rights	-	-	r/w	dy	dy	dy	dy	dy

Table 11. Description of CommandReg bits

Bit	Symbol	Description
7 to 6	-	Reserved for future use.
5	RcvOff	Set to 1, the analog part of the receiver is switched off.
4	PowerDown	Set to 1, Soft Power-down mode is entered. Set to 0, the PT501 starts the wake up procedure. During this procedure this bit still shows a 1. A 0 indicates that the PT501 is ready for operations; see Section 15.2 “Soft power-down mode”. Note: The bit Power Down cannot be set, when the command SoftReset has been activated.
3 to 0	Command	Activates a command according to the Command Code. Reading this register shows, which command is actually executed (see Section 18.3 “PT501 command overview”).

9.2.1.2 CommIEnReg

Control bits to enable and disable the passing of interrupt requests.

Table 12. CommIEnReg register (address 02h); reset value: 80h, 10000000b

	7	6	5	4	3	2	1	0
	IRqInv	TxIEn	RxIEn	IdleIEn	HiAlertIEn	LoAlertIEn	ErrIEn	TimerIEn
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 13. Description of CommIEnReg bits

Bit	Symbol	Description
7	IRqInv	Set to 1, the signal on pin IRQ is inverted with respect to bit IRq in the register Status1Reg. Set to 0, the signal on pin IRQ is equal to bit IRq. In combination with bit IRqPushPull in register DivIEnReg, the default value of 1 ensures, that the output level on pin IRQ is 3-state.
6	TxIEn	Allows the transmitter interrupt request (indicated by bit TxIRq) to be propagated to pin IRQ.
5	RxIEn	Allows the receiver interrupt request (indicated by bit RxIRq) to be propagated to pin IRQ.
4	IdleIEn	Allows the idle interrupt request (indicated by bit IdleIRq) to be propagated to pin IRQ.

Table 13. Description of CommIEnReg bits *…continued*

Bit	Symbol	Description
3	HiAlertIEn	Allows the high alert interrupt request (indicated by bit HiAlertIRq) to be propagated to pin IRQ.
2	LoAlertIEn	Allows the low alert interrupt request (indicated by bit LoAlertIRq) to be propagated to pin IRQ.
1	ErrIEn	Allows the error interrupt request (indicated by bit ErrIRq) to be propagated to pin IRQ.
0	TimerIEn	Allows the timer interrupt request (indicated by bit TimerIRq) to be propagated to pin IRQ.

9.2.1.3 DivIEnReg

Control bits to enable and disable the passing of interrupt requests.

Table 14. DivIEnReg register (address 03h); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	IRQPushPull	0	0	SiginActIEn	ModeIEn	CRCIEn	RFOnIEn	RFOffIEn
Access Rights	r/w	-	-	r/w	r/w	r/w	r/w	r/w

Table 15. Description of DivIEnReg bits

Bit	Symbol	Description
7	IRQPushPull	Set to 1, the pin IRQ works as standard CMOS output pad. Set to 0, the pin IRQ works as open drain output pad.
6 to 5	0	Is set to 0.
4	SiginActIEn	Allows the SIGIN active interrupt request to be propagated to pin IRQ.
3	ModeIEn	Allows the mode interrupt request (indicated by bit ModeIRq) to be propagated to pin IRQ.
2	CRCIEn	Allows the CRC interrupt request (indicated by bit CRCIRq) to be propagated to pin IRQ.
1	RfOnIEn	Allows the RF field on interrupt request (indicated by bit RfOnIRq) to be propagated to pin IRQ.
0	RfOffIEn	Allows the RF field off interrupt request (indicated by bit RfOffIRq) to be propagated to pin IRQ.

9.2.1.4 CommIRqReg

Contains Interrupt Request bits.

Table 16. CommIRqReg register (address 04h); reset value: 14h, 00010100b

	7	6	5	4	3	2	1	0
	Set1	TxIRq	RxIRq	IdleIRq	HiAlertIRq	LoAlertIRq	ErrIRq	TimerIRq
Access Rights	w	dy	dy	dy	dy	dy	dy	dy

Table 17. Description of CommIRqReg bits

All bits in the register CommIRqReg shall be cleared by software.

Bit	Symbol	Description
7	Set1	Set to 1, Set1 defines that the marked bits in the register CommIRqReg are set. Set to 0, Set1 defines, that the marked bits in the register CommIRqReg are cleared.
6	TxIRq	Set to 1 immediately after the last bit of the transmitted data was sent out.
5	RxIRq	Set to 1 when the receiver detects the end of a valid datastream. If the bit RxNoErr in register RxModeReg is set to 1, bit RxIRq is only set to 1 when data bytes are available in the FIFO.
4	IdleIRq	Set to 1, when a command terminates by itself e.g. when the CommandReg changes its value from any command to the Idle Command. If an unknown command is started, the CommandReg changes its content to the idle state and the bit IdleIRq is set. Starting the Idle Command by the μ-Controller does not set bit IdleIRq.
3	HiAlertIRq	Set to 1, when bit HiAlert in register Status1Reg is set. In opposition to HiAlert, HiAlertIRq stores this event and can only be reset as indicated by bit Set1.
2	LoAlertIRq	Set to 1, when bit LoAlert in register Status1Reg is set. In opposition to LoAlert, LoAlertIRq stores this event and can only be reset as indicated by bit Set1.
1	ErrIRq	Set to 1 if any error bit in the Error Register is set.
0	TimerIRq	Set to 1 when the timer decrements the TimerValue Register to zero.

9.2.1.5 DivIRqReg

Contains Interrupt Request bits

Table 18. DivIRqReg register (address 05h); reset value: XXh, 000X00XXb

	7	6	5	4	3	2	1	0
	Set2	0	0	0	ModeIRq	CRCIRq	RFOnIRq	RFOffIRq
Access Rights	w	-	-	dy	dy	dy	dy	dy

Table 19. Description of DivIRqReg bits

All bits in the register DivIRqReg shall be cleared by software.

Bit	Symbol	Description
7	Set2	Set to 1, Set2 defines that the marked bits in the register DivIRqReg are set. Set to 0, Set2 defines, that the marked bits in the register DivIRqReg are cleared
6 to 5	0	Is set to 0.
4	0	Is set to 0.
3	ModeIRq	Set to 1, when the mode has been detected by the Data mode detector. The Data mode detector can only be activated by the AutoColl command and is terminated automatically having detected the Communication mode. The Data mode detector is automatically restarted after each RF Reset.
2	CRCIRq	Set to 1, when the CRC command is active and all data are processed.
1	RFOnIRq	Set to 1, when an external RF field is detected.
0	RFOffIRq	Set to 1, when a present external RF field is switched off.

9.2.1.6 ErrorReg

Error bit register showing the error status of the last command executed.

Table 20. ErrorReg register (address 06h); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	WrErr	RFU	RFU	BufferOvfl	CollErr	CRCErr	ParityErr	ProtocolErr
Access Rights	r	r	r	r	r	r	r	r

Table 21. Description of ErrorReg bits

Bit	Symbol	Description
7	WrErr	Set to 1, when data is written into FIFO by the host controller during the AutoColl command or if data is written into FIFO by the host controller during the time between sending the last bit on the RF interface and receiving the last bit on the RF interface.
6	RFU	Reserved for Future Use
5	RFU	Reserved for Future Use
4	BufferOvfl	Set to 1, if the host controller or a PT501's internal state machine (e.g. receiver) tries to write data into the FIFO-bufferFIFO-buffer although the FIFO-buffer is already full.
3	CollErr	Set to 1, if a bit-collision is detected. It is cleared automatically at receiver start-up phase. This bit is only valid during the bitwise anticollision at 106 kbit. During communication schemes at 212 and 424 kbit this bit is always set to 1.
2	CRCErr	Set to 1, if bit RxCRCEn in register RxModeReg is set and the CRC calculation fails. It is cleared to 0 automatically at receiver start-up phase.
1	ParityErr	Set to 1, if the parity check has failed. It is cleared automatically at receiver start-up phase. Only valid for ISO/IEC 14443A or NFCIP-1 communication at 106 kbit.
0	ProtocolErr	Set to 1, if one out of the following cases occur: • Set to 1 if the SOF is incorrect. It is cleared automatically at receiver start-up phase. The bit is only valid for 106 kbit. • During the AutoColl command, bit ProtocolErr is set to 1, if the bit Initiator in register ControlReg is set to 1. • Set to 1, if the Miller Decoder detects 2 pulses below the minimum time according to the ISO/IEC 14443A definitions.

9.2.1.7 Status1Reg

Contains status bits of the CRC, Interrupt and FIFO-buffer.

Table 22. Status1Reg register (address 07h); reset value: XXh, X100X01Xb

	7	6	5	4	3	2	1	0
	RFFreqOK	CRCOk	CRCReady	IRq	TRunning	RFOn	HiAlert	LoAlert
Access Rights	r	r	r	r	r	r	r	r

Table 23. Description of Status1Reg bits

Bit	Symbol	Description
7	RFFreqOK	Indicates if the frequency detected at the RX pin is in the range of 13.56 MHz. Set to 1, if the frequency at the RX pin is in the range 12 MHz < RX pin frequency < 15 MHz. Note: The value of RFFreqOK is not defined if the external RF frequency is in the range from 9 to 12 MHz or in the range from 15 to 19 MHz.
6	CRCOk	Set to 1, if the CRC Result is zero. For data transmission and reception the bit CRCOk is undefined (use CRCErr in register ErrorReg). CRCOk indicates the status of the CRC co-processor, during calculation the value changes to ZERO, when the calculation is done correctly, the value changes to ONE.
5	CRCReady	Set to 1, when the CRC calculation has finished. This bit is only valid for the CRC co-processor calculation using the command CalcCRC.
4	IRq	This bit shows, if any interrupt source requests attention (with respect to the setting of the interrupt enable bits, see register CommIEnReg and DivIEnReg).
3	TRunning	Set to 1, if the PT501's timer unit is running, e.g. the timer will decrement the TCounterValReg with the next timer clock. Note: In the gated mode the bit TRunning is set to 1, when the timer is enabled by the register bits. This bit is not influenced by the gated signal.
2	RFOn	Set to 1, if an external RF field is detected. This bit does not store the state of the RF field.
1	HiAlert	Set to 1, when the number of bytes stored in the FIFO-buffer fulfills the following equation: $HiAlert = (64 - FIFOLength) \leq WaterLevel$ Example: FIFOLength = 60, WaterLevel = 4 → HiAlert = 1 FIFOLength = 59, WaterLevel = 4 → HiAlert = 0
0	LoAlert	Set to 1, when the number of bytes stored in the FIFO-buffer fulfills the following equation: $LoAlert = FIFOLength \leq WaterLevel$ Example: FIFOLength = 4, WaterLevel = 4 → LoAlert = 1 FIFOLength = 5, WaterLevel = 4 → LoAlert = 0

9.2.1.8 Status2Reg

Contains status bits of the Receiver, Transmitter and Data mode detector.

Table 24. Status2Reg register (address 08h); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	RFU	I^2CForceHS	0	TargetActivated	RFU	Modem State		
Access Rights	r/w	r/w	-	dy	dy	r	r	r

Table 25. Description of Status2Reg bits

Bit	Symbol	Description	
7	RFU	Reserved for Future Use	
6	I^2CForceHS	I^2C input filter settings. Set to 1, the I^2C input filter is set to the High-speed mode independent of the I^2C protocol. Set to 0, the I^2C input filter is set to the used I^2C protocol.	
5	0	Is set to 0.	
4	TargetActivated	Shall be set to 1	
3	RFU	Reserved for Future Use	
2 to 0	Modem State	ModemState shows the state of the transmitter and receiver state machines.	
		Value	**Description**
		000	IDLE
		001	Wait for StartSend in register BitFramingReg
		010	TxWait: Wait until RF field is present, if the bit TxWaitRF is set to 1. The minimum time for TxWait is defined by the TxWaitReg register.
		011	Sending
		100	RxWait: Wait until RF field is present, if the bit RxWaitRF is set to 1. The minimum time for RxWait is defined by the RxWaitReg register.
		101	Wait for data
		110	Receiving

9.2.1.9 FIFODataReg

In- and output of 64 byte FIFO-buffer.

Table 26. FIFODataReg register (address 09h); reset value: XXh, XXXXXXXXb

	7	6	5	4	3	2	1	0
	FIFOData							
Access Rights	dy	dy	dy	dy	dy	dy	dy	dy

Table 27. Description of FIFODataReg bits

Bit	Symbol	Description
7 to 0	FIFOData	Data input and output port for the internal 64 byte FIFO-buffer. The FIFO-buffer acts as parallel in/parallel out converter for all serial data stream in- and outputs.

9.2.1.10 FIFOLevelReg

Indicates the number of bytes stored in the FIFO.

Table 28. FIFOLevelReg register (address 0Ah); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	FlushBuffer	FIFOLevel						
Access Rights	w	r	r	r	r	r	r	r

Table 29. Description of FIFOLevelReg bits

Bit	Symbol	Description
7	FlushBuffer	Set to 1, this bit clears the internal FIFO-buffer's read- and write-pointer and the bit BufferOvfl in the register ErrReg immediately. Reading this bit will always return 0.
6 to 0	FIFOLevel	Indicates the number of bytes stored in the FIFO-buffer. Writing to the FIFODataReg increments, reading decrements the FIFOLevel.

9.2.1.11 WaterLevelReg

Defines the level for FIFO under- and overflow warning.

Table 30. WaterLevelReg register (address 0Bh); reset value: 08h, 00001000b

	7	6	5	4	3	2	1	0
	0	0	WaterLevel					
Access Rights	-	-	r/w	r/w	r/w	r/w	r/w	r/w

Table 31. Description of WaterLevelReg bits

Bit	Symbol	Description
7 to 6	0	Is set to 0.
5 to 0	WaterLevel	This register defines a warning level to indicate a FIFO-buffer over- or underflow: The bit HiAlert in Status1Reg is set to 1, if the remaining number of bytes in the FIFO-buffer space is equal or less than the defined number of WaterLevel bytes. The bit LoAlert in Status1Reg is set to 1, if equal or less than WaterLevel bytes are in the FIFO. Note: For the calculation of HiAlert and LoAlert see Table 23

9.2.1.12 ControlReg

Miscellaneous control bits.

Table 32. ControlReg register (address 0Ch); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	TStopNow	TStartNow	WrNFCIDtoFIFO	0	0	RxLastBits		
Access Rights	w	w	dy	-	-	r	r	r

Table 33. Description of ControlReg bits

Bit	Symbol	Description
7	TStopNow	Set to 1, the timer stops immediately. Reading this bit will always return 0.
6	TStartNow	Set to 1 starts the timer immediately. Reading this bit will always return 0.
5	WrNFCIDtoFIFO	Set to 1, the internal stored NFCID (10 bytes) is copied into the FIFO. The NFC ID an be configured using the command Section 18.3.1.2 “Config command” on page 70. Afterwards the bit is cleared automatically. This is needed to provide the ‘name’ of the card (e.g. UID). This is needed for card operation.
4	0	Is set to 0.
3	0	Is set to 0.
2 to 0	RxLastBits	Shows the number of valid bits in the last received byte. If zero, the whole byte is valid.

9.2.1.13 CollReg

Defines the first bit collision detected on the RF interface.

Table 34. CollReg register (address 0Eh); reset value: XXh, 101XXXXXb

	7	6	5	4	3	2	1	0
	1	0	1			x		
Access Rights	r/w	-	r	r	r	r	r	r

Table 35. Description of CollReg bits

Bit	Symbol	Description
7	1	Shall be set to 1.
6	0	Shall be set to 0.
5	1	Shall be set to 1.
4 to 0	x	These bits cannot be interpreted.

9.2.2 Communication

9.2.2.1 ModeReg

Defines general mode settings for transmitting and receiving.

Table 36. ModeReg register (address 11h); reset value: 3Bh, 00111011b

	7	6	5	4	3	2	1	0
	MSBFirst	DetectSync	RFU	RFU	RFU	ModeDetOff	CRCPreset	
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 37. Description of ModeReg bits

Bit	Symbol	Description	
7	MSBFirst	Set to 1, the CRC co-processor calculates the CRC with MSB first and the CRCResultMSB and the CRCResultLSB in the CRCResultReg register are bit reserved. During RF communication this bit is ignored.	
6	DetectSync	If set to 1, the contactless UART waits for the value F0h before the receiver is activated, and F0h is added as a Sync-byte for transmission. The bit is only valid for 106 Kbit NFCIP-1 data exchange. Else the bit shall be set to 0.	
5	RFU	Shall be set to 1.	
4	RFU	Shall be set to 1.	
3	RFU	Shall be set to 1. Changing this bit to 0 will generate a SiginActIRq event.	
2	ModeDetOff	Set to 1, the internal mode detector is switched off. The mode detector is only active during the AutoColl command.	
1 to 0	CRCPreset	Defines the preset value for the CRC co-processor for the command CalCRC. During any communication, the preset values is selected automatically according to the definition in the bits RxMode and TxMode.	
		Value	**Description**
		00	0000
		01	6363
		10	A671
		11	FFFF

9.2.2.2 TxModeReg

Defines the data rate and framing during transmission.

Table 38. TxModeReg register (address 12h); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	TxCRCEn	TxSpeed			InvMod	0	TxFraming	
Access Rights	r/w	dy	dy	dy	r/w	r/w	dy	dy

Table 39. Description of TxModeReg bits

Bit	Symbol	Description	
7	TxCRCEn	Set to 1, this bit enables the CRC generation during data transmission. Note: This bit shall only be set to 0 at 106 kbit.	
6 to 4	TxSpeed	Defines the bit rate while data transmission.	
		Value	**Description**
		000	106 kbit
		001	212 kbit
		010	424 kbit
3	InvMod	Is set to 0.	
2	0	Is set to 0.	
1 to 0	TxFraming	Defines the framing used for data transmission.	
		Value	**Description**
		00	ISO/IEC 14443-A 106 kbit
		10	FeliCa 212 and 424 kbit

9.2.2.3 RxModeReg

Defines the data rate and framing during reception.

Table 40. RxModeReg register (address 13h); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	RxCRCEn	RxSpeed			RxNoErr	0	RxFraming	
Access Rights	r/w	dy	dy	dy	r/w	r/w	dy	dy

Table 41. Description of RxModeReg bits

Bit	Symbol	Description	
7	RxCRCEn	Set to 1, this bit enables the CRC calculation during reception. Note: This bit shall only be set to 0 at 106 kbit.	
6 to 4	RxSpeed	Defines the bit rate while data transmission. The PT501's analog part handles only transfer speeds up to 424 kbit internally.	
		Value	**Description**
		000	106 kbit
		001	212 kbit
		010	424 kbit
3	RxNoErr	If set to 1 a not valid received data stream (less than 4 bits received) will be ignored. The receiver will remain active.	
2	0	Shall be set to 0	
1 to 0	RxFraming	Defines the expected framing for data reception.	
		Value	**Description**
		00	ISO/IEC 14443A 106 kbit
		10	FeliCa 212 and 424 kbit

9.2.2.4 TxControlReg

Controls the logical behavior of the antenna driver pins Tx1 and Tx2.

Table 42. TxControlReg register (address 14h); reset value: 80h, 10000000b

	7	6	5	4	3	2	1	0
	0	0	InvTx2RF Off	InvTx1RF Off	0	0	0	0
Access Rights	r/w	r/w	r/w	r/w	r/w	w	r/w	r/w

Table 43. Description of TxControlReg bits

Bit	Symbol	Description
7	0	Shall be set to 0
6	0	Shall be set to 0
5	InvTx2RFOff	Set to 1, the output signal at pin TX2 will be inverted. Bit 5 and bit 4 shall be the same value.
4	InvTx1RFOff	Set to 1, the output signal at pin TX1 will be inverted.
3	0	Shall be set to 0
2	0	Shall be set to 0
1	0	Shall be set to 0
0	0	Shall be set to 0

9.2.2.5 TxAutoReg

Controls the settings of the antenna driver.

Table 44. TxAutoReg register (address 15h); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	0	0	Auto WakeUp	0	0	0	0	0
Access Rights	r/w	r/w	r/w	RFU	r/w	r/w	r/w	r/w

Table 45. Description of TxAutoReg bits

Bit	Symbol	Description
7	0	Shall be set to 0
6	0	Shall be set to 0
5	AutoWakeUp	Set to 1, the PT501 in soft Power-down mode will be started by the RF level detector.
4	0	Reserved for future use.
3	0	Shall be set to 0
2	0	Shall be set to 0
1	0	Shall be set to 0
0	0	Shall be set to 0

9.2.2.6 TxSelReg

Selects the sources for the analog part.

Table 46. TxSelReg register (address 16h); reset value: 10h, 00010000b

	7	6	5	4	3	2	1	0
	0	0	DriverSel		SigOutSel			
Access Rights	-	-	r/w	r/w	r/w	r/w	r/w	r/w

Table 47. Description of TxSelReg bits

Bit	Symbol	Description	
7 to 6	0	Is set to 0.	
5 to 4	DriverSel	Selects the input of driver Tx1 and Tx2.	
		Value	**Description**
		00	Tristate Note: In soft power down the drivers are only in Tristate mode if DriverSel is set to Tristate mode.
		01	Modulation signal (envelope) from the internal coder
		10	Modulation signal (envelope) from SIGIN
		11	HIGH
3 to 0	SigOutSel	Selects the input for the SIGOUT Pin.	
		Value	**Description**
		0000	Tristate
		0001	Low
		0010	High
		0011	TestBus signal as defined by bit TestBusBitSel in register TestSel1Reg.
		0100	Modulation signal (envelope) from the internal coder
		0101	Serial data stream to be transmitted
		0110	Output signal of the receiver circuit (card modulation signal regenerated and delayed). This signal is used as data output signal for SAM interface connection using 3 lines. Note: To have a valid signal the PT501 has to be set to the receiving mode by either the Transceive or Receive command.
		0111	Serial data stream received.
		1000-1011	FeliCa Sam modulation 1000 RX* 1010 Demodulator comparator output 1011 RFU Note: * To have a valid signal the PT501 has to be set to the receiving mode by either the Transceive or Receive command.
		1100-1111	MIFARE Sam modulation 1100 RX* with RF carrier 1110 RX with RF carrier un-filtered 1111 RX envelope un-filtered Note: *To have a valid signal the PT501 has to be set to the receiving mode by either the Transceive or Receive command.

9.2.2.7 RxSelReg

Selects internal receiver settings.

Table 48. RxSelReg register (address 17h); reset value: 84h, 10000100b

	7	6	5	4	3	2	1	0
	UartSel		RxWait					
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 49. Description of RxSelReg bits

Bit	Symbol	Description	
7 to 6	UartSel	Selects the input of the contactless UART	
		Value	**Description**
		00	Constant Low
		01	Envelope signal at SIGIN
		10	Modulation signal from the internal analog part
		11	Modulation signal from SIGIN pin. Only valid for transfer speeds above 424 kbit
5 to 0	RxWait	After data transmission, the activation of the receiver is delayed for RxWait bit-clocks. During this 'frame guard time' any signal at pin RX is ignored. This parameter is ignored by the Receive command. All other commands (e.g. Autocoll) use this parameter. Depending on the mode of the PT501, the counter starts with the last modulation pulse of the transmitted data stream.	

9.2.2.8 RxThresholdReg

Selects thresholds for the bit decoder.

Table 50. RxThresholdReg register (address 18h); reset value: 84h, 10000100b

	7	6	5	4	3	2	1	0
	MinLevel				0	CollLevel		
Access Rights	r/w	r/w	r/w	r/w	-	r/w	r/w	r/w

Table 51. Description of RxThresholdReg bits

Bit	Symbol	Description
7 to 4	MinLevel	Defines the minimum signal strength at the decoder input that shall be accepted. If the signal strength is below this level, it is not evaluated.
3	0	Shall be set to 0.
2 to 0	CollLevel	Defines the minimum signal strength at the decoder input that has to be reached by the weaker half-bit of the Manchester-coded signal to generate a bit-collision relatively to the amplitude of the stronger half-bit.

9.2.2.9 DemodReg

Defines demodulator settings.

Table 52. DemodReg register (address 19h); reset value: 4Dh, 01001101b

	7	6	5	4	3	2	1	0
	0	1	FixIQ	TPrescal Even	TauRcv		TauSync	
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 53. Description of DemodReg bits

Bit	Symbol	Description
7 to 6	01	Shall be set to 01.
5	FixIQ	If set to 1 and the bits of AddIQ are set to X0, the reception is fixed to I channel. NOTE: If SIGIN/SIGOUT is used as S2C interface FixIQ set to 1 and AddIQ set to X0 is rewired.
4	TPrescalEven	If set to 0 the following formula is used to calculate fTimer of the prescaler: f_{Timer} = 13.56 MHz / (2 * TPreScaler + 1). If set to 1 the following formula is used to calculate fTimer of the prescaler: fTimer = 13.56 MHz / (2 * TPreScaler + 2). (Default TPrescalEven is 0)
3 to 2	TauRcv	Changes the time constant of the internal during data reception. Note: If set to 00, the PLL is frozen during data reception.
1 to 0	TauSync	Changes the time constant of the internal PLL during burst.

9.2.2.10 FelNFC2Reg

Defines the maximum length of the received packet.

Table 54. FelNFC2Reg register (address1Bh); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	WaitForSelected	ShortTimeSlot	0					
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 55. Description of FelNFC2Reg bits

Bit	Symbol	Description
7	WaitForSelected	Set to 1, the AutoColl command is only terminated automatically when: 1. A valid command has been received after performing a valid Select procedure according ISO/IEC 14443A. 2. A valid command has been received after performing a valid Polling procedure according to the FeliCa specification. Note: If this bit is set, no active communication is possible. Note: Setting this bit reduces the host controller interaction in case of a communication to another device in the same RF field during Passive Communication mode.
6	ShortTimeSlot	Defines the time slot length for Passive Communication mode at 424 kbit. Set to 1 a short time slot is used (half of the timeslot at 212 kbit). Set to 0 a long timeslot is used (equal to the timeslot for 212 kbit).
5 to 0	0	Shall be set to 0

9.2.2.11 MifNFCReg

Defines ISO/IEC 14443A/MIFARE/NFC specific settings in target or Card Operating mode.

Table 56. MifNFCReg register (address 1Ch); reset value: 62h, 01100010b

	7	6	5	4	3	2	1	0
	SensMiller			TauMiller		MFHalted	TxWait	
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 57. Description of MifNFCReg bits

Bit	Symbol	Description
7 to 5	SensMiller	These bits define the sensitivity of the Miller decoder.
4 to 3	TauMiller	These bits define the time constant of the Miller decoder.
2	MFHalted	Set to 1, this bit indicates that the PT501 is set to HALT mode in Card Operation mode at 106 kbit. This bit is either set by the host controller or by the internal state machine and indicates that only the code 52h is accepted as a request command. This bit is cleared automatically by a RF reset.
1 to 0	TxWait	These bits define the additional response time for the target at 106 kbit in Passive Communication mode and during the AutoColl command. Per default 7 bits are added to the value of the register bit.

9.2.2.12 ManualRCVReg

Allows manual fine tuning of the internal receiver.

Remark: For standard applications it is not recommended to change this register settings.

Table 58. ManualRCVReg register (address 1Dh); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	0	FastFilt MF_SO	Delay MF_SO	Parity Disable	LargeBW PLL	Manual HPCF	HPFC	
Access Rights	-	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 59. Description of ManualRCVReg bits

Bit	Symbol	Description
7	0	Shall be set to 0.
6	FastFilt MF_SO	If this bit is set to 1, the internal filter for the Miller-Delay Circuit is set to Fast mode. Note: This bit should only set to 1, if Millerpulses of less than 400 ns Pulse length are expected. At 106 kBaud the typical value is 3 us.
5	Delay MF_SO	If this bit is set to 1, the Signal at SIGOUT-pin is delayed, so that in SAM mode the Signal at SIGIN must be 128/fc faster compared to the ISO/IEC 14443A, to reach the ISO/IEC 14443A restrictions on the RF-Field. Note: This delay shall only be activated for setting bits SigOutSel to (1110b) or (1111b) in register TxSelReg.
4	Parity Disable	If this bit is set to 1, the generation of the Parity bit for transmission and the Parity-Check for receiving is switched off. The received Parity bit is handled like a data bit.
3	LargeBWPLL	Set to 1, the bandwidth of the internal PLL used for clock recovery is extended.
2	ManualHPCF	Set to 0, the HPCF bits are ignored and the HPCF settings are adapted automatically to the receiving mode. Set to 1, values of HPCF are valid.
1 to 0	HPFC	Selects the High Pass Corner Frequency (HPCF) of the filter in the internal receiver chain 00 For signals with frequency spectrum down to 106 kHz. 01 For signals with frequency spectrum down to 212 kHz. 10 For signals with frequency spectrum down to 424 kHz.

9.2.2.13 SerialSpeedReg

Selects the speed of the serial UART interface.

Table 60. SerialSpeedReg register (address 1Fh); reset value: EBh, 11101011b

	7	6	5	4	3	2	1	0
	BR_T0			BR_T1				
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 61. Description of SerialSpeedReg bits

Bit	Symbol	Description
7 to 5	BR_T0	Factor BR_T0 to adjust the transfer speed, for description see Section 10.3.2 “Selectable UART transfer speeds”.
4		Set to 1.
3 to 0	BR_T1	Factor BR_T1 to adjust the transfer speed, for description see Section 10.3.2 “Selectable UART transfer speeds”.

9.2.3 Configuration

9.2.3.1 CRCResultReg

Shows the actual MSB and LSB values of the CRC calculation.

Note: The CRC is split into two 8-bit register.

Table 62. CRCResultReg register (address 21h); reset value: FFh, 11111111b

	7	6	5	4	3	2	1	0
	CRCResultMSB							
Access Rights	r	r	r	r	r	r	r	r

Table 63. Description of CRCResultReg bits

Bit	Symbol	Description
7 to 0	CRCResultMSB	This register shows the actual value of the most significant byte of the CRCResultReg register. It is valid only if bit CRCReady in register Status1Reg is set to 1.

Table 64. CRCResultReg register (address 22h); reset value: FFh, 11111111b

	7	6	5	4	3	2	1	0
	CRCResultLSB							
Access Rights	r	r	r	r	r	r	r	r

Table 65. Description of CRCResultReg bits

Bit	Symbol	Description
7 to 0	CRCResultLSB	This register shows the actual value of the least significant byte of the CRCResult register. It is valid only if bit CRCReady in register Status1Reg is set to 1.

9.2.3.2 GsNOffReg

Selects the conductance for the N-driver of the antenna driver pins TX1 and TX2.

Table 66. GsNOffReg register (address 23h); reset value: 88h, 10001000b

	7	6	5	4	3	2	1	0
	CWGsNOff				ModGsNOff			
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 67. Description of GsNOffReg bits

Bit	Symbol	Description
7 to 4	CWGsNOff	The value of this register defines the conductance of the output N-driver during times of no modulation. The conductance value is binary weighted. During soft Power-down mode the highest bit is forced to 1.The value of the register is only used if the driver is switched off. Otherwise the bit value CWGsNOn of register GsNOnReg is used.This value is used for LoadModulation.
3 to 0	ModGsNOff	The value of this register defines the conductance of the output N-driver for the time of modulation. This may be used to regulate the modulation index.The conductance value is binary weighted.During soft Power-down mode the highest bit is forced to 1.The value of the register is only used if the driver is switched off. Otherwise the bit value ModGsNOn of register GsNOnReg is use.This value is used for LoadModulation.

3Fh is seen in practice as a very good value for stable operation of this product.

9.2.3.3 TxBitPhaseReg

Adjust the bitphase at 106 kbit during transmission.

Table 68. TxBitPhaseReg register (address 25h); reset value: 87h, 10000111b

	7	6	5	4	3	2	1	0
	RcvClkChange	TxBitPhase						
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 69. Description of TxBitPhaseReg bits

Bit	Symbol	Description
7	RcvClkChange	Set to 1, the demodulator’s clock is derived by the external RF field.
6 to 0	TxBitPhase	These bits are representing the number of carrier frequency clock cycles, which are added to the waiting period before transmitting data in all communication modes. TXBitPhase is used to adjust the TX bit synchronization during passive NFCIP-1 communication mode at 106 kbit and in ISO/IEC 14443 card mode.

It is seen in practice that the value 84h is a good value for stable operation

9.2.3.4 RFCfgReg

Configures the receiver gain and RF level detector sensitivity.

Table 70. RFCfgReg register (address 26h); reset value: 48h, 01001000b

	7	6	5	4	3	2	1	0
	RFLevelAmp	RxGain				RFLevel		
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 71. Description of RFCfgReg bits

Bit	Symbol	Description	
7	RFLevelAmp	Set to 1, this bit activates the RF level detectors' amplifier.	
6 to 4	RxGain	This register defines the receivers signal voltage gain factor:	
		Value	**Description**
		000	18 dB
		001	23 dB
		010	18 dB
		011	23 dB
		100	33 dB
		101	38 dB
		110	43 dB
		111	48 dB
3 to 0	RFLevel	Defines the sensitivity of the RF level detector, for description see Section 11.2 "RF level detector".	

9.2.3.5 TModeReg, TPrescalerReg

Defines settings for the timer.

Note: The Prescaler value is split into two 8-bit registers

Table 72. TModeReg register (address 2Ah); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	TAuto	0		TAutoRestart	TPrescaler_Hi			
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 73. Description of TModeReg bits

Bit	Symbol	Description
7	TAuto	If RxMultiple is set to 1, the timer never stops. In this case the timer can be stopped by setting the bit TStopNow in register ControlReg to 1. Set to 0 indicates, that the timer is not influenced by the protocol.

Table 73. Description of TModeReg bits *…continued*

Bit	Symbol	Description
6 to 5	0	Shall be set to 0.
4	TAutoRestart	Set to 1, the timer automatically restart its count-down from TReloadValue, instead of counting down to zero. Set to 0 the timer decrements to ZERO and the bit TimerIRq is set to 1.
3 to 0	TPrescaler_Hi	Defines higher 4 bits for TPrescaler. The following formula is used to calculate f_{Timer} if TPrescalEven bit in Demot Reg is set to 0: f_{Timer} = 13.56 MHz/(2*TPreScaler+1). Where TPreScaler = [TPrescaler_Hi:TPrescaler_Lo] (TPrescaler value on 12 bits) (Default TPrescalEven is 0) The following formula is used to calculate fTimer if TPrescalEven bit in Demot Reg is set to 1: f_{Timer} = 13.56 MHz/(2*TPreScaler+2). For detailed description see Section 14 “Timer unit”.

Table 74. TPrescalerReg register (address 2Bh); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	TPrescaler_Lo							
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 75. Description of TPrescalerReg bits

Bit	Symbol	Description
7 to 0	TPrescaler_Lo	Defines lower 8 bits for TPrescaler. The following formula is used to calculate f_{Timer} if TPrescalEven bit in Demot Reg is set to 0: f_{Timer} = 13.56 MHz/(2*TPreScaler+1). Where TPreScaler = [TPrescaler_Hi:TPrescaler_Lo] (TPrescaler value on 12 bits) The following formula is used to calculate fTimer if TPrescalEven bit in Demot Reg is set to 1: f_{Timer} = 13.56 MHz/(2*TPreScaler+2). Where TPreScaler = [TPrescaler_Hi:TPrescaler_Lo] (TPrescaler value on 12 bits) For detailed description see Section 14 “Timer unit”.

9.2.3.6 TReloadReg

Describes the 16-bit long timer reload value.

Note: The Reload value is split into two 8-bit registers.

Table 76. TReloadReg (Higher bits) register (address 2Ch); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	TReloadVal_Hi							
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 77. Description of the higher TReloadReg bits

Bit	Symbol	Description
7 to 0	TReloadVal_Hi	Defines the higher 8 bits for the TReloadReg. With a start event the timer loads the TReloadVal. Changing this register affects the timer only at the next start event.

Table 78. TReloadReg (Lower bits) register (address 2Dh); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	TReloadVal_Lo							
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 79. Description of lower TReloadReg bits

Bit	Symbol	Description
7 to 0	TReloadVal_Lo	Defines the lower 8 bits for the TReloadReg. With a start event the timer loads the TReloadVal. Changing this register affects the timer only at the next start event.

9.2.3.7 TCounterValReg

Contains the current value of the timer.

Note: The Counter value is split into two 8-bit register.

Table 80. TCounterValReg (Higher bits) register (address 2Eh); reset value: XXh, XXXXXXXXb

	7	6	5	4	3	2	1	0
	TCounterVal_Hi							
Access Rights	r	r	r	r	r	r	r	r

Table 81. Description of the higher TCounterValReg bits

Bit	Symbol	Description
7 to 0	TCounterVal_Hi	Current value of the timer, higher 8 bits.

Table 82. TCounterValReg (Lower bits) register (address 2Fh); reset value: XXh, XXXXXXXXb

	7	6	5	4	3	2	1	0
	TCounterVal_Lo							
Access Rights	r	r	r	r	r	r	r	r

Table 83. Description of lower TCounterValReg bits

Bit	Symbol	Description
7 to 0	TCounterVal_Lo	Current value of the timer, lower 8 bits.

9.2.4 Page 3: Test

9.2.4.1 TestSel1Reg

General test signal configuration.

Table 84. TestSel1Reg register (address 31h); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	-	-	SAMClockSel		SAMClkD1	TstBusBitSel		
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 85. Description of TestSel1Reg bits

Bit	Symbol	Description	
7 to 6	-	Reserved for future use.	
5 to 4	SAMClockSel	Defines the source for the 13.56 MHz SAM clock	
		Value	**Description**
		00	GND- Sam Clock switched off
		01	clock derived by the internal oscillator
		10	internal UART clock
		11	clock derived by the RF field
3	SAMClkD1	Set to 1, the SAM clock is delivered to I^2C ADR5, see Figure 3	
2 to 0	TstBusBitSel	Select the TestBus bit from the testbus to be propagated to SIGOUT, see Figure 3.	

9.2.4.2 TestSel2Reg

General test signal configuration and PRBS control

Table 86. TestSel2Reg register (address 32h); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	0	PRBS9	PRBS15	TestBusSel				
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 87. Description of TestSel2Reg bits

Bit	Symbol	Description
7	0	Shall be set to 0.
6	PRBS9	Starts and enables the PRBS9 sequence according ITU-TO150. Note: All relevant registers to transmit data have to be configured before entering PRBS9 mode. Note: The data transmission of the defined sequence is started by the send command.
5	PRBS15	Starts and enables the PRBS15 sequence according ITU-TO150. Note: All relevant registers to transmit data have to be configured before entering PRBS15 mode. Note: The data transmission of the defined sequence is started by the send command.
4 to 0	TestBusSel	Selects the testbus. See Section 19 “Test signals”

9.2.4.3 TestPinEnReg

Disabling MX and DTRQ.

Table 88. TestPinEnReg register (address 33h); reset value: 80h, 10000000b

	7	6	5	4	3	2	1	0
	RS232LineEn	0						0
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 89. Description of TestPinEnReg bits

Bit	Symbol	Description
7	RS232LineEn	Set to 0, the lines MX and DTRQ for the serial UART are disabled.
6 to 0	0	Shall be set to 0.

9.2.4.4 TestBusReg

Shows the status of the internal testbus.

Table 90. TestBusReg register (address 35h); reset value: XXh, XXXXXXXXb

	7	6	5	4	3	2	1	0
	TestBus							
Access Rights	r	r	r	r	r	r	r	r

Table 91. Description of TestBusReg bits

Bit	Symbol	Description
7 to 0	TestBus	Shows the status of the internal testbus. The testbus is selected by the register TestSel2Reg. See Section 19 “Test signals”.

9.2.4.5 AutoTestReg

Controls the digital selftest.

Table 92. AutoTestReg register (address 36h); reset value: 40h, 01000000b

	7	6	5	4	3	2	1	0
	0	AmpRcv	0	RFU	SelfTest			
Access Rights	RFT	r/w	-	-	r/w	r/w	r/w	r/w

Table 93. Description of bits

Bit	Symbol	Description
7	-	Reserved for production tests.
6	AmpRcv	If set to 1, the internal signal processing in the receiver chain is performed non-linear. This increases the operating distance in communication modes at 106 kbit. Note: Due to the non linearity the effect of the bits MinLevel and CollLevel in the register RxThreshholdReg are as well non linear.
5	0	Shall be set to 0.
4	RFU	Reserved for future use
3 to 0	SelfTest	Enables the digital self test. The selftest can be started by the selftest command “CalcCRC” (see Section 18.3.1.4 “CalcCRC”) in the command register. The selftest is enabled by 1001. Note: For default operation the selftest has to be disabled by 0000.

9.2.4.6 VersionReg

Shows the version.

Table 94. VersionReg register (address 37h); reset value: XXh, XXXXXXXXb

	7	6	5	4	3	2	1	0
	Version							
Access Rights	r	r	r	r	r	r	r	r

Table 95. Description of VersionReg bits

Bit	Symbol	Description
7 to 0	Version	E2h indicates PT501 version 1.0.

9.2.4.7 AnalogTestReg

Controls the pins AUX1 and AUX2

Table 96. AnalogTestReg register (address 38h); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	AnalogSelAux1				AnalogSelAux2			
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 97. Description of AnalogTestReg bits

Bit	Symbol	Description	
7 to 4	AnalogSelAux1	Controls the AUX pin.	
3 to 0	AnalogSelAux2	Note: All test signals are described in Section 19 “Test signals”.	
		Value	**Description**
		0000	Tristate
		0001	Output of TestDAC1 (AUX1), output of TESTDAC2 (AUX2) Note: Current output. The use of 1 kΩ pull-down resistor on AUX is recommended.
		0010	Testsignal Corr1 Note: Current output. The use of 1 kΩ pull-down resistor on AUX is recommended.
		0011	Testsignal Corr2 Note: Current output. The use of 1 kΩ pull-down resistor on AUX is recommended.
		0100	Testsignal MinLevel Note: Current output. The use of 1 kΩ pull-down resistor on AUX is recommended.
		0101	Testsignal ADC channel I Note: Current output. The use of 1 kΩ pull-down resistor on AUX is recommended.
		0110	Testsignal ADC channel Q Note: Current output. The use of 1 kΩ pull-down resistor on AUX is recommended.
		0111	Testsignal for production test Note: Current output. The use of 1 kΩ pull-down resistor on AUX is recommended.
		1000	Testsignal for production test Note: Current output. The use of 1 kΩ pull-down resistor on AUX is recommended.
		1001	SAM clock (13.56 MHz)
		1010	HIGH
		1011	LOW
		1100	TxActive At 106 kbit: HIGH during Startbit, Data bit, Parity and CRC. At 212 and 424 kbit: High during Preamble, Sync, Data and CRC.
		1101	RxActive At 106 kbit: High during databit, Parity and CRC. At 212 and 424 kbit: High during data and CRC.
		1110	Subcarrier detected 106 kbit: not applicable 212 and 424 kbit: High during last part of Preamble, Sync data and CRC
		1111	TestBus-Bit as defined by the TstBusBitSel in register TestSel1Reg.

9.2.4.8 TestDAC1Reg

Defines the testvalues for TestDAC1.

Table 98. TestDAC1Reg register (address 39h); reset value: XXh, 00XXXXXXb

	7	6	5	4	3	2	1	0
	0	0	TestDAC1					
Access Rights	RFT	RFU	r/w	r/w	r/w	r/w	r/w	r/w

Table 99. Description of TestDAC1Reg bits

Bit	Symbol	Description
7	-	Reserved for production tests.
6	-	Reserved for future use.
5 to 0	TestDAC1	Defines the testvalue for TestDAC1. The output of the DAC1 can be switched to AUX1 by setting AnalogSelAux1 to 0001 in register AnalogTestReg.

9.2.4.9 TestDAC2Reg

Defines the testvalue for TestDAC2.

Table 100. TestDAC2Reg register (address 3Ah); reset value: XXh, 00XXXXXXb

	7	6	5	4	3	2	1	0
	0	0	TestDAC2					
Access Rights	RFU	RFU	r/w	r/w	r/w	r/w	r/w	r/w

Table 101. Description ofTestDAC2Reg bits

Bit	Symbol	Description
7 to 6	-	Reserved for future use.
5 to 0	TestDAC2	Defines the testvalue for TestDAC2. The output of the DAC2 can be switched to AUX2 by setting AnalogSelAux2 to 0001 in register AnalogTestReg.

9.2.4.10 TestADCReg

Shows the actual value of ADC I and Q channel.

Table 102. TestADCReg register (address 3Bh); reset value: XXh, XXXXXXXXb

	7	6	5	4	3	2	1	0
	ADC_I				ADC_Q			
Access Rights								

Table 103. Description of TestADCReg bits

Bit	Symbol	Description
7 to 4	ADC_I	Shows the actual value of ADC I channel.
3 to 0	ADC_Q	Shows the actual value of ADC Q channel.

9.2.4.11 RFTReg

Table 104. RFTReg register (address 3Ch); reset value: FFh, 11111111b

	7	6	5	4	3	2	1	0
	1	1	1	1	1	1	1	1
Access Rights	RFT	RFT	RFT	RFT	RFT	RFT	RFT	RFT

Table 105. Description of RFTReg bits

Bit	Symbol	Description
7 to 0	-	Reserved for production tests.

Table 106. RFTReg register (address 3Dh, 3Fh); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0
Access Rights	RFT	RFT	RFT	RFT	RFT	RFT	RFT	RFT

Table 107. Description of RFTReg bits

Bit	Symbol	Description
7 to 0	-	Reserved for production tests.

Table 108. RFTReg register (address 3Eh); reset value: 03h, 00000011b

	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	1	1
Access Rights	RFT	RFT	RFT	RFT	RFT	RFT	RFT	RFT

Table 109. Description of RFTReg bits

Bit	Symbol	Description
7 to 0	-	Reserved for production tests.

10. Digital interfaces

10.1 Automatic microcontroller interface detection

The PT501 supports direct interfacing of hosts using SPI, I²C-bus or serial UART interfaces. The PT501 resets its interface and checks the current host interface type automatically after performing a power-on or hard reset. The PT501 identifies the host interface by sensing the logic levels on the control pins after the reset phase. This is done using a combination of fixed pin connections. Table 110 shows the different connection configurations.

Table 110. Connection protocol for detecting different interface types

PT501	Interface type		
Pin	**UART (input)**	**SPI (output)**	**I²C-bus (I/O)**
ALE-UART	RX	NSS	SDA
I²C SEL	0	0	1
SPI SEL	0	1	EA
TX/MISO/SCL	TX	MISO	SCL
MX/MOSI/ADR0	MX	MOSI	ADR_0
DTRQ/SCK/ADR1	DTRQ	SCK	ADR_1
I²C ADR2	-	-	ADR_2
I²C ADR3	-	-	ADR_3
I²C ADR4	-	-	ADR_4
I²C ADR5	-	-	ADR_5

10.2 Serial Peripheral Interface

A serial peripheral interface (SPI compatible) is supported to enable high-speed communication to the host. The interface can handle data speeds up to 10 Mbit/s. When communicating with a host, the PT501 acts as a slave, receiving data from the external host for register settings, sending and receiving data relevant for RF interface communication.

An interface compatible with SPI enables high-speed serial communication between the PT501 and a microcontroller. The implemented interface is in accordance with the SPI standard.

The timing specification is given in Section 23.1 on page 82.

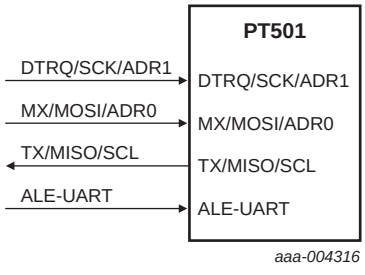


Fig 6. SPI connection to host

The PT501 acts as a slave during SPI communication. The SPI clock signal SCK must be generated by the master. Data communication from the master to the slave uses the MOSI line. The MISO line is used to send data from the PT501 to the master.

Data bytes on both MOSI and MISO lines are sent with the MSB first. Data on both MOSI and MISO lines must be stable on the rising edge of the clock and can be changed on the falling edge. Data is provided by the PT501 on the falling clock edge and is stable during the rising clock edge.

10.2.1 SPI read data

Reading data using SPI requires the byte order shown in Table 111 to be used. It is possible to read out up to n-data bytes.

The first byte sent defines both the mode and the address.

Table 111. MOSI and MISO byte order

Line	Byte 0	Byte 1	Byte 2	To	Byte n	Byte n + 1
MOSI	address 0	address 1	address 2	...	address n	00
MISO	X[1]	data 0	data 1	...	data n – 1	data n

[1] X = Do not care.

Remark: The MSB must be sent first.

10.2.2 SPI write data

To write data to the PT501 using SPI requires the byte order shown in Table 112. It is possible to write up to n data bytes by only sending one address byte.

The first send byte defines both the mode and the address byte.

Table 112. MOSI and MISO byte order

Line	Byte 0	Byte 1	Byte 2	To	Byte n	Byte n + 1
MOSI	address 0	data 0	data 1	...	data n – 1	data n
MISO	X[1]	X[1]	X[1]	...	X[1]	X[1]

[1] X = Do not care.

Remark: The MSB must be sent first.

10.2.3 SPI address byte

The address byte has to meet the following format.

The MSB of the first byte defines the mode used. To read data from the PT501 the MSB is set to 1. To write data to the PT501 the MSB must be set to 0. Bits 6 to 1 define the address and the LSB is set to 0.

Table 113. Address byte 0 register; address MOSI

7 (MSB)	6	5	4	3	2	1	0 (LSB)
1 = read 0 = write	address						0

10.3 UART interface

10.3.1 Connection to a host

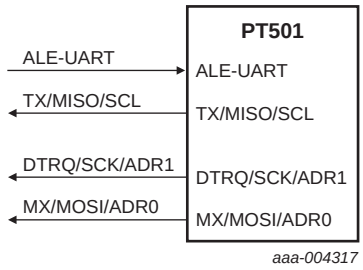


Fig 7. UART connection to microcontrollers

Remark: Signals DTRQ and MX can be disabled by clearing TestPinEnReg register's RS232LineEn bit.

10.3.2 Selectable UART transfer speeds

The internal UART interface is compatible with an RS232 serial interface.

The default transfer speed is 9.6 kBd. To change the transfer speed, the host controller must write a value for the new transfer speed to the SerialSpeedReg register. Bits BR_T0[2:0] and BR_T1[4:0] define the factors for setting the transfer speed in the SerialSpeedReg register.

Table 114. BR_T0 and BR_T1 settings

BR_Tn	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
BR_T0 factor	1	1	2	4	8	16	32	64
BR_T1 range	1 to 32	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64

Table 115. Selectable UART transfer speeds

Transfer speed (kBd)	SerialSpeedReg value		Transfer speed accuracy (%)[1]
	Decimal	Hexadecimal	
7.2	250	FAh	–0.25
9.6	235	EBh	0.32
14.4	218	DAh	–0.25
19.2	203	CBh	0.32
38.4	171	ABh	0.32
57.6	154	9Ah	–0.25
115.2	122	7Ah	–0.25
128	116	74h	–0.06
230.4	90	5Ah	–0.25
460.8	58	3Ah	–0.25
921.6	28	1Ch	1.45
1228.8	21	15h	0.32

[1] The resulting transfer speed error is less than 1.5 % for all described transfer speeds.

The selectable transfer speeds are calculated according to the following equations:

If BR_T0[2:0] = 0:

$$transfer\ speed = \frac{27.12 \times 10^6}{(BR\_T0 + 1)} \quad (1)$$

If BR_T0[2:0] > 0:

$$transfer\ speed = \left(\frac{\frac{27.12 \times 10^6}{(BR\_T1 + 33)}}{2^{(BR\_T0 - 1)}} \right) \quad (2)$$

Remark: Transfer speeds above 1228.8 kBd are not supported.

10.3.3 UART framing

Table 116. UART framing

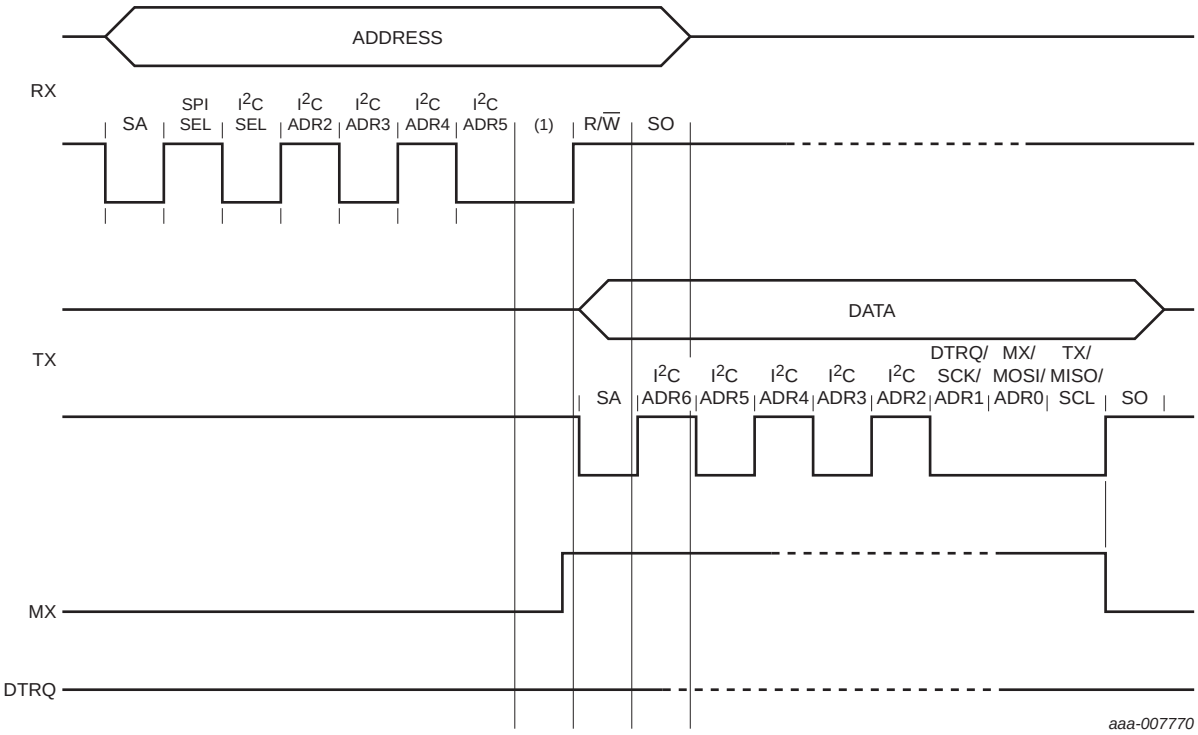
Bit	Length	Value
Start	1-bit	0
Data	8 bits	data
Stop	1-bit	1

Remark: The LSB for data and address bytes must be sent first. No parity bit is used during transmission.

Read data: To read data using the UART interface, the flow shown in Table 117 must be used. The first byte sent defines both the mode and the address.

Table 117. Read data byte order

Pin	Byte 0	Byte 1
ALE-UART	address	-
TX/MISO/SCL	-	data 0



(1) Reserved.

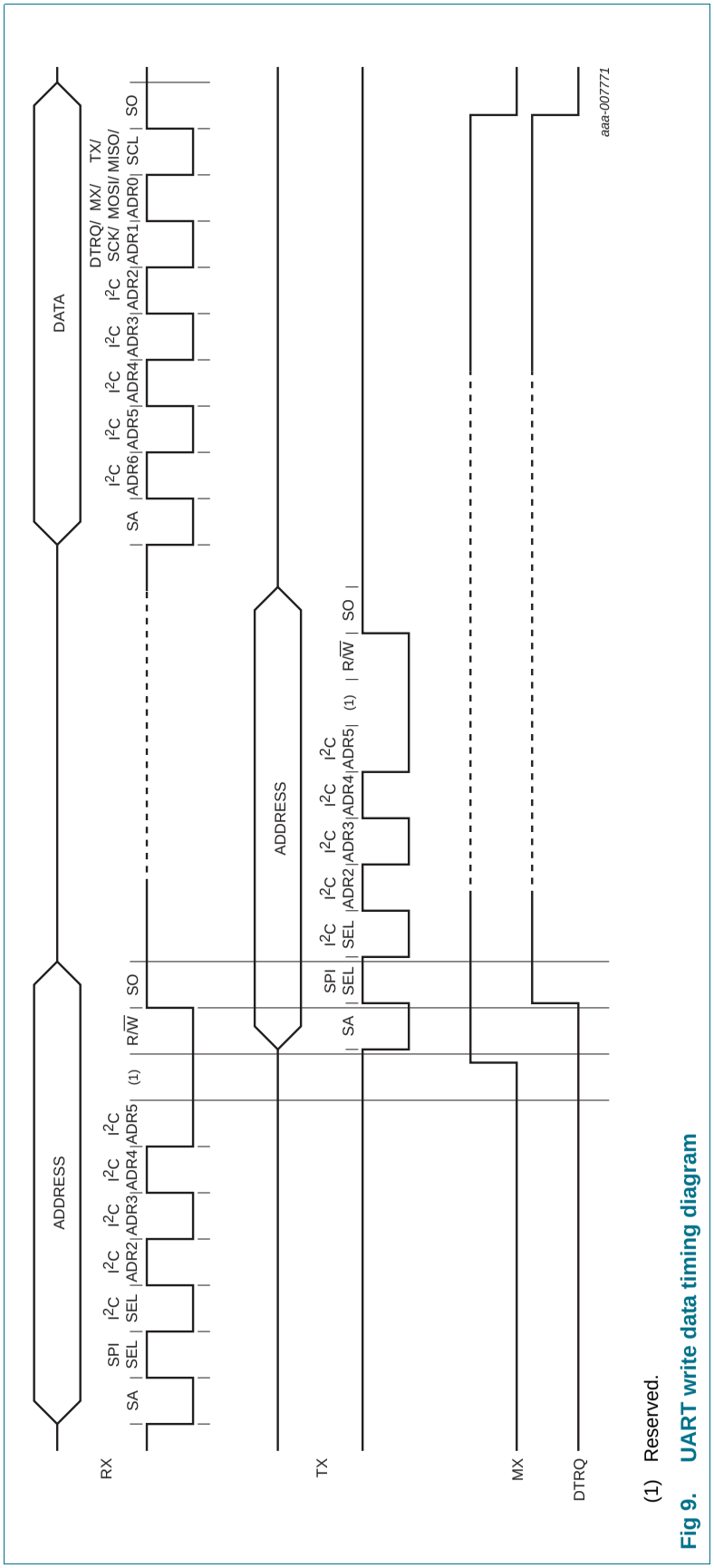
Fig 8. UART read data timing diagram

Write data: To write data to the PT501 using the UART interface, the structure shown in Table 118 must be used.

The first byte sent defines both the mode and the address.

Table 118. Write data byte order

Pin	Byte 0	Byte 1
ALE-UART	address 0	data 0
TX/MISO/SCL	-	address 0



(1) Reserved.

Fig 9. UART write data timing diagram

Remark: The data byte can be sent directly after the address byte on pin RX.

Address byte: The address byte has to meet the following format:

The MSB of the first byte sets the mode used. To read data from the PT501, the MSB is set to 1. To write data to the PT501 the MSB is set to 0. Bit 6 is reserved for future use, and bits 5 to 0 define the address; see Table 119.

Table 119. Address byte 0 register; address MOSI

7 (MSB)	6	5	4	3	2	1	0 (LSB)
1 = read 0 = write	reserved	address					

10.4 I²C Bus Interface

An I²C-bus (Inter-IC) interface is supported to enable a low-cost, low pin count serial bus interface to the host. The I²C-bus interface is implemented according to NXP Semiconductors' *I²C-bus interface specification, rev. 2.1, January 2000*. The interface can only act in Slave mode. Therefore the PT501 does not implement clock generation or access arbitration.

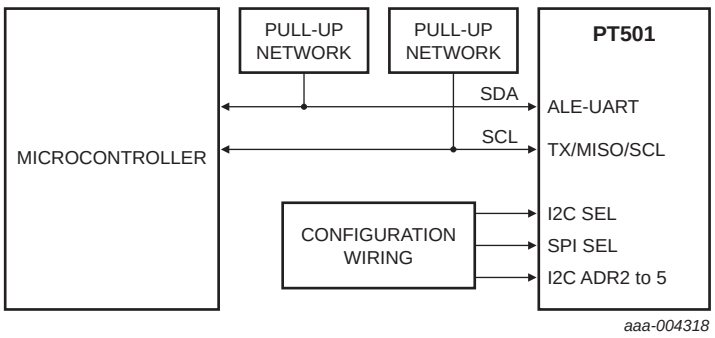


Fig 10. I²C-bus interface

The PT501 can act either as a slave receiver or slave transmitter in Standard mode, Fast mode and High-speed mode.

ALE-UART is a bidirectional line connected to a positive supply voltage using a current source or a pull-up resistor. Both ALE-UART and TX/MISO/SCL lines are set HIGH when data is not transmitted. The PT501 has a 3-state output stage to perform the wired-AND function. Data on the I²C-bus can be transferred at data rates of up to 100 kBd in Standard mode, up to 400 kBd in Fast mode or up to 3.4 Mbit/s in High-speed mode.

If the I²C-bus interface is selected, spike suppression is activated on lines TX/MISO/SCL and ALE-UART as defined in the I²C-bus interface specification.

See Table 136 on page 82 for timing requirements.

10.4.1 Data validity

Data on the SDA line must be stable during the HIGH clock period. The HIGH or LOW state of the data line must only change when the clock signal on SCL is LOW.

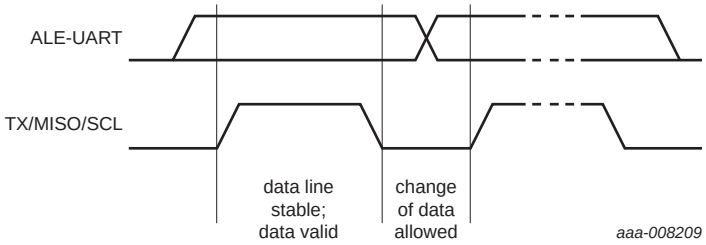


Fig 11. Bit transfer on the I²C-bus

10.4.2 START and STOP conditions

To manage the data transfer on the I²C-bus, unique START (S) and STOP (P) conditions are defined.

- A START condition is defined with a HIGH-to-LOW transition on the SDA line while SCL is HIGH.
- A STOP condition is defined with a LOW-to-HIGH transition on the SDA line while SCL is HIGH.

The I²C-bus master always generates the START and STOP conditions. The bus is busy after the START condition. The bus is free again a certain time after the STOP condition.

The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. The START (S) and repeated START (Sr) conditions are functionally identical. Therefore, S is used as a generic term to represent both the START (S) and repeated START (Sr) conditions.

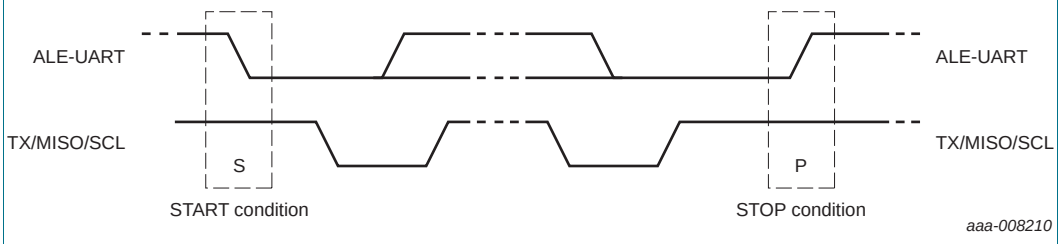


Fig 12. START and STOP conditions

10.4.3 Byte format

Each byte must be followed by an acknowledge bit. Data is transferred with the MSB first; see Figure 15. The number of transmitted bytes during one data transfer is unrestricted but must meet the read/write cycle format.

10.4.4 Acknowledge

An acknowledge must be sent at the end of one data byte. The acknowledge-related clock pulse is generated by the master. The transmitter of data, either master or slave, releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver pulls down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse.

The master can then generate either a STOP (P) condition to stop the transfer or a repeated START (Sr) condition to start a new transfer.

A master-receiver indicates the end of data to the slave-transmitter by not generating an acknowledge on the last byte that was clocked out by the slave. The slave-transmitter releases the data line to allow the master to generate a STOP (P) or repeated START (Sr) condition.

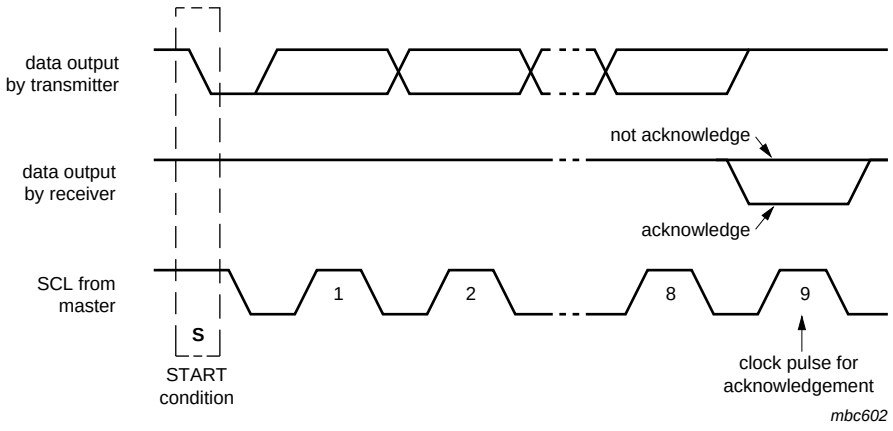


Fig 13. Acknowledge on the I²C-bus

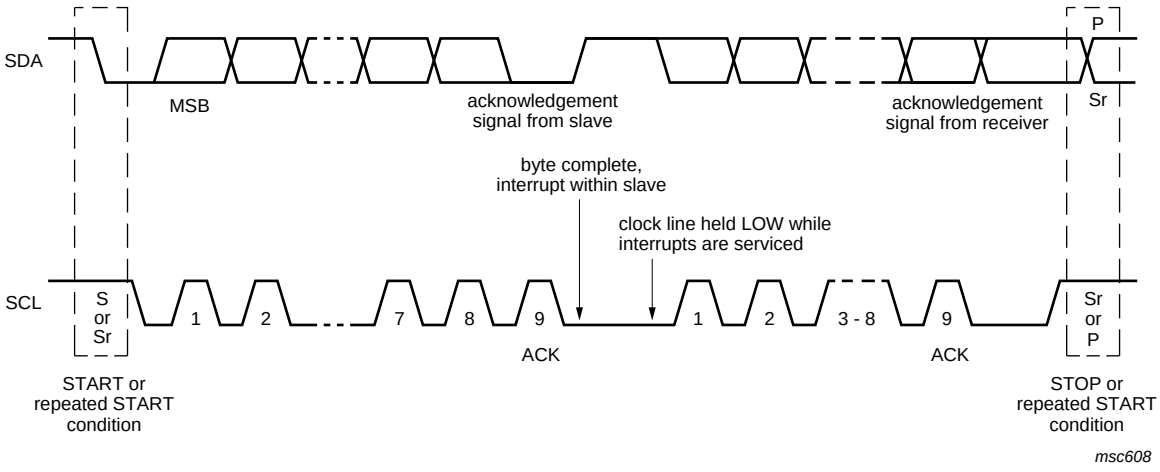


Fig 14. Data transfer on the I²C-bus

10.4.5 7-Bit addressing

During the I²C-bus address procedure, the first byte after the START condition is used to determine which slave will be selected by the master.

Several address numbers are reserved. During device configuration, the designer must ensure that collisions with these reserved addresses cannot occur. Check the *I²C-bus specification* for a complete list of reserved addresses.

The I²C-bus address specification is dependent on the definition of pin EA. Immediately after releasing pin NRSTPD or after a power-on reset, the device defines the I²C-bus address according to pin EA.

If pin EA is set LOW, the upper 4 bits of the device bus address are reserved by NXP Semiconductors and set to 0101b for all PT501 devices. The remaining 3 bits (ADR_0, ADR_1, ADR_2) of the slave address can be freely configured by the customer to prevent collisions with other I²C-bus devices.

If pin EA is set HIGH, ADR_0 to ADR_5 can be completely specified at the external pins according to Table 110 on page 47. ADR_6 is always set to 0.

In both modes, the external address coding is latched immediately after releasing the reset condition. Further changes at the used pins are not taken into consideration. Depending on the external wiring, the I²C-bus address pins can be used for test signal outputs.

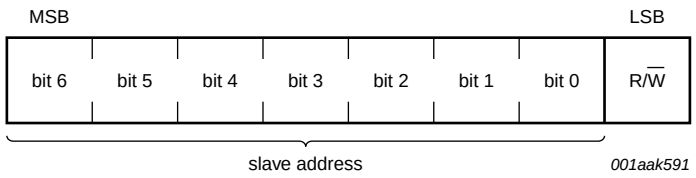


Fig 15. First byte following the START procedure

10.4.6 Register write access

To write data from the host controller using the I²C-bus to a specific register in the PT501 the following frame format must be used.

- The first byte of a frame indicates the device address according to the I²C-bus rules.
- The second byte indicates the register address followed by up to n-data bytes.

In one frame all data bytes are written to the same register address. This enables fast FIFO buffer access. The Read/Write (R/$\overline{W}$) bit is set to 0.

10.4.7 Register read access

To read out data from a specific register address in the PT501, the host controller must use the following procedure:

- Firstly, a write access to the specific register address must be performed as indicated in the frame that follows
- The first byte of a frame indicates the device address according to the I²C-bus rules
- The second byte indicates the register address. No data bytes are added
- The Read/Write bit is 0

After the write access, read access can start. The host sends the device address of the PT501. In response, the PT501 sends the content of the read access register. In one frame all data bytes can be read from the same register address. This enables fast FIFO buffer access or register polling.

The Read/Write (R/W) bit is set to 1.

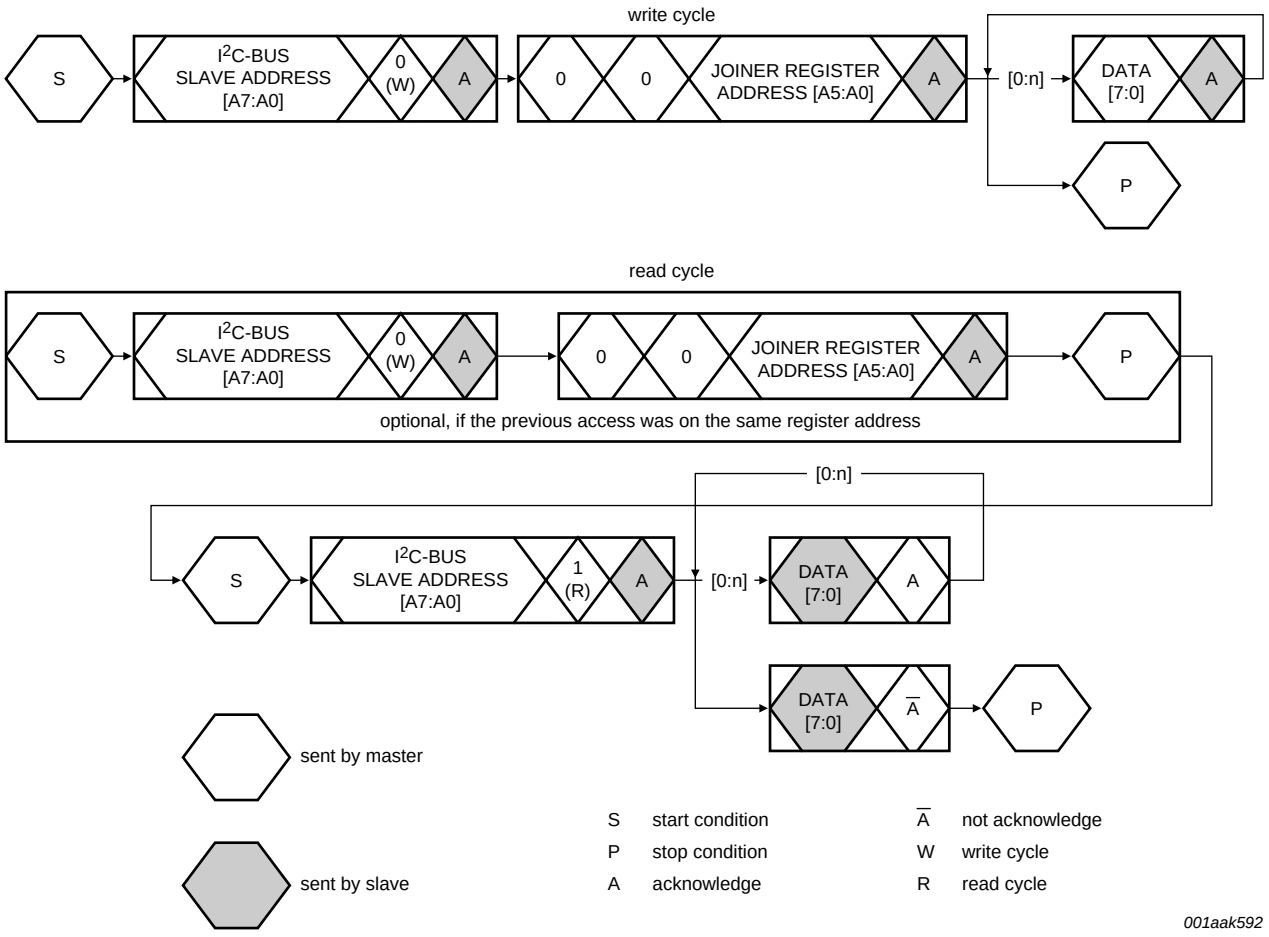


Fig 16. Register read and write access

10.4.8 High-speed mode

In High-speed mode (HS mode), the device can transfer information at data rates of up to 3.4 Mbit/s, while remaining fully downward-compatible with Fast or Standard mode (F/S mode) for bidirectional communication in a mixed-speed bus system.

10.4.9 High-speed transfer

To achieve data rates of up to 3.4 Mbit/s the following improvements have been made to I^2C-bus operation.

- The inputs of the device in HS mode incorporate spike suppression, a Schmitt trigger on the SDA and SCL inputs and different timing constants when compared to F/S mode
- The output buffers of the device in HS mode incorporate slope control of the falling edges of the SDA and SCL signals with different fall times compared to F/S mode

10.4.10 Serial data transfer format in HS mode

The HS mode serial data transfer format meets the Standard mode I^2C-bus specification. HS mode can only start after all of the following conditions (all of which are in F/S mode):

1. START condition (S)
2. 8-bit master code (00001XXXb)
3. Not-acknowledge bit ($\overline{A}$)

When HS mode starts, the active master sends a repeated START condition (Sr) followed by a 7-bit slave address with a R/W bit address and receives an acknowledge bit (A) from the selected PT501.

Data transfer continues in HS mode after the next repeated START (Sr), only switching back to F/S mode after a STOP condition (P). To reduce the overhead of the master code, a master links a number of HS mode transfers, separated by repeated START conditions (Sr).

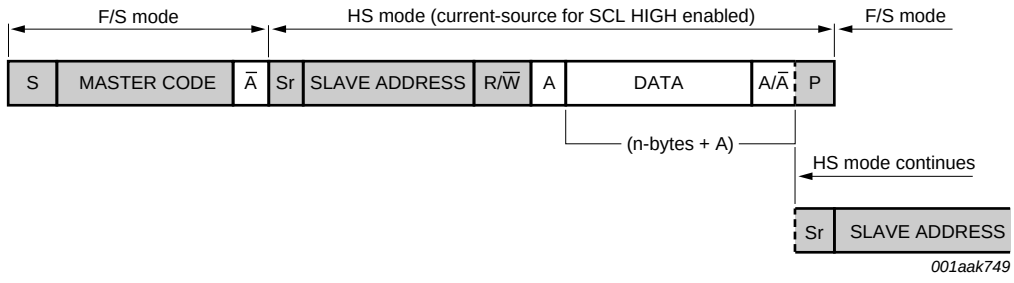


Fig 17. I^2C-bus HS mode protocol switch

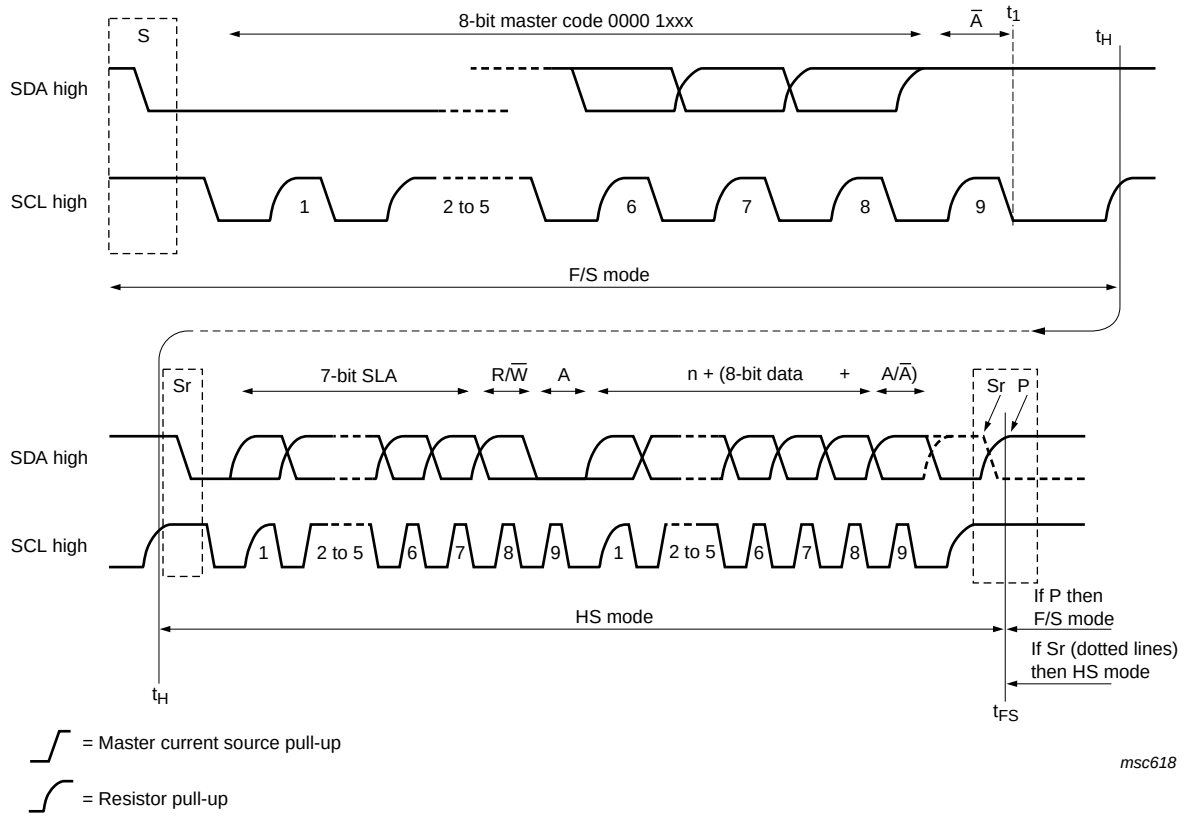


Fig 18. I²C-bus HS mode protocol frame

10.4.11 Switching between F/S mode and HS mode

After reset and initialization, the PT501 is in Fast mode (which is in effect F/S mode as Fast mode is downward-compatible with Standard mode). The connected PT501 recognizes the “S 00001XXX A” sequence and switches its internal circuitry from the Fast mode setting to the HS mode setting.

The following actions are taken:

1. Adapt the SDA and SCL input filters according to the spike suppression requirement in HS mode.
2. Adapt the slope control of the SDA output stages.

It is possible for system configurations that do not have other I^2C-bus devices involved in the communication to switch to HS mode permanently. This is implemented by setting Status2Reg register’s I^2CForceHS bit to 1. In permanent HS mode, the master code is not required to be sent. This is not defined in the specification and must only be used when no other devices are connected on the bus. In addition, spikes on the I^2C-bus lines must be avoided because of the reduced spike suppression.

10.4.12 PT501 at lower speed modes

PT501 is fully downward-compatible and can be connected to an F/S mode I^2C-bus system. The device stays in F/S mode and communicates at F/S mode speeds because a master code is not transmitted in this configuration.

11. Analog interface and contactless UART

11.1 General

The integrated contactless UART supports the external host online with framing and error checking of the protocol requirements up to 424 kBd. An external circuit can be connected to the communication interface pins SGIN and SIGOUT to modulate and demodulate the data.

The contactless UART handles the protocol requirements for the communication protocols in cooperation with the host. Protocol handling generates bit and byte-oriented framing. In addition, it handles error detection such as parity and CRC, based on the various supported contactless communication protocols.

11.2 RF level detector

The RF level detector is integrated to fulfill NFCIP1 protocol requirements (e.g. RF collision avoidance). Furthermore the RF level detector can be used to wake up the PT501 and to generate an interrupt.

The sensitivity of the RF level detector is adjustable in a 4-bit range using the bits RFLevel in register RFCfgReg. The sensitivity itself depends on the antenna configuration and tuning.

Table 120. Setting of the bits RF level in register RFCfgReg (RF level amplifier deactivated)

V~Rx [Vpp]	RFLevel
~2	1111
~1.4	1110
~0.99	1101
~0.69	1100
~0.49	1011
~0.35	1010
~0.24	1001
~0.17	1000
~0.12	0111
~0.083	0110
~0.058	0101
~0.041	0100
~0.029	0011
~0.020	0010
~0.014	0001
~0.010	0000

To increase the sensitivity of the RF level detector an amplifier can be activated by setting the bit RFLevelAmp in register RFCfgReg to 1.

Remark: During soft Power-down mode the RF level detector amplifier is automatically switched off to ensure that the power consumption is less than 10 μA at 3 V.

Remark: With typical antennas lower sensitivity levels can provoke misleading results because of intrinsic noise in the environment.

Note: It is recommended to use the bit RFLevelAmp only with higher RF level settings.

11.3 Data mode detector

The Data mode detector gives the possibility to detect received signals according to the ISO/IEC 14443A, FeliCa or NFCIP-1 schemes at the standard transfer speeds for 106 kbit, 212 kbit and 424 kbit in order to prepare the internal receiver in a fast and convenient way for further data processing.

The Data mode detector can only be activated by the AutoColl command. The mode detector resets, when no external RF field is detected by the RF level detector. The Data mode detector could be switched off during the AutoColl command by setting bit ModeDetOff in register ModeReg to 1.

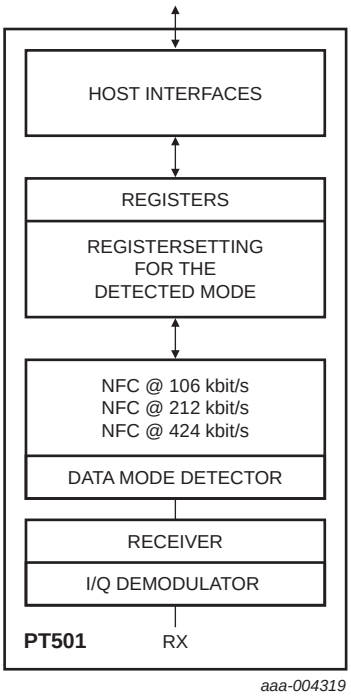


Fig 19. Data mode detector

11.4 Serial data switch

Two main blocks are implemented in the PT501. The digital block comprises the state machines, encoder/decoder logic. The analog block comprises the modulator and antenna drivers, the receiver and amplifiers. The interface between these two blocks can be configured in the way, that the interfacing signals may be routed to the pins SIGIN and SIGOUT. SIGIN is capable of processing digital NFC signals on transfer speeds above 424 kbit. The SIGOUT pin can provide a digital signal that can be used with an additional external circuit to generate transfer speeds above 424 kbit (including 106, 212 and 424 kbit). Furthermore SIGOUT and SIGIN can be used to enable the S^2C interface in the card SAM mode to emulate a card functionality with the PT501 and a secure IC. A secure IC can be the Smart*MX* smart card controller IC.

This topology allows the analog block of the PT501 to be connected to the digital block of another device.

The serial signal switch is controlled by the TxSelReg and RxSelReg registers.

Figure 20 shows the serial data switch for TX1 and TX2.

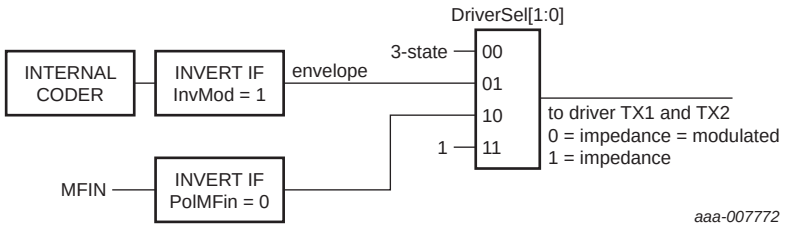


Fig 20. Serial data switch for TX1 and TX2

11.5 Hardware support for FeliCa and NFC polling

11.5.1 Additional hardware support for FeliCa and NFC

Additionally to the polling sequence support for the Felica mode, the PT501 supports the check of the Len-byte.

11.5.2 CRC coprocessor

The following CRC coprocessor parameters can be configured:

- The CRC preset value can be either 0000h, 6363h, A671h or FFFFh depending on the ModeReg register's CRCPreset[1:0] bits setting
- The CRC polynomial for the 16-bit CRC is fixed to $x^{16} + x^{12} + x^5 + 1$
- The CRCResultReg register indicates the result of the CRC calculation. This register is split into two 8-bit registers representing the higher and lower bytes.
- The ModeReg register's MSBFirst bit indicates that data will be loaded with the MSB first.

Table 121. CRC coprocessor parameters

Parameter	Value
CRC register length	16-bit CRC
CRC algorithm	algorithm according to ISO/IEC 14443 A and ITU-T
CRC preset value	0000h, 6363h, A671h or FFFFh depending on the setting of the ModeReg register's CRCPreset[1:0] bits

12. FIFO buffer

An 8 × 64 bit FIFO buffer is used in the PT501. It buffers the input and output data stream between the host and the PT501's internal state machine. This makes it possible to manage data streams up to 64 bytes long without the need to take timing constraints into account.

12.1 Accessing the FIFO buffer

The FIFO buffer input and output data bus is connected to the FIFODataReg register. Writing to this register stores one byte in the FIFO buffer and increments the internal FIFO buffer write pointer. Reading from this register shows the FIFO buffer contents stored in the FIFO buffer read pointer and decrements the FIFO buffer read pointer. The distance between the write and read pointer can be obtained by reading the FIFOLevelReg register.

When the microcontroller starts a command, the PT501 can, while the command is in progress, access the FIFO buffer according to that command. Only one FIFO buffer has been implemented which can be used for input and output. The microcontroller must ensure that there are not any unintentional FIFO buffer accesses.

12.2 Controlling the FIFO buffer

The FIFO buffer pointers can be reset by setting FIFOLevelReg register's FlushBuffer bit to 1. Consequently, the FIFOLevel[6:0] bits are all set to 0 and the ErrorReg register's BufferOvfl bit is cleared. The bytes stored in the FIFO buffer are no longer accessible allowing the FIFO buffer to be filled with another 64 bytes.

12.3 FIFO buffer status information

The host can get the following FIFO buffer status information:

- Number of bytes stored in the FIFO buffer: FIFOLevelReg register's FIFOLevel[6:0]
- FIFO buffer almost full warning: Status1Reg register's HiAlert bit
- FIFO buffer almost empty warning: Status1Reg register's LoAlert bit
- FIFO buffer overflow warning: ErrorReg register's BufferOvfl bit. The BufferOvfl bit can only be cleared by setting the FIFOLevelReg register's FlushBuffer bit.

The PT501 can generate an interrupt signal when:

- ComIEnReg register's LoAlertIEn bit is set to 1. It activates pin IRQ when Status1Reg register's LoAlert bit changes to 1.
- ComIEnReg register's HiAlertIEn bit is set to 1. It activates pin IRQ when Status1Reg register's HiAlert bit changes to 1.

If the maximum number of WaterLevel bytes (as set in the WaterLevelReg register) or less are stored in the FIFO buffer, the HiAlert bit is set to 1. It is generated according to Equation 3:

$$HiAlert = (64 - FIFOLength) \leq WaterLevel \quad (3)$$

If the number of WaterLevel bytes (as set in the WaterLevelReg register) or less are stored in the FIFO buffer, the LoAlert bit is set to 1. It is generated according to Equation 4:

$$LoAlert = FIFOLength \leq WaterLevel \quad (4)$$

13. Interrupt request system

The PT501 indicates certain events by setting the Status1Reg register's IRq bit and, if activated, by pin IRQ. The signal on pin IRQ can be used to interrupt the host using its interrupt handling capabilities. This allows the implementation of efficient host software.

13.1 Interrupt sources overview

Table 122 shows the available interrupt bits, the corresponding source and the condition for its activation. The ComIrqReg register's TimerIRq interrupt bit indicates an interrupt set by the timer unit which is set when the timer decrements from 1 to 0.

The ComIrqReg register's TxIRq bit indicates that the transmitter has finished. If the state changes from sending data to transmitting the end of the frame pattern, the transmitter unit automatically sets the interrupt bit. The CRC coprocessor sets the DivIrqReg register's CRCIRq bit after processing all the FIFO buffer data which is indicated by CRCReady bit = 1.

The ComIrqReg register's RxIRq bit indicates an interrupt when the end of the received data is detected. The ComIrqReg register's IdleIRq bit is set if a command finishes and the Command[3:0] value in the CommandReg register changes to idle (see Table 123 on page 70).

The ComIrqReg register's HiAlertIRq bit is set to 1 when the Status1Reg register's HiAlert bit is set to 1 which means that the FIFO buffer has reached the level indicated by the WaterLevel[5:0] bits.

The ComIrqReg register's LoAlertIRq bit is set to 1 when the Status1Reg register's LoAlert bit is set to 1 which means that the FIFO buffer has reached the level indicated by the WaterLevel[5:0] bits.

The ComIrqReg register's ErrIRq bit indicates an error detected by the contactless UART during send or receive. This is indicated when any bit is set to 1 in register ErrorReg.

Table 122. Interrupt sources

Interrupt flag	Interrupt source	Trigger action
TimerIRq	timer unit	the timer counts from 1 to 0
TxIRq	transmitter	a transmitted data stream ends
CRCIRq	CRC coprocessor	all data from the FIFO buffer has been processed
RxIRq	receiver	a received data stream ends

Table 122. Interrupt sources *…continued*

Interrupt flag	Interrupt source	Trigger action
IdleIRq	ComIrqReg register	command execution finishes
HiAlertIRq	FIFO buffer	the FIFO buffer is almost full
LoAlertIRq	FIFO buffer	the FIFO buffer is almost empty
ErrIRq	contactless UART	an error is detected

14. Timer unit

A timer unit is implemented in the PT501. The external host controller may use this timer to manage timing relevant tasks. The timer unit may be used in one of the following configurations:

- Time-out counter
- Watch-dog counter
- Stop watch
- Programmable one-shot
- Periodical trigger

The timer unit can be used to measure the time interval between two events or to indicate that a specific event occurred after a specific time. The timer can be triggered by events which will be explained in the following, but the timer itself does not influence any internal event (e.g. A time-out during data reception does not influence the reception process automatically). Furthermore, several timer related bits are set and these bits can be used to generate an interrupt.

Timer

The timer has an input clock of 13.56 MHz (derived from the 27.12 MHz quartz). The timer consists of two stages: 1 prescaler and 1 counter.

The prescaler is a 12-bit counter. The reload value for TPrescaler can be defined between 0 and 4095 in register TModeReg and TPrescalerReg.

The reload value for the counter is defined by 16 bits in a range of 0 to 65535 in the register TReloadReg.

The current value of the timer is indicated by the register TCounterValReg.

If the counter reaches 0 an interrupt will be generated automatically indicated by setting the TimerIRq bit in the register CommonIRqReg. If enabled, this event can be indicated on the IRQ line. The bit TimerIRq can be set and reset by the host controller. Depending on the configuration the timer will stop at 0 or restart with the value from register TReloadReg.

The status of the timer is indicated by bit TRunning in register Status1Reg.

The timer can be manually started by TStartNow in register ControlReg or manually stopped by TStopNow in register ControlReg.
Furthermore the timer can be activated automatically by setting the bit TAuto in the register TModeReg to fulfill dedicated protocol requirements automatically.

The time delay of a timer stage is the reload value +1.
The definition of total time is: t = ((TPrescaler*2+1)*TReload+1)/13.56MHz or if TPrescaleEven bit is set: t = ((TPrescaler*2+2)*TReload+1)/13.56MHz

Maximum time: TPrescaler = 4095,TReloadVal = 65535
=> (2*4095 +2)*65536/13.56 MHz = 39.59 s

Example:

To indicate 25 us it is required to count 339 clock cycles. This means the value for TPrescaler has to be set to TPrescaler = 169.The timer has now an input clock of 25 us. The timer can count up to 65535 timeslots of each 25 μs.

15. Power reduction modes

15.1 Hard power-down

Hard power-down is enabled when pin NRSTPD is LOW. This turns off all internal current sinks including the oscillator. All digital input buffers are separated from the input pins and clamped internally (except pin NRSTPD). The output pins are frozen at either a HIGH or LOW level.

15.2 Soft power-down mode

Soft Power-down mode is entered immediately after the CommandReg register's PowerDown bit is set to 1. All internal current sinks are switched off, including the oscillator buffer. However, the digital input buffers are not separated from the input pins and keep their functionality. The digital output pins do not change their state.

During soft power-down, all register values, the FIFO buffer content and the configuration keep their current contents.

After setting the PowerDown bit to 0, it takes 1024 clocks until the Soft power-down mode is exited indicated by the PowerDown bit. Setting it to 0 does not immediately clear it. It is cleared automatically by the PT501 when Soft power-down mode is exited.

Remark: If the internal oscillator is used, you must take into account that it is supplied by pin AVDD and it will take a certain time (t_{osc}) until the oscillator is stable and the clock cycles can be detected by the internal logic. It is recommended for the serial UART, to first send the value 55h to the PT501. The oscillator must be stable for further access to the registers. To ensure this, perform a read access to address 0 until the PT501 answers to the last read command with the register content of address 0. This indicates that the PT501 is ready.

15.3 Transmitter power-down mode

The Transmitter Power-down mode switches off the internal antenna drivers thereby, turning off the RF field. Transmitter power-down mode is entered by setting either the TxControlReg register's Tx1RFEn bit or Tx2RFEn bit to 0.

16. Oscillator circuitry

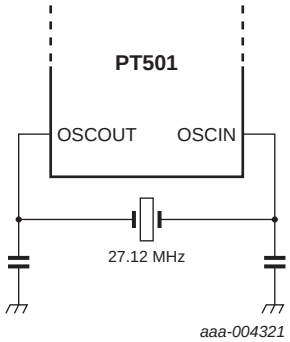


Fig 21. Quartz crystal connection

The clock applied to the PT501 provides a time basis for the synchronous system's encoder and decoder. The stability of the clock frequency, therefore, is an important factor for correct operation. To obtain optimum performance, clock jitter must be reduced as much as possible. This is best achieved using the internal oscillator buffer with the recommended circuitry.

If an external clock source is used, the clock signal must be applied to pin OSCIN. In this case, special care must be taken with the clock duty cycle and clock jitter and the clock quality must be verified.

17. Reset and oscillator start-up time

17.1 Reset timing requirements

The reset signal is filtered by a hysteresis circuit and a spike filter before it enters the digital circuit. The spike filter rejects signals shorter than 10 ns. In order to perform a reset, the signal must be LOW for at least 100 ns.

17.2 Oscillator start-up time

If the PT501 has been set to a Power-down mode or is powered by a V_{DDX} supply, the start-up time for the PT501 depends on the oscillator used and is shown in Figure 22.

The time ($t_{startup}$) is the start-up time of the crystal oscillator circuit. The crystal oscillator start-up time is defined by the crystal.

The time (t_d) is the internal delay time of the PT501 when the clock signal is stable before the PT501 can be addressed.

The delay time is calculated by:

$$t_d = \frac{1024}{27\ \mu s} = 37.74\ \mu s \quad (5)$$

The time (t_{osc}) is the sum of t_d and $t_{startup}$.

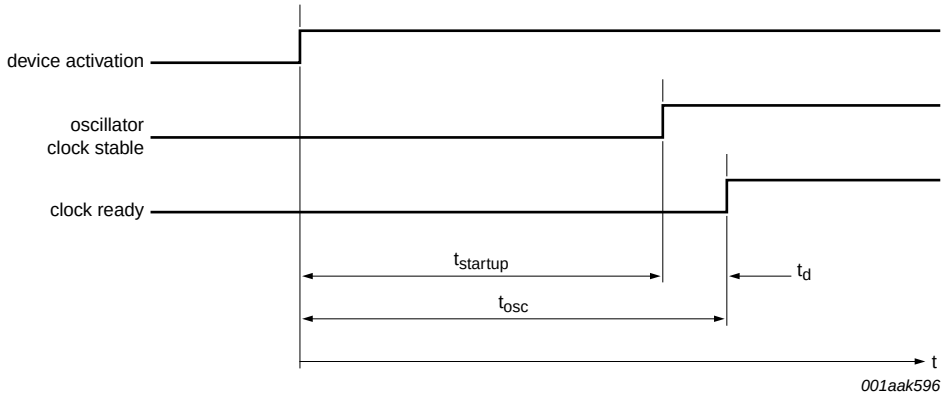


Fig 22. Oscillator start-up time

18. PT501 command set

The PT501 operation is determined by a state machine capable of performing a set of commands. A command is executed by writing a command code (see Table 123) to the CommandReg register.

Arguments and/or data necessary to process a command are exchanged via the FIFO buffer.

18.1 General description

The PT501 operation is determined by a state machine capable of performing a set of commands. A command is executed by writing a command code (see Table 123) to the CommandReg register.

Arguments and/or data necessary to process a command are exchanged via the FIFO buffer.

18.2 General behavior

- Each command that needs a data bit stream (or data byte stream) as an input immediately processes any data in the FIFO buffer. An exception to this rule is the Transceive command. Using this command, transmission is started with the BitFramingReg register's StartSend bit.
- Each command that needs a certain number of arguments, starts processing only when it has received the correct number of arguments from the FIFO buffer.
- The FIFO buffer is not automatically cleared when commands start. This makes it possible to write command arguments and/or the data bytes to the FIFO buffer and then start the command.
- Each command can be interrupted by the host writing a new command code to the CommandReg register, for example, the Idle command.

18.3 PT501 command overview

Table 123. Command overview

Command	Command code	Action
Idle	0000	no action, cancels current command execution
Configure	0001	Configures the PT501 for FeliCa, MIFARE and NFCIP-1 communication
Generate RandomID	0010	generates a 10-byte random ID number
CalcCRC	0011	activates the CRC coprocessor or performs a self test
Transmit	0100	transmits data from the FIFO buffer
NoCmdChange	0111	no command change, can be used to modify the CommandReg register bits without affecting the command, for example, the PowerDown bit
Receive	1000	activates the receiver circuits
Transceive	1100	transmits data from FIFO buffer to antenna and automatically activates the receiver after transmission
AutoColl	1101	Handles FeliCa polling (Card Operation mode only) and MIFARE anticollision (Card Operation mode only)
SoftReset	1111	resets the PT501

18.3.1 PT501 command descriptions

18.3.1.1 Idle

Places the PT501 in Idle mode. The Idle command also terminates itself.

18.3.1.2 Config command

To use the automatic MIFARE Anticollision, FeliCa Polling and NFCID3 the data used for these transactions has to be stored internally. All the following data have to be written to the FIFO in this order:

SENS_RES (2 bytes); in order byte 0, byte 1

NFCID1 (3 Bytes); in order byte 0, byte 1, byte 2; the first NFCID1 byte is fixed to 08h and the check byte is calculated automatically. As such the IC can only use Random ID.

SEL_RES (1 Byte)

polling response (2 bytes (shall be 01h, FEh) + 6 bytes NFCID2 + 8 bytes Pad + 2 bytes system code)

NFCID3 (1 byte)

In total 25 bytes are transferred into an internal buffer.

The complete NFCID3 is 10 bytes long and consists of the 3 NFCID1 bytes, the 6 NFCID2 bytes and the one NFCID3 byte which are listed above.

To read out this configuration the command Config with an empty FIFO-buffer has to be started. In this case the 25 bytes are transferred from the internal buffer to the FIFO.

The PT501 has to be configured after each power up, before using the automatic Anticollision/Polling function (AutoColl command). During a hard power down (reset pin) this configuration remains unchanged.

This command terminates automatically when finished and the active command is idle.

18.3.1.3 Generate RandomID

This command generates a 10-byte random number which is initially stored in the internal buffer. This then overwrites the 10 bytes in the internal 25-byte buffer. This command automatically terminates when finished and the PT501 returns to Idle mode.

18.3.1.4 CalcCRC

The FIFO buffer content is transferred to the CRC coprocessor and the CRC calculation is started. The calculation result is stored in the CRCResultReg register. The CRC calculation is not limited to a dedicated number of bytes. The calculation is not stopped when the FIFO buffer is empty during the data stream. The next byte written to the FIFO buffer is added to the calculation.

The CRC preset value is controlled by the ModeReg register's CRCPreset[1:0] bits. The value is loaded in to the CRC coprocessor when the command starts.

This command must be terminated by writing a command to the CommandReg register, such as, the Idle command.

If the AutoTestReg register's SelfTest[3:0] bits are set correctly, the PT501 enters Self Test mode. Starting the CalcCRC command initiates a digital self test. The result of the self test is written to the FIFO buffer.

18.3.1.5 Transmit

The FIFO buffer content is immediately transmitted after starting this command. Before transmitting the FIFO buffer content, all relevant registers must be set for data transmission.

This command automatically terminates when the FIFO buffer is empty. It can be terminated by another command written to the CommandReg register.

18.3.1.6 NoCmdChange

This command does not influence any running command in the CommandReg register. It can be used to manipulate any bit except the CommandReg register Command[3:0] bits, for example, the RcvOff bit or the PowerDown bit.

18.3.1.7 Receive

The PT501 activates the receiver path and waits for a data stream to be received. The correct settings must be chosen before starting this command.

This command automatically terminates when the data stream ends. This is indicated either by the end of frame pattern or by the length byte depending on the selected frame type and speed.

18.3.1.8 Transceive

This command continuously repeats the transmission of data from the FIFO buffer and the reception of data from the RF field. The first action is transmit and after transmission the command is changed to receive a data stream.

Each transmit process must be started by setting the BitFramingReg register's StartSend bit to 1. This command must be cleared by writing any command to the CommandReg register.

18.3.1.9 AutoColl

This command automatically handles the MIFARE activation and the FeliCa polling in the Card Operation mode. The bit Initiator in the register ControlReg has to be set to 0 for correct operation. During this command also the mode detector is active if not deactivated by setting the bit ModeDetOff in the ModeReg register. After the mode detector detects a mode, all the mode dependent registers are set according to the received data. In case of no external RF field the command resets the internal state machine and returns to the initial state but it will not be terminated. When the command terminates the transceive command gets active.

During protocol processing the IRQ bits are not supported. Only the last received frame will serve the IRQ's. The treatment of the TxCRCEn and RxCRCEn bits is different to the protocol. During ISO/IEC 14443A activation the enable bits are defined by the command AutoColl. The changes cannot be observed at the register TXModeReg and RXModeReg. After the Transceive command is active, the value of the register bit is relevant.

The FIFO will also receive the two CRC check bytes of the last command even if they already checked and correct, if the state machine (Anticollision and Select routine) has to not been executed and 106 kbit is detected.

During Felica activation the register bit is always relevant and is not overruled by the command settings. This command can be cleared by software by writing any other command to the CommandReg register, e.g. the idle command. Writing the same content again to the CommandReg register resets the state machine.

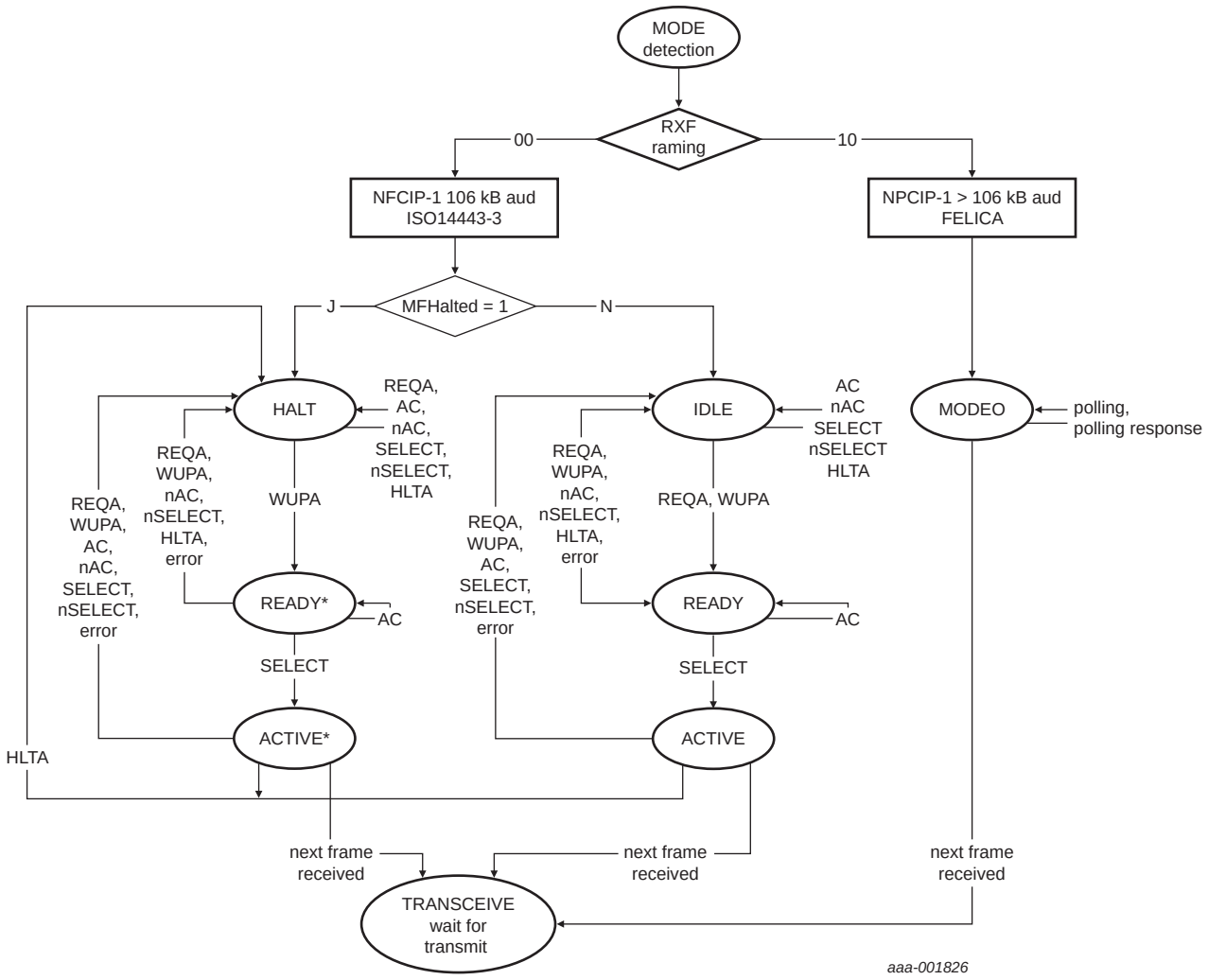


Fig 23. Autocoll Command

NFCIP-1 106 kbps Passive Communication mode:

The MIFARE anticollision is finished and the command has automatically changed to Transceive. The FIFO contains the ATR_REQ frame including the start byte F0h. The bit TargetActivated in the Status2Reg register is set to 1.

NFCIP-1 212/424 kbps Passive Communication mode:

The FeliCa polling command is finished and the command has automatically changed to Transceive. The FIFO contains the ATR_REQ. The bit TargetActivated in the Status2Reg register is set to 1.

MIFARE (Card Operation mode):

The MIFARE anticollision is finished and the command has automatically changed to transceive. The FIFO contains the first command after the Select. The bit TargetActivated in the Status2Reg register is set to 1.

Felica (Card Operation mode):

The FeliCa polling command is finished and the command has automatically changed to transceive. The FIFO contains the first command followed after the Poling by the FeliCa protocol. The bit TargetActivated in the Status2Reg register is set to 1.

18.3.1.10 SoftReset

This command performs a reset of the device. The configuration data of the internal buffer remains unchanged. All registers are set to the reset values. This command automatically terminates when finished.

Remark: The SerialSpeedReg register is reset and therefore the serial data rate is set to 9.6 kBd.

19. Test signals

19.1 Selftest

The PT501 has the capability to perform a digital selftest. To start the selftest the following procedure has to be performed:

1. Perform a soft reset.
2. Clear the internal buffer by writing 25 bytes of 00h and perform the Config Command.
3. Enable the Selftest by writing the value 09h to the register AutoTestReg.
4. Write 00h to the FIFO.
5. Start the Selftest with the CalcCRC Command.
6. The Selftest will be performed.
7. When the Selftest is finished, the FIFO contains the following bytes:

   Correct answer for VersionReg equal to E2h:

```
00h, EBh, 66h, BAh, 57h, BFh, 23h, 95h, D0h, E3h, 0Dh, 3Dh, 27h, 89h, 5Ch, DEh,
     9Dh, 3Bh, A7h, 00h, 21h, 5Bh, 89h, 82h, 51h, 3Ah, EBh, 02h, 0Ch, A5h, 00h,
     49h, 7Ch, 84h, 4Dh, B3h, CCh, D2h, 1Bh, 81h, 5Dh, 48h, 76h, D5h, 71h, 61h,
     21h, A9h, 86h, 96h, 83h, 38h, CFh, 9Dh, 5Bh, 6Dh, DCh, 15h, BAh, 3Eh, 7Dh,
     95h, 3Bh, 2Fh
```

19.2 Testbus

The testbus is implemented for production test purposes. The following configuration can be used to improve the design of a system using the PT501. The testbus allows to route internal signals to the digital interface. The testbus signals are selected by accessing TestBusSel in register TestSel2Reg.

Table 124. Testsignal routing (TestSel2Reg = 07h)

Pins	MX/MOSI/ ADR0	DTRQ/SCK/ ADR1	I²C ADR2	I²C ADR3	I²C ADR4	I²C ADR5	I²C ADR6
Testsignal	sdata	scoll	svalid	sover	RCV_reset	RFon,filtered	Envelope

Table 125. Description of test signals

Pins	Test signal	Description
MX/MOSI/ADR0	sdata	shows the actual received data stream.
DTRQ/SCK/ADR1	scoll	shows if in the actual bit a collision has been detected (106 kbit only)
I²C ADR2	svalid	shows if sdata and scoll are valid
I²C ADR3	sover	shows that the receiver has detected a stop condition (ISO/IEC 14443A/ MIFARE mode only).
I²C ADR4	RCV_reset	shows if the receiver is reset
I²C ADR5	RFon, filtered	shows the value of the internal RF level detector

Table 126. Testsignal routing (TestSel2Reg = 0Dh)

Pins	MX/MOSI/ ADR0	DTRQ/SCK/ ADR1	I²C ADR2	I²C ADR3	I²C ADR4	I²C ADR5	I²C ADR6
Testsignal	clkstable	clk27/8	clk27rf/8	clkrf13rf/4	clk27	clk27rf	clk13rf

Table 127. Description of test signals

Pins	Testsignal	Description
MX/MOSI/ADR0	clkstable	shows if the oscillator delivers a stable signal.
DTRQ/SCK/ADR1	clk27/8	shows the output signal of the oscillator divided by 8
I²C ADR2	clk27rf/8	shows the clk27rf signal divided by 8
I²C ADR3	clkrf13/4	shows the clk13rf divided by 4.
I²C ADR4	clk27	shows the output signal of the oscillator
I²C ADR5	clk27rf	shows the RF clock multiplied by 2.

Table 128. Testsignal routing (TestSel2Reg = 19h)

Pins	MX/MOSI/ ADR0	DTRQ/SCK/ ADR1	I²C ADR2	I²C ADR3	I²C ADR4	I²C ADR5	I²C ADR6
Testsignal	-	TRunning	-	-	-	-	-

Table 129. Description of test signals

Pins	Testsignal	Description
MX/MOSI/ADR0	-	-
DTRQ/SCK/ADR1	TRunning	TRunning stops 1 clockcycle after TimerIRQ is raised
I²C ADR2	-	-
I²C ADR3	-	-
I²C ADR4	-	-
I²C ADR5	-	-

19.3 Test signals at pin AUX

Table 130. Test signals description

SelAux	Description for Aux1 / Aux2
0000	Tristate
0001	DAC: register TestDAC 1/2
0010	DAC: testsignal corr1
0011	DAC: testsignal corr2
0100	DAC: testsignal MinLevel
0101	DAC: ADC_I
0110	DAC: ADC_Q
0111	DAC: testsignal ADC_I combined with ADC_Q
1000	Testsignal for production test
1001	RFU
1010	High
1011	low
1100	TxActive

Table 130. Test signals description *...continued*

SelAux	Description for Aux1 / Aux2
1101	RxActive
1110	Subcarrier detected
1111	TstBusBit

Each signal can be switched to pin AUX1 or AUX2 by setting SelAux1 or SelAux2 in the register AnalogTestReg.

Note: The DAC has a current output, it is recommended to use a 1 kΩ pull-down resistance at pins AUX1/AUX2.

19.4 PRBS

Enables the PRBS9 or PRBS15 sequence according to ITU-TO150. To start the transmission of the defined datastream the command send has to be activated. The preamble/Sync byte/start bit/parity bit are generated automatically depending on the selected mode.

Note: All relevant register to transmit data have to be configured before entering PRBS mode according ITU-TO150.

20. Limiting values

Table 131. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDA}	analog supply voltage		–0.5	+4.0	V
V_{DDD}	digital supply voltage		–0.5	+4.0	V
$V_{DD(PVDD)}$	PVDD supply voltage		–0.5	+4.0	V
$V_{DD(TVDD)}$	TVDD supply voltage		–0.5	+4.0	V
$V_{DD(SVDD)}$	SVDD supply voltage		–0.5	+4.0	V
V_I	input voltage	all input pins except pins SIGIN and RX	$V_{SS(PVSS)}$ – 0.5	$V_{DD(PVDD)}$ + 0.5	V
		pin SIGIN	$V_{SS(PVSS)}$ – 0.5	$V_{DD(SVDD)}$ + 0.5	V
P_{tot}	total power dissipation	per package; and V_{DDD} in shortcut mode	-	200	mW
T_j	junction temperature		-	100	°C
V_{ESD}	electrostatic discharge voltage	HBM; 1500 Ω, 100 pF; JESD22-A114-B	-	2000	V
		MM; 0.75 µH, 200 pF; JESD22-A114-A	-	200	V
		Field induced model; JESC22-C101-A	-	500	V

21. Recommended operating conditions

Table 132. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	analog supply voltage	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V [1][2]	2.5	-	3.6	V
V_{DDD}	digital supply voltage	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V [1][2]	2.5	-	3.6	V
$V_{DD(TVDD)}$	TVDD supply voltage	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V [1][2]	2.5	-	3.6	V
$V_{DD(PVDD)}$	PVDD supply voltage	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V [3]	1.6	-	3.6	V
$V_{DD(SVDD)}$	SVDD supply voltage	$V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	1.6	-	3.6	V
T_{amb}	ambient temperature	HVQFN32	–30	-	+85	°C
Industrial version:						
T_{amb}	ambient temperature	HVQFN32	–40	-	+90	°C

[1] Supply voltages below 3 V reduce the performance (the achievable operating distance).

[2] V_{DDA}, V_{DDD} and $V_{DD(TVDD)}$ must always be the same voltage.

[3] $V_{DD(PVDD)}$ must always be the same or lower voltage than V_{DDD}.

22. Thermal characteristics

Table 133. Thermal characteristics

Symbol	Parameter	Conditions	Package	Typ	Unit
R_{thj-a}	Thermal resistance from junction to ambient	In still air with exposed pad soldered on a 4 layer Jedec PCB In still air	HVQFN32	40	K/W

23. Characteristics

Table 134. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input characteristics						
Pins SPI SEL, I^2C SEL and NRSTPD						
I_{LI}	input leakage current		–1	-	+1	µA
V_{IH}	HIGH-level input voltage		$0.7V_{DD(PVDD)}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD(PVDD)}$	V
Pin SIGIN						
I_{LI}	input leakage current		–1	-	+1	µA
V_{IH}	HIGH-level input voltage		$0.7V_{DD(SVDD)}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD(SVDD)}$	V
Pin ALE-UART						
I_{LI}	input leakage current		–1	-	+1	µA
V_{IH}	HIGH-level input voltage		$0.7V_{DD(PVDD)}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD(PVDD)}$	V
Pin RX[1]						
V_i	input voltage		–1	-	V_{DDA} +1	V
C_i	input capacitance	V_{DDA} = 3 V; receiver active; $V_{RX(p-p)}$ = 1 V; 1.5 V (DC) offset	-	10	-	pF
R_i	input resistance	V_{DDA} = 3 V; receiver active; $V_{RX(p-p)}$ = 1 V; 1.5 V (DC) offset	-	350	-	Ω
Input voltage range; see Figure 24						
$V_{i(p-p)(min)}$	minimum peak-to-peak input voltage	Manchester encoded; V_{DDA} = 3 V	-	100	-	mV
$V_{i(p-p)(max)}$	maximum peak-to-peak input voltage	Manchester encoded; V_{DDA} = 3 V	-	4	-	V
Input sensitivity; see Figure 24						
V_{mod}	modulation voltage	minimum Manchester encoded; V_{DDA} = 3 V; RxGain[2:0] = 111b (48 dB)	-	5	-	mV
Pin OSCIN						
I_{LI}	input leakage current		–1	-	+1	µA
V_{IH}	HIGH-level input voltage		$0.7V_{DDA}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DDA}$	V

Table 134. Characteristics *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_i	input capacitance	V_{DDA} = 2.8 V; DC = 0.65 V; AC = 1 V (p-p)	-	2	-	pF
Input/output characteristics						
pins I²C ADR5, I²C ADR4, I²C ADR3, I²C ADR2, DTRQ/SCK/ADR1, MX/MOSI/ADR0, TX/MISO/SCL						
I_{LI}	input leakage current		−1	-	+1	µA
V_{IH}	HIGH-level input voltage		$0.7V_{DD(PVDD)}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD(PVDD)}$	V
V_{OH}	HIGH-level output voltage	$V_{DD(PVDD)}$ = 3 V; I_O = 4 mA	$V_{DD(PVDD)}$ − 0.4	-	$V_{DD(PVDD)}$	V
V_{OL}	LOW-level output voltage	$V_{DD(PVDD)}$ = 3 V; I_O = 4 mA	$V_{SS(PVSS)}$	-	$V_{SS(PVSS)}$ + 0.4	V
I_{OH}	HIGH-level output current	$V_{DD(PVDD)}$ = 3 V	-	-	4	mA
I_{OL}	LOW-level output current	$V_{DD(PVDD)}$ = 3 V	-	-	4	mA
Output characteristics						
Pin SIGOUT						
V_{OH}	HIGH-level output voltage	$V_{DD(SVDD)}$ = 3 V; I_O = 4 mA	$V_{DD(SVDD)}$ − 0.4	-	$V_{DD(SVDD)}$	V
V_{OL}	LOW-level output voltage	$V_{DD(SVDD)}$ = 3 V; I_O = 4 mA	$V_{SS(PVSS)}$	-	$V_{SS(PVSS)}$ + 0.4	V
I_{OL}	LOW-level output current	$V_{DD(SVDD)}$ = 3 V	-	-	4	mA
I_{OH}	HIGH-level output current	$V_{DD(SVDD)}$ = 3 V	-	-	4	mA
Pin IRQ						
V_{OH}	HIGH-level output voltage	$V_{DD(PVDD)}$ = 3 V; I_O = 4 mA	$V_{DD(PVDD)}$ − 0.4	-	$V_{DD(PVDD)}$	V
V_{OL}	LOW-level output voltage	$V_{DD(PVDD)}$ = 3 V; I_O = 4 mA	$V_{SS(PVSS)}$	-	$V_{SS(PVSS)}$ + 0.4	V
I_{OL}	LOW-level output current	$V_{DD(PVDD)}$ = 3 V	-	-	4	mA
I_{OH}	HIGH-level output current	$V_{DD(PVDD)}$ = 3 V	-	-	4	mA
Pins AUX1 and AUX2						
V_{OH}	HIGH-level output voltage	V_{DDD} = 3 V; I_O = 4 mA	V_{DDD} − 0.4	-	V_{DDD}	V
V_{OL}	LOW-level output voltage	V_{DDD} = 3 V; I_O = 4 mA	$V_{SS(PVSS)}$	-	$V_{SS(PVSS)}$ + 0.4	V
I_{OL}	LOW-level output current	V_{DDD} = 3 V	-	-	4	mA
I_{OH}	HIGH-level output current	V_{DDD} = 3 V	-	-	4	mA
Pins TX1 and TX2						
Current consumption						
I_{pd}	power-down current	V_{DDA} = V_{DDD} = $V_{DD(TVDD)}$ = $V_{DD(PVDD)}$ = 3 V				
		hard power-down; pin NRSTPD set LOW [2]	-	-	5	µA
		soft power-down; RF level detector on [2]	-	-	10	µA
$I_{DD(PVDD)}$	PVDD supply current	pin PVDD [3]	-	-	40	mA
$I_{DD(SVDD)}$	SVDD supply current	pin SVDD [4]	-	-	4	mA

Table 134. Characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DDD}	digital supply current	pin DVDD; V_{DDD} = 3 V	-	6.5	9	mA
I_{DDA}	analog supply current	pin AVDD; V_{DDA} = 3 V, CommandReg register's RcvOff bit = 0	-	7	10	mA
		pin AVDD; receiver switched off; V_{DDA} = 3 V, CommandReg register's RcvOff bit = 1	-	3	5	mA
Clock frequency						
f_{clk}	clock frequency		-	27.12	-	MHz
δ_{clk}	clock duty cycle		40	50	60	%
t_{jit}	jitter time	RMS	-	-	10	ps
Crystal oscillator						
V_{OH}	HIGH-level output voltage	pin OSCOUT	-	1.1	-	V
V_{OL}	LOW-level output voltage	pin OSCOUT	-	0.2	-	V
C_i	input capacitance	pin OSCOUT	-	2	-	pF
		pin OSCIN	-	2	-	pF
Typical input requirements						
f_{xtal}	crystal frequency		-	27.12	-	MHz
ESR	equivalent series resistance		-	-	100	Ω
C_L	load capacitance		-	10	-	pF
P_{xtal}	crystal power dissipation		-	50	100	μW

[1] The voltage on pin RX is clamped by internal diodes to pins AVSS and AVDD.

[2] I_{pd} is the total current for all supplies.

[3] $I_{DD(PVDD)}$ depends on the overall load at the digital pins.

[4] $I_{DD(SVDD)}$ depends on the load at pin SIGOUT.

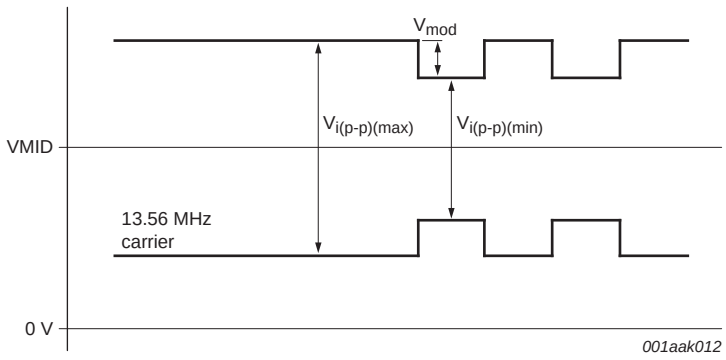


Fig 24. Pin RX input voltage range

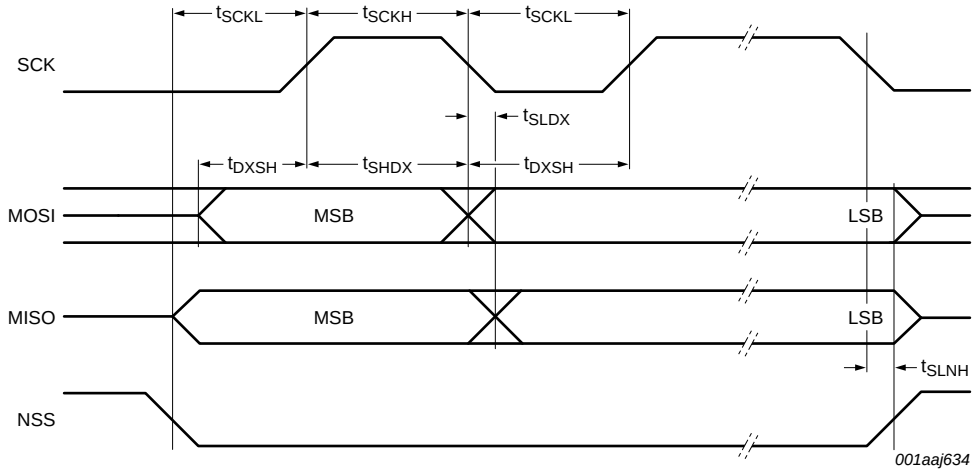
23.1 Timing characteristics

Table 135. SPI timing characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{WL}	pulse width LOW	line SCK	50	-	-	ns
t_{WH}	pulse width HIGH	line SCK	50	-	-	ns
$t_{h(SCKH-D)}$	SCK HIGH to data input hold time	SCK to changing MOSI	25	-	-	ns
$t_{su(D-SCKH)}$	data input to SCK HIGH set-up time	changing MOSI to SCK	25	-	-	ns
$t_{h(SCKL-Q)}$	SCK LOW to data output hold time	SCK to changing MISO	-	-	25	ns
$t_{(SCKL-NSSH)}$	SCK LOW to NSS HIGH time		0	-	-	ns

Table 136. I^2C-bus timing in Fast mode

Symbol	Parameter	Conditions	Fast mode		High-speed mode		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	400	0	3400	kHz
$t_{HD;STA}$	hold time (repeated) START condition	after this period, the first clock pulse is generated	600	-	160	-	ns
$t_{SU;STA}$	set-up time for a repeated START condition		600	-	160	-	ns
$t_{SU;STO}$	set-up time for STOP condition		600	-	160	-	ns
t_{LOW}	LOW period of the SCL clock		1300	-	160	-	ns
t_{HIGH}	HIGH period of the SCL clock		600	-	60	-	ns
$t_{HD;DAT}$	data hold time		0	900	0	70	ns
$t_{SU;DAT}$	data set-up time		100	-	10	-	ns
t_r	rise time	SCL signal	20	300	10	40	ns
t_f	fall time	SCL signal	20	300	10	40	ns
t_r	rise time	SDA and SCL signals	20	300	10	80	ns
t_f	fall time	SDA and SCL signals	20	300	10	80	ns
t_{BUF}	bus free time between a STOP and START condition		1.3	-	1.3	-	µs



Remark: The signal NSS must be LOW to be able to send several bytes in one data stream. To send more than one data stream NSS must be set HIGH between the data streams.

Fig 25. Timing diagram for SPI

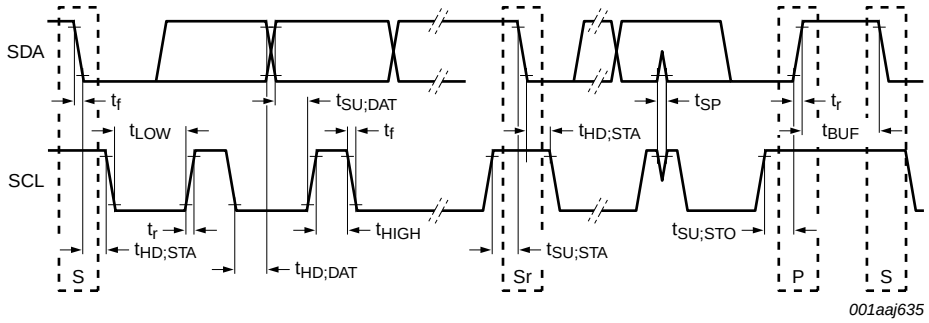


Fig 26. Timing for Fast and Standard mode devices on the I^2C-bus

24. Package information

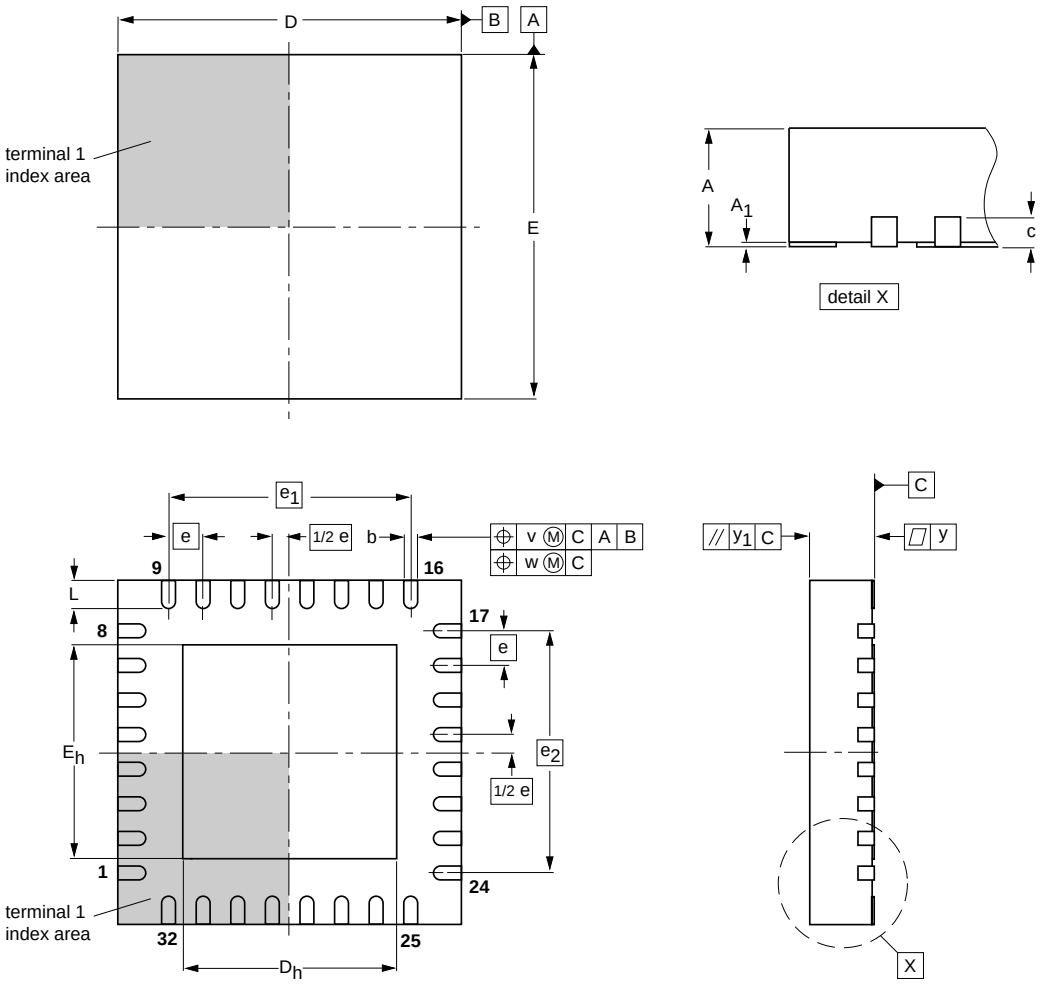
The PT501 can be delivered in the following package:

Table 137. Package information

Package	Remarks
HVQFN32	-

25. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.5	3.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT617-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-18

Fig 27. Package outline package version (HVQFN32)

26. Abbreviations

Table 138. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
ASK	Amplitude Shift keying
BPSK	Binary Phase Shift Keying
CRC	Cyclic Redundancy Check
CW	Continuous Wave
DAC	Digital-to-Analog Converter
EOF	End of frame
HBM	Human Body Model
I^2C	Inter-integrated Circuit
LSB	Least Significant Bit
MISO	Master In Slave Out
MM	Machine Model
MOSI	Master Out Slave In
MSB	Most Significant Bit
NSS	Not Slave Select
PCB	Printed-Circuit Board
PLL	Phase-Locked Loop
PRBS	Pseudo-Random Bit Sequence
RX	Receiver
SOF	Start Of Frame
SPI	Serial Peripheral Interface
TX	Transmitter
UART	Universal Asynchronous Receiver Transmitter

27. Glossary

Modulation index — Defined as the voltage ratio $(V_{max} - V_{min}) / (V_{max} + V_{min})$.

Load modulation index — Defined as the voltage ratio for the card $(V_{max} - V_{min}) / (V_{max} + V_{min})$ measured at the card's coil.

Initiator — Generates RF field at 13.56 MHz and starts the NFCIP-1 communication.

Target — Responds to command either using load modulation scheme (RF field generated by Initiator) or using modulation of self generated RF field (no RF field generated by initiator).

28. Revision history

Table 139. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PT501 v. 3.2	20140326	Product data sheet	-	PT501 v. 3.1
Modifications:	Section 29.4 “Licenses”: updated			
PT501 v. 3.1	20131210	Product data sheet	-	PT501 v. 3.0
Modifications:	• Section 8.3 “ISO/IEC 14443-A Card operation mode”: updated			
PT501 v. 3.0	20131023	Product data sheet	-	-

29. Legal information

29.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Date of release: 26 March 2014
224632

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