SGM48005
Zero Overshoot, Large Swing MOSFET Driver with Precision Dual-Rail Generation Circuit

GENERAL DESCRIPTION

The SGM48005 is a high current MOSFET driver with a dual power rail generation circuit using a single inductor for getting both positive rail and negative rail. With its unique overshoot cancellation mechanism and its extended precision power rails, the SGM48005 drives the gate with no series damping resistor for sharp and clean rise and fall seen at the gate, which is important for high power design of switch mode power supplies running faster than a few hundred kHz. The adaptive overshoot cancellation allows placing the driver in a different location (temperature zone) from the power MOSFET's, which simplifies circuit layout and cooling. The inverted input buffer is out of phase with the ground bouncing. Along with its current and voltage hysteresis, this assures high noise immunity and easy input signal coupling. The propagation delay of input low to output high is programmed with a resistor, for pairing switches in totem pole with no shooting through. The saturation voltage of power switch is sensed for over-current protection.

The SGM48005 is available in a Green TSSOP-14 package. It operates over an ambient temperature range of -40℃ to +125℃.

FEATURES

- **Negative and Positive Large Precision Swings**
- **12A Peak Sourcing and 9A Peak Sinking**
- **No Overshoot even without Damping Resister**
- **Positive and Negative Rail Generation**
- **MOSFET On-Delay Resistor Programming**
- **Fast Rise/Fall Time 2.9ns/3.6ns at 1.5cm Away**
- **Remote Placement Capable**
  - **4ns/4ns Rise/Fall Time at 3cm Away**
- **Inverted Input Buffer**
  - **3V ~ 5V Logic Level Input**
  - **Current Hysteresis and Voltage Hysteresis**
- **MOSFET Saturation Voltage Sensing for Protection**
- **Programmable Output Swings:**
  - **SGM48005-1: Swing = -4V ~ +15V**
  - **SGM48005-2: Swing = -4V ~ +20V**
- **Minimum and Maximum On-Times: 250ns and 400μs**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green TSSOP-14 Package**

APPLICATION

High Power SiC MOSFET, Si MOSFET, IGBT Circuits
High Power Switch Mode Power Supply
High Power Motor Driver

TYPICAL APPLICATION

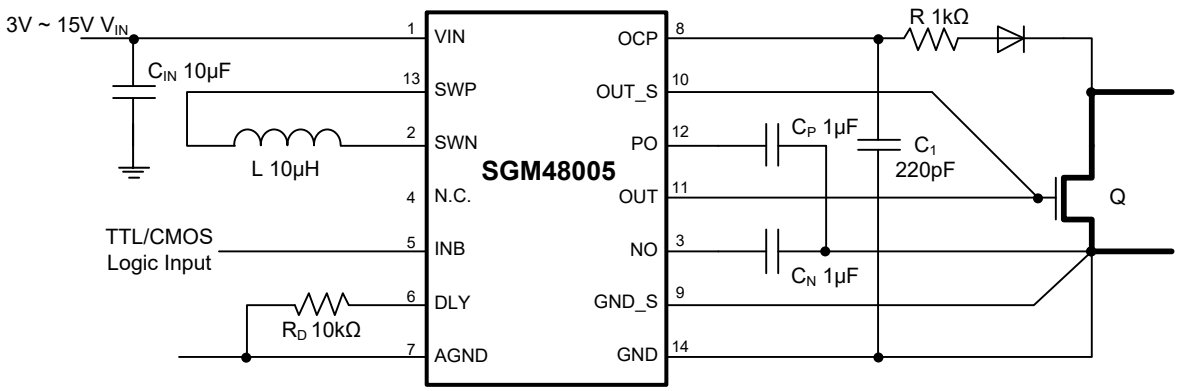


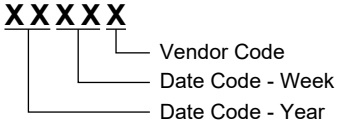
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM48005-1	TSSOP-14	-40℃ to +125℃	SGM48005-1XTS14G/TR	SGM480051 XTS14 XXXXX	Tape and Reel, 4000
SGM48005-2	TSSOP-14	-40℃ to +125℃	SGM48005-2XTS14G/TR	SGM480052 XTS14 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

XXXXX = Date Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN to GND ..... -0.3V to 16.5V
SWN to GND ..... -5V to 15V
SWP to GND ..... -0.3V to 22V
NO to GND ..... -4.4V to 0.3V
PO to GND ..... -0.3V to 26.5V
DLY to GND ..... -0.3V to 6V
INB to GND ..... -0.3V to V_{IN} + 0.3V
OCP to GND ..... -0.3V to 13.2V
OUT to GND ..... V_{NO} - 0.3V to V_{PO} + 0.3V
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
MM 200V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ..... 3V to 15V
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

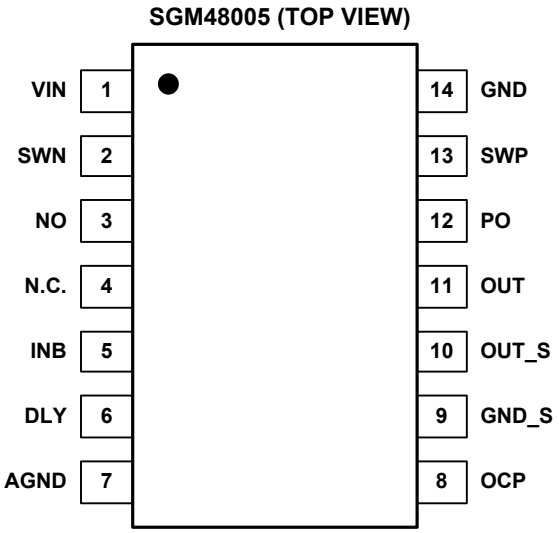
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	VIN	P	Power supply.
2	SWN	O	Switch node for generating the negative rail. Connect to one end of the power inductor.
3	NO	O	Internally generated negative rail. It biases the driver stage for the negative swing.
4	N.C.	NC	No connection. Leaving it open or connecting to any static level is recommended.
5	INB	I	Inverted buffer input. INB low for OUT high and INB high for OUT low correspondingly.
6	DLY	O	INB low to OUT high propagation delay programming. Connect a resistor (R_D) between this pin and ground to program the delay time.
7	AGND	IO	Ground node of the input buffer and the delay programming circuit. This AGND pin connects to the GND pin through an internal circuit.
8	OCP	IO	For over-current protection sensing. The saturation voltage of the external MOSFET is sensed during the on-period in a time window after leading edge transient blanking. This pin cannot withstand high voltage; an external high voltage blocking diode is required.
9	GND_S	I	Ground sensing. Connect to the source of the power MOSFET with a dedicated trace or wire.
10	OUT_S	I	Gate sensing. Connect to the gate of the power MOSFET with a dedicated trace or wire.
11	OUT	O	The MOSFET gate driving output.
12	PO	O	Internally generated positive rail. It biases the driver stage for the positive swing.
13	SWP	O	Switch node for generating the positive rail. Connect to the other end of the power inductor.
14	GND	G	Driver stage ground.

NOTE: G: ground; I: input; IO: input and output; NC: no connection; O: output; P: power.

ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, V_{IN} = 5V, typical values are at T_A = +25℃, C_{LOAD} = 1.8nF, 100kHz and 50% duty cycle, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
Supply and Power Up								
Minimum Operation Supply Voltage	V_{OPMIN}			+25℃			3	V
Maximum Operation Supply Voltage	V_{OPMAX}			+25℃	15			V
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} falling.		+25℃		2.3	2.8	V
Under-Voltage Threshold Hysteresis	V_{HYS}	V_{IN} rising.		+25℃		0.3		V
Quiescent Current	I_{IN}	INB = 3.3V, force V_{NO} = -102%, V_{PO} = 102% with external power supplies, measure the current into the VIN pin for the I_{IN} and into the PO pin for I_{PO}.		+25℃		1	1.3	mA
	I_{PO}					1.2	1.6	
Power On Blanking Time	t_{BLANK}	The OUT drives low and the INB is pulled up regardless of the input status.		+25℃		32		ms
INB Buffer Input and Propagation Programming								
Low Level Input Voltage Threshold	V_{IL}	Test with DC biasing.		Full			1.2	V
High Level Input Voltage Threshold	V_{IH}	Test with DC biasing.		Full	2.4			V
INB Pull-Up and Pull-Down Current	I_{PULL}			+25℃		0.5		mA
Minimum Effective Pulse Width	twpp	0.5V over-driving DC thresholds.	Rising	+25℃		50		ns
	twnp		Falling	+25℃		50		
Pull-Up Voltage	V_{BIASM}	For V_{IN} > 4.3V		+25℃		4.3		V
	V_{BIAS}	For V_{IN} < 4.3V		+25℃		V_{IN}		
Input High Over-Driving Clamp Current	I_{CLPIN}	Forcing into INB, no malfunction.		+25℃		0.5		mA
Input Low Over-Driving Clamp Current	I_{CLPOUT}	Forcing out of INB, no malfunction.		+25℃		0.5		mA
Input Low to Output High Propagation Delay	t_{ON_DLY}	C_{LOAD} = 1.8nF, 1.5cm away, 3.3V input pulse, R_D = 10kΩ.		+25℃		48		ns
Input Low to Output High Propagation Skew	t_{ONSKEW}					0.65		ns
Input High to Output Low Propagation Delay	t_{OFF_DLY}					34		ns
Input High to Output Low Propagation Skew	$t_{OFFSKEW}$					0.85		ns
Driver								
Peak Driving Current	I_{SINK}	Source from PO, sink to NO in 10ns (1), measured with a current sensing loop.		+25℃		9		A
	I_{SOURCE}					-12		
Output Pull-Up Resistance of Forced Driving (1)	R_{OH}			+25℃		0.6		Ω
Output Pull-Down Resistance	R_{OL}			+25℃		1		
Rise Time, 10% ~ 90% Swing	t_R	C_{LOAD} = 1.8nF, 1.5cm away.		+25℃		6		ns
		C_{LOAD} = 1.8nF, 3cm away.		+25℃		20		
Fall Time, 10% ~ 90% Swing	t_F	C_{LOAD} = 1.8nF, 1.5cm away.		+25℃		8		ns
		C_{LOAD} = 1.8nF, 3cm away.		+25℃		20		
1V to 5V Rise Time	t_{R1to5}	C_{LOAD} = 1.8nF, 1.5cm away.		+25℃		2.9		ns
		C_{LOAD} = 1.8nF, 3cm away.		+25℃		4		
5V to 1V Fall Time	t_{F5to1}	C_{LOAD} = 1.8nF, 1.5cm away.		+25℃		3.6		ns
		C_{LOAD} = 1.8nF, 3cm away.		+25℃		4		
Minimum On-Time	t_{MIN}			+25℃		250		ns
Maximum On-Time	t_{MAX}			+25℃	200	400	600	μs

NOTE: 1. The high current pull-up may be terminated by the internal anti-ringing circuit after 10ns forced driving.

ELECTRICAL CHARACTERISTICS (continued)

(Full = -40℃ to +125℃, V_{IN} = 5V, typical values are at T_A = +25℃, C_{LOAD} = 1.8nF, 100kHz and 50% duty cycle, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
MOSFET Over Current Detection And Protection								
Over-Current Protection Threshold	V_{OCP}	V_{OCP} rising.		Full	5.9	6.6	7.3	V
Over-Current Protection Blanking Time	t_{OCPB}	From V_{INB} falling below 1V to protection circuit enabled.		+25℃		600		ns
PO to OCP Internal Biasing Resistance	R_{BIAS}			+25℃		12.5		kΩ
OCP Clamp Voltage	V_{OVPCLP}	OCP floating.		+25℃		8.55		V
		Force 1mA into OCP.				8.78		
OCP Pin Parasitic Capacitance	C_{BIAS}			+25℃		5		pF
OCP Effective to OUT Falling Propagation	$t_{OCP\ (90\%)}$	C_{LOAD} = 1.8nF, OUT falls to 90%.		+25℃		1		μs
Driver Blanking Time due to OCP Forced OUT Low	t_{MASK}			+25℃		5.5		ms
Soft Switching Time for Forced Off Event	t_{SOFF}	C_{LOAD} = 1.8nF, OUT falls from 90% to 10%.		+25℃		4.2		μs
Rails Generation								
Positive-Rail Voltage	V_{PO}	SGM48005-1		+25℃	14.2	14.7	15.2	V
		SGM48005-2		+25℃	18.9	19.6	20.3	
Negative-Rail Voltage	V_{NO}	SGM48005-1		+25℃	-4.2	-4	-3.8	
		SGM48005-2		+25℃	-4.2	-4	-3.8	
5V VIN Load Capacity	I_{5to15}	Measured when PO or NO drops 10% from the no load voltage.	SGM48005-1	+25℃	30			mA
	I_{5to20}		SGM48005-2	+25℃	20			
12V VIN Load Capacity	I_{12to15}		SGM48005-1	+25℃	90			
	I_{12to20}		SGM48005-2	+25℃	70			
Inductor Peak Current	I_{PEAK}			+25℃	0.48	0.6	0.7	A
Discharge Resistor of Positive Output	R_{DP}			+25℃		50		Ω
Discharge Resistor of Negative Output	R_{DN}			+25℃		50		
Switching Frequency	f_{SW}			+25℃	0.85	1.0	1.25	MHz

RECOMMENDED COMPONENTS OF TEST CIRCUITS

	COMPONENT
INDUCTOR	10μH/CD75NP-100KC
CAPACITOR	1μF/C2012X7R1H105JT
	10μF/C2012X7R1H106JT
	1.8nF/GRM155R71H182KA01D
	220pF/08055A221JAT2A

TIMING TABLE OF DRIVER

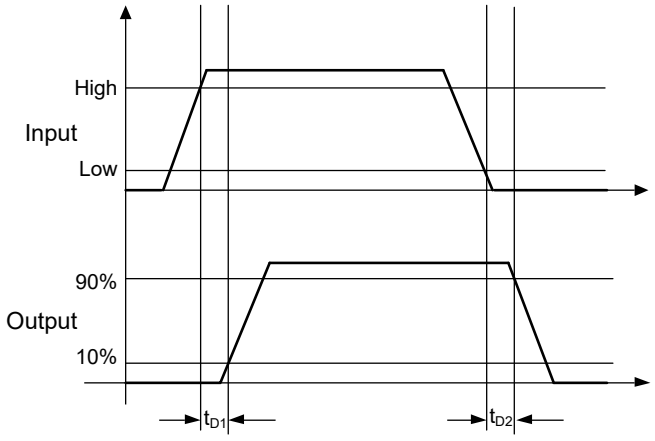
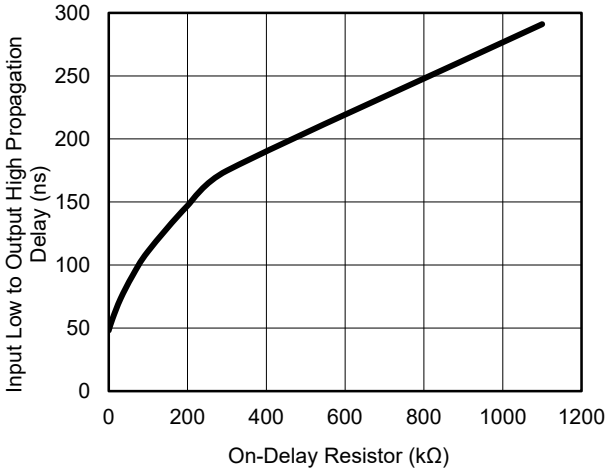


Figure 2. Non-Inverting Input Driver Operation

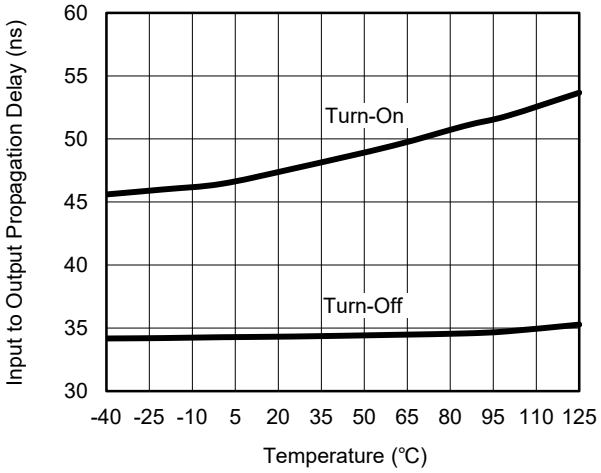
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 5V, C_{IN} = 10μF, L = 10μH, C_P = C_N = 1μF, C_1 = 220pF, R_D = 10kΩ, C_{LOAD} = 1.8nF, unless otherwise noted.

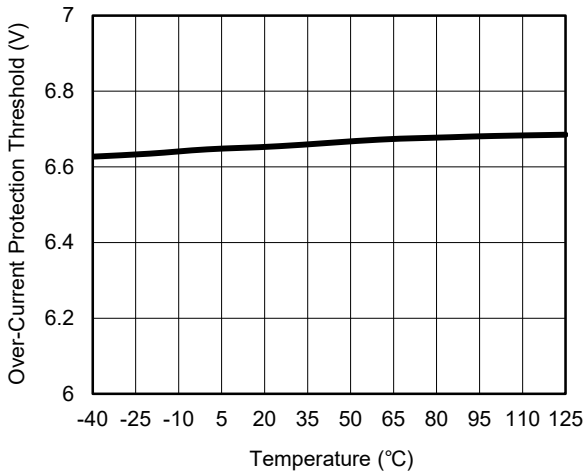
Input Low to Output High Propagation Delay vs. On-Delay Resistor



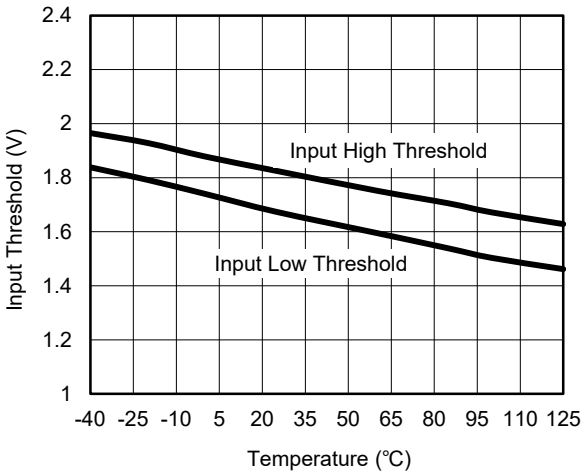
Input to Output Propagation Delay vs. Temperature



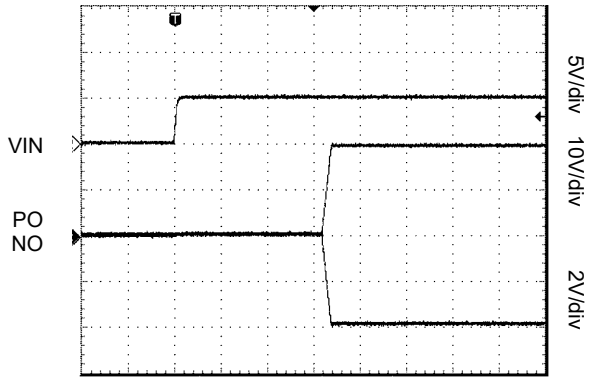
Over-Current Protection Threshold vs. Temperature



Input Threshold vs. Temperature



Start-Up



Time (10ms/div)

FUNCTIONAL BLOCK DIAGRAM

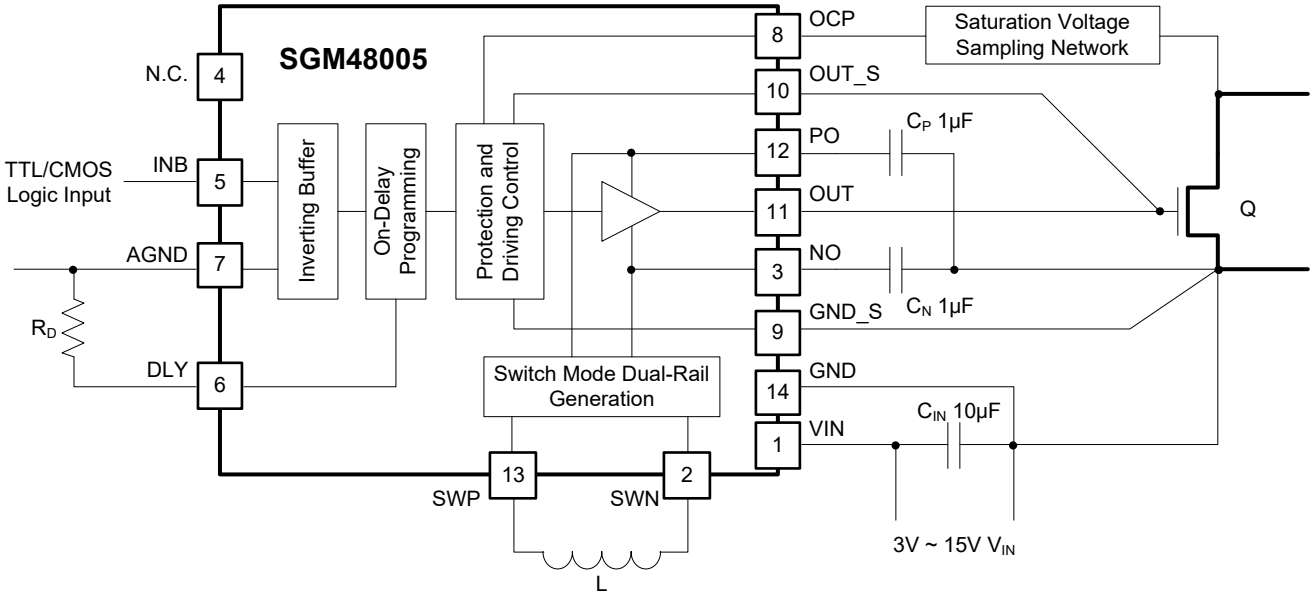


Figure 3. Functional Block Diagram

TEST SET-UP

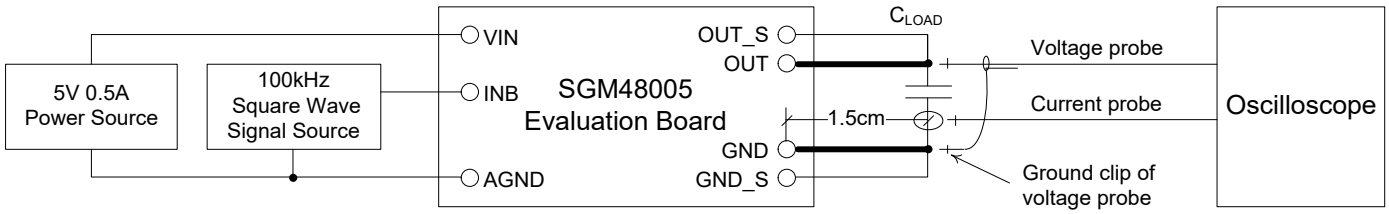


Figure 4. Peak Current and Timing Test Set-Up

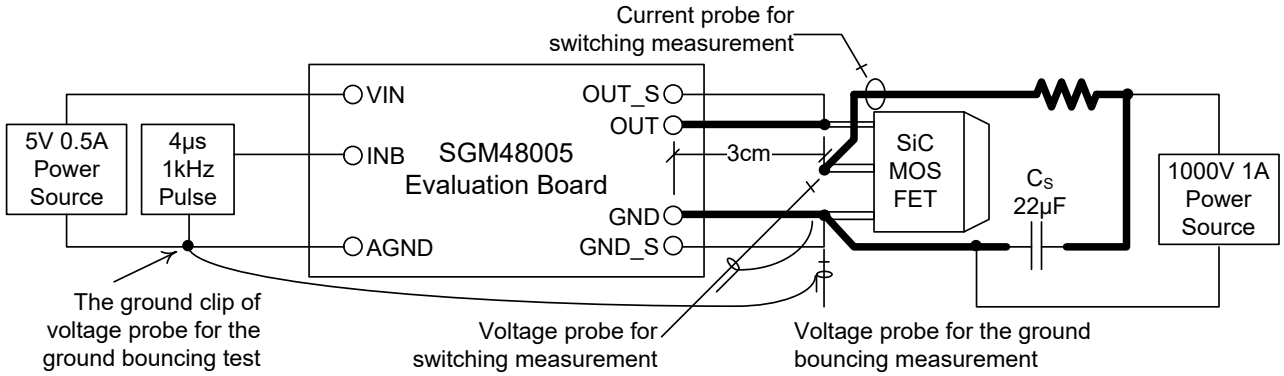


Figure 5. Resistive Load Switching and Ground Bouncing Test Set-Up

DETAILED DESCRIPTION

The SGM48005 has four circuit blocks: a logic input buffer with programmable on-delay, a drive stage with level shifter, a MOSFET current protection, and a dual-rail generator.

The output swings from the negative rail voltage to the positive rail voltage at an adaptive rate that makes the on/off fast. Figure 6 and Figure 7 are the waveforms of gate driving current and the drain voltage of a SiC MOSFET.

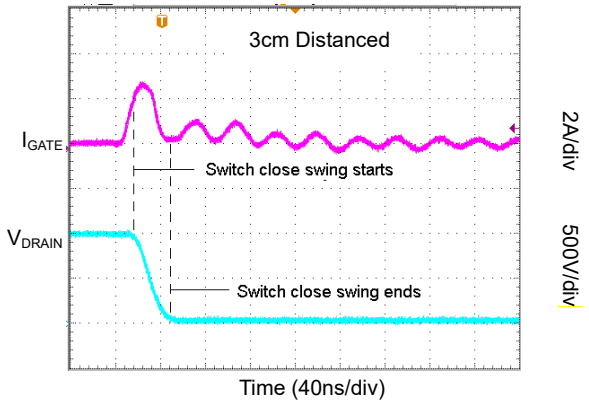


Figure 6. Gate Driving Current and Switch Close Swing

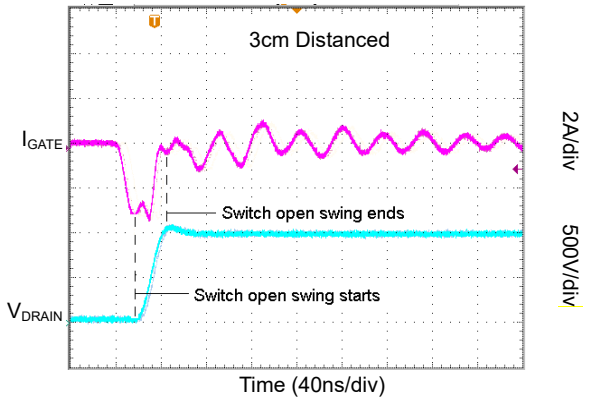


Figure 7. Gate Driving Current and Switch Open Swing

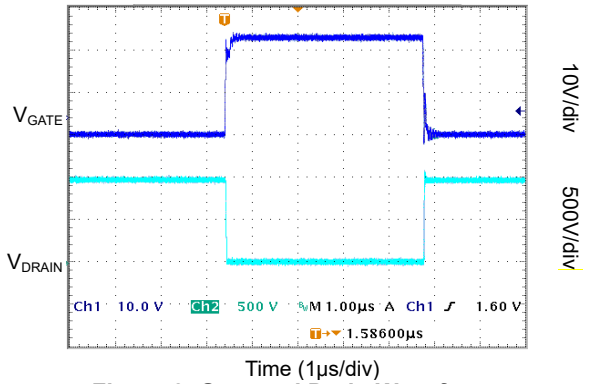


Figure 8. Gate and Drain Waveforms

The dual rail generation circuit converts a wide range of 3V to 15V unregulated input to regulated rails of -4V and 15V (SGM48005-1) or -4V and 20V (SGM48005-2), with only few external components. Figure 8 shows the gate driving waveform and the waveform seen at the drain of MOSFET.

Under-Voltage Lockout

The SGM48005 device has an internal VIN under-voltage lockout (UVLO) protection circuit block. When VIN falls below UVLO threshold, this circuit holds the output low, regardless of the INB input. The typical UVLO level is 2.3V with 300mV hysteresis.

Inverted Input Buffer and On-Delay Programming

Figure 9 shows input buffer circuit, which is basically a schmitt trigger with two controlled current sources, for enhanced noise immunity.

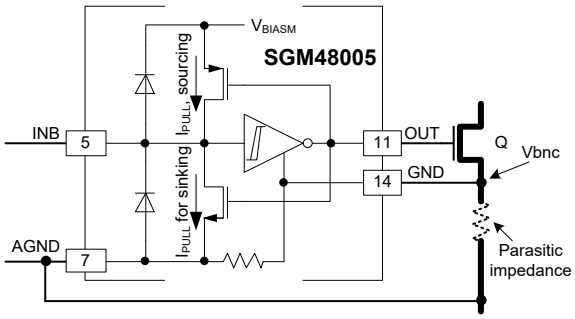


Figure 9. The Buffer with Current and Voltage Hysteresis

Ground bouncing is the result of surge current flowing through the parasitic impedance in the power return path, which has peak values in the range of 40V ~ 70V in the 50A-1000V SiC MOSFET switching test (3cm distance). As the ground bouncing is in the same direction of the input signal change to the SGM48005, it doesn't cause chattering. The surge to the INB input is bypassed by diodes in parallel with the INB input.

The input low to output high transition delay is programmed by the R_D. This function is used for tuning the dead time in the complementary parallel pairs or the totem pole push-pull pile, to prevent shoot through. The delay time as a function of resistance R_D is shown in Typical Performance Characteristics.

CIRCUIT DESCRIPTION AND APPLICATION INFORMATION

Interfacing with the Controller

With its strengthened noise immunity, the SGM48005 can directly interface a logic output of 3V ~ 5V levels easily for low-side switch application, even if the ground bounces a few dozen volts. For high-side application, either a high speed photo-coupler or a simple tiny pulse transformer can work properly. However, a transformer might be more beneficial for its faster transmission.

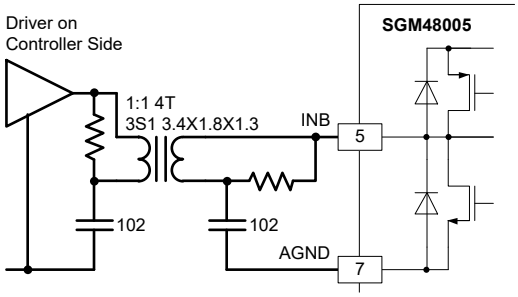


Figure 10. Transformer for High-side I/F

Figure 10 shows the circuit used in the SGM48005 evaluation test. The INB is biased high by the end of power up blanking time or by the end of over current protection mute. The DC level at the INB is determined by the duty cycle of the input signal and the pull-up or pull-down currents in the SGM48005.

Over-Current Protection

The SGM48005 OCP (over-current protection) circuit monitors the drain saturation voltage of the power switch in the closed state, and triggers a switch off sequence if the voltage on OCP exceeds a given threshold V_{OCP}. When the switch off sequence is triggered, the normal gate drive operation is stopped instantly and an additional controlled path discharges the driving output slowly to avoid causing an excessive voltage spike. After an OCP event, normal operation is disabled for t_{MASK}, and the input buffer is reset to hold OUT low. After the t_{MASK} is timed out, the normal operation resumes.

Figure 11 shows the over-current protection circuit. The R_{BIAS} is pulled to the PO only when the OUT goes high, and the comparator is enabled after a blanking time t_{OCPB}. C_0 is the parasitic capacitance additional to the real capacitor capacitance C_1. C_0 and C_1 are equivalent to a total capacitance C for design estimation; the fast recovery diode D with junction capacitance C_D is essential to the sampling circuit. The R and the Z are for fine tuning the circuit behavior.

The voltage at OCP is used for current sensing. The typical trigger voltage is 6.6V. The protected current value can be approximated as the ratio of the OCP trigger voltage and the on resistance of the external power switch.

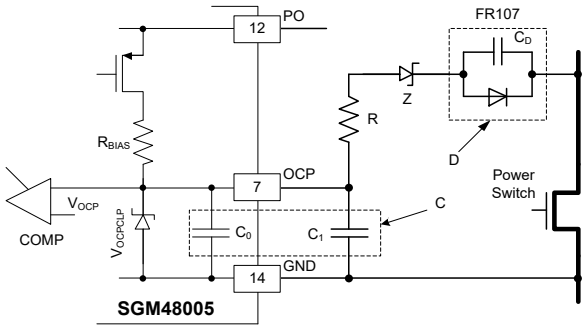


Figure 11. The Circuit of the OCP Function

The diode D blocks the high voltage when the switch turns off. A few of its key parameters are listed in Table 1.

Table 1. Typical Parameters of FR107

Reverse Voltage	600V
Recover Time	75ns
Reverse Leakage, V_{RV} = 600V	30μA
Forward Voltage, I_{FD} = 1A	1.3V
Junction Capacitance, V_{RV} = 4V	15pF

CIRCUIT DESCRIPTION AND APPLICATION INFORMATION (continued)

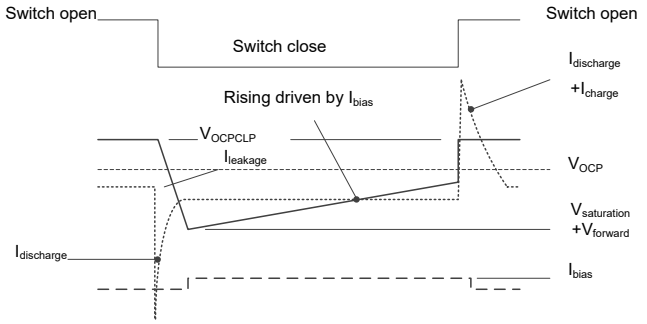


Figure 12. The Key Variables for OCP Design Estimation

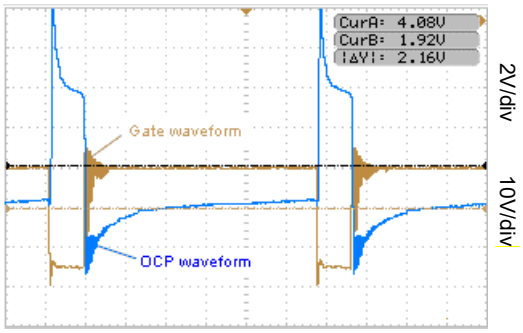


Figure 13. OCP Waveform

Figure 12 illustrates the key variables that form the voltage at the OCP node. Figure 13 is a real waveform at the OCP pin.

Over On-Time Protection

The SGM48005 limits the maximum on-time regardless the input status, to protect the switch from irregular turn-on. Once input low happens again, normal switching resumes.

Driving Different Power Switches

The SGM48005 could drive a fast power switch which is 3cm ~ 6cm away, with less restrictions on on/off time, which gives possibilities for flexible layout/partition and system test. One example is to place it behind a thermal isolation wall of the hot power SiC MOSFET or out of the hot power module case. Another example is to wire the driver board to a MOSFET on another board for test.

With its programmable on-delay, it is suitable for driving any types of SiC MOSFET, Si MOSFET and IGBT. The SGM48005 maintains low impedance driving and could source large current when the output is low, which makes it ideal for driving a high power IGBT. Either IGBT or Si MOSFET has dV/dt and dI/dt. The SGM48005's driving capability may be too high for small power devices and a damp circuit might be desired.

Board Design Consideration

Current loops, ground bouncing and leakage from high voltage need to be carefully handled in the layout and board design. There is large transient current flowing in the OUT-GND loop. The ground plane shielding the OUT-gate connection should be continuous and uninterrupted, or run a ground stripe alongside the connection. Both tracing and wiring should be kept straight, wide and smooth, even if the driver and the power switches are not far apart. Two sensing inputs, the OUT_S stripe and GND_S stripe should be parallel with the OUT stripe and GND stripe, and connect at the far end close to the power switch.

The large current in the power path creates voltage drop over the path. The drive stage has to bootstrap over the ground bounce to maintain effective drive. The complexity of handling ground bouncing is the product of power switch numbers and control/signal path length. Low coupling isolation for both signal and power using transformers or photo-coupler plus transformer is the most comprehensive solution to the ground bouncing issue.

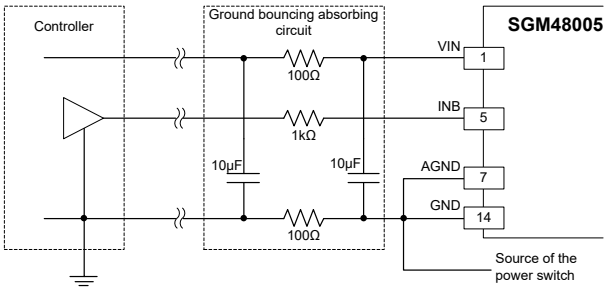


Figure 14. The Simple Circuit for Absorbing Ground Bounce

CIRCUIT DESCRIPTION AND APPLICATION INFORMATION (continued)

As the ground bounce is in the reverse direction to the control input and the input buffer is self-sustained, it is feasible to use the simple circuit with resistor, capacitor and diode for absorbing ground bounce in the controller to driver (SGM48005) connections. Figure 14 is a simple absorbing circuit, which is part of the SGM48005 evaluation circuit and it is proved to be effective during the SGM48005 characterization. The ground bounce pulse at the source of the power MOSFET switch seen from the controller side is absorbed with the resistors.

Figure 15 is another circuit proven with the SGM48005 evaluation board, which is known as flying driver, bootstrapped over the output of the high-side switch.

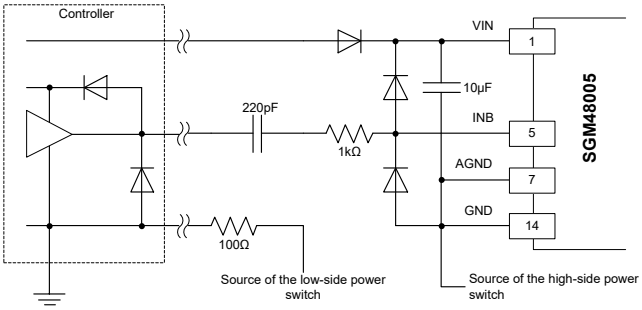


Figure 15. The Flying Driver for High-side Driving

However, both the bouncing absorbing circuit and the flying driver are vulnerable to rare accident like load short circuit, creepage and irregular power resuming. The isolation between powering and signaling is recommended in heavy load applications.

REVISION HISTORY

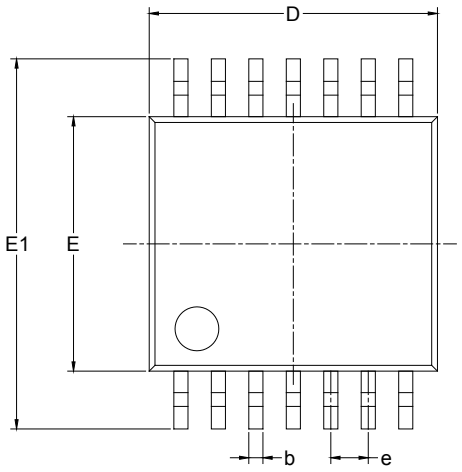
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

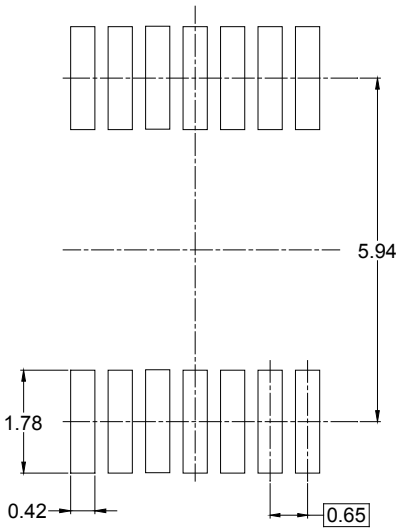
Changes from Original (DECEMBER 2017) to REV.A

Changed from product preview to production data ..... All

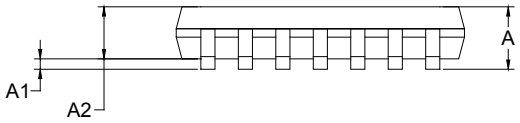
PACKAGE OUTLINE DIMENSIONS

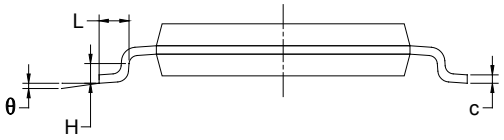
TSSOP-14





RECOMMENDED LAND PATTERN (Unit: mm)

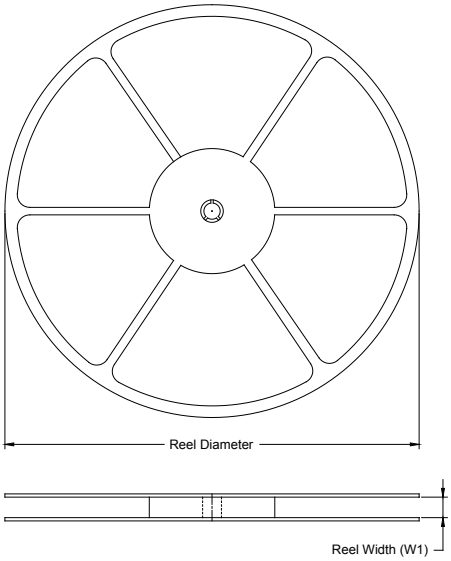




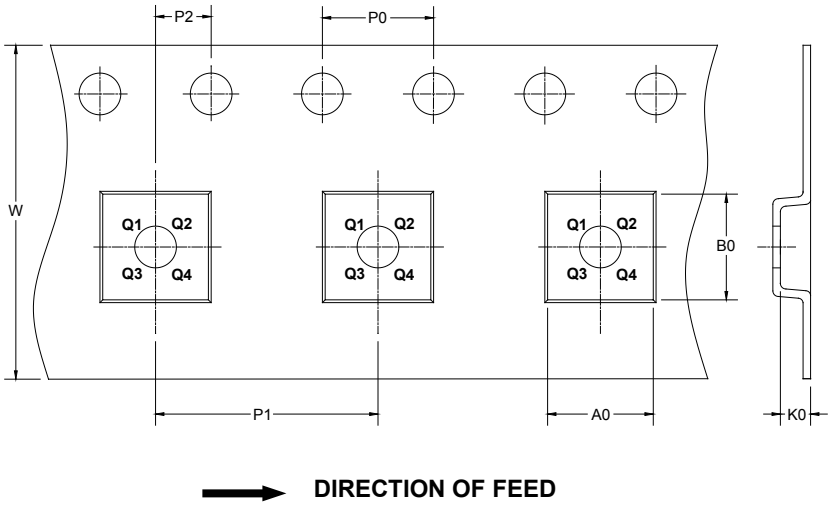
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.860	5.100	0.191	0.201
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.02	0.028
H	0.25 TYP		0.01 TYP	
θ	1°	7°	1°	7°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



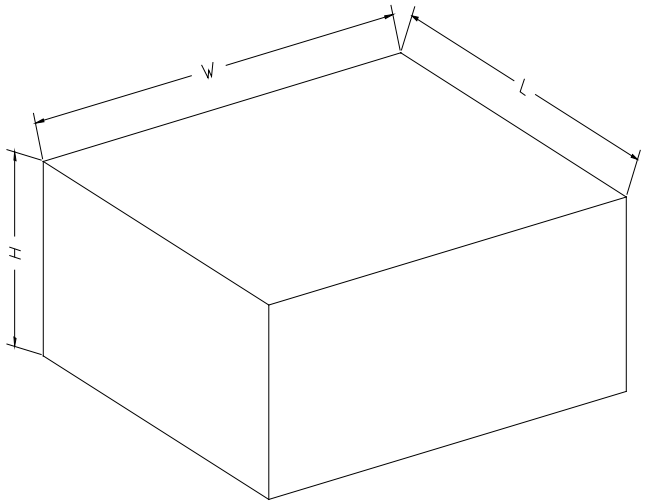
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-14	13″	12.4	6.95	5.60	1.20	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002