

MC14051B, MC14052B, MC14053B



ON Semiconductor

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Analog Multiplexers/Demultiplexers

The MC14051B, MC14052B, and MC14053B analog multiplexers are digitally-controlled analog switches. The MC14051B effectively implements an SP8T solid state switch, the MC14052B a DP4T, and the MC14053B a Triple SPDT. All three devices feature low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

- Triple Diode Protection on Control Inputs
- Switch Function is Break Before Make
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Analog Voltage Range ($V_{DD} - V_{EE}$) = 3.0 to 18 V
Note: V_{EE} must be $\leq V_{SS}$
- Linearized Transfer Characteristics
- Low-noise – 12 nV/ $\sqrt{\text{Cycle}}$, $f \geq 1.0$ kHz Typical
- Pin-for-Pin Replacement for CD4051, CD4052, and CD4053
- For 4PDT Switch, See MC14551B
- For Lower R_{ON} , Use the HC4051, HC4052, or HC4053 High-Speed CMOS Devices

MAXIMUM RATINGS (Note 1.)

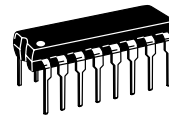
| Symbol | Parameter | Value | Unit |
|-------------------|---|------------------------|--------------------|
| V_{DD} | DC Supply Voltage (Referenced to V_{EE} , $V_{SS} \geq V_{EE}$) | -0.5 to +18.0 | V |
| V_{in}, V_{out} | Input or Output Voltage Range (DC or Transient) (Referenced to V_{SS} for Control Inputs and V_{EE} for Switch I/O) | -0.5 to $V_{DD} + 0.5$ | V |
| I_{in} | Input Current (DC or Transient) per Control Pin | ± 10 | mA |
| I_{SW} | Switch Through Current | ± 25 | mA |
| P_D | Power Dissipation, per Package (Note 2.) | 500 | mW |
| T_A | Ambient Temperature Range | -55 to +125 | $^{\circ}\text{C}$ |
| T_{stg} | Storage Temperature Range | -65 to +150 | $^{\circ}\text{C}$ |
| T_L | Lead Temperature (8-Second Soldering) | 260 | $^{\circ}\text{C}$ |

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}\text{C}$ From 65 $^{\circ}\text{C}$ To 125 $^{\circ}\text{C}$

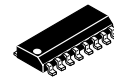
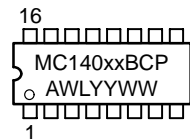
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} , V_{EE} or V_{DD}). Unused outputs must be left open.

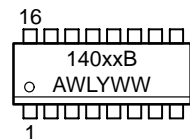
MARKING DIAGRAMS



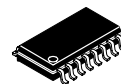
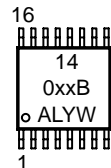
PDIP-16
P SUFFIX
CASE 648



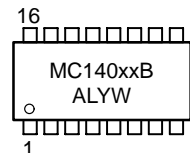
SOIC-16
D SUFFIX
CASE 751B



TSSOP-16
DT SUFFIX
CASE 948F



SOEIAJ-16
F SUFFIX
CASE 966



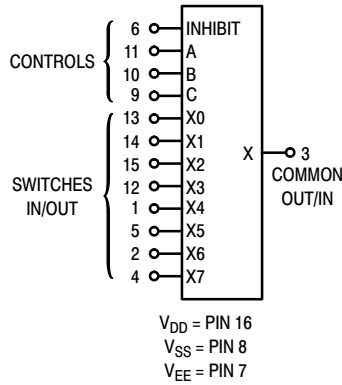
xx = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

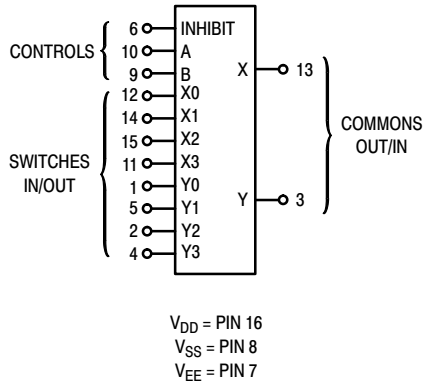
See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

MC14051B, MC14052B, MC14053B

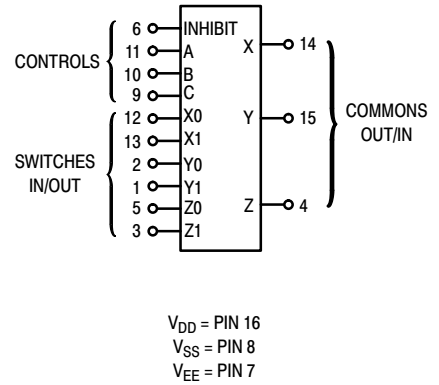
MC14051B
8-Channel Analog
Multiplexer/Demultiplexer



MC14052B
Dual 4-Channel Analog
Multiplexer/Demultiplexer

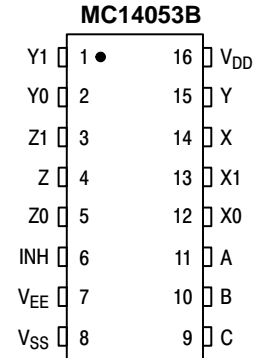
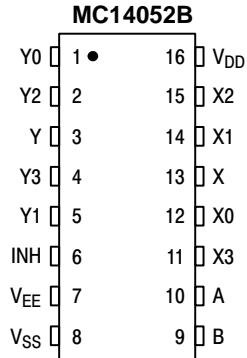
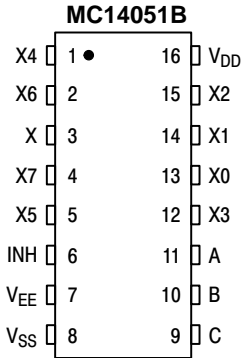


MC14053B
Triple 2-Channel Analog
Multiplexer/Demultiplexer



Note: Control Inputs referenced to V_{SS} , Analog Inputs and Outputs reference to V_{EE} . V_{EE} must be $\leq V_{SS}$.

PIN ASSIGNMENT



MC14051B, MC14052B, MC14053B

ELECTRICAL CHARACTERISTICS

| Characteristic | Symbol | V _{DD} | Test Conditions | -55°C | | 25°C | | | 125°C | | Unit |
|----------------|--------|-----------------|-----------------|-------|-----|------|----------|-----|-------|-----|------|
| | | | | Min | Max | Min | Typ (3.) | Max | Min | Max | |

SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})

| | | | | | | | | | | | |
|--|--------------------|-----------------|--|---|-----|-----|-------|-----|-----|-----|----|
| Power Supply Voltage Range | V _{DD} | — | V _{DD} - 3.0 ≥ V _{SS} ≥ V _{EE} | 3.0 | 18 | 3.0 | — | 18 | 3.0 | 18 | V |
| Quiescent Current Per Package | I _{DD} | 5.0 | Control Inputs: V _{in} = V _{SS} or V _{DD} , Switch I/O: V _{EE} ≤ V _{I/O} ≤ V _{DD} , and ΔV _{switch} ≤ 500 mV (4.) | — | 5.0 | — | 0.005 | 5.0 | — | 150 | μA |
| | | 10 | | — | 10 | — | 0.010 | 10 | — | 300 | |
| | | 15 | | — | 20 | — | 0.015 | 20 | — | 600 | |
| Total Supply Current (Dynamic Plus Quiescent, Per Package) | I _{D(AV)} | 5.0 10 15 | T _A = 25°C only (The channel component, (V _{in} - V _{out})/R _{on} , is not included.) | Typical (0.07 μA/kHz) f + I _{DD} (0.20 μA/kHz) f + I _{DD} (0.36 μA/kHz) f + I _{DD} | | | | | | μA | |

CONTROL INPUTS — INHIBIT, A, B, C (Voltages Referenced to V_{SS})

| | | | | | | | | | | | |
|--------------------------|-----------------|-----|--|-----|------|-----|----------|------|-----|-----|----|
| Low-Level Input Voltage | V _{IL} | 5.0 | R _{on} = per spec, I _{off} = per spec | — | 1.5 | — | 2.25 | 1.5 | — | 1.5 | V |
| | | 10 | | — | 3.0 | — | 4.50 | 3.0 | — | 3.0 | |
| | | 15 | | — | 4.0 | — | 6.75 | 4.0 | — | 4.0 | |
| High-Level Input Voltage | V _{IH} | 5.0 | R _{on} = per spec, I _{off} = per spec | 3.5 | — | 3.5 | 2.75 | — | 3.5 | — | V |
| | | 10 | | 7.0 | — | 7.0 | 5.50 | — | 7.0 | — | |
| | | 15 | | 11 | — | 11 | 8.25 | — | 11 | — | |
| Input Leakage Current | I _{in} | 15 | V _{in} = 0 or V _{DD} | — | ±0.1 | — | ±0.00001 | ±0.1 | — | 1.0 | μA |
| Input Capacitance | C _{in} | — | | — | — | — | 5.0 | 7.5 | — | — | pF |

SWITCHES IN/OUT AND COMMONS OUT/IN — X, Y, Z (Voltages Referenced to V_{EE})

| | | | | | | | | | | | |
|---|----------------------|-----|---|---|-----------------|---|-------|-----------------|---|-----------------|-----------------|
| Recommended Peak-to-Peak Voltage Into or Out of the Switch | V _{I/O} | — | Channel On or Off | 0 | V _{DD} | 0 | — | V _{DD} | 0 | V _{DD} | V _{PP} |
| Recommended Static or Dynamic Voltage Across the Switch (4.) (Figure 5) | ΔV _{switch} | — | Channel On | 0 | 600 | 0 | — | 600 | 0 | 300 | mV |
| Output Offset Voltage | V _{OO} | — | V _{in} = 0 V, No Load | — | — | — | 10 | — | — | — | μV |
| ON Resistance | R _{on} | 5.0 | ΔV _{switch} ≤ 500 mV (4.) V _{in} = V _{IL} or V _{IH} (Control), and V _{in} = 0 to V _{DD} (Switch) | — | 800 | — | 250 | 1050 | — | 1200 | Ω |
| | | 10 | | — | 400 | — | 120 | 500 | — | 520 | |
| | | 15 | | — | 220 | — | 80 | 280 | — | 300 | |
| ΔON Resistance Between Any Two Channels in the Same Package | ΔR _{on} | 5.0 | | — | 70 | — | 25 | 70 | — | 135 | Ω |
| | | 10 | | — | 50 | — | 10 | 50 | — | 95 | |
| | | 15 | | — | 45 | — | 10 | 45 | — | 65 | |
| Off-Channel Leakage Current (Figure 10) | I _{off} | 15 | V _{in} = V _{IL} or V _{IH} (Control) Channel to Channel or Any One Channel | — | ±100 | — | ±0.05 | ±100 | — | ±1000 | nA |
| Capacitance, Switch I/O | C _{I/O} | — | Inhibit = V _{DD} | — | — | — | 10 | — | — | — | pF |
| Capacitance, Common O/I | C _{O/I} | — | Inhibit = V _{DD} (MC14051B) (MC14052B) (MC14053B) | — | — | — | 60 | — | — | — | pF |
| | | | | — | — | — | 32 | — | — | | |
| | | | | — | — | — | 17 | — | — | | |
| Capacitance, Feedthrough (Channel Off) | C _{I/O} | — | Pins Not Adjacent Pins Adjacent | — | — | — | 0.15 | — | — | — | pF |
| | | | | — | — | — | 0.47 | — | — | — | |

3. Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

4. For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn, i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

MC14051B, MC14052B, MC14053B

ELECTRICAL CHARACTERISTICS ⁽⁵⁾ ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$) ($V_{EE} \leq V_{SS}$ unless otherwise indicated)

| Characteristic | Symbol | $V_{DD} - V_{EE}$ Vdc | Typ ⁽⁶⁾ All Types | Max | Unit | | | |
|---|--------------------|---|---|-----|------|-----|-----|----|
| Propagation Delay Times (Figure 6) Switch Input to Switch Output ($R_L = 10 \text{ k}\Omega$) MC14051 $t_{PLH}, t_{PHL} = (0.17 \text{ ns/pF}) C_L + 26.5 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.08 \text{ ns/pF}) C_L + 11 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.06 \text{ ns/pF}) C_L + 9.0 \text{ ns}$ MC14052 $t_{PLH}, t_{PHL} = (0.17 \text{ ns/pF}) C_L + 21.5 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.08 \text{ ns/pF}) C_L + 8.0 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.06 \text{ ns/pF}) C_L + 7.0 \text{ ns}$ MC14053 $t_{PLH}, t_{PHL} = (0.17 \text{ ns/pF}) C_L + 16.5 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.08 \text{ ns/pF}) C_L + 4.0 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.06 \text{ ns/pF}) C_L + 3.0 \text{ ns}$ | t_{PLH}, t_{PHL} | 5.0 | 35 | 90 | ns | | | |
| | | 10 | 15 | 40 | | | | |
| | | 15 | 12 | 30 | | | | |
| | | 5.0 | 30 | 75 | | ns | | |
| | | 10 | 12 | 30 | | | | |
| | | 15 | 10 | 25 | | | | |
| | | 5.0 | 25 | 65 | | ns | | |
| | | 10 | 8.0 | 20 | | | | |
| | | 15 | 6.0 | 15 | | | | |
| | | Inhibit to Output ($R_L = 10 \text{ k}\Omega$, $V_{EE} = V_{SS}$) Output "1" or "0" to High Impedance, or High Impedance to "1" or "0" Level MC14051B | $t_{PHZ}, t_{PLZ},$ t_{PZH}, t_{PZL} | 5.0 | | 350 | 700 | ns |
| | | | | 10 | | 170 | 340 | |
| | | | | 15 | | 140 | 280 | |
| MC14052B | 5.0 | | | 300 | 600 | ns | | |
| 10 | 155 | | | 310 | | | | |
| 15 | 125 | | | 250 | | | | |
| MC14053B | 5.0 | | | 275 | 550 | ns | | |
| 10 | 140 | | | 280 | | | | |
| 15 | 110 | | | 220 | | | | |
| Control Input to Output ($R_L = 10 \text{ k}\Omega$, $V_{EE} = V_{SS}$) MC14051B | t_{PLH}, t_{PHL} | 5.0 | 360 | 720 | ns | | | |
| | | 10 | 160 | 320 | | | | |
| | | 15 | 120 | 240 | | | | |
| | | MC14052B | 5.0 | 325 | 650 | ns | | |
| | | 10 | 130 | 260 | | | | |
| | | 15 | 90 | 180 | | | | |
| | | MC14053B | 5.0 | 300 | 600 | ns | | |
| | | 10 | 120 | 240 | | | | |
| | | 15 | 80 | 160 | | | | |
| Second Harmonic Distortion ($R_L = 10 \text{ k}\Omega$, $f = 1 \text{ kHz}$) $V_{in} = 5 V_{PP}$ | — | 10 | 0.07 | — | % | | | |
| Bandwidth (Figure 7) ($R_L = 1 \text{ k}\Omega$, $V_{in} = 1/2 (V_{DD} - V_{EE})$ p-p, $C_L = 50 \text{ pF}$ $20 \text{ Log} (V_{out}/V_{in}) = -3 \text{ dB}$) | BW | 10 | 17 | — | MHz | | | |
| Off Channel Feedthrough Attenuation (Figure 7) $R_L = 1 \text{ k}\Omega$, $V_{in} = 1/2 (V_{DD} - V_{EE})$ p-p $f_{in} = 4.5 \text{ MHz}$ — MC14051B $f_{in} = 30 \text{ MHz}$ — MC14052B $f_{in} = 55 \text{ MHz}$ — MC14053B | — | 10 | -50 | — | dB | | | |
| Channel Separation (Figure 8) ($R_L = 1 \text{ k}\Omega$, $V_{in} = 1/2 (V_{DD} - V_{EE})$ p-p, $f_{in} = 3.0 \text{ MHz}$) | — | 10 | -50 | — | dB | | | |
| Crosstalk, Control Input to Common O/I (Figure 9) ($R_1 = 1 \text{ k}\Omega$, $R_L = 10 \text{ k}\Omega$ Control $t_{TLH} = t_{THL} = 20 \text{ ns}$, Inhibit = V_{SS}) | — | 10 | 75 | — | mV | | | |

5. The formulas given are for the typical characteristics only at 25°C .

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MC14051B, MC14052B, MC14053B

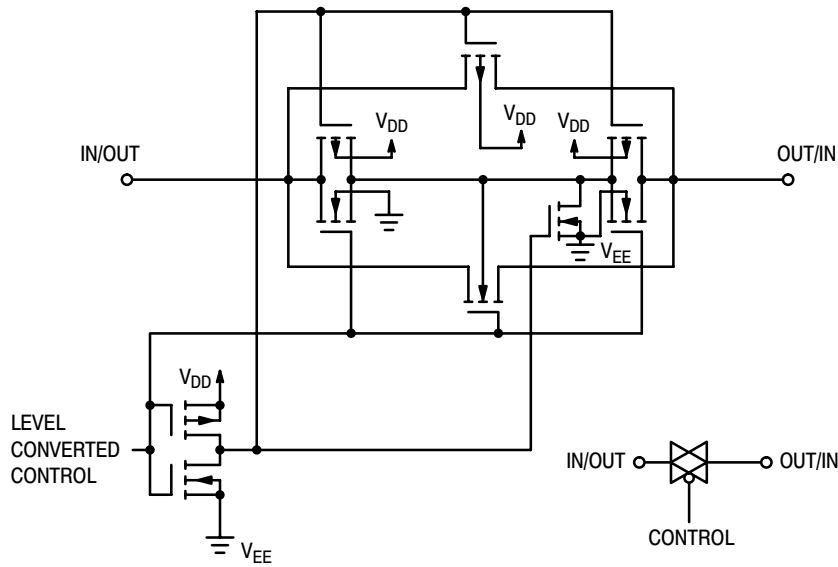


Figure 1. Switch Circuit Schematic

TRUTH TABLE

| Control Inputs | | | ON Switches | | |
|----------------|--------|-----|-------------|----------|----------|
| Inhibit | Select | | MC14051B | MC14052B | MC14053B |
| | C* | B A | | | |
| 0 | 0 | 0 0 | X0 | Y0 X0 | Z0 Y0 X0 |
| 0 | 0 | 0 1 | X1 | Y1 X1 | Z0 Y0 X1 |
| 0 | 0 | 1 0 | X2 | Y2 X2 | Z0 Y1 X0 |
| 0 | 0 | 1 1 | X3 | Y3 X3 | Z0 Y1 X1 |
| 0 | 1 | 0 0 | X4 | | Z1 Y0 X0 |
| 0 | 1 | 0 1 | X5 | | Z1 Y0 X1 |
| 0 | 1 | 1 0 | X6 | | Z1 Y1 X0 |
| 0 | 1 | 1 1 | X7 | | Z1 Y1 X1 |
| 1 | x | x x | None | None | None |

*Not applicable for MC14052

x = Don't Care

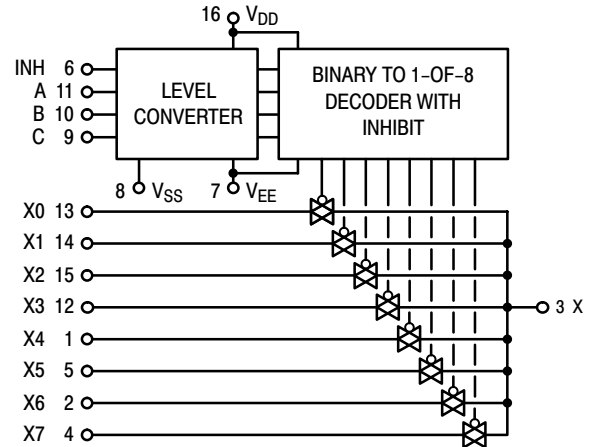


Figure 2. MC14051B Functional Diagram

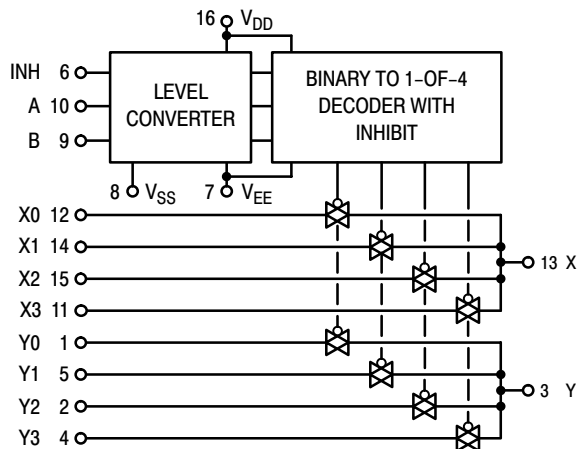


Figure 3. MC14052B Functional Diagram

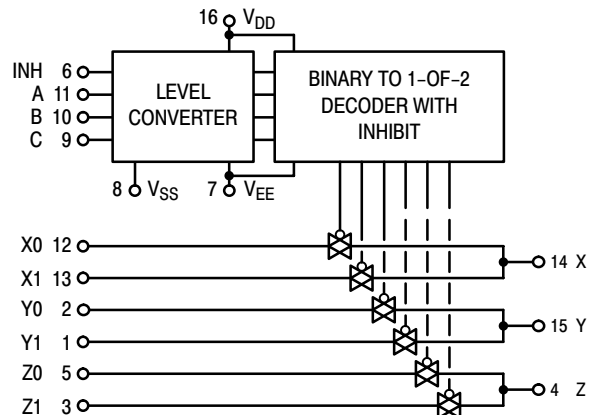


Figure 4. MC14053B Functional Diagram

TEST CIRCUITS

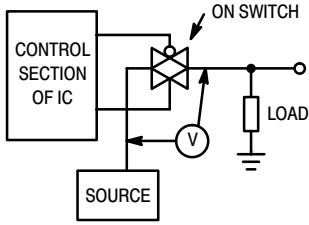


Figure 5. ΔV Across Switch

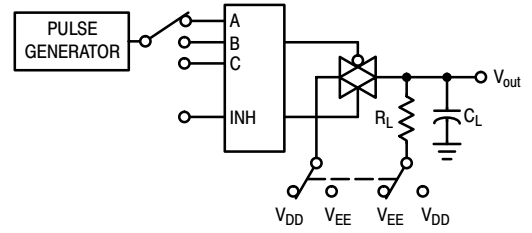


Figure 6. Propagation Delay Times, Control and Inhibit to Output

A, B, and C inputs used to turn ON or OFF the switch under test.

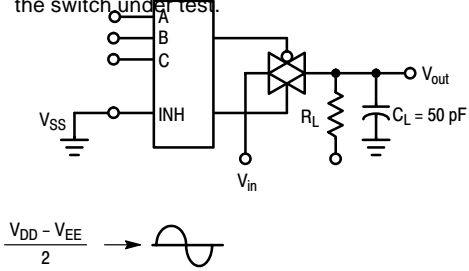


Figure 7. Bandwidth and Off-Channel Feedthrough Attenuation

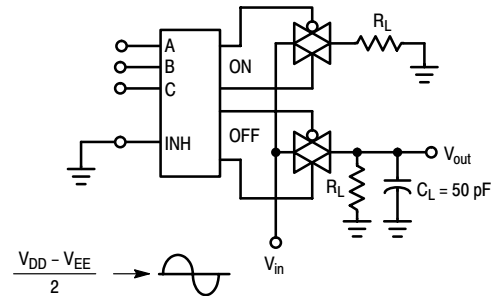


Figure 8. Channel Separation (Adjacent Channels Used For Setup)

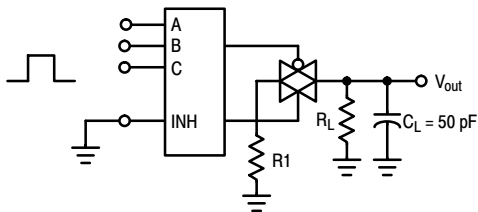


Figure 9. Crosstalk, Control Input to Common O/I

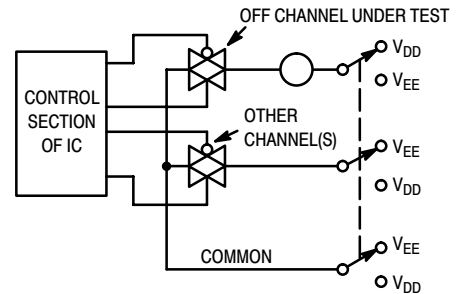


Figure 10. Off Channel Leakage

NOTE: See also Figures 7 and 8 in the MC14016B data sheet.

MC14051B, MC14052B, MC14053B

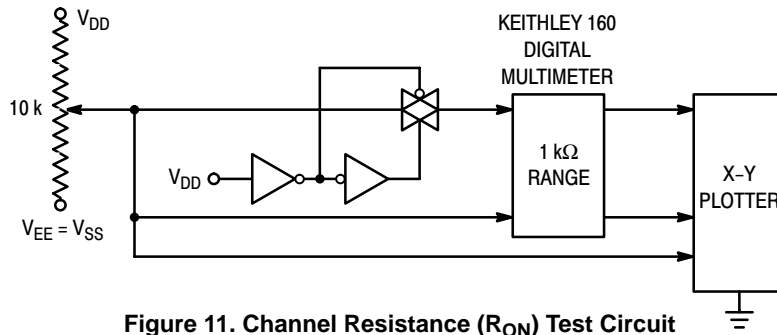


Figure 11. Channel Resistance (R_{ON}) Test Circuit

TYPICAL RESISTANCE CHARACTERISTICS

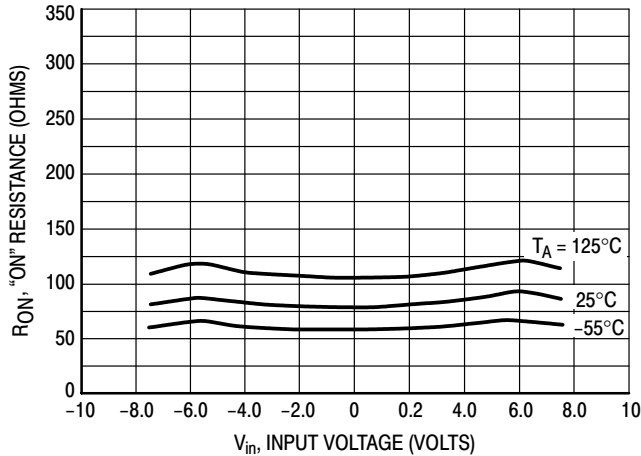


Figure 12. $V_{DD} = 7.5\text{ V}$, $V_{EE} = -7.5\text{ V}$

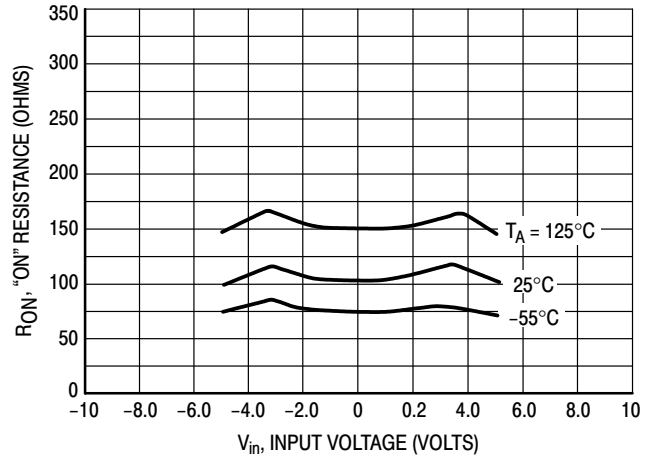


Figure 13. $V_{DD} = 5.0\text{ V}$, $V_{EE} = -5.0\text{ V}$

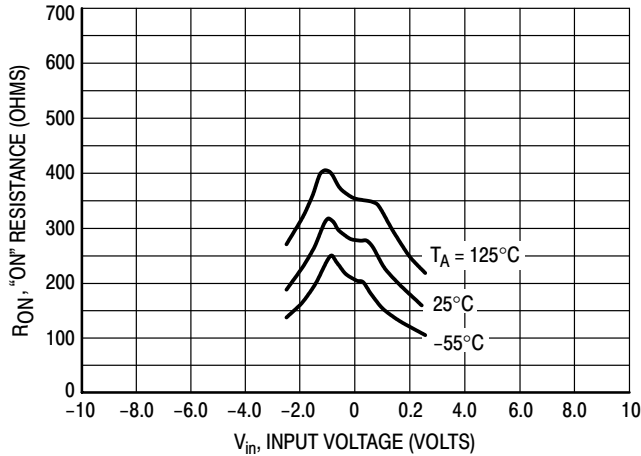


Figure 14. $V_{DD} = 2.5\text{ V}$, $V_{EE} = -2.5\text{ V}$

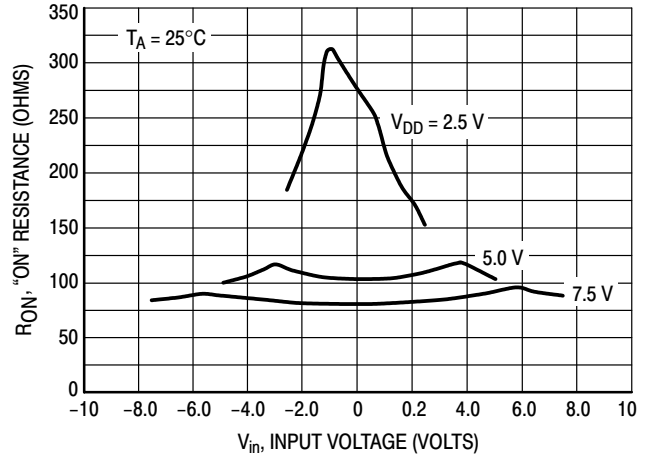


Figure 15. Comparison at 25°C , $V_{DD} = -V_{EE}$

APPLICATIONS INFORMATION

Figure A illustrates use of the on-chip level converter detailed in Figures 2, 3, and 4. The 0-to-5 V Digital Control signal is used to directly control a 9 V_{p-p} analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, V_{DD} = +5 V = logic high at the control inputs; V_{SS} = GND = 0 V = logic low.

The maximum analog signal level is determined by V_{DD} and V_{EE}. The V_{DD} voltage determines the maximum recommended peak above V_{SS}. The V_{EE} voltage determines the maximum swing below V_{SS}. For the example, V_{DD} - V_{SS} = 5 V maximum swing above V_{SS}; V_{SS} - V_{EE} = 5 V maximum swing below V_{SS}. The example shows a ±4.5 V signal which allows a 1/2 volt margin at each

peak. If voltage transients above V_{DD} and/or below V_{EE} are anticipated on the analog channels, external diodes (D_x) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{EE} is 18.0 V. Most parameters are specified up to 15 V which is the *recommended* maximum difference between V_{DD} and V_{EE}.

Balanced supplies are not required. However, V_{SS} must be greater than or equal to V_{EE}. For example, V_{DD} = +10 V, V_{SS} = +5 V, and V_{EE} = -3 V is acceptable. See the Table below.

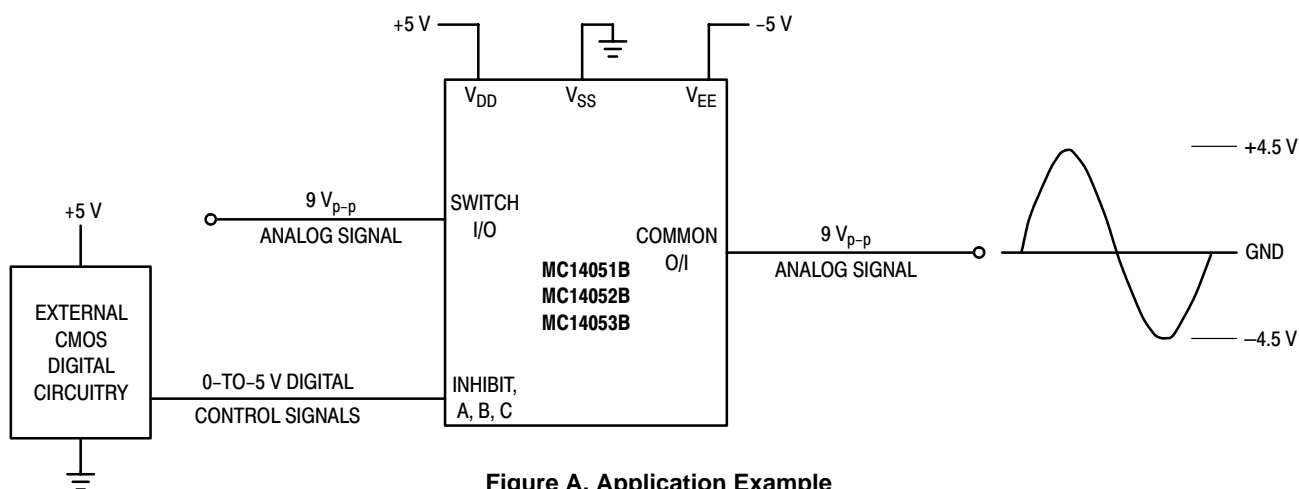


Figure A. Application Example

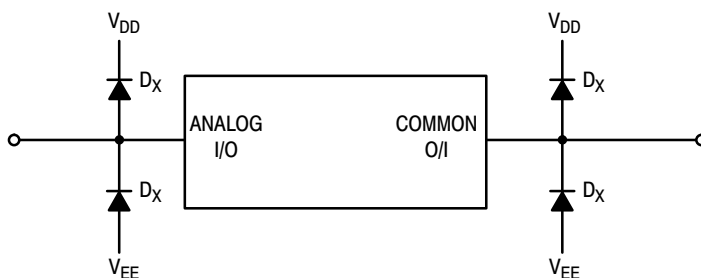


Figure B. External Germanium or Schottky Clipping Diodes

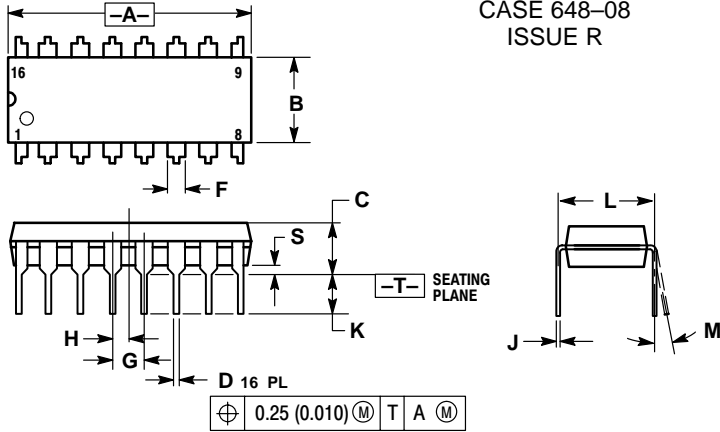
POSSIBLE SUPPLY CONNECTIONS

| V _{DD} In Volts | V _{SS} In Volts | V _{EE} In Volts | Control Inputs Logic High/Logic Low In Volts | Maximum Analog Signal Range In Volts |
|-----------------------------|-----------------------------|-----------------------------|--|---|
| + 8 | 0 | - 8 | + 8/0 | + 8 to - 8 = 16 V _{p-p} |
| + 5 | 0 | - 12 | + 5/0 | + 5 to - 12 = 17 V _{p-p} |
| + 5 | 0 | 0 | + 5/0 | + 5 to 0 = 5 V _{p-p} |
| + 5 | 0 | - 5 | + 5/0 | + 5 to - 5 = 10 V _{p-p} |
| + 10 | + 5 | - 5 | + 10/+ 5 | + 10 to - 5 = 15 V _{p-p} |

MC14051B, MC14052B, MC14053B

PACKAGE DIMENSIONS

PDIP-16 P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R

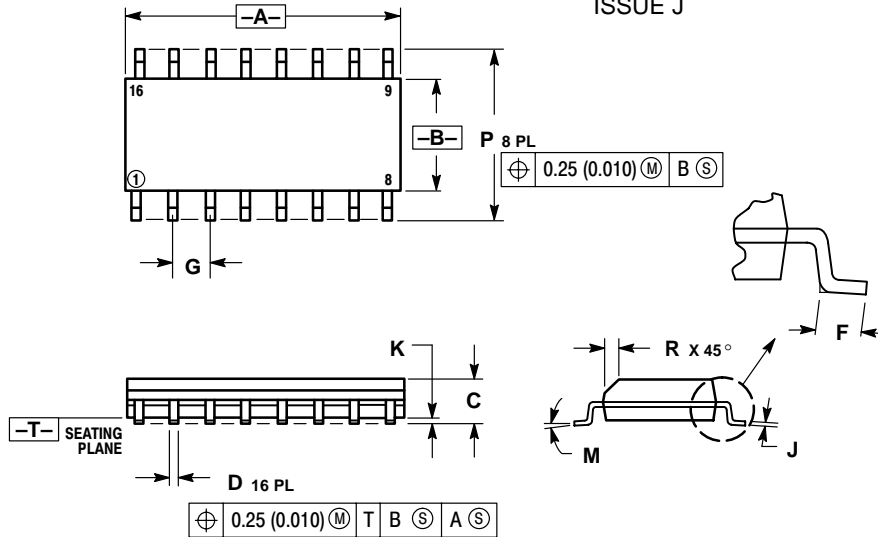


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0° | 10° | 0° | 10° |
| S | 0.020 | 0.040 | 0.51 | 1.01 |

SOIC-16 D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



NOTES:

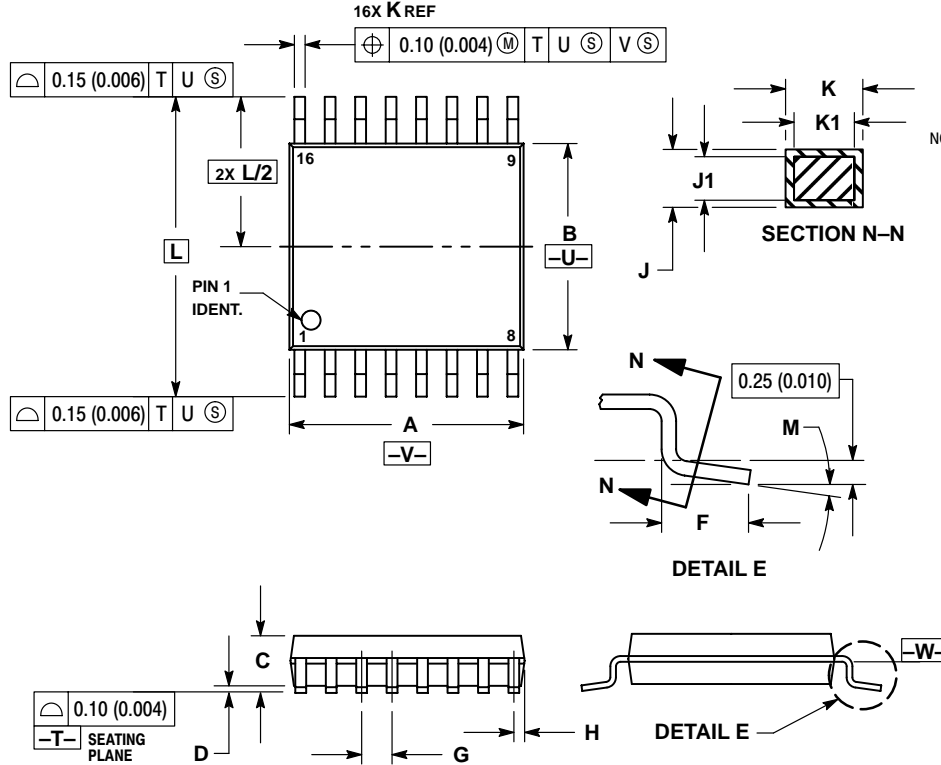
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

MC14051B, MC14052B, MC14053B

PACKAGE DIMENSIONS

TSSOP-16
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948F-01
ISSUE O



NOTES:

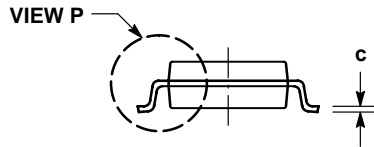
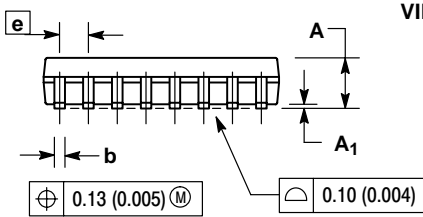
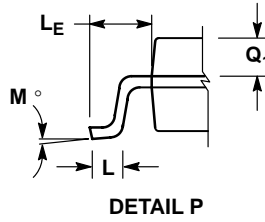
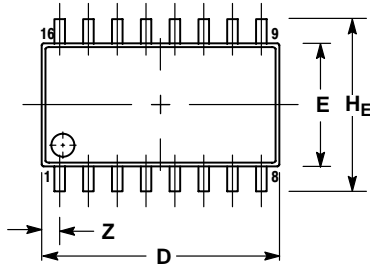
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

MC14051B, MC14052B, MC14053B

PACKAGE DIMENSIONS

SOEIAJ-16 F SUFFIX PLASTIC EIAJ SOIC PACKAGE CASE 966-01 ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM | MILLIMETERS | | INCHES | |
|----------------|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| A ₁ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.18 | 0.27 | 0.007 | 0.011 |
| D | 9.90 | 10.50 | 0.390 | 0.413 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| H _E | 7.40 | 8.20 | 0.291 | 0.323 |
| L | 0.50 | 0.85 | 0.020 | 0.033 |
| L _E | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0° | 10° | 0° | 10° |
| Q ₁ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 0.78 | --- | 0.031 |

MC14051B, MC14052B, MC14053B


ORDERING & SHIPPING INFORMATION:

| Device | Package | Shipping |
|--------------|-----------|--------------------------|
| MC14051BCP | PDIP-16 | 2000 Units per Box |
| MC14051BD | SOIC-16 | 48 Units per Rail |
| MC14051BDR2 | SOIC-16 | 2500 Units / Tape & Reel |
| MC14051BDT | TSSOP-16 | 96 Units per Rail |
| MC14051BDTEL | TSSOP-16 | 2000 Units / Tape & Reel |
| MC14051BDTR2 | TSSOP-16 | 2500 Units / Tape & Reel |
| MC14051BF | SOEIAJ-16 | See Note 7. |
| MC14051BFEL | SOEIAJ-16 | See Note 7. |
| | | |
| MC14052BCP | PDIP-16 | 2000 Units per Box |
| MC14052BD | SOIC-16 | 48 Units per Rail |
| MC14052BDR2 | SOIC-16 | 2500 Units / Tape & Reel |
| MC14052BDT | TSSOP-16 | 96 Units per Rail |
| MC14052BDTR2 | TSSOP-16 | 2500 Units / Tape & Reel |
| MC14052BF | SOEIAJ-16 | See Note 7. |
| MC14052BFEL | SOEIAJ-16 | See Note 7. |

ORDERING & SHIPPING INFORMATION:

| | | |
|--------------|-----------|--------------------------|
| MC14053BCP | PDIP-16 | 2000 Units per Box |
| MC14053BD | SOIC-16 | 48 Units per Rail |
| MC14053BDR2 | SOIC-16 | 2500 Units / Tape & Reel |
| MC14053BDT | TSSOP-16 | 96 Units per Rail |
| MC14053BDTEL | TSSOP-16 | 2000 Units / Tape & Reel |
| MC14053BDTR2 | TSSOP-16 | 2500 Units / Tape & Reel |
| MC14053BF | SOEIAJ-16 | See Note 7. |
| MC14053BFEL | SOEIAJ-16 | See Note 7. |

7. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

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