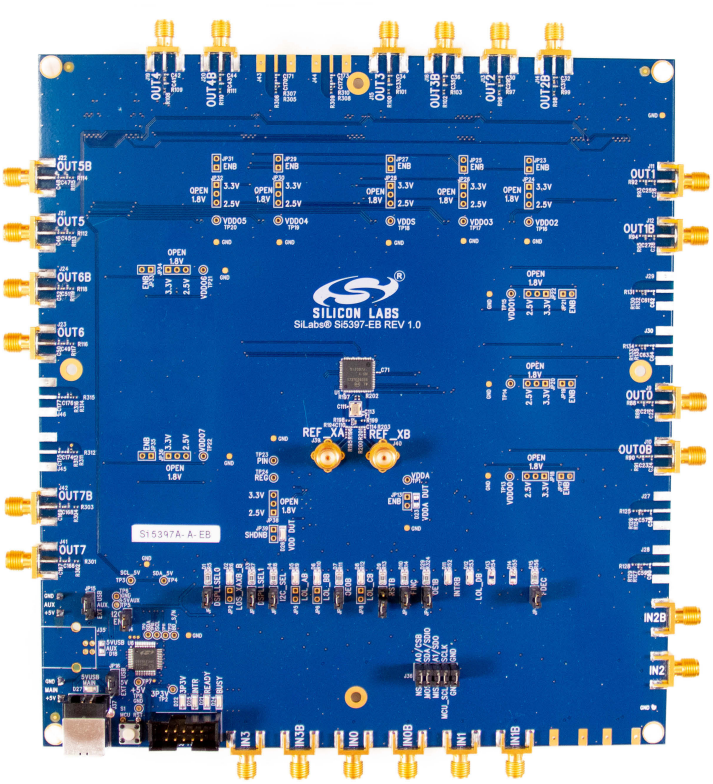
UG353: Si5397 Evaluation Board User's Guide

The Si5397-EVB is used for evaluating the Si5397 Any-Frequency, Any-Output, Jitter-Attenuating Clock Any-Frequency, Any-Output, Jitter-Attenuating Clock Multiplier Revision A. The device grade and revision is distinguished by a white 1 inch x 0.187 inch label installed in the lower left hand corner of the board. In the example below, the label "SI5397A-A-EB" indicates the evaluation board has been assembled with an Si5397 device, Grade A,Revision A, installed. (For ordering purposes only, the terms “EB” and “EVB” refer to the board and the kit, respectively. For the purpose of this document, the terms are synonymous in context.)



KEY FEATURES

- Powered from USB port or external +5 V power supply via screw terminals
- Onboard 48 MHz XTAL allows standalone or holdover mode of operation on the Si5397
- ClockBuilder Pro® (CBPro) GUI programmable VDD supply allows device supply voltages of 3.3, 2.5, or 1.8 V
- CBPro GUI programmable VDDO supplies allow each of the eight outputs to have its own supply voltage selectable from 3.3, 2.5, or 1.8 V
- CBPro GUI allows control and measurement of voltage, current, and power of VDD and all eight VDDO supplies
- Status LEDs for power supplies and control/status signals of the Si5397
- SMA connectors for input clocks, output clocks and optional external timing reference clock

1. Functional Block Diagram

Below is a functional block diagram of the Si5397-A-EB. This evaluation board can be connected to a PC via the main USB connector for programming, control, and monitoring. See 3. Quick Start or 10.3 Overview of ClockBuilder Pro Applications for more information.

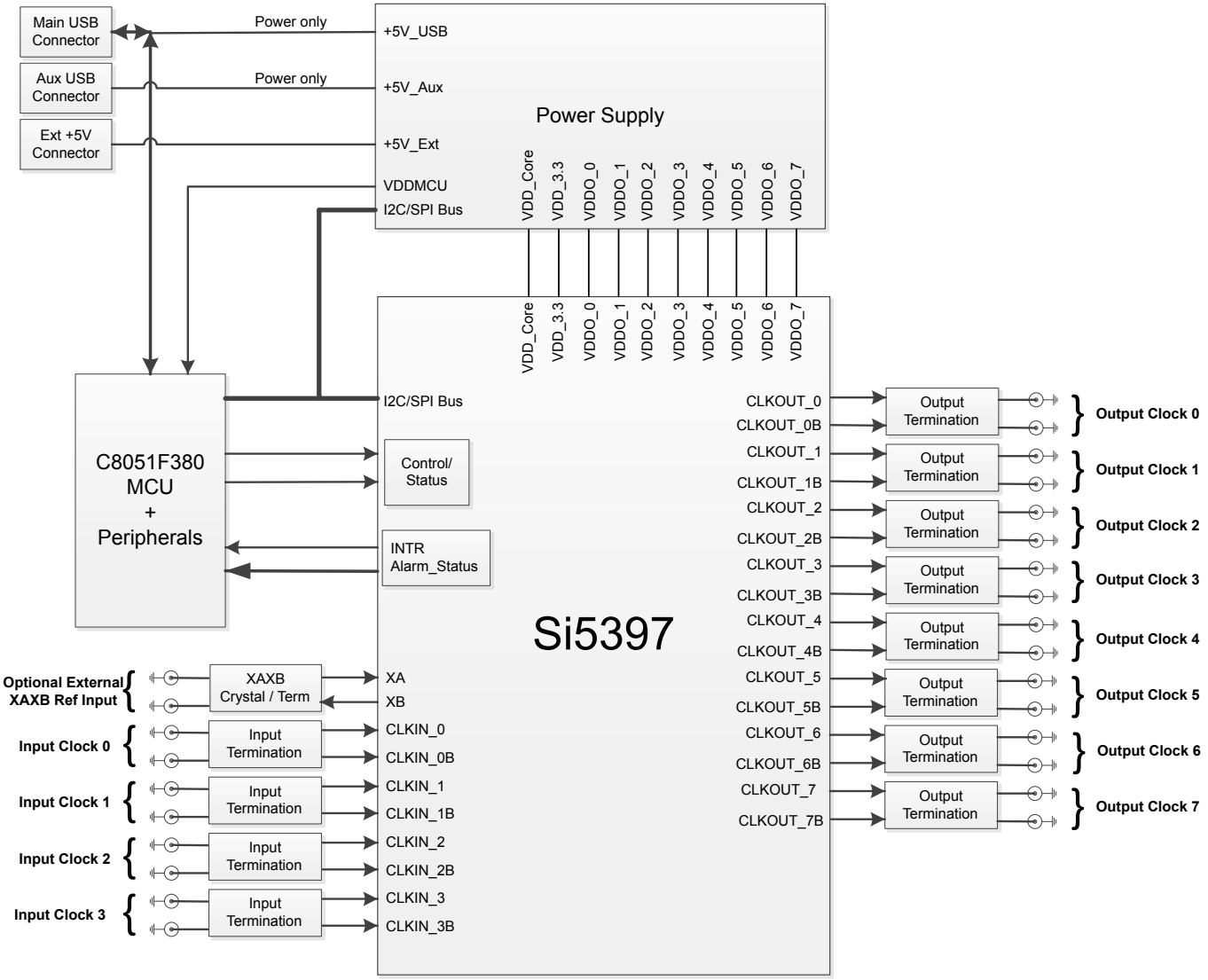


Figure 1.1. Si5397-A-EB Functional Block Diagram

2. Si5397-A-EVB Support Documentation and ClockBuilder Pro Software

All Si5397-A-EVB schematics, BOMs, User's Guides, and software can be found online at: http://www.silabs.com/products/clocksoscillators/pages/si539x-evb.aspx.

3. Quick Start

1. Install the ClockBuilder Pro desktop software from http://www.silabs.com/CBPro.
2. Connect a USB cable from the Si5397-A-EB to the PC where the software was installed.
3. Confirm jumpers are installed as shown in Table 4.1 Si5397-EB Jumper Defaults[1] on page 5.
4. Launch the ClockBuilder Pro Software.
5. You can use ClockBuilder Pro to create, download, and run a frequency plan on the Si5397-A-EB.
6. For the Si5397 data sheet, go to http://www.silabs.com/timing.

4. Jumper Defaults

Table 4.1. Si5397-EB Jumper Defaults[1]

Location	Type	I= Installed 0 = Open	Location	Type	I = Installed 0 = Open
JP1	2-pin	I	JP23	2-pin	O
JP2	2-pin	O	JP24	2-pin	O
JP3	2-pin	I	JP25	2-pin	O
JP4	2-pin	I	JP26	2-pin	O
JP5	2-pin	O	JP27	2-pin	O
JP6	2-pin	O	JP28	2-pin	O
JP7	2-pin	I	JP29	2-pin	O
JP8	2-pin	O	JP30	2-pin	O
JP9	2-pin	O	JP31	2-pin	O
JP10	2-pin	I	JP32	2-pin	O
JP13	2-pin	O	JP33	2-pin	O
JP14	2-pin	I	JP34	2-pin	O
JP15	3-pin	all open	JP35	2-pin	O
JP16	3-pin	1 to 2	JP36	2-pin	O
JP17	2-pin	O	JP38	3-pin	All Open
JP18	2-pin	O	JP39	2-pin	O
JP19	2-pin	O	JP40	2-pin	I
JP20	2-pin	O	JP41	2-pin	I
JP21	2-pin	O	J36	5 x 2 Hdr	All 5 installed
JP22	2-pin	O			

Note:

1. Refer to the Si5397-A-EB schematics for the functionality associated with each jumper.

5. Status LEDs

Location	Silkscreen	Color	Status Function Indication
D27	5VUSBMAIN	Blue	Main USB +5 V present
D22	3P3V	Blue	DUT +3.3 V is present
D26	VDD DUT	Blue	DUT VDD voltage present
D25	INTR	Red	MCU INTR (Interrupt) active
D21	READY	Green	MCU Ready
D24	BUSY	Green	MCU Busy
D2	LOS_XAXB_B	Blue	Loss of Signal at XAXB input
D5	LOL_AB	Blue	Lossof Lock - DSPLL A
D6	LOL_BB	Blue	Lossof Lock - DSPLL B
D8	LOL_CB	Blue	Lossof Lock - DSPLL C
D11	INTRB	Blue	Si5397 Interrupt Active
D12	LOL_DB	Blue	Loss of Lock _ DSPLL D

D27, D22, and D26 are illuminated when USB +5 V, Si5397 +3.3 V, and Si5397 Vcore supply voltages, respectively, are present. D25, D21, and D24 are status LEDs showing onboard MCU activity. D2 indicates loss of signal at XAXB input (either crystal osc or external reference). D5, D6, D8, D12 indicate loss of lock for one of four internal DSPLLs (A–D). D11 indicates the Si5397 interrupt output is active (as configured by Si5397 register programming). LED locations are highlighted below with LED function name indicated on board silkscreen.

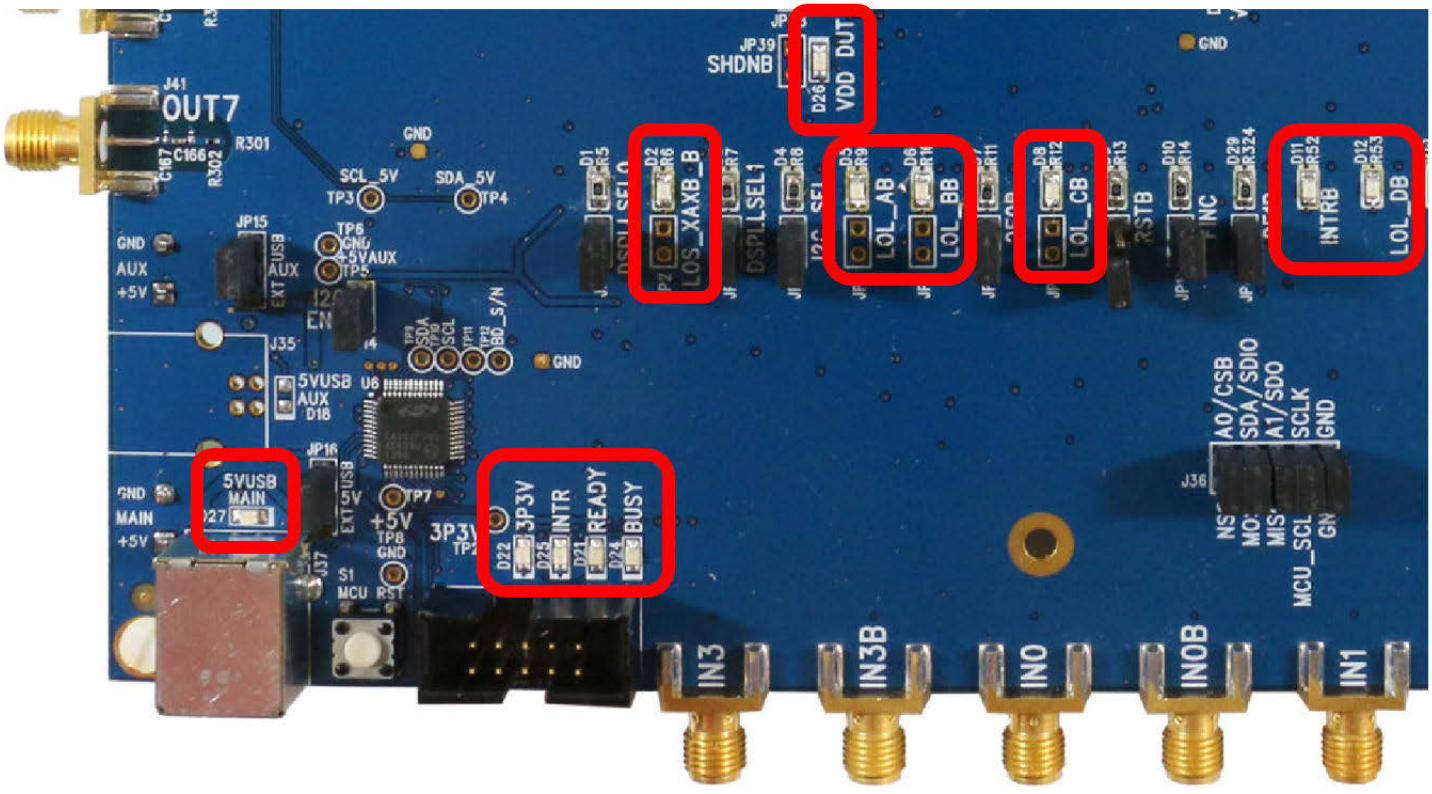


Figure 5.1. Status LEDs

6. External Reference Input (XA/XB)

An external timing reference (48 MHz XTAL) is used in combination with the internal oscillator to produce an ultra-low jitter reference clock for the DSPLL and for providing a stable reference for the free-run and holdover modes.The Si5397-A-EB can also accommodate an external reference clock instead of a crystal.To evaluate the device with an external REFCLK, C111 and C113 must be populated and XTAL Y1 removed (see figure below). The REFCLK can then be applied to SMA connectors J39 and J40.

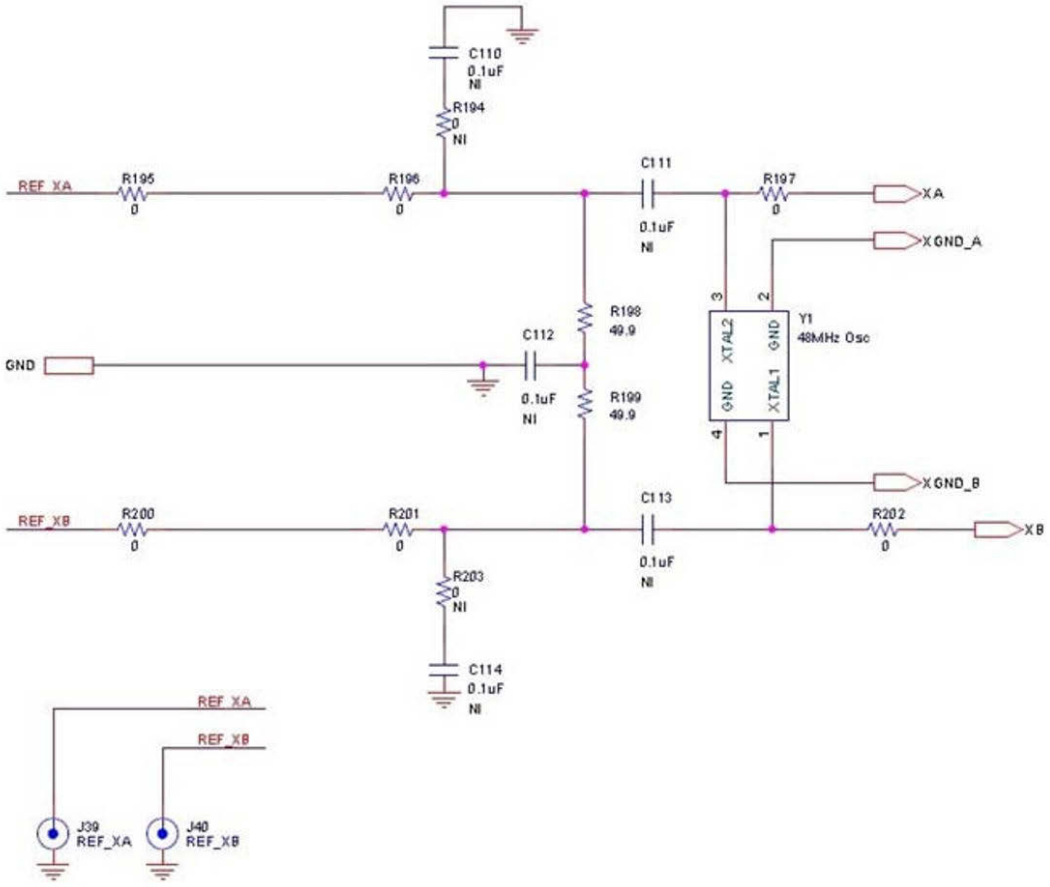


Figure 6.1. External Reference Input Circuit

7. Clock Input Circuits (INx/INxB)

The Si5397-A-EB has eight SMA connectors (IN0, IN0B–IN3, IN3B) for receiving external clock signals. All input clocks are terminated as shown below. Note that input clocks are ac-coupled and 50 Ω terminated. This represents four differential input clock pairs. Single-ended clocks can be used by appropriately driving one side of the differential pair with a single-ended clock. For details on how to configure inputs as single-ended, please refer to the Si5397 data sheet.

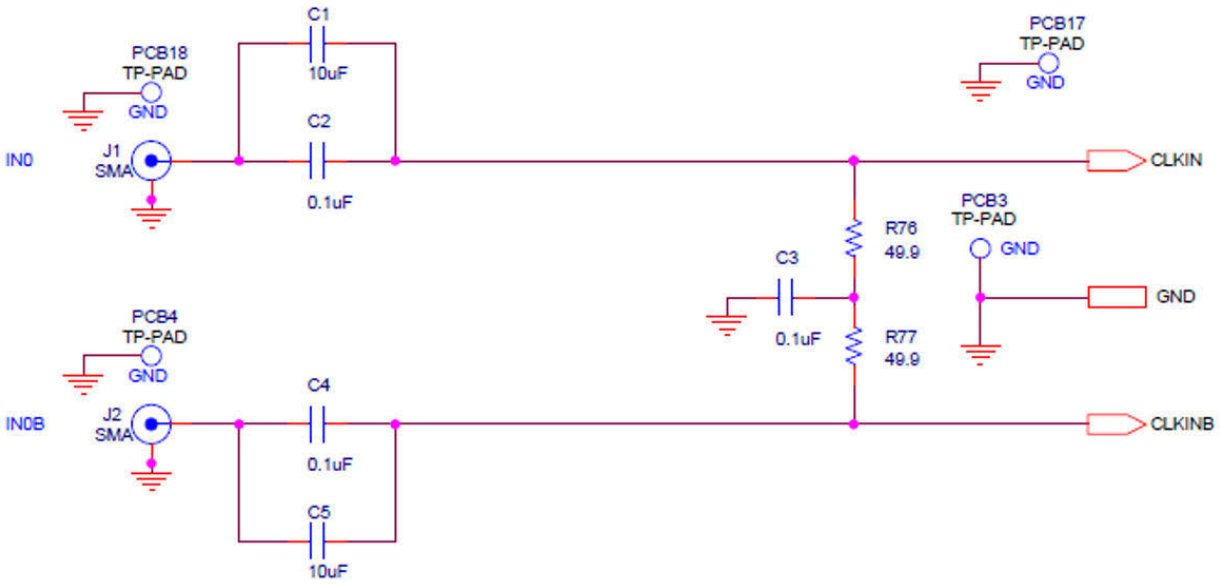


Figure 7.1. Input Clock Termination Circuit

8. Clock Output Circuits (OUTx/OUTxB)

Each of the sixteen output drivers (eight differential pairs, OUT0/OUT0B—OUT7/OUT7B) is ac-coupled to its respective SMA connector. The output clock termination circuit is shown below. The output signal will have no dc bias. If dc coupling is required, the ac coupling capacitors can be replaced with a resistor of appropriate value. The Si5397-A-EB provides pads for optional output termination resistors and/or low-frequency capacitors. Note that components with a schematic “NI” designation are not normally populated on the Si5397-A-EB and provide locations on the PCB for optional dc/ac terminations by the end user.

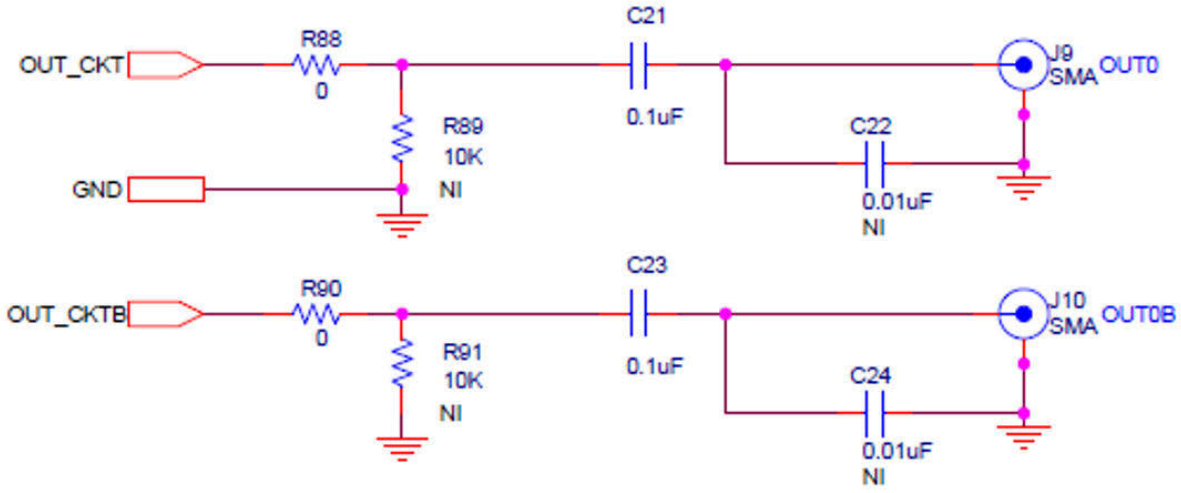


Figure 8.1. Output Clock Termination Circuit

9. Installing ClockBuilder Pro Desktop Software

To install the CBPro software on any **Windows 7** (or above) PC, go to http://www.silabs.com/CBPro and download the ClockBuilder Pro software.

Installation instructions and User's Guide for ClockBuilder Pro can be found at the download link shown above.

10. Using the Si5397-EVB

10.1 Connecting the EVB to Your Host PC

Once ClockBuilderPro software is installed, connect to the EVB with a USB cable as shown in the figure below:

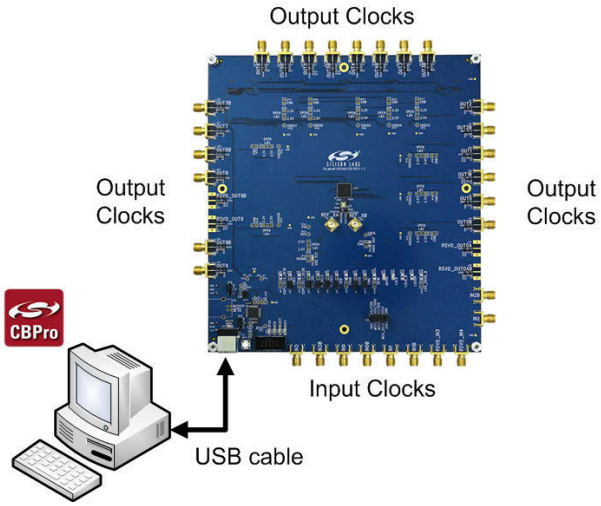


Figure 10.1. EVB Connection Diagram

10.2 Additional Power Supplies

The Si5397-A-EB comes preconfigured with jumpers installed at JP15 and JP16 (pins1–2 in both cases) in order to select “USB”. These jumpers, together with the components installed, configure the evaluation board to obtain all +5 V power solely through the main USB connector at J37. This setup is the default configuration and should normally be sufficient.

The following figure shows the correct installation of the jumper shunts at JP15 and JP16 for default or standard operation.

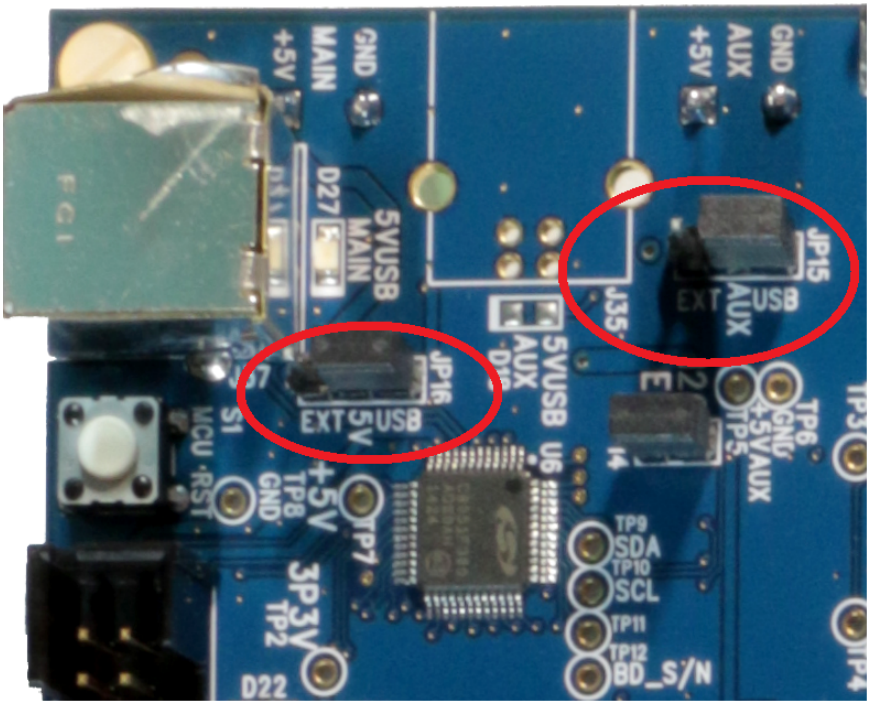


Figure 10.2. JP15–JP16 Standard Jumper Shunt Installation

The general guidelines for single USB power supply operation are as follows:

- Use either a USB 3.0 or USB 2.0 port. These ports are specified to supply 900 mA and 500 mA, respectively, at +5 V.
- If you are working with a USB 2.0 port and you are current limited, turn off enough DUT output voltage regulators to drop the total DUT current ≤470 mA. (Note: USB 2.0 ports may supply > 500 mA. Provided the nominal +5 V drops gracefully by less than 10%, the EVB will still work.)
- If you are working with a USB 2.0 and you are current limited and need all output clock drivers enabled, reconfigure the EVB to drive the DUT output voltage regulators from an external +5 V power supply as follows:
  - Connect an external +5 V power supply to terminal block J33 on the back side of the PCB.
  - Move the jumper at JP15 from pins 1–2 USB to pins 2–3 EXT.

10.3 Overview of ClockBuilder Pro Applications

Note: The following instructions and screen captures may vary slightly depending on your version of ClockBuilder Pro. The ClockBuilder Pro installer will install **two** main applications:

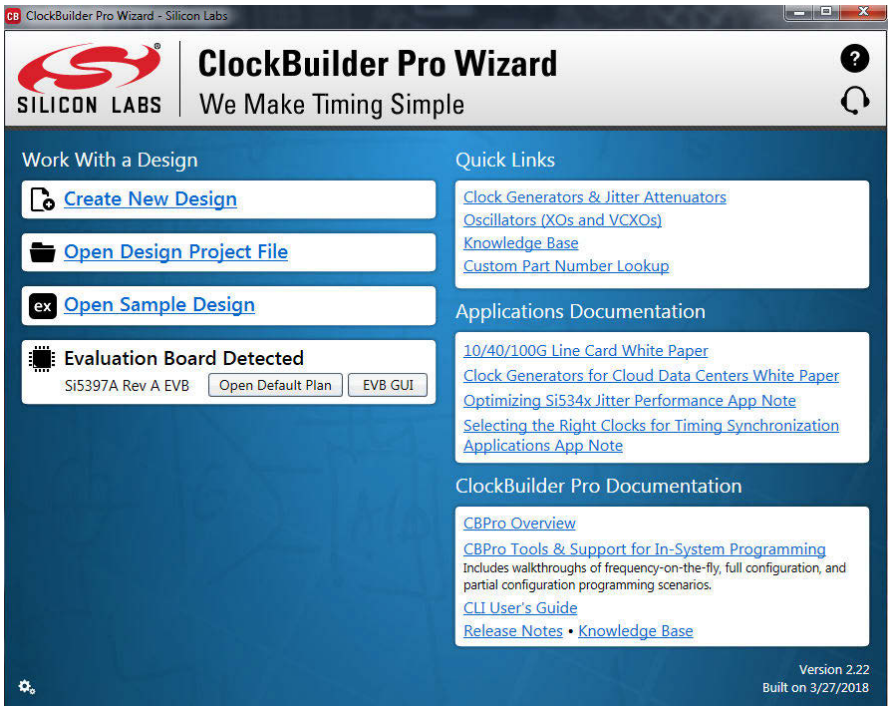


Figure 10.3. Application #1: ClockBuilder ProWizard

Use the CBPro wizard to:

- Create a new design
- Review or edit an existing design
- Export: create in-system programming

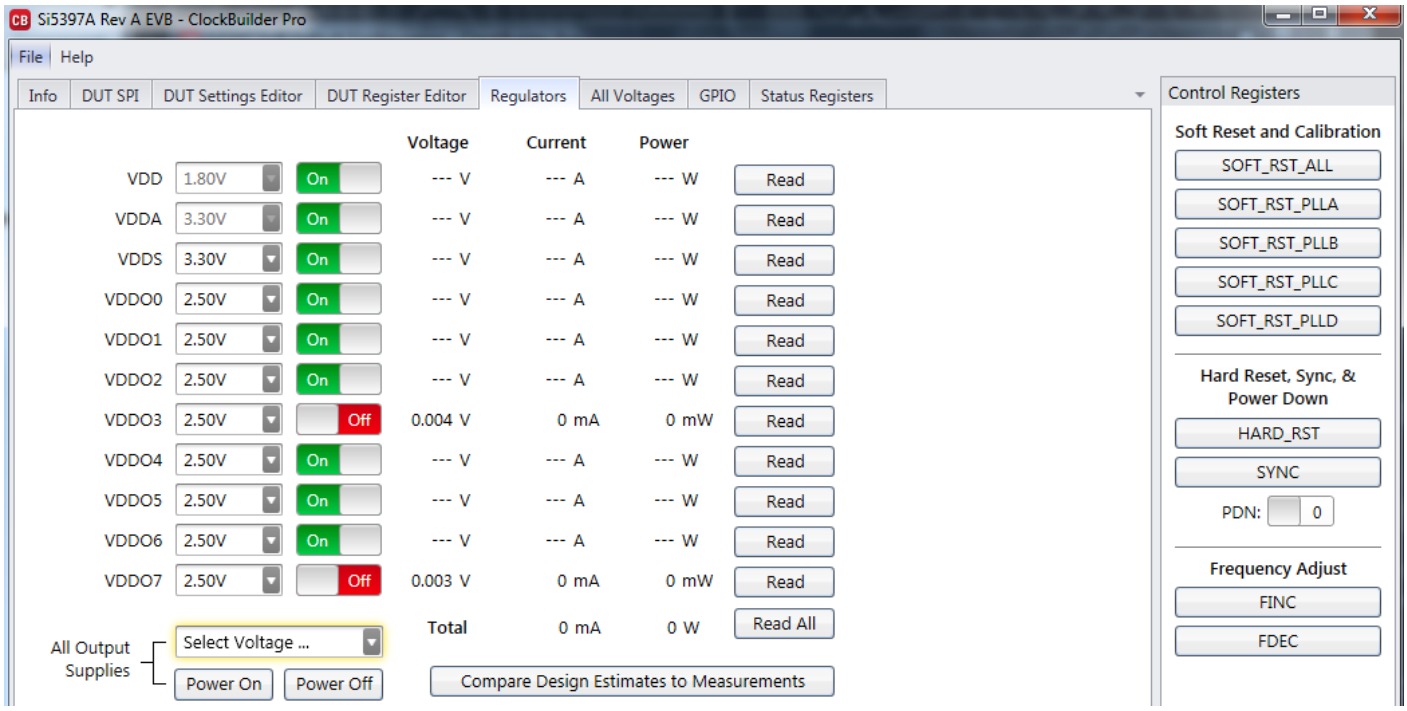


Figure 10.4. Application #2: EVBGUI

Use the EVB GUI to:

- Download configuration to EVB's DUT (Si5397)
- Control the EVB's regulators
- Monitor voltage, current, and power on the EVB

10.4 Common ClockBuilderPro Workflow Scenarios

There are three common workflow scenarios when using CBPro and the Si5397-A-EVB. These workflow scenarios are:

- Workflow Scenario 1: Testing a Silicon Labs-Created Default Configuration
- Workflow Scenario 2: Modifying the Default Silicon Labs-Created Device Configuration
- Workflow Scenario 3: Testing a User-Created Device Configuration

Each workflow scenario is described in more detail in the following sections.

10.5 Workflow Scenario 1: Testing a Silicon Labs Default Configuration

The flow for using the EVB GUI to initialize and control a device on the EVB is as follows:

Once the PC and EVB are connected, launch **ClockBuilderPro** by clicking this icon on your PC's desktop:

Figure 10.5. ClockBuilderPro Desktop Icon

If an EVB is detected, click on the "Open Default Plan" button on the Wizard's main menu. CBPro automatically detects the EVB and device type.

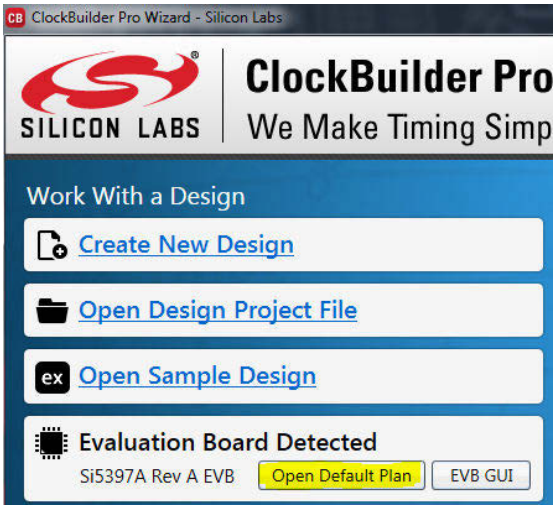


Figure 10.6. Open Default Plan

Once you open the default plan (based on your EVB model number), a popup will appear:

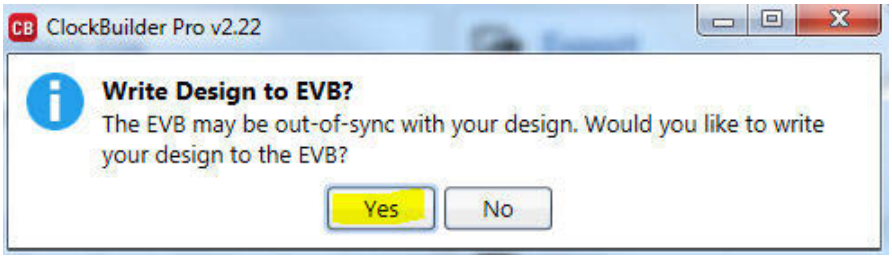


Figure 10.7. Write Design to EVB Dialog

Select “Yes” to write the default plan to the Si5395 device mounted on your EVB. This ensures the device is completely reconfigured per the Silicon Labs default plan for the DUT type mounted on the EVB.

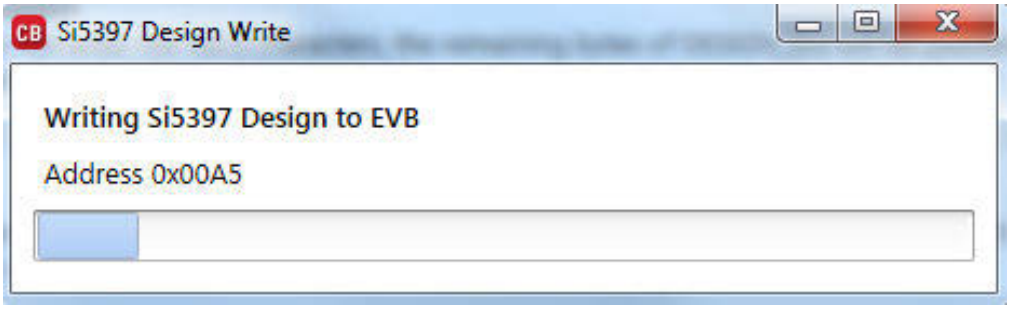


Figure 10.8. Writing Design Status

After CBPro writes the default plan to the EVB, click on “Open EVB GUI” as shown below:

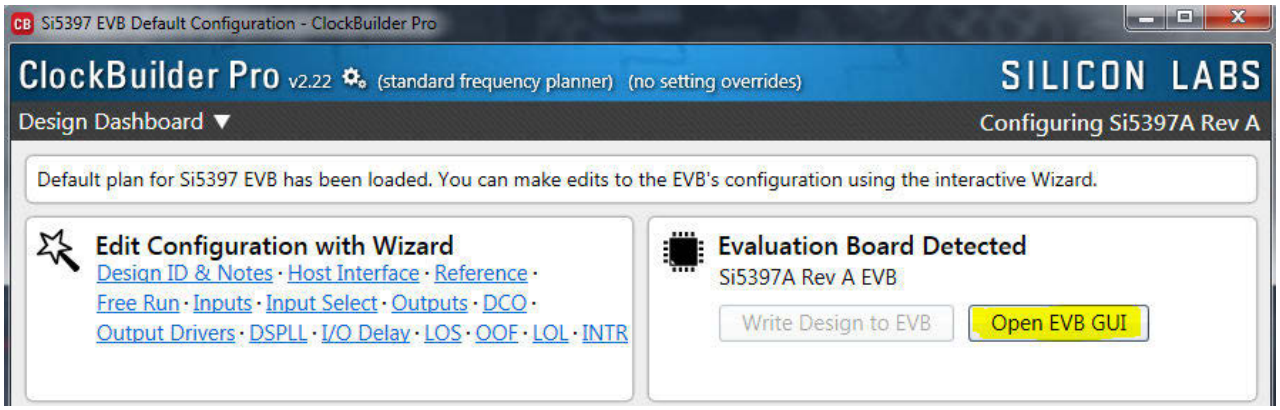


Figure 10.9. Open EVB GUI

The EVB GUI will appear. Note that all power supplies will be set to the values defined in the device’s default CBPro project file created by Silicon Labs, as shown in the following figure:

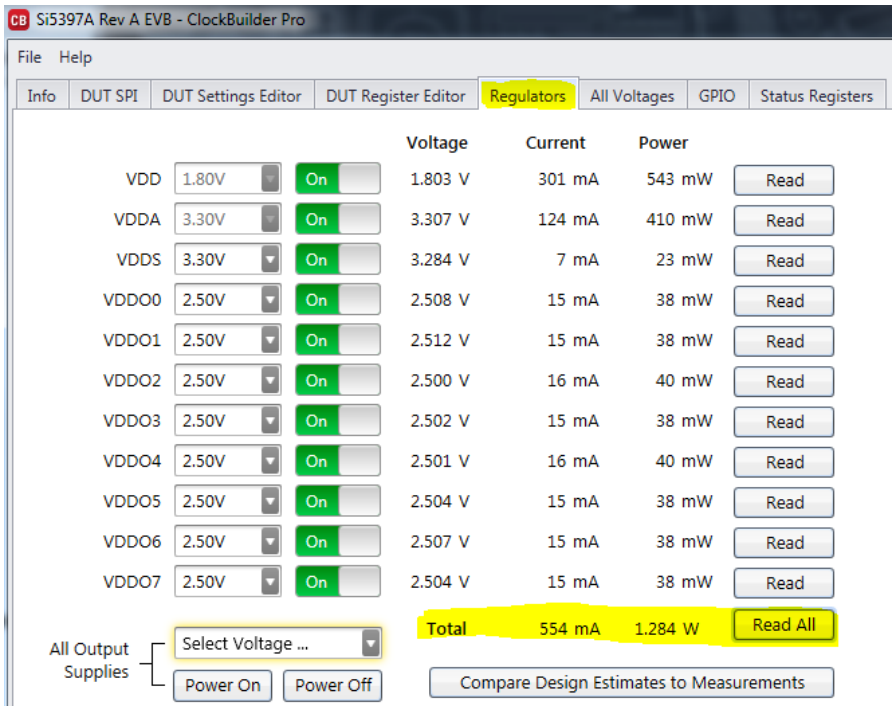


Figure 10.10. EVB GUI Window

10.5.1 Verify Free-Run Mode Operation

Assuming no external clocks have been connected to the INPUT CLOCK differential SMA connectors (labeled “INx/INxB”) located around the perimeter of the EVB, the DUT should now be operating in free-run mode, as the DUT will be locked to the crystal in this case.

You can run a quick check to determine if the device is powered up and generating output clocks (and consuming power) by clicking on the Read All button highlighted above and then reviewing the voltage, current, and power readings for each VDDx supply.

Note: Shutting the VDD and VDDA supplies “Off” then “On” will power-down and reset the DUT. Every time you do this, to reload the Silicon Labs-created default plan into the DUT’s register space, you must go back to the Wizard’s main menu and select “Write Design to EVB” as shown below.

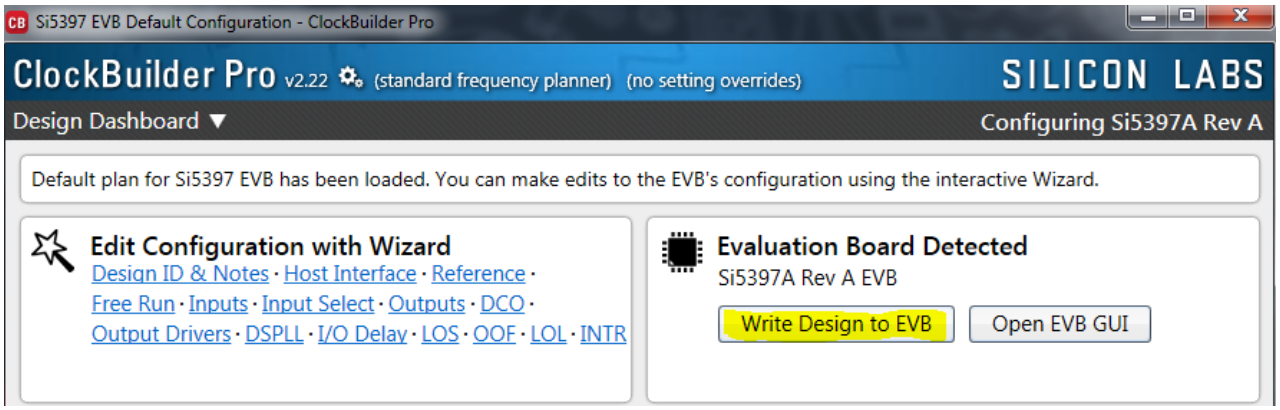


Figure 10.11. Write Design to EVB

Failure to perform this step will cause the device to read in a preprogrammed plan from its non-volatile memory (NVM). However, the plan loaded from the NVM may not be the latest plan recommended by Silicon Labs for evaluation.

At this point, you should verify the presence and frequencies of the output clocks (running to free-run mode from the crystal) using appropriate external instrumentation connected to the output clock SMA connectors. To verify the output clocks are toggling at the correct frequency and signal format, click on View Design Report as highlighted below.

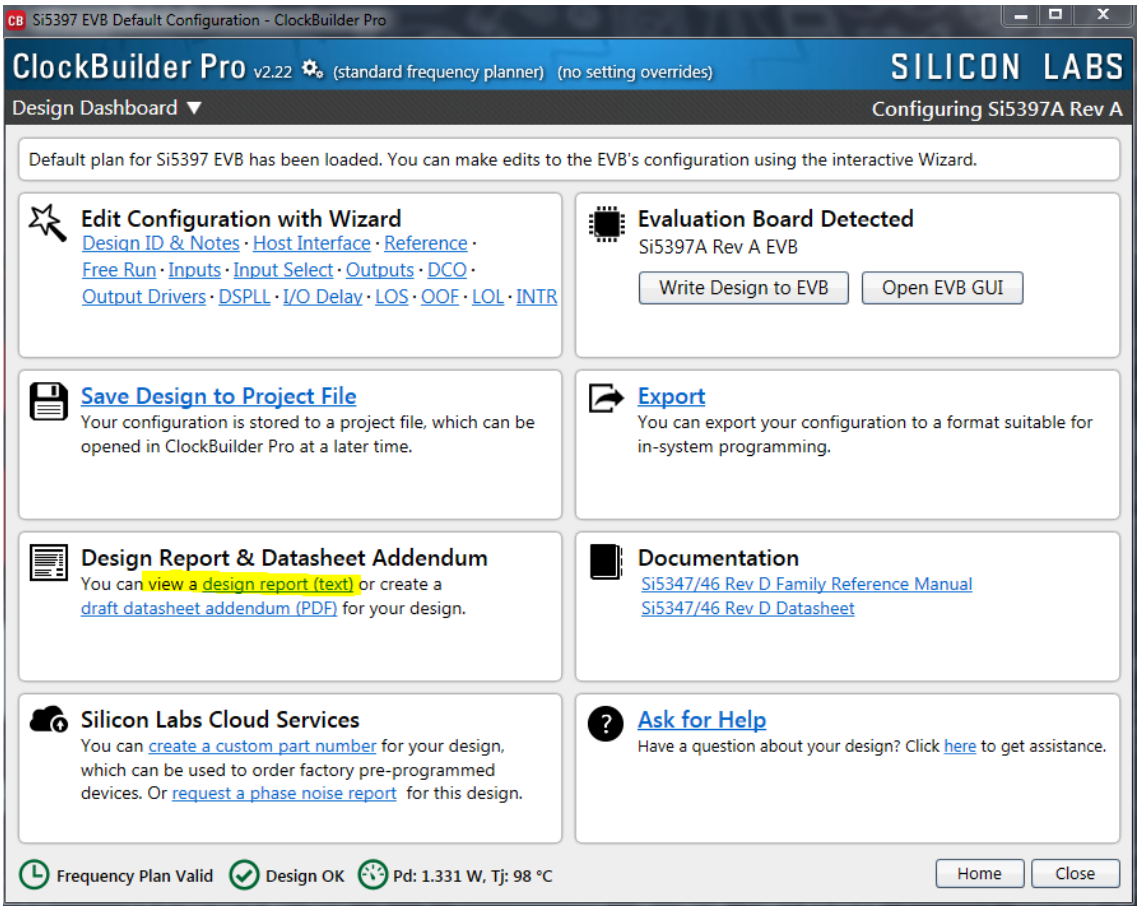


Figure 10.12. View Design Report

Your configuration's design report will appear in a new window, as shown below. Compare the observed output clocks to the frequencies and formats noted in your default project's Design Report.

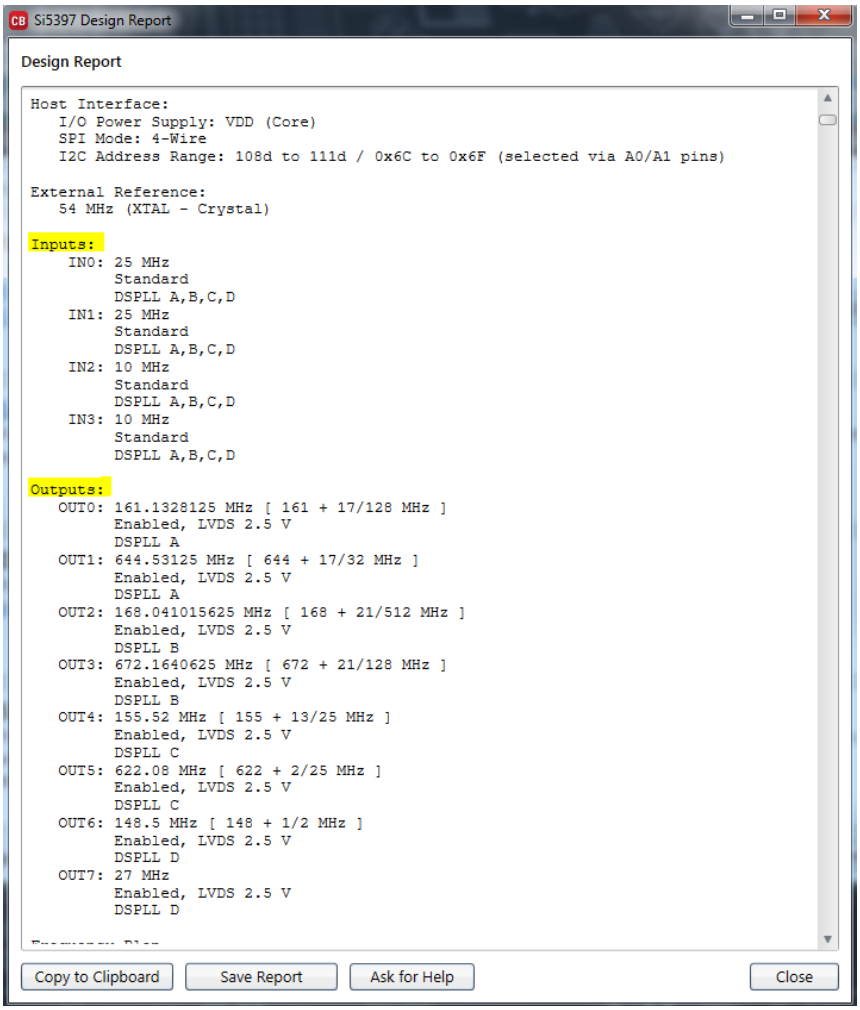


Figure 10.13. Design Report Window

10.5.2 Verify Locked Mode Operation

Assuming you connect the correct input clocks to the EVB (as noted in the Design Report shown above), the DUT on your EVB will be running in “locked” mode.

10.6 Workflow Scenario 2: Modifying the Default Silicon Labs-Created Device Configuration

To modify the “default” configuration using the CBPro Wizard, click on the links below under “Edit Configuration with Wizard”.

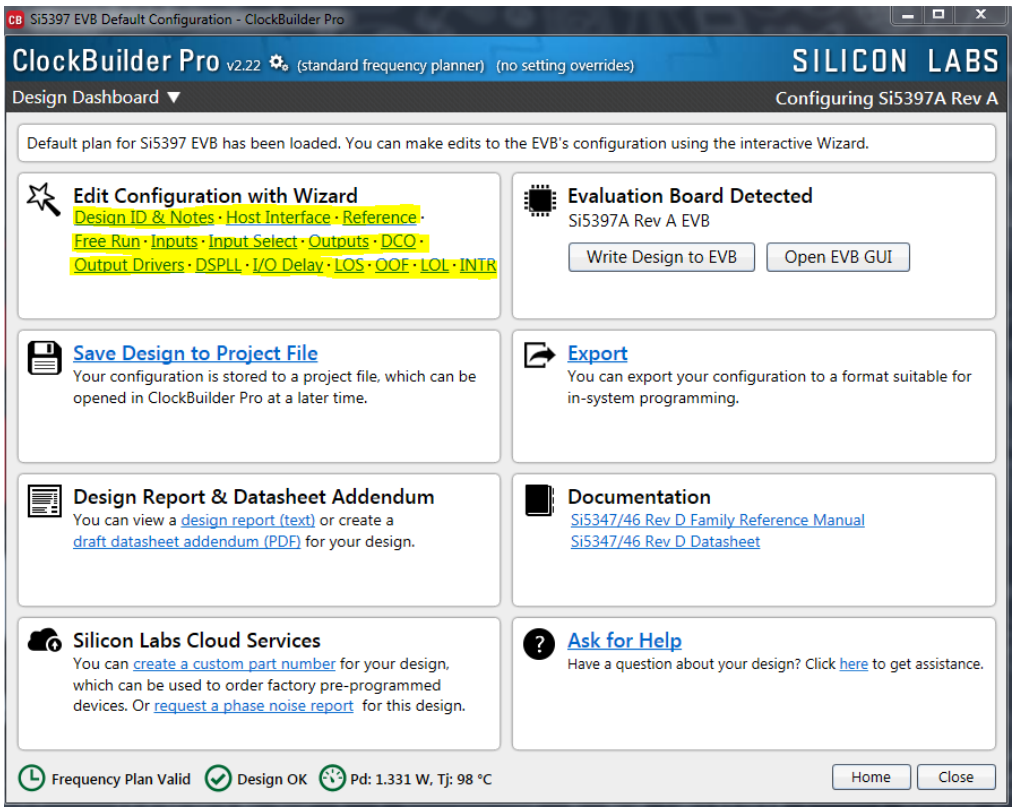


Figure 10.14. Edit Configuration with Wizard

You will now be taken to the Wizard’s step-by-step menus to allow you to change any of the default plan’s operating configurations.

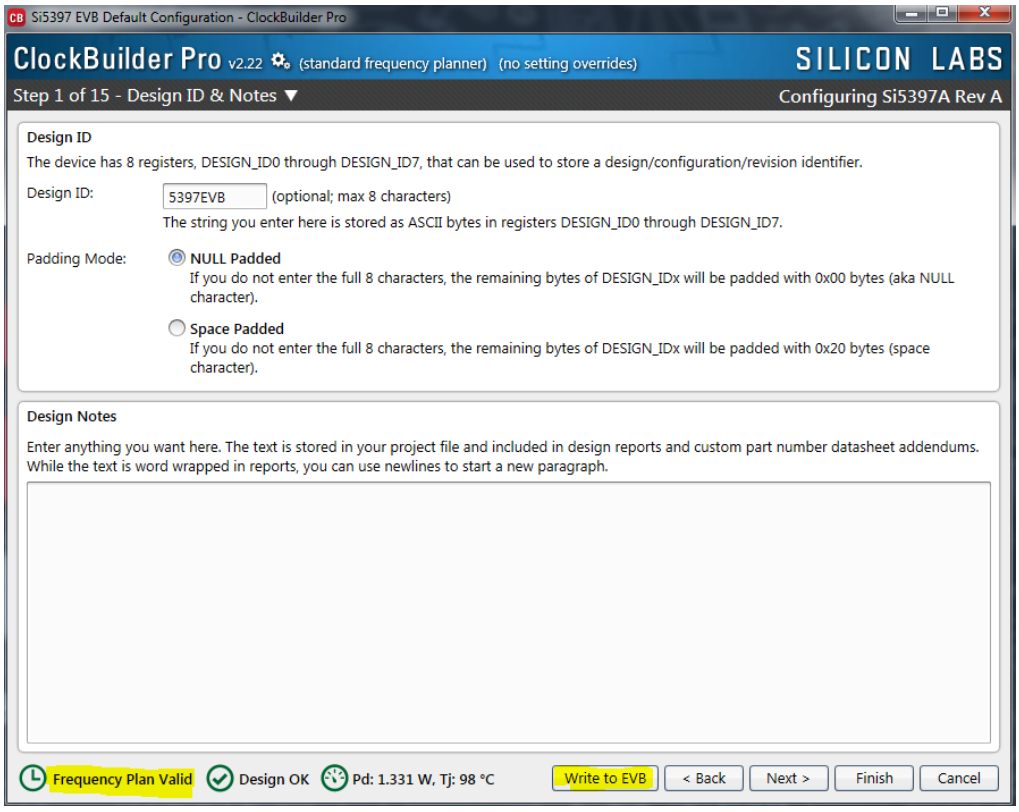


Figure 10.15. Design Wizard

Note that you can click on the icon on the lower left hand corner of the menu to confirm if your frequency plan is valid. After making your desired changes, you can click on Write to EVB to update the DUT to reconfigure your device real-time. The Design Write status window will appear each time you make a change.

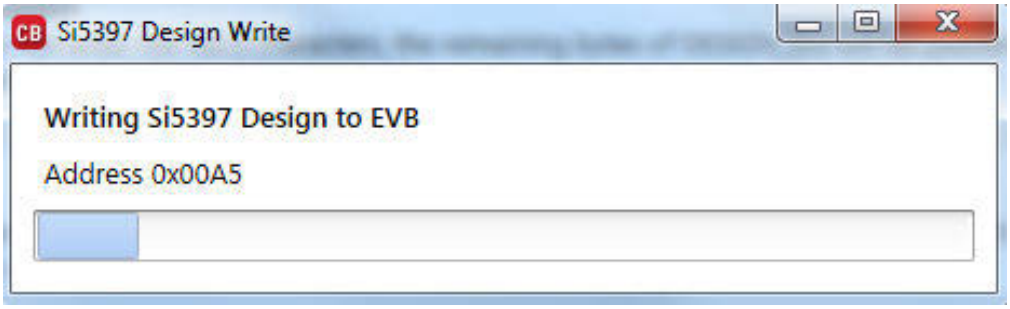


Figure 10.16. Writing Design Status

10.7 Workflow Scenario 3: Testing a User-Created Device Configuration

To test a previously created user configuration, open the CBPro Wizard by clicking on the icon on your desktop and then selecting Open Design Project File.

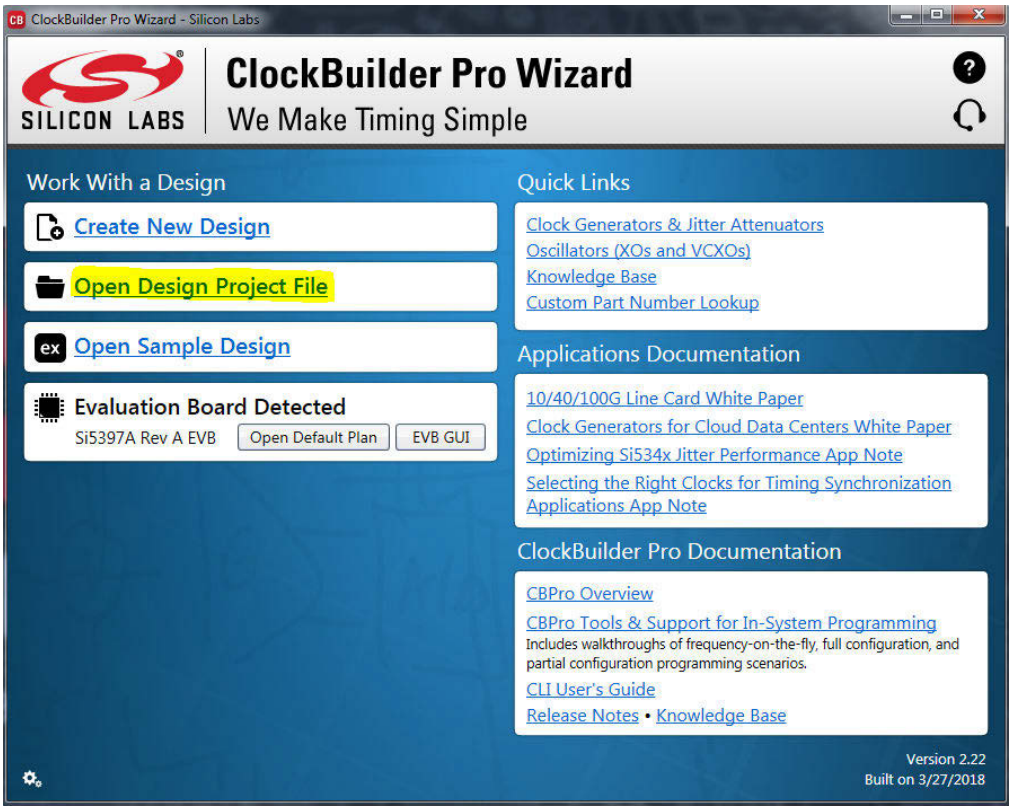


Figure 10.17. Open Design Project File

Locate your CBPro design file (*.slabtimeproj or *.sitproj file).design file in the Windows file browser.

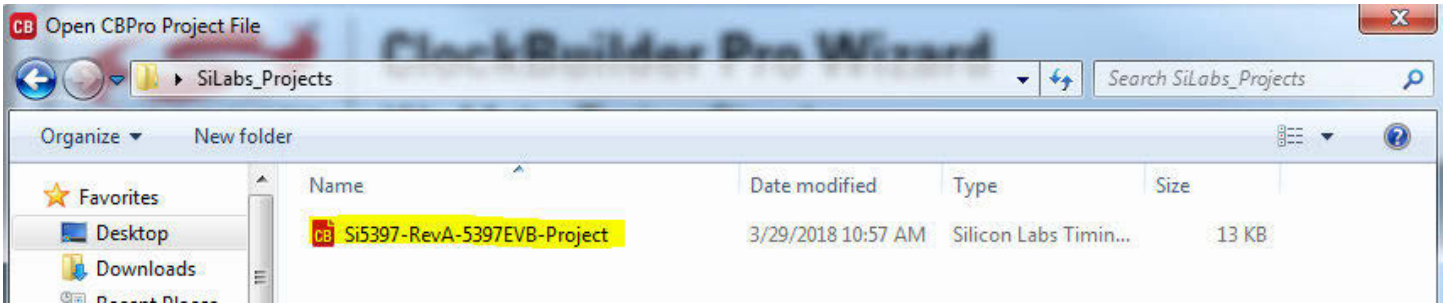


Figure 10.18. Browse to Project File

Select "Yes" when the WRITE DESIGN to EVB popup appears:

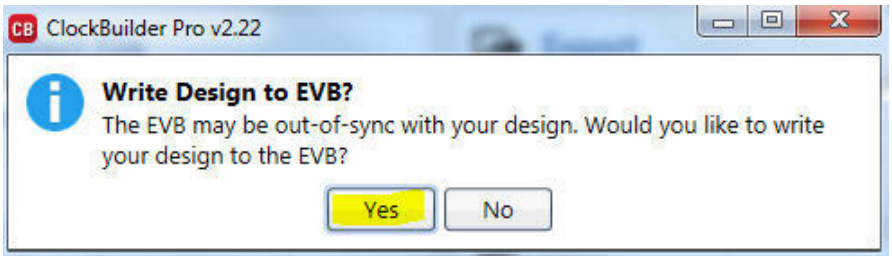


Figure 10.19. Write Design to EVB Dialog

The progress bar will be launched. Once the new design project file has been written to the device, verify the presence and frequencies of your output clocks and other operating configurations using external instrumentation.

10.8 Exporting the Register Map File for Device Programming by a Host Processor

You can also export your configuration to a file format suitable for in-system programming by selecting Export as shown below:

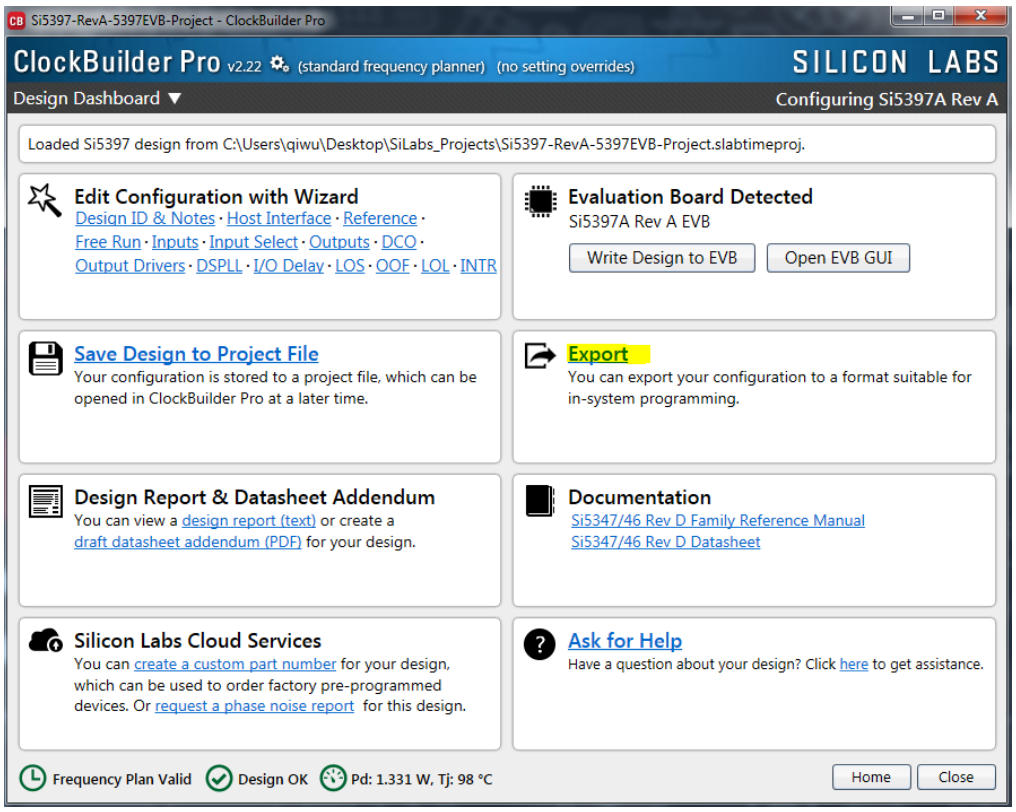


Figure 10.20. Export Register Map File

You can now write your device's complete configuration to file formats suitable for in-system programming:

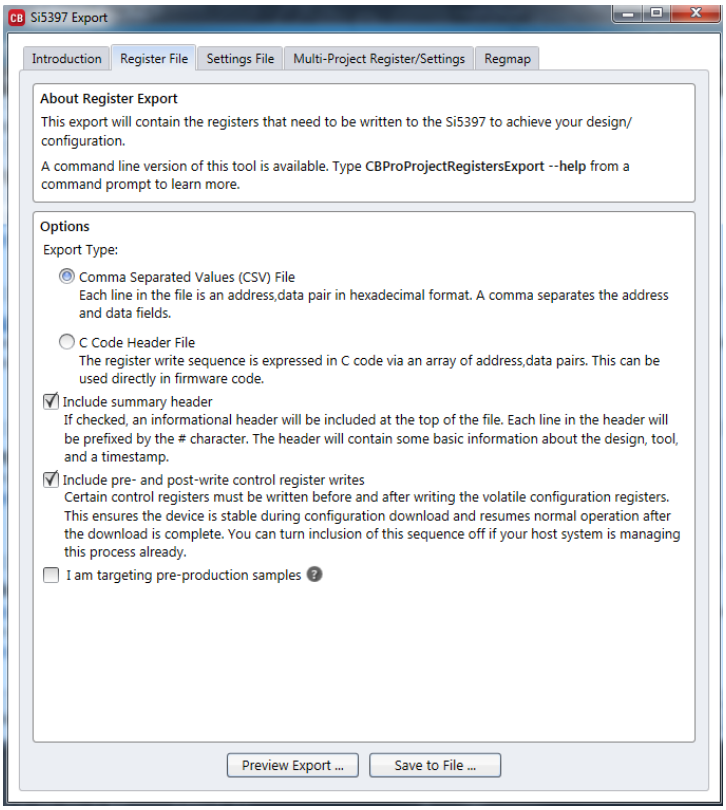


Figure 10.21. Export Settings

11. Writing a New Frequency Plan or Device Configuration to Non-Volatile Memory (OTP)

Note: Writing to the device non-volatile memory (OTP is **NOT** the same as writing a configuration into the Si5397 using Clock- Builder-PRo on the Si5397-A-EB. Writing a configuration into the EVB from ClockBuilderPro is done using Si5397 RAM space and can be done a virtually unlimited numbers of times. Writing to OTP is limited as described below.

Refer to the Si534x/8x Family Reference Manuals and device data sheets for information on how to write a configuration to the EVB DUT's non-volatile memory (OTP). The OTP can be programmed a maximum of **two** times only. Care must be taken to ensure the desired configuration is valid when choosing to write to OTP.

12. Serial Device Communications

12.1 Onboard SPI Support

The MCU onboard the Si5397-A-EB communicates with the Si5397 device through a 4-wire SPI (Serial Peripheral Interface) link. The MCU is the SPI master and the Si5397 device is the SPI slave. The Si5397 device can also support a 2-wire I^2C serial interface, although the Si5397-A-EB does NOT support the I^2C mode of operation. SPI mode was chosen for the EVB because of the relatively higher speed transfers supported by SPI vs. I^2C.

13. Si5397-EVB Schematic, Layout, and Bill of Materials (BOM)

The Si5397-EB Schematic, Layout, and Bill of Materials (BOM) can be found online at: http://www.silabs.com/products/clocksoscillators/pages/si539x-evb.aspx.

Note: Please be aware that the Si5397-A-EB schematic is in **OrCad Capture** *hierarchical format* and not in a typical “flat” schematic format.

ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

www.silabs.com/CBPro

Timing Portfolio
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