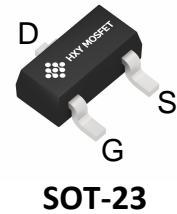




## Description

The ZXMN10A07F uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



## General Features

$V_{DS} = 100V$   $I_D = 3A$

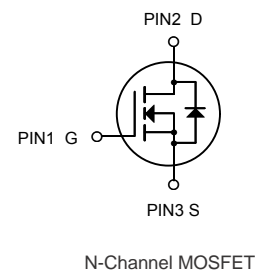
$R_{DS(ON)} < 248m\Omega$  @  $V_{GS}=10V$

## Application

Battery protection

Load switch

Uninterruptible power supply



## Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
ZXMN10A07F	SOT-23	HXY MOSFET	3000

## Absolute Maximum Ratings (TC=25°C unless otherwise specified)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	100	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_A=25^\circ C$	Continuous Drain Current, $V_{GS}$ @ 10V <sup>1</sup>	3	A
$I_D@T_A=70^\circ C$	Continuous Drain Current, $V_{GS}$ @ 10V <sup>1</sup>	1	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	5	A
$P_D@T_A=25^\circ C$	Total Power Dissipation <sup>3</sup>	1	W
$T_{STG}$	Storage Temperature Range	-55 to 150	°C
$T_J$	Operating Junction Temperature Range	-55 to 150	°C
$R_{\theta JA}$	Thermal Resistance Junction-ambient <sup>1</sup>	125	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	80	°C/W



Electrical Characteristics ( $T_J=25^\circ\text{C}$ , unless otherwise noted)

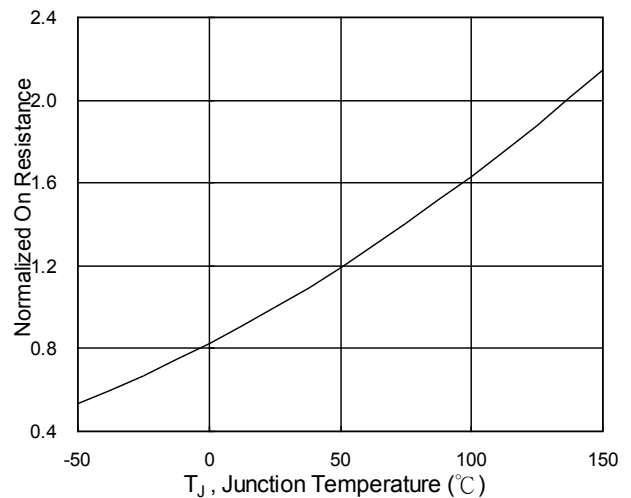
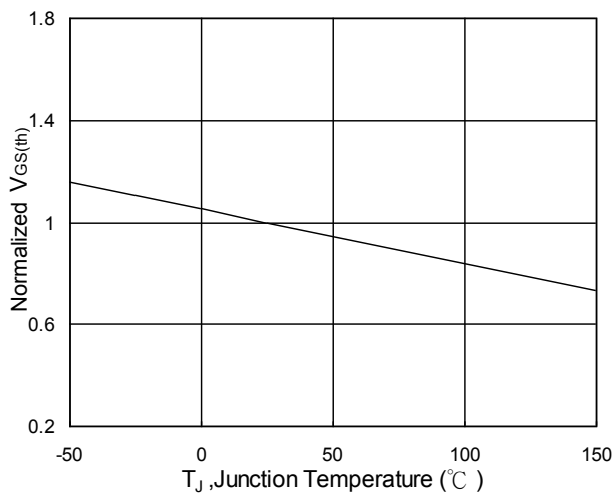
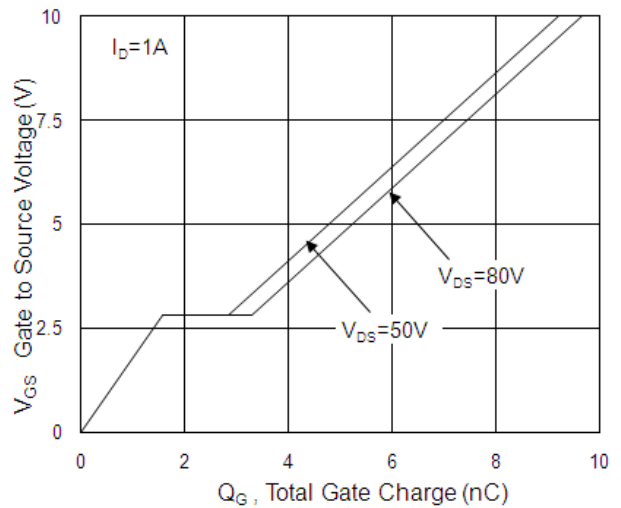
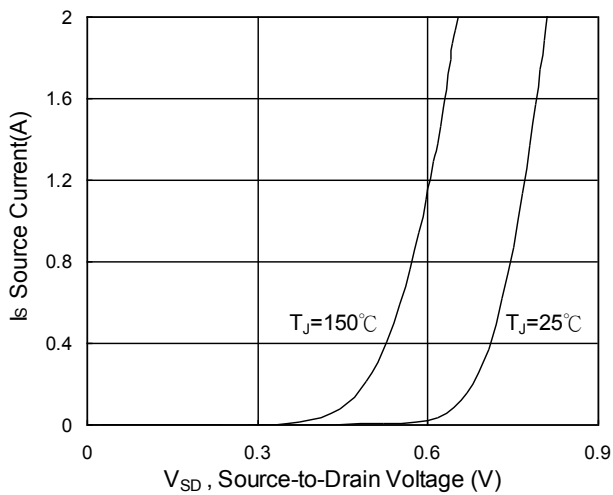
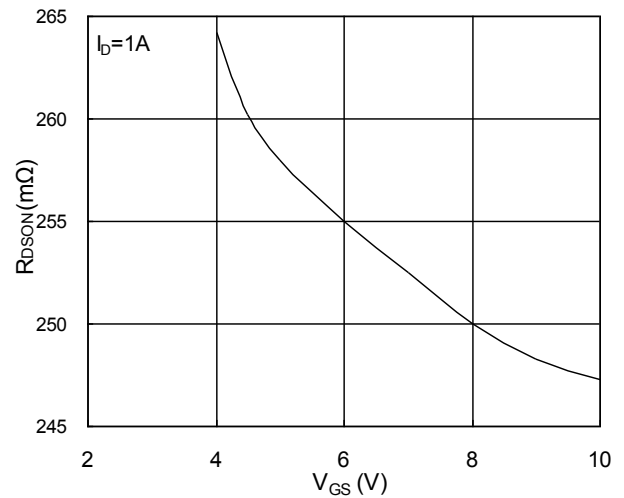
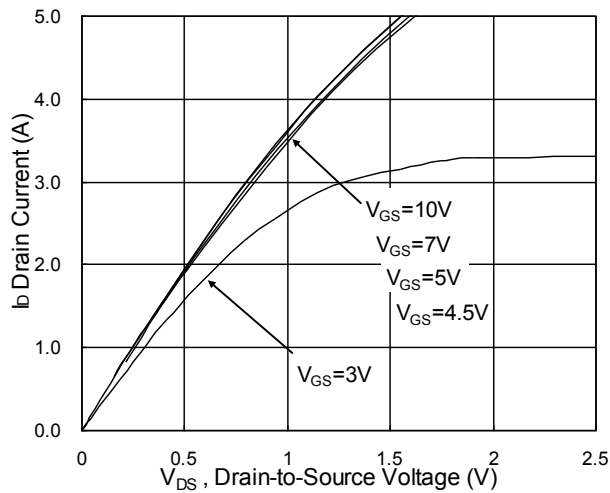
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V$ , $I_D=250\mu A$	100	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BVDSS Temperature Coefficient	Reference to $25^\circ\text{C}$ , $I_D=1mA$	---	0.067	---	$V/^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10V$ , $I_D=1A$	---	210	248	$m\Omega$
		$V_{GS}=4.5V$ , $I_D=0.5A$	---	244	290	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$ , $I_D=250\mu A$	1.0	1.5	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-4.2	---	$mV/^\circ\text{C}$
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=80V$ , $V_{GS}=0V$ , $T_J=25^\circ\text{C}$	---	---	1	$\mu A$
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=80V$ , $V_{GS}=0V$ , $T_J=25^\circ\text{C}$	---	---	5	$\mu A$
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 20V$ , $V_{DS}=0V$	---	---	$\pm 100$	nA
$g_{fs}$	Forward Transconductance	$V_{DS}=5V$ , $I_D=1A$	---	2.4	---	S
$R_g$	Gate Resistance	$V_{DS}=0V$ , $V_{GS}=0V$ , $f=1MHz$	---	2.8	5.6	
$Q_g$	Total Gate Charge (10V)	$V_{DS}=80V$ , $V_{GS}=10V$ , $I_D=1A$	---	9.7	13.6	nC
$Q_{gs}$	Gate-Source Charge		---	1.6	2.2	
$Q_{gd}$	Gate-Drain Charge		---	1.7	2.4	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=50V$ , $V_{GS}=10V$ , $R_g=3.3$ $I_D=1A$	---	1.6	3.2	ns
$T_r$	Rise Time		---	19	34	
$T_{d(off)}$	Turn-Off Delay Time		---	13.6	27	
$T_f$	Fall Time		---	19	38	
$C_{iss}$	Input Capacitance	$V_{DS}=15V$ , $V_{GS}=0V$ , $f=1MHz$	---	508	711	pF
$C_{oss}$	Output Capacitance		---	29	41	
$C_{rss}$	Reverse Transfer Capacitance		---	16.4	23	
$I_S$	Continuous Source Current <sup>1,4</sup>	$V_G=V_D=0V$ , Force Current	---	---	1.2	A
$I_{SM}$	Pulsed Source Current <sup>2,4</sup>		---	---	5	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V$ , $I_S=1A$ , $T_J=25^\circ\text{C}$	---	---	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F=1A$ , $dI/dt=100A/\mu s$ , $T_J=25^\circ\text{C}$	---	14	---	nS
$Q_{rr}$	Reverse Recovery Charge		---	9.3	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup>FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- 3.The power dissipation is limited by  $150^\circ\text{C}$  junction temperature
- 4 .The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.



## Typical Characteristics



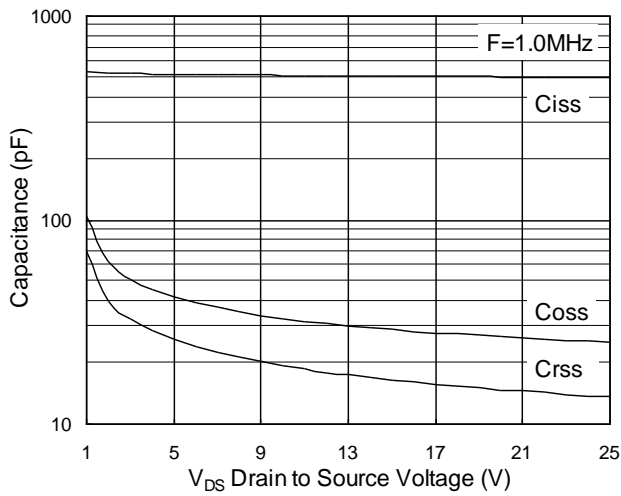


Fig.7 Capacitance

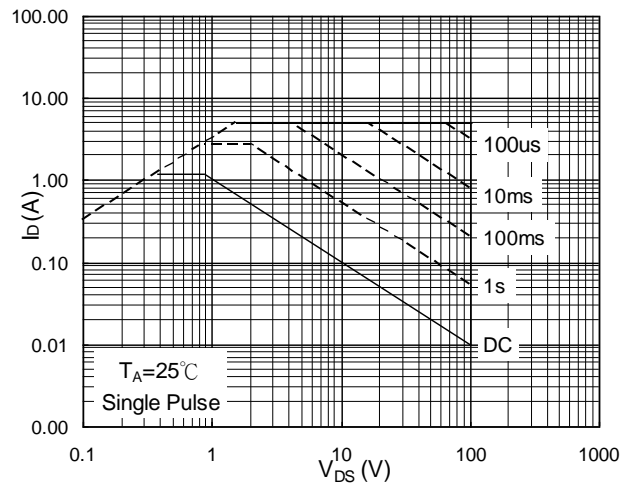


Fig.8 Safe Operating Area

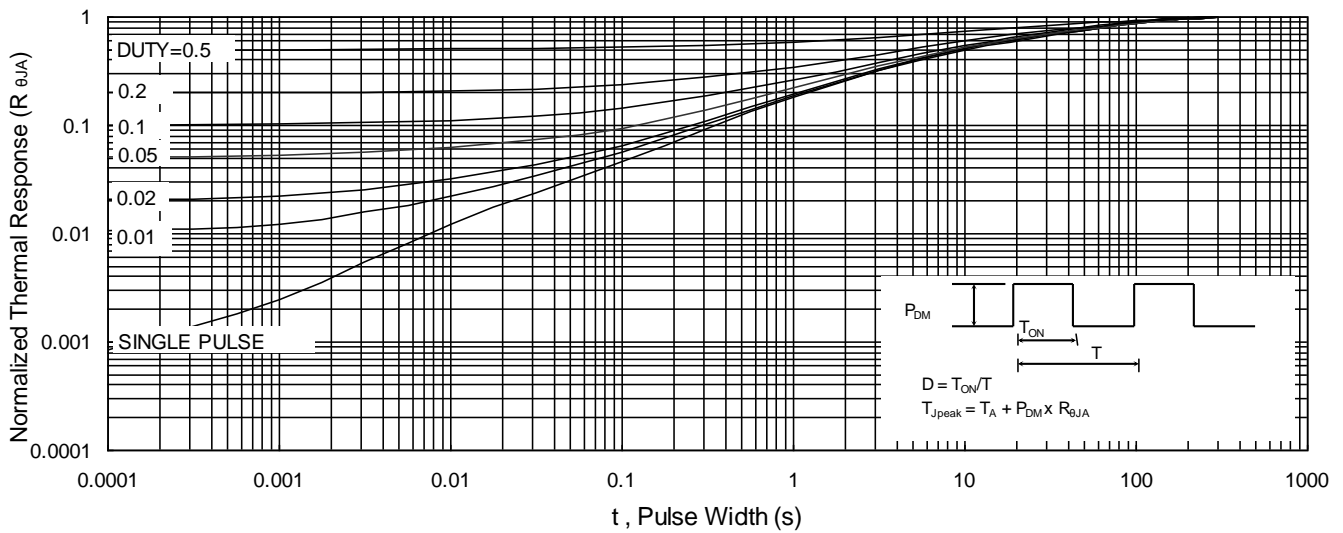


Fig.9 Normalized Maximum Transient Thermal Impedance

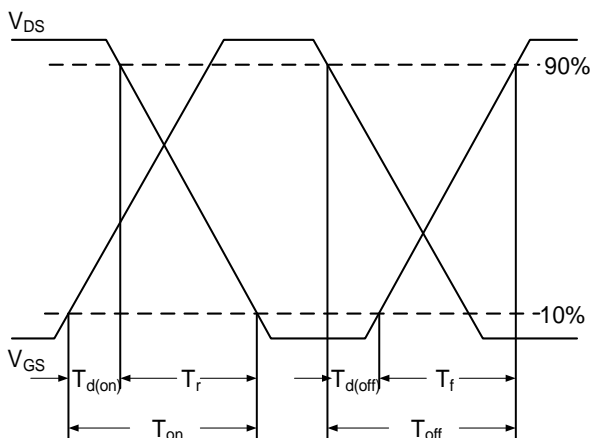


Fig.10 Switching Time Waveform

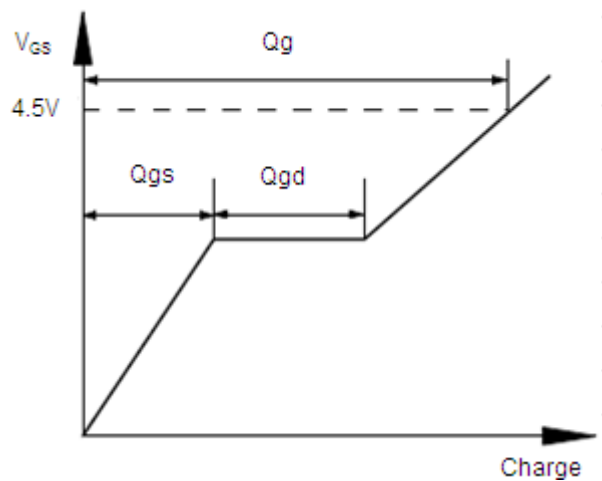
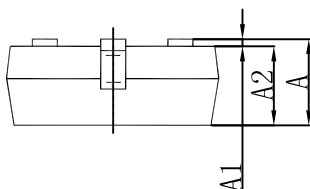
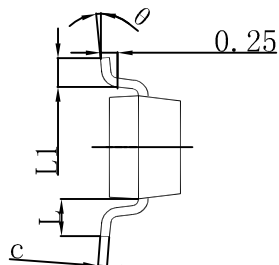
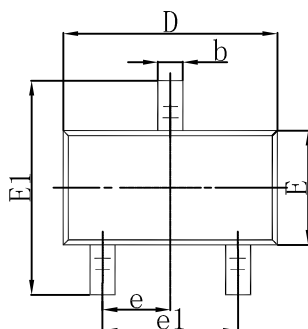


Fig.11 Gate Charge Waveform

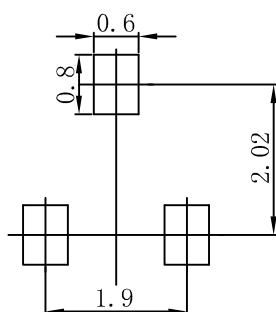


## SOT-23 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

## SOT-23 Suggested Pad Layout



### Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.05\text{mm}$ .
3. The pad layout is for reference purposes only.



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