User's Guide

TPSM8A29 Power Module Evaluation Module User's Guide

ABSTRACT

The TPSM8A29EVM is designed as a versatile and easy to use evaluation module (EVM) that facilitates the evaluation and performance of the TPSM8A29 power module. This user's guide provides information on how to use the TPSM8A29EVM, and provides an explanation of the featured test points.

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Trademarks

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1 Introduction

The TPSM8A29 is a highly integrated synchronous buck converter module capable of delivering up to 15 A to a load. The TPSM8A29 has an input operating voltage of 4 V to 16 V, and an output voltage of 0.6 V to 5.5 V. The TPSM8A29 features integrated power MOSFETs, an integrated inductor, as well as several integrated capacitors, allowing for a small solution size to minimize the board layout area. By integrating several passive components, the TPSM8A29 module simplifies routing and reduces EMI for fast time-to-market designs.

The TPSM8A29EVM is designed with several test points which allow the user to evaluate the performance of the TPSM8A29 buck converter module. The recommended operating conditions of the TPSM8A29 are given in Table 1-1.

Table 1-1. TPSM8A29 Operating Conditions

Test Point	Operating Condition
Input voltage range	4 V to 16 V without external bias, 2.7 V to 16 V with external bias
Output voltage range	0.6 V to 5.5 V
Output current	15 A max

2 Description

The TPSM8A29EVM is configured for operation with a 4-V to 16-V input voltage. A wide range of output voltages (0.8 V to 5 V) can be configured using the included header (see Section 3.5). Three different switching frequencies (600 kHz, 800 kHz, 1 MHz), as well as forced-continuous conduction mode (FCCM) or discontinuous conduction mode (DCM) operation are also configured using the included header (see Section 3.4). Any output voltage from 0.6 V to 5.5 V can be set by using Equation 3 and Equation 4.

Several test points are included to facilitate the measurement and evaluation of device performance. Several other test points can be used to monitor control signals, or to use as external input control signals to the TPSM8A29. See Section 4 for a detailed description of the TPSM8A29EVM test points.

The wide input voltage range, output voltage range, high current output, small solutions size, and flexible operating modes of the TPSM8A29 make the TPSM8A29 an excellent choice for a wide range of markets.

3 Getting Started With the TPSM8A29EVM

Figure 3-1 and Figure 3-2 show the user interface of the TPSM8A29EVM. A description of the input and output connections is shown in Table 3-1. A description of the headers is shown in Table 3-2 . Further details and considerations are given after the tables.

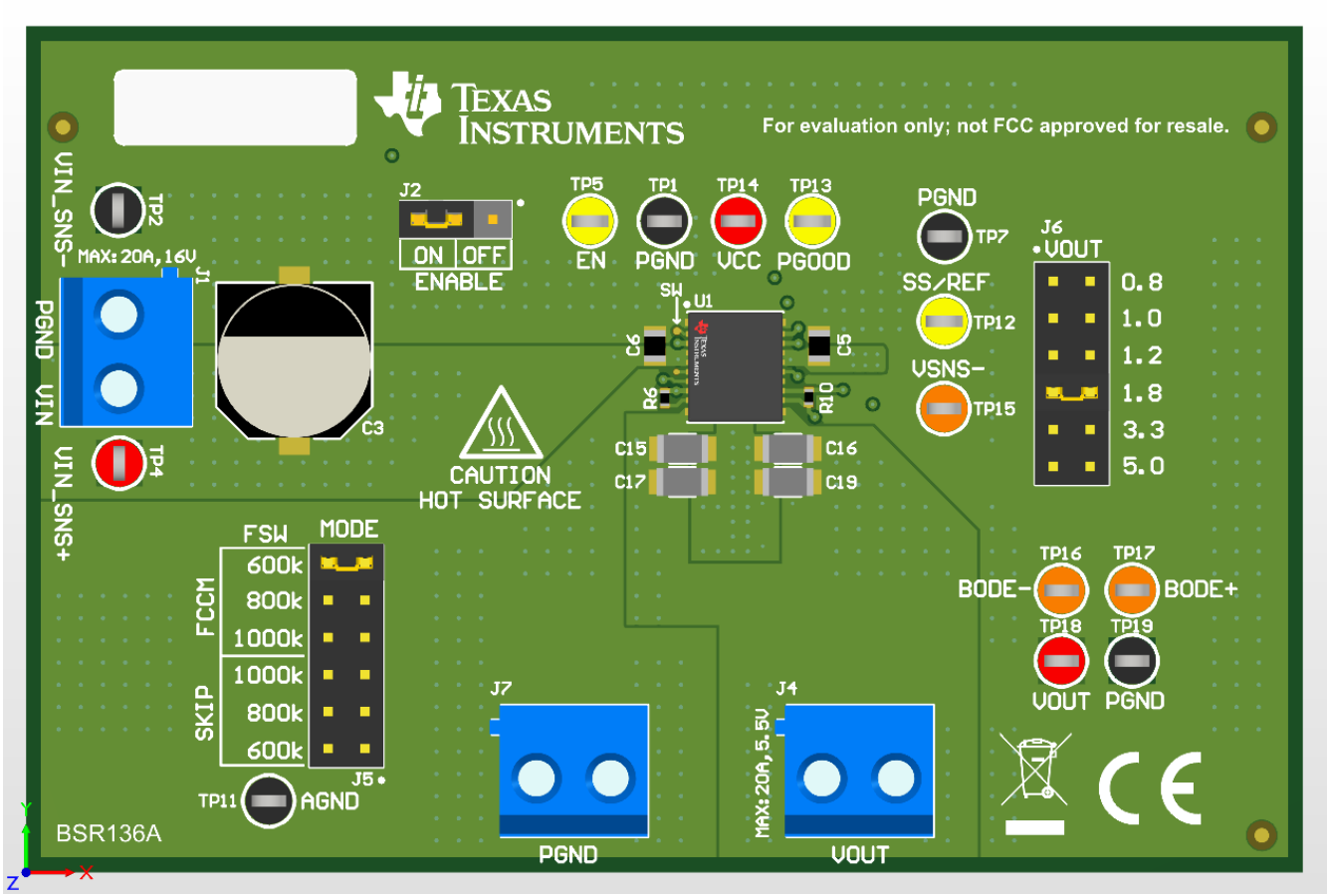


Figure 3-1. TPSM8A29EVM 3-D Top View

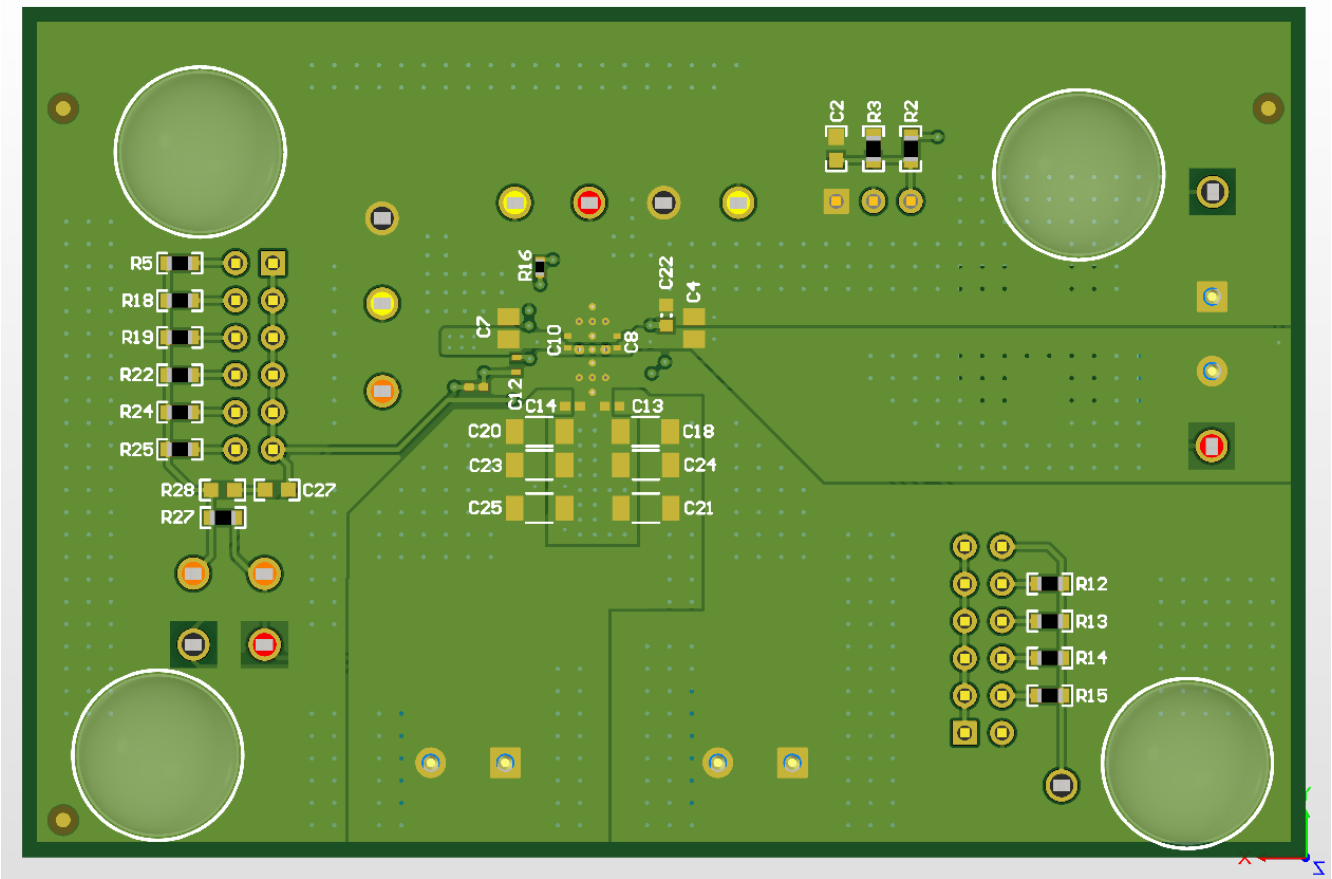


Figure 3-2. TPSM8A29EVM 3-D Bottom View

Table 3-1. Input and Output Connection Descriptions

Connector	Description
J1	Positive and negative input voltage supply connection, 4 V - 16 V
J4	Positive output voltage connection, 0.8 V - 5 V
J7	Negative output voltage connection

Table 3-2. Header Descriptions

Header	Description
J2	Enable header
J5	Switching frequency and FCCM/DCM operation selection header
J6	Output voltage selection header

3.1 J1 - Input Voltage Supply Connector

The connector J1 is used to connect the DC input voltage supply to the EVM. The positive connection of the input supply is connected to J1-1 (J1, pin 1), and the negative connection of the input supply is connected to J1-2. This is indicated by the silkscreen markings on the EVM. This connector is designed to accept a wire size of 14 AWG - 22 AWG. To minimize voltage drops across the input voltage supply cable, wire lengths should be minimized, and a heavier gauge wire should be favored over a lighter gauge. TI recommends using 18 AWG or greater.

For power supplies that support remote sensing, the positive sense point is connected to TP4 (VIN_SNS+), and the negative sense point is connected to TPS (VIN_SNS-).

3.2 J4 and J7 - Positive and Negative Output Connectors

J4 and J7 are the positive and negative connection points for a load, respectively. Because the expected output current is greater than that of the input current, dedicated connectors are used. For output currents greater than 10 A, it is recommended that both screw terminals of each connector are utilized for connection to the load. This connector is designed to accept a wire size of 14 AWG - 22 AWG. To minimize voltage drops across the output cable, wire lengths should be minimized, and a heavier gauge wire should be favored over a lighter gauge. TI recommends using 16 AWG or greater for connection to a load.

The output voltage can be monitored using the TP18 (VOUT) and TP19 (PGND) test points located on the lower right-hand side of the EVM. These test points are connected across C19 (see Figure 7-5).

3.3 J2 - Enable Header

The TPSM8A29 can be enabled or disabled using the J2 header. A jumper is placed between J2-2 and J2-3 to enable the device, as indicated by the silkscreen on the EVM. Using this configuration, undervoltage lockout (UVLO) can be implemented by adjusting resistors R_{EN_HS} (R2) and R_{EN_LS} (R3), which form a voltage divider between V_{IN} and PGND. By default, the EVM is designed to work over the entire input voltage supply range of 4 V to 16 V. To configure the EVM for UVLO, see Equation 1, where R_{EN_HS} is the high-side resistor of the UVLO divider (R2), V_{START} is the desired turn-on voltage, V_{ENH} is the typical enable pin threshold, and V_{EN_B} is the low-side resistor of the UVLO divider (R3).

The TPSM8A29 can also enabled by floating the enable header. An internal pullup current source enables the device over the entire input voltage supply range. This reduces the BOM count and solution size in applications where UVLO is not required.

To disable the device, a jumper is placed in the OFF position between J2-1 and J2-2, as indicated by the silkscreen on the EVM. This shorts the EN pin of the TPSM8A29 to PGND, disabling the device.

Note that if the EN pin is to be controlled by an external source, the J2 header should be left floating, and the control source should be connected to the EN test point (TP5). The maximum recommended voltage on the EN pin is 5.5 V.

$$R_{ENHS} = \frac{R_{ENLS} \times V_{start}}{V_{ENH}} - R_{ENLS} \tag{1}$$

$$R_{ENHS} = \frac{10\ k\Omega \times 3.7\ V}{1.22\ V} - 10\ k\Omega = 20\ k\Omega \tag{2}$$

3.4 J5 - Switching Frequency and Operating Mode

A jumper on the J5 header configures both the switching frequency and operating mode of the TPSM8A29 with a single resistor as described in Table 3-3. The dual functionality of the TPSM8A29 MODE pin reduces BOM count and solution size.

Three switching frequencies (600 kHz, 800 kHz, 1 MHz) allow the user to optimize the tradeoff between efficiency and layout area. Because the TPSM8A29 has a fixed integrated inductor, the designer only needs to choose an appropriate output capacitance to meet their output voltage ripple and transient response requirements.

The TPSM8A29 can operate in either FCCM or auto-skip DCM mode. When operating in FCCM, the switching frequency is fixed for all output load current conditions. Operating in this mode yields the best output voltage ripple and load regulation at low load currents at the expense of reduced light-load efficiency. When operating in auto-skip DCM, the switching frequency is reduced to maintain high efficiency, even for light load conditions. The disadvantage to operating in DCM is that the light-load output ripple may be greater than in FCCM, the load regulation may be slightly reduced, and the non-fixed switching frequency at light loads may not be desirable for some applications requiring low system noise.

Table 3-3. Switching Frequency and Operating Mode Header

J5 Jumper Connection	MODE Pin Connection Description	Switching Frequency (kHz)	Operating Mode
Pins 1 and 2	Shorted to VCC	600	Auto-skip DCM
Pins 3 and 4	AGND through 243 kΩ	800	
Pins 5 and 6	AGND through 121 kΩ	1000	
Pins 7 and 8	AGND through 60.4 kΩ	1000	FCCM
Pins 9 and 10	AGND through 30.1 kΩ	800	
Pins 11 and 12	Shorted to AGND	600	

3.5 J6 - Output Voltage Selection Header

A jumper on the J6 header is used to configure a range of output voltage from 0.8 V to 5 V. Note that while the default maximum output voltage of the EVM is 5 V, the minimum and maximum output voltage can be increased to 0.6 V and 5.5 V, respectively, by changing one of the high-side feedback resistors.

The output voltage is configured with a voltage divider between V_{OUT} and PGND, where the midpoint is connected to the FB pin of the TPSM8A29. On this EVM, the low-side feedback resistor (R_{FB_LS}, R10) is fixed by default at 10 kΩ, and the jumper on J6 changes the high-side feedback resistor (R_{FB_HS}, see Figure 6-1). To calculate the high-side feedback resistor for any valid output voltage (0.6 V to 5.5 V) for this EVM, Equation 3 is used, where R_{FB_HS} is the high-side resistor of the output voltage divider (several options for this EVM, see Figure 6-1), V_{OUT} is the desired output voltage, V_{INTREF} is the internal reference voltage (typical 0.6 V), and R_{FB_LS} is the low-side resistor of the output voltage divider (R10). For high DC accuracy, 1% or better resistors should be used with a temperature coefficient of ±100 ppm/°C or lower.

$$R_{FBHS} = \frac{V_{OUT} - V_{INTREF}}{V_{INTREF}} \times R_{FBLS} \tag{3}$$

$$R_{FBHS} = \frac{V_{OUT} - 0.6V}{0.6V} \times 10\ k\Omega \tag{4}$$

4 Test Point Description

This section explains the test points found on the TPSM8A29EVM, as well as how to use them. Test points that may benefit from further explanation are addressed after Table 4-1.

Table 4-1. Description of Test Points

Test Point	Function	Description
TP1	PGND	Connection to PGND
TP2	VIN_SNS-	Negative side of input voltage sensing point, connected to PGND
TP4	VIN_SNS+	Positive side of input voltage sensing point, connected to V_{IN}
TP5	EN	Enable pin of TPSM8A29 - can be used to monitor the EN voltage, or can be used to connect external EN signal, max 5.5 V. See Section 3.3
TP7	PGND	Connection to PGND
TP11	AGND	Connection to AGND - reference point for TRIP and MODE resistors. AGND connected to PGND through single point, NT1, on bottom of EVM
TP12	SS/REF_IN	Soft-start and reference voltage tracking, max 1.5 V. See Section 4.1
TP13	PGOOD	Open-drain power good status signal. Pulled up to VCC when voltage on FB pin is within limits of correct operation
TP14	VCC	Monitor internal LDO voltage or override internal LDO with external bias for improved efficiency. See Section 4.2
TP15	VSNS-	Negative return signal for remote sensing applications, connected to PGND through cuttable jumper net tie NT1 by default.
TP16	BODE-/VSNS+	Negative connection point for Bode measurements, connected to V_{OUT}
TP17	BODE+	Positive connection point for Bode measurements
TP18	VOUT_SNS+	Positive sense point for V_{OUT} measurements. Do not use to connect to load
TP19	VOUT_SNS-	Negative sense point for V_{OUT} measurements. Do not use to connect to load
TP21	PGND	Connection to PGND

4.1 TP12 - SS/REF_IN

TP12 is connected to the SS/REF_IN pin of the TPSM8A29. Connecting a capacitor to this pin increases the soft-start time of the converter, as described by Equation 5, where C_{SS} is the calculated external soft-start capacitor, in nF, t_{SS} is the desired soft-start time, in ms, 36 has units of µA, and V_{INTREF} is the internal 0.6 V reference voltage. If no soft-start capacitor is used, the minimum internal soft-start time of 1.5 ms typical is used. By default, a soft-start capacitor is not populated on the EVM, though a footprint for one exists on the bottom of the PCB (C12). The maximum recommended soft-start capacitor is 1 µF.

$$C_{SS}\left(nF\right) = \frac{t_{SS}(ms) \times 36\,(\mu A)}{V_{INTREF}(V)} \tag{5}$$

The SS/REF_IN pin can also be used to connect an external bias supply to adjust the control loop voltage reference. The FB pin tracks the voltage on the SS/VREF_IN pin. This can be useful in applications where the output voltage needs to by adjusted dynamically in-circuit. The maximum recommended external supply voltage to the SS/REF_IN pin is 1.5 V.

4.2 TP14 - VCC

TP14 is the VCC test point for the internal LDO. It can be used to monitor the VCC voltage, or it can be used to override the internal LDO of the TPSM8A29 for higher efficiency. Frequently, systems will have an LDO present somewhere in the design which can be used here to reduce the power losses associated with producing a low-noise supply rail with a linear regulator. The internal LDO produces a typical voltage of 4.5 V, so the recommended input range for an external bias on the VCC pin is 4.75 V to 5.3 V. Because of the limited sourcing current capability of the internal LDO, do not connect any external loading to this pin.

5 Test Setup and Results

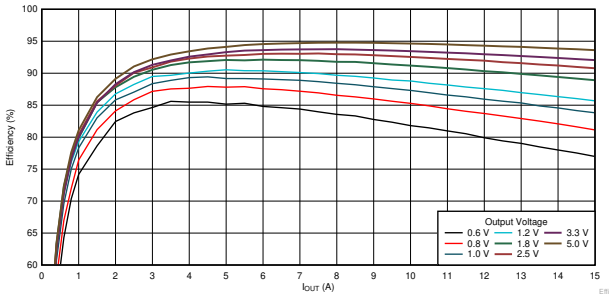
This section describes how to properly connect, set up, and use the TPSM8A29EVM. This section also includes test results typical for the evaluation module and covers efficiency, load regulation, line regulation, output voltage ripple, startup and shutdown waveforms, transient response, and frequency response.

5.1 Startup Procedure

1. Make sure EN jumper is in the ON position.
2. (Optional) Apply appropriate external bias voltage between VCC (TP14) and PGND test points. If no external bias, please go directly to next step. The external bias range is 4.7 V to 5.3 V.
3. Select desired output voltage using J6 header.
4. Select desired operating mode and frequency using J5 header.
5. Connect input power supply positive and negative to J1 VIN and PGND, respectively. If used, connect power supply remote sense connections to VIN_SNS+ and VIN_SNS- test points. The input voltage range is 4 V to 16 V.
6. Connect external load to J4 VOUT and J7 PGND. The output voltage can be monitored using TP18 and TP19.
7. Turn on input power supply.

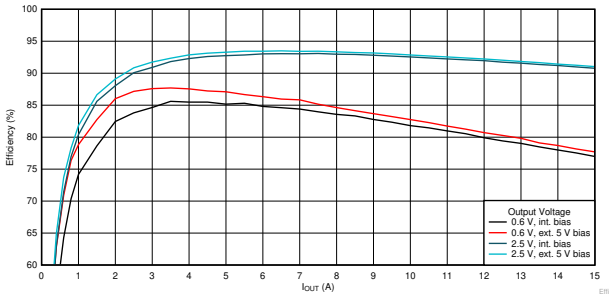
5.2 Efficiency

This section presents efficiency data for several conditions. Unless stated otherwise, all measurements were taken at an ambient temperature of 25°C.



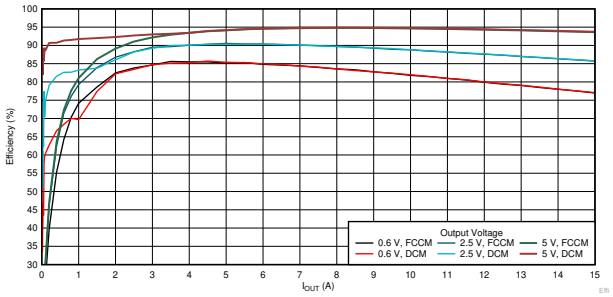
V_{IN} = 12 V f_{sw} = 600 kHz Internal bias FCCM

Figure 5-1. Efficiency, V_{OUT} = 0.6 V to 5.0 V



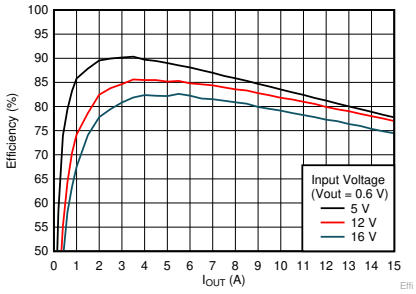
V_{IN} = 12 V f_{sw} = 600 kHz Int. vs. ext. 5 V bias FCCM

Figure 5-2. Efficiency, V_{OUT} = 0.6 V and 2.5 V



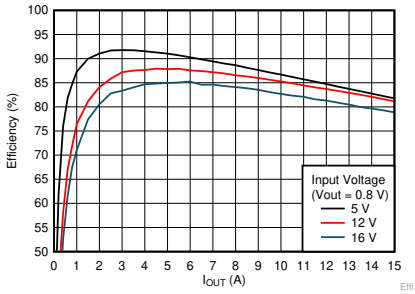
V_{IN} = 12 V f_{sw} = 600 kHz Internal bias FCCM vs. DCM

Figure 5-3. Efficiency, V_{OUT} = 0.6 V, 2.5 V, and 5 V



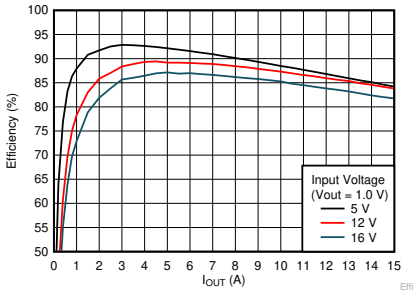
V_{IN} = 12 V f_{sw} = 600 kHz Internal bias FCCM

Figure 5-4. Efficiency, V_{OUT} = 0.6 V



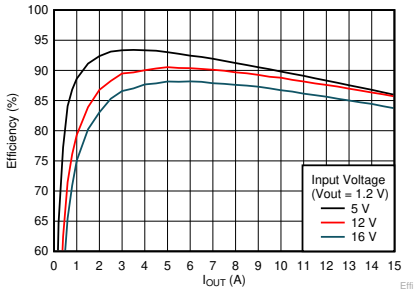
V_{IN} = 12 V f_{sw} = 600 kHz Internal bias FCCM

Figure 5-5. Efficiency, V_{OUT} = 0.8 V



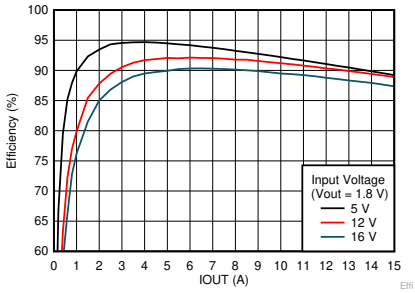
V_{IN} = 12 V f_{sw} = 600 kHz Internal bias FCCM

Figure 5-6. Efficiency, V_{OUT} = 1.0 V



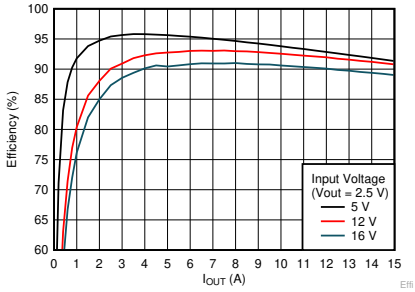
V_{IN} = 12 V f_{sw} = 600 kHz Internal bias FCCM

Figure 5-7. Efficiency, V_{OUT} = 1.2 V



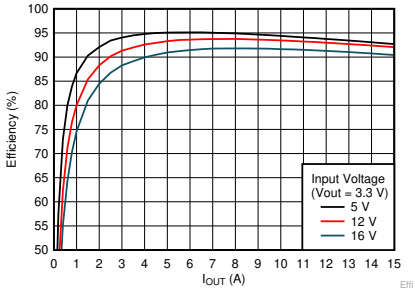
V_{IN} = 12 V f_{sw} = 600 kHz Internal bias FCCM

Figure 5-8. Efficiency, V_{OUT} = 1.8 V



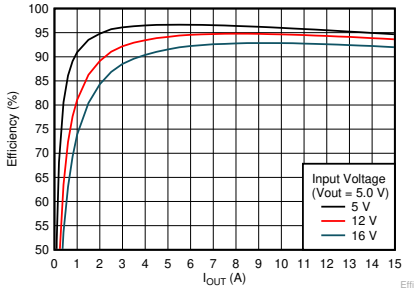
V_{IN} = 12 V f_{sw} = 600 kHz Internal bias FCCM

Figure 5-9. Efficiency, V_{OUT} = 2.5 V



V_{IN} = 12 V f_{sw} = 600 kHz Internal bias FCCM

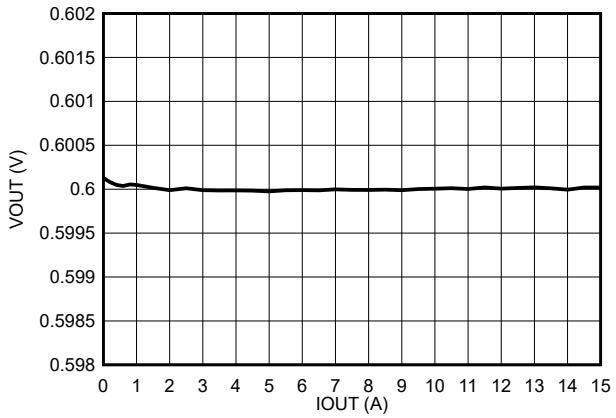
Figure 5-10. Efficiency, V_{OUT} = 3.3 V



V_{IN} = 12 V f_{sw} = 600 kHz Internal bias FCCM

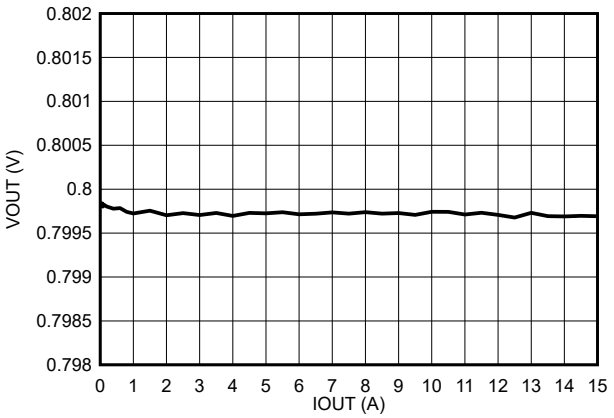
Figure 5-11. Efficiency, V_{OUT} = 5.0 V

5.3 Load Regulation



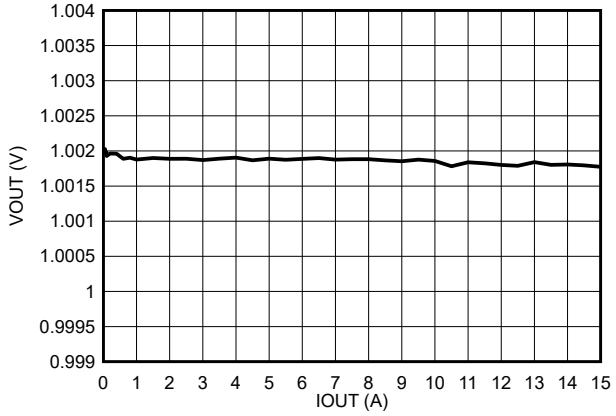
V_{IN} = 12 V f_{sw} = 600 kHz Internal bias FCCM

Figure 5-12. Load Regulation, V_{OUT} = 0.6 V



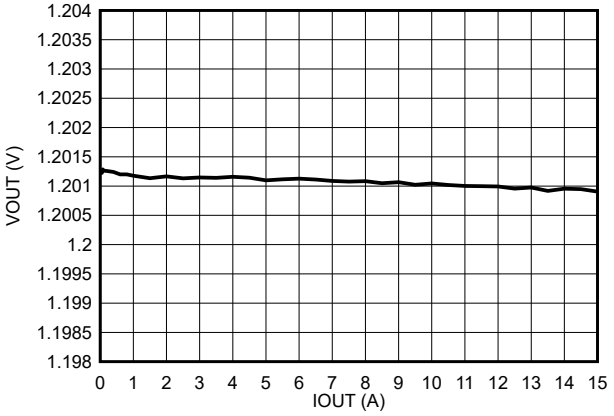
V_{IN} = 12 V f_{sw} = 600 kHz Internal bias FCCM

Figure 5-13. Load Regulation, V_{OUT} = 0.8 V



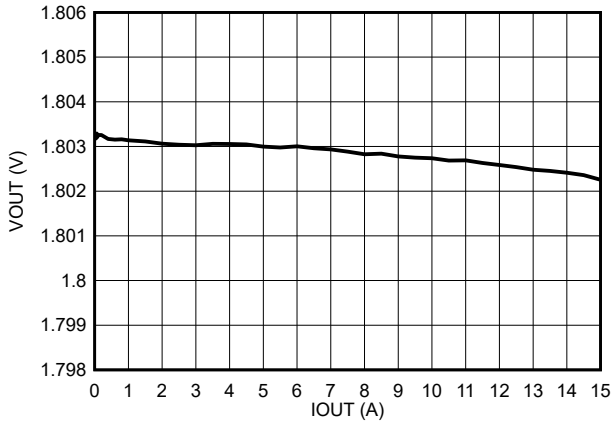
V_{IN} = 12 V f_{sw} =600 kHz Internal bias FCCM

Figure 5-14. Load Regulation, V_{OUT} = 1.0 V



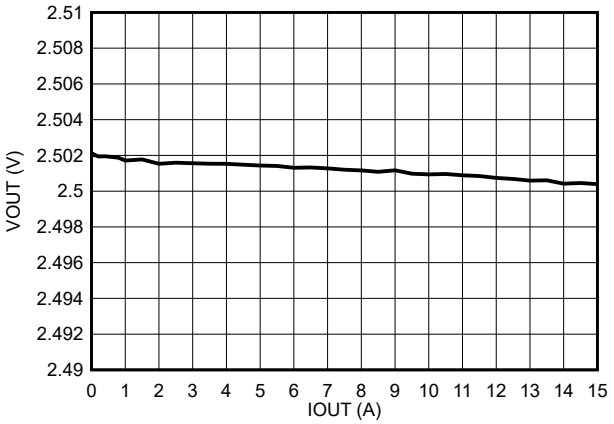
V_{IN} = 12 V f_{sw} = 600 kHz Internal bias FCCM

Figure 5-15. Load Regulation, V_{OUT} = 1.2 V



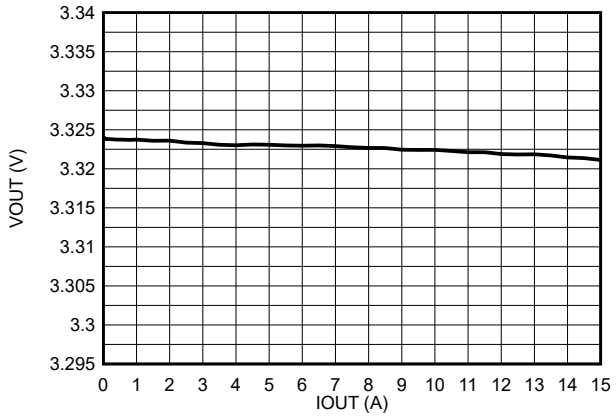
V_{IN} = 12 V f_{sw} =600 kHz Internal bias FCCM

Figure 5-16. Load Regulation, V_{OUT} = 1.8 V



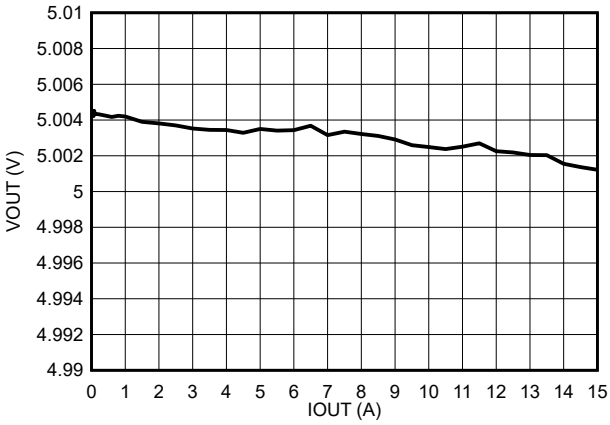
V_{IN} = 12 V f_{sw} = 600 kHz Internal bias FCCM

Figure 5-17. Load Regulation, V_{OUT} = 2.5 V



V_{IN} = 12 V f_{sw} = 600 kHz Internal bias FCCM

Figure 5-18. Load Regulation, V_{OUT} = 3.3V

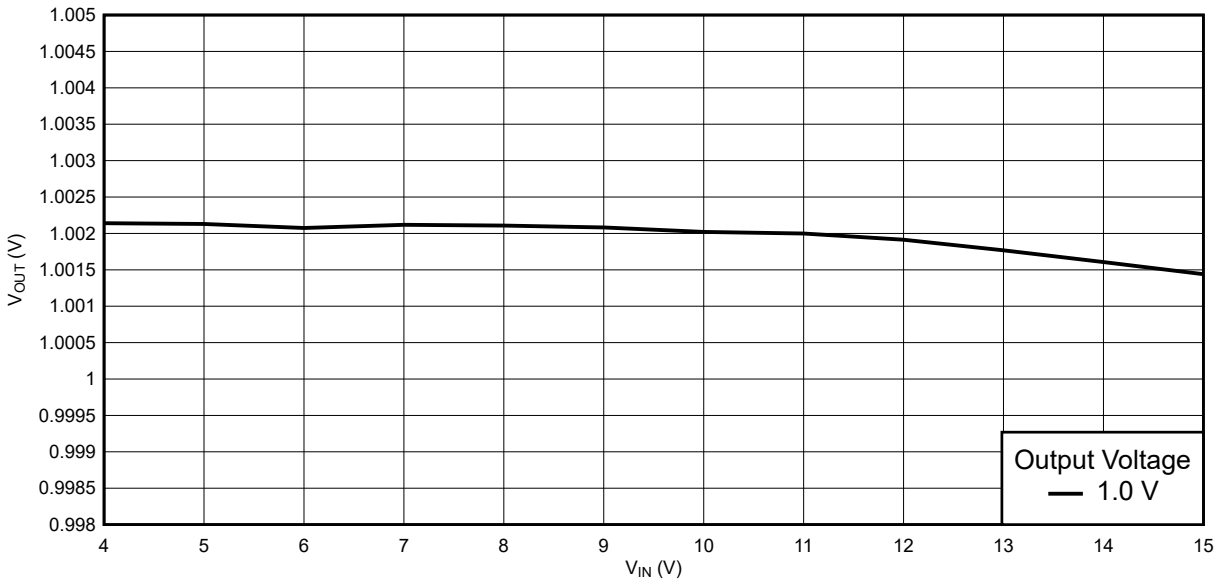


V_{IN} = 12 V f_{sw} = 600 kHz Internal bias FCCM

Figure 5-19. Load Regulation, V_{OUT} = 5.0 V

5.4 Line Regulation

V_{IN} = 12 V, V_{OUT} = 1.0 V, C_{OUT} = 8x47 µF (6)



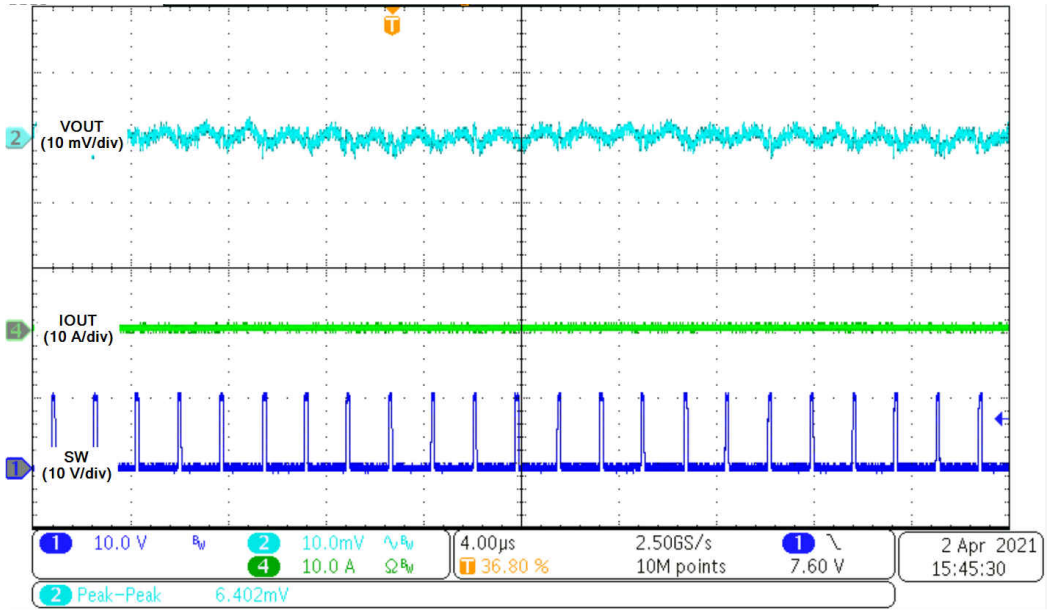
V_{IN} = 12 V I_{OUT} = 5 A f_{sw} = 600 kHz Internal bias FCCM

Figure 5-20. Line regulation, V_{OUT} = 1.0 V

5.5 Output Voltage Ripple

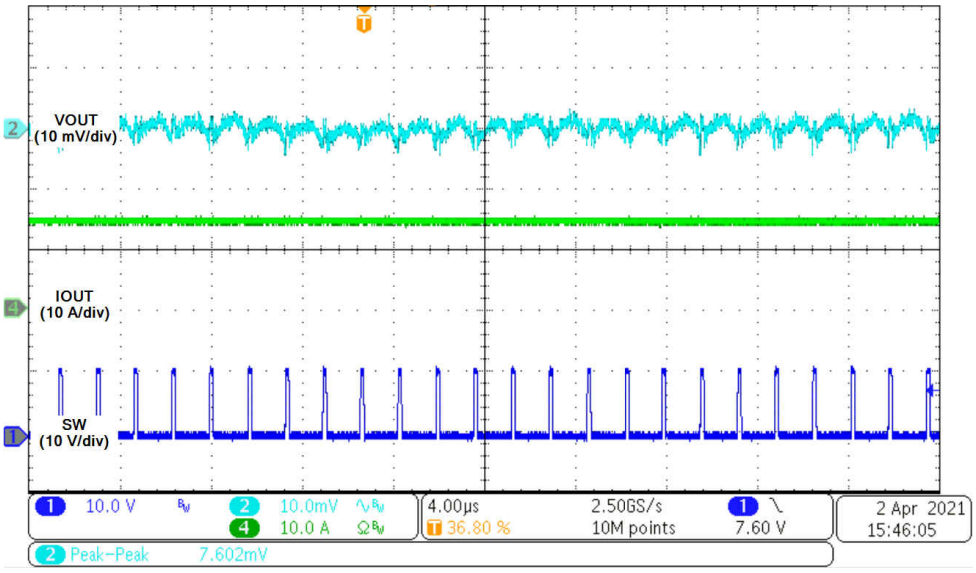
This section contains oscilloscope images showing the output voltage ripple under various load and FCCM/DCM conditions. All images taken at 25°C.

V_{IN} = 12 V, V_{OUT} = 1.0 V, C_{OUT} = 8x47 µF (7)



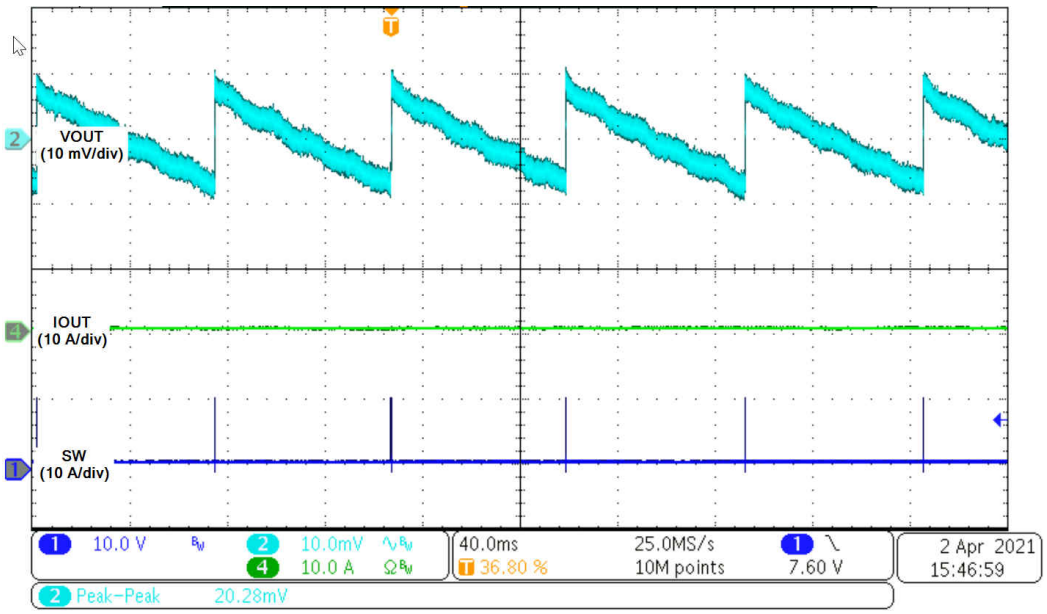
V_{IN} = 12 V I_{OUT} = 0 A f_{sw} = 600 kHz Internal bias FCCM

Figure 5-21. Output Ripple, V_{OUT} = 1.0 V, V_{RIPPLE} = 6.4 mV



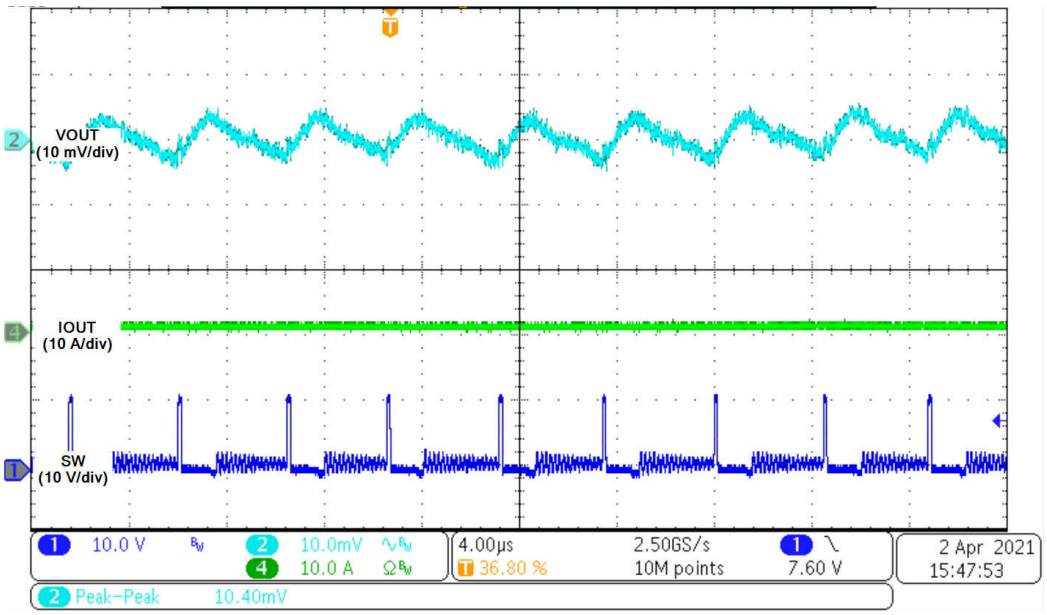
V_{IN} = 12 V I_{OUT} = 15 A f_{sw} = 600 kHz Internal bias FCCM

Figure 5-22. Output Ripple, V_{OUT} = 1.0 V, V_{RIPPLE} = 7.6 mV



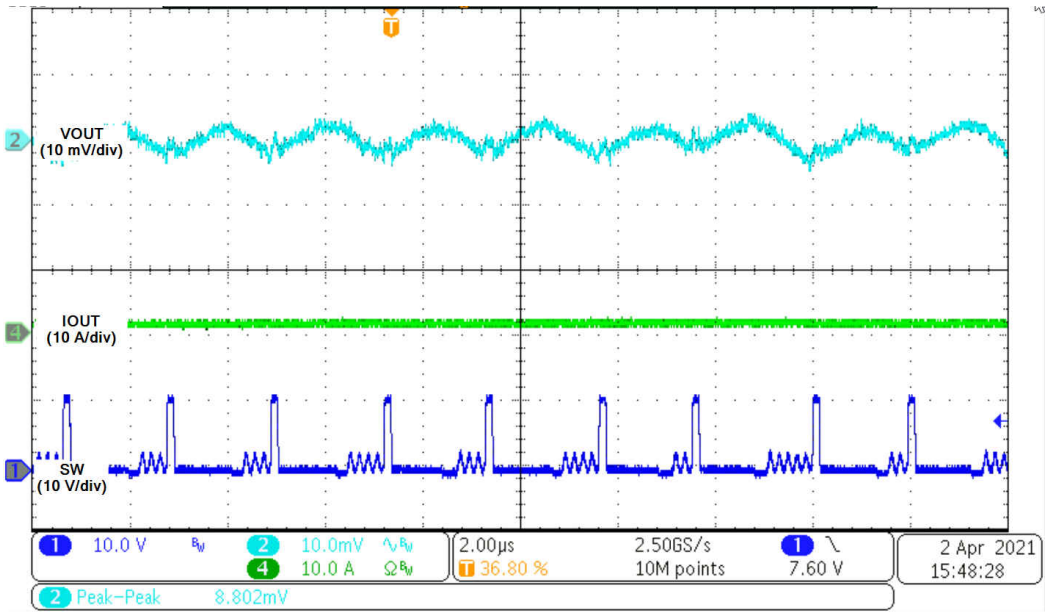
V_{IN} = 12 V I_{OUT} = 0 A f_{sw} = 600 kHz Internal bias DCM

Figure 5-23. Output Ripple, V_{OUT} = 1.0 V, V_{RIPPLE} = 20.3 mV



V_{IN} = 12 V I_{OUT} = 0.5 A f_{sw} = 600 kHz Internal bias DCM

Figure 5-24. Output Ripple, V_{OUT} = 1.0 V, V_{RIPPLE} = 10.4 mV



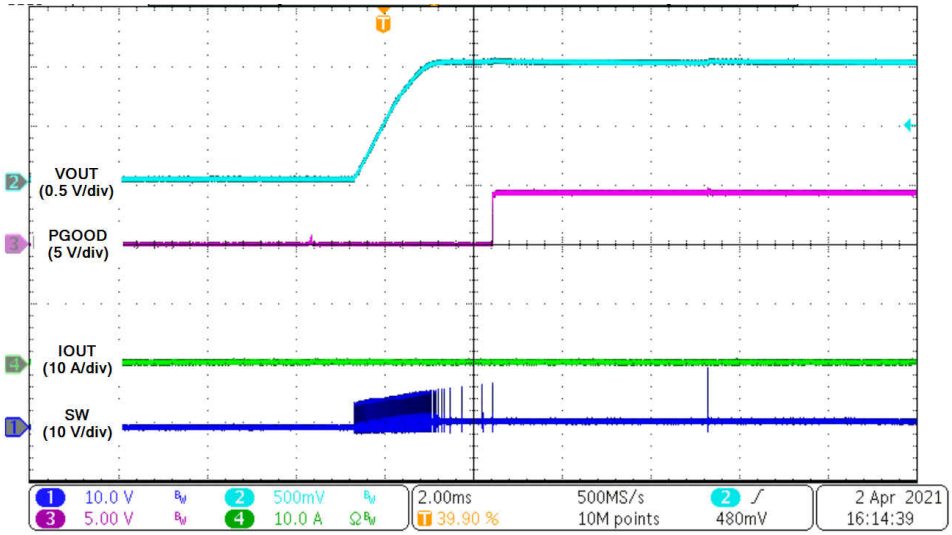
V_{IN} = 12 V I_{OUT} = 1 A f_{sw} = 600 kHz Internal bias DCM

Figure 5-25. Output Ripple, V_{OUT} = 1.0 V, V_{RIPPLE} = 8.8 mV

5.6 Startup and Shutdown

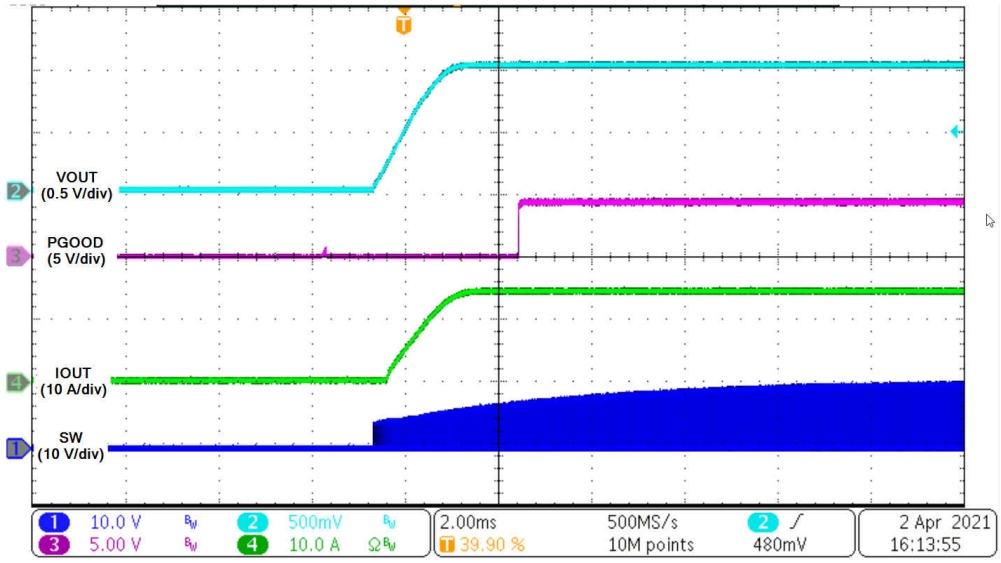
This section contains oscilloscope images showing the startup and shutdown behavior of the TPSM8A29 under different load conditions. All images were taken at 25°C.

V_{IN} = 12 V, V_{OUT} = 1.0 V, C_{OUT} = 8x47 µF (8)



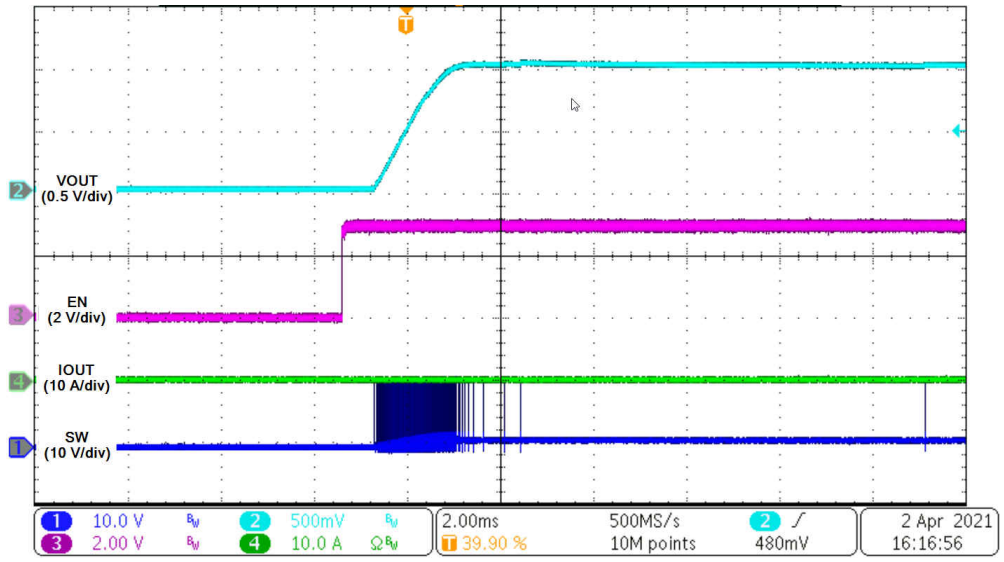
V_{IN} = 12 V I_{OUT} = 0 A f_{sw} = 600 kHz Internal bias DCM

Figure 5-26. Startup Through V_{IN} (enable floating), 0 A load



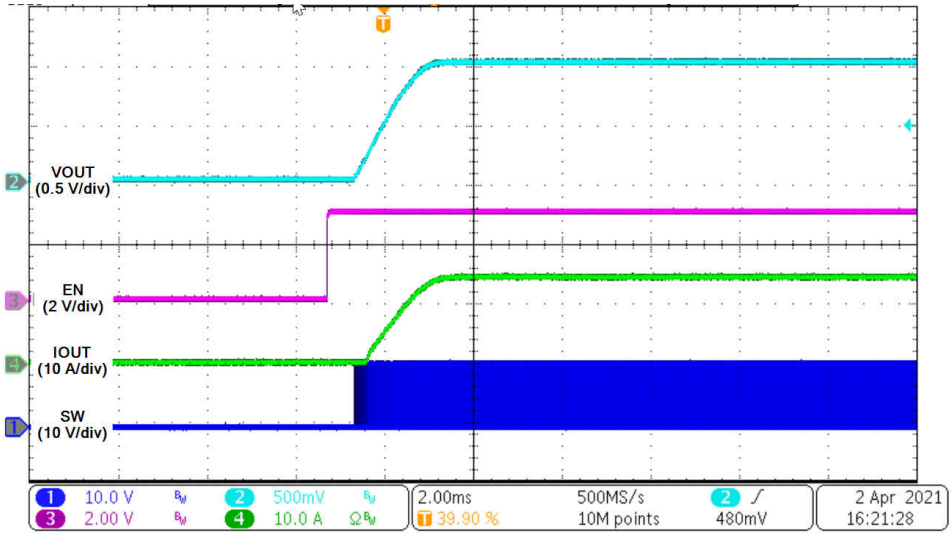
V_{IN} = 12 V I_{OUT} = 15 A f_{sw} = 600 kHz Internal bias FCCM

Figure 5-27. Startup Through V_{IN} (enable floating), 15 A load



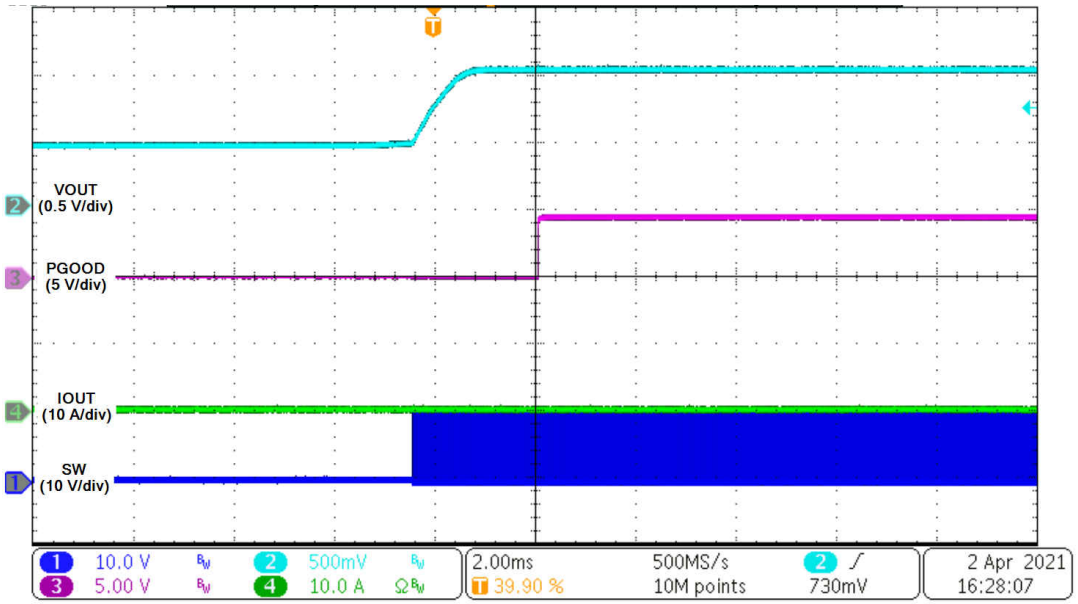
V_{IN} = 12 V I_{OUT} = 0 A f_{sw} = 600 kHz Internal bias DCM

Figure 5-28. Startup Through Enable, 0 A load



V_{IN} = 12 V I_{OUT} = 15 A f_{sw} = 600 kHz Internal bias FCCM

Figure 5-29. Startup Through Enable, 15 A load

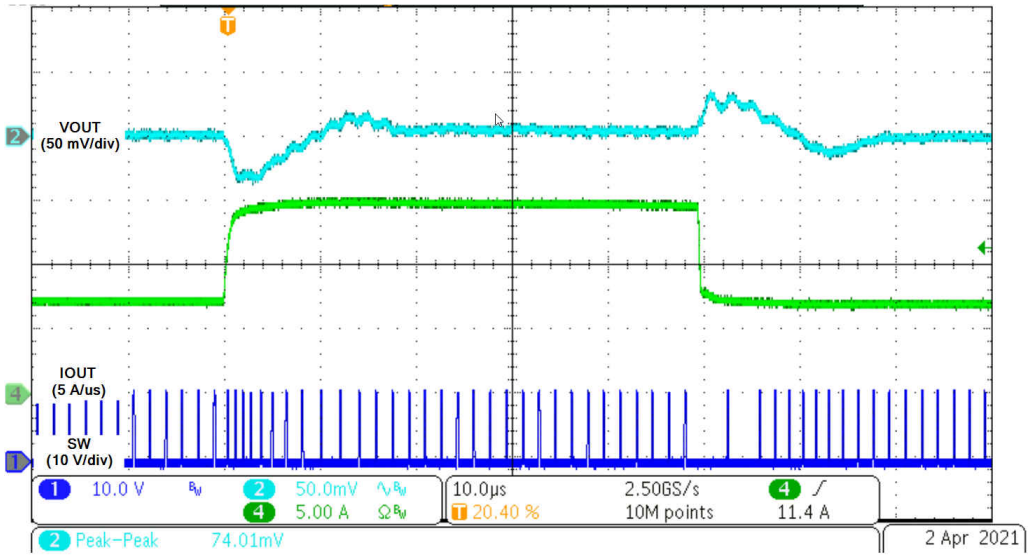


V_{IN} = 12 V I_{OUT} = 0 A f_{sw} = 600 kHz Internal bias FCCM

Figure 5-30. Startup Through Enable Into Prebiased Output ($V_{OUT, PREBIAS}$ = 0.5 V)

5.7 Load Transient

V_{IN} = 12 V, V_{OUT} = 1.0 V, C_{OUT} = 8x47 µF (9)

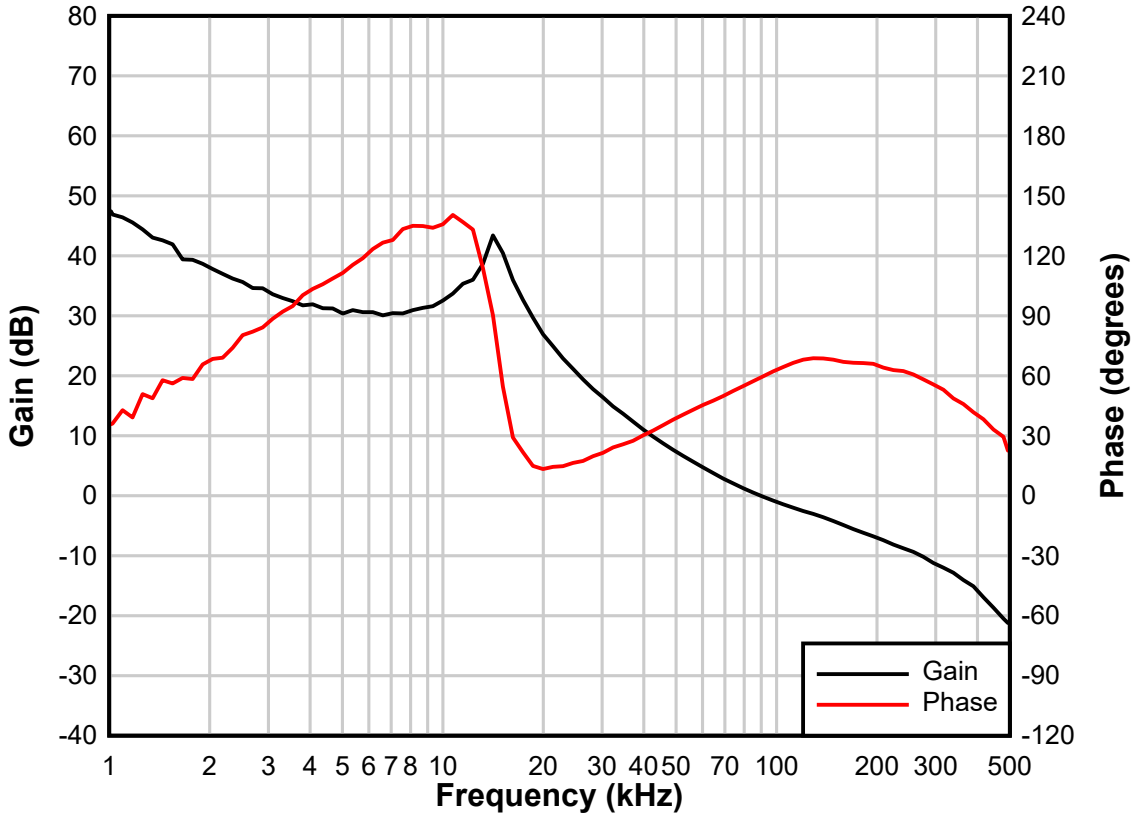


V_{IN} = 12 V I_{STEP} = 7.5 A-15 A-7.5 A f_{sw} = 600 kHz Internal bias FCCM

Figure 5-31. Load Transient, 7.5 A step, 10 µs/div, V_{TRANS} = 74 mV

5.8 Bode Plot

V_{IN} = 12 V, V_{OUT} = 1.0 V, C_{OUT} = 8x47 µF (10)



V_{IN} = 12 V I_{OUT} = 15 A f_{sw} = 600 kHz Internal bias FCCM

Figure 5-32. Bode Plot, V_{OUT} = 1 V, I_{OUT} = 15 A

6 TPSM8A29EVM Schematic

The schematic for the default TPSM8A29EVM is shown in Figure 6-1. Note that many components are not populated to allow for flexibility for testing designs with a wide range of performance requirements.

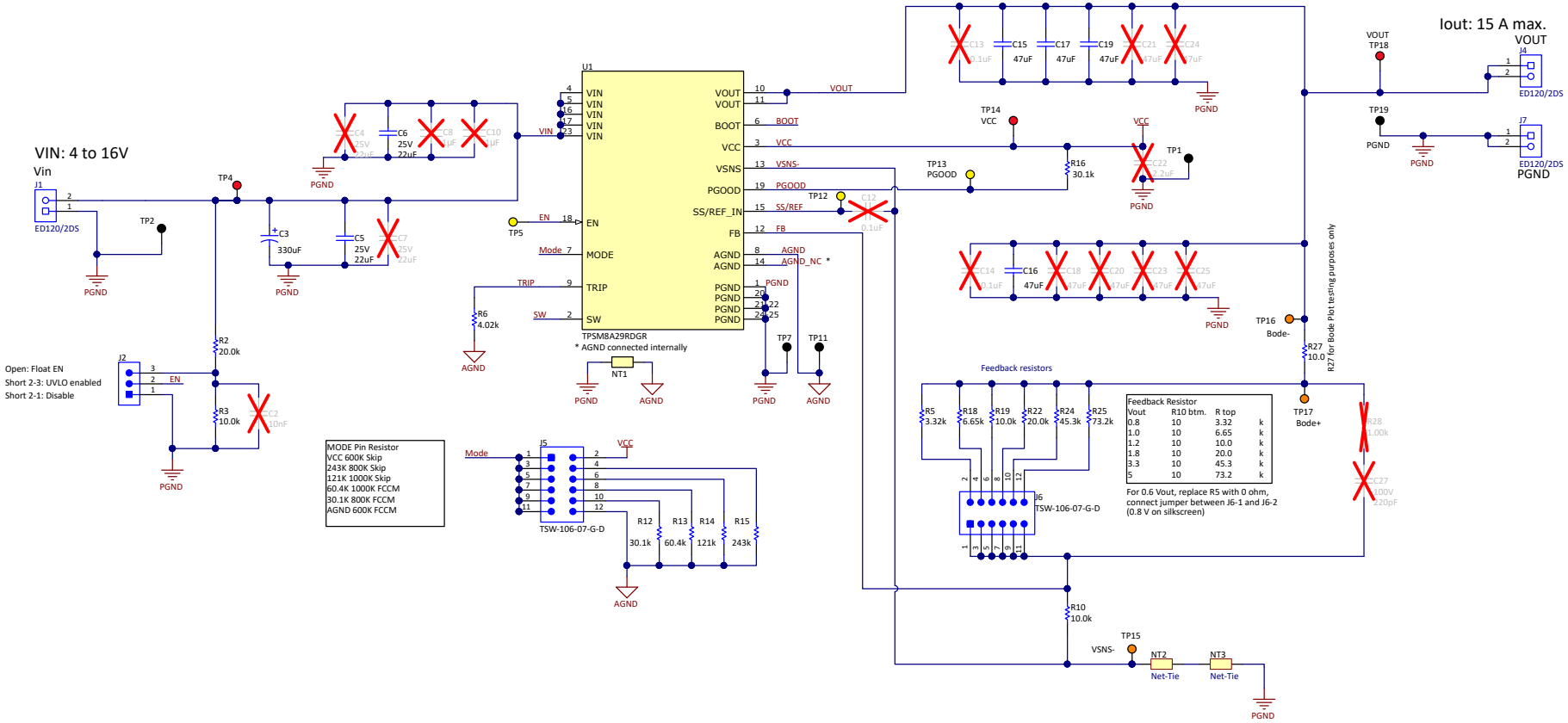


Figure 6-1. TPSM8A29EVM Schematic

7 TPSM8A29EVM PCB Layers

This section contains the composite views of the top and bottom layer (copper and silkscreen), as well as the copper views of all layers.

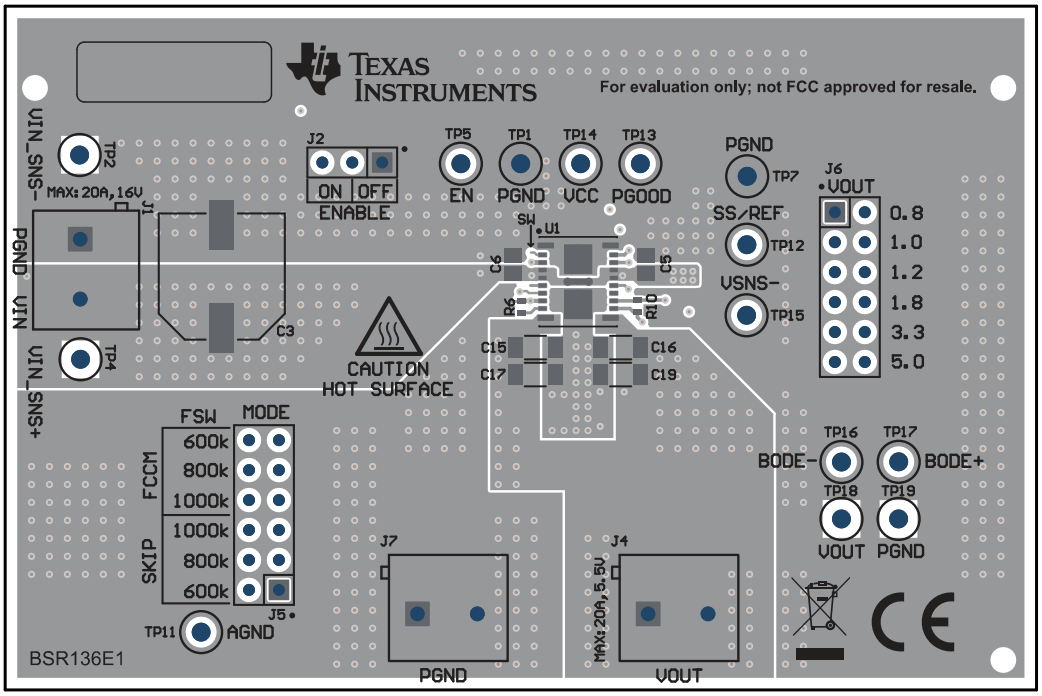


Figure 7-1. TPSM8A29EVM Top Layer Composite View

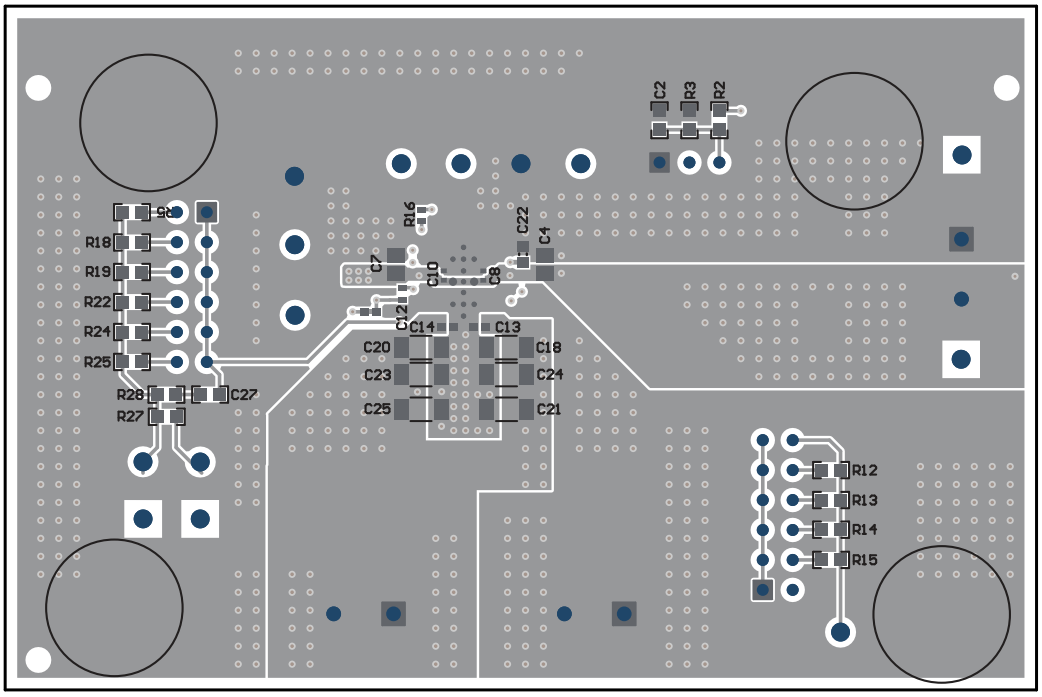


Figure 7-2. TPSM8A29EVM Bottom Layer Composite View

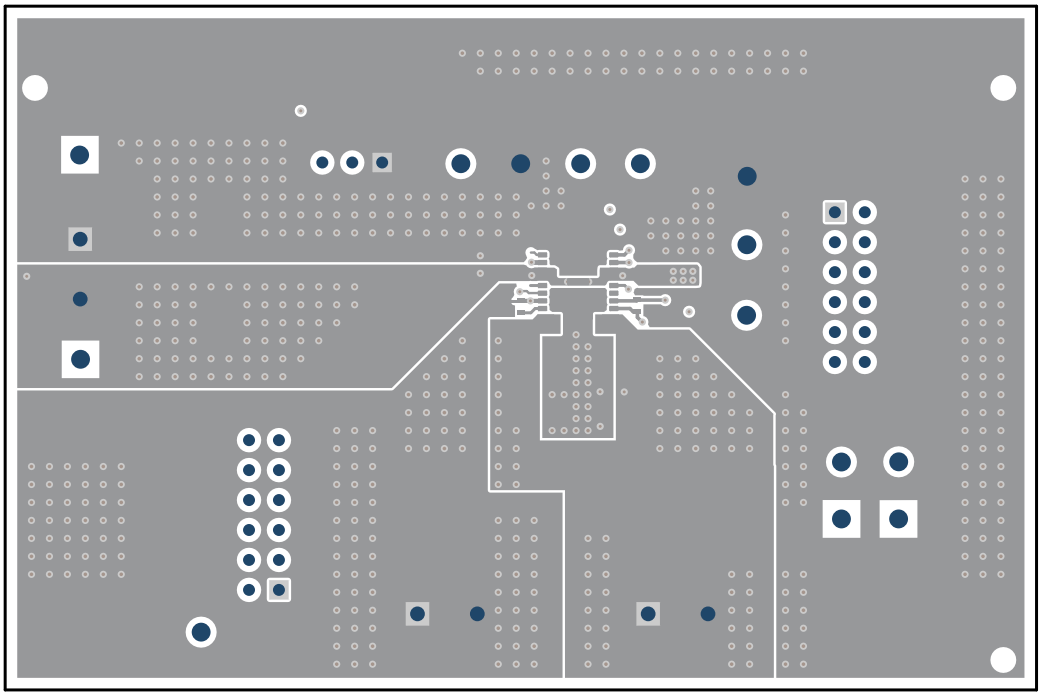


Figure 7-3. TPSM8A29EVM Top Layer Copper, Top-Down View

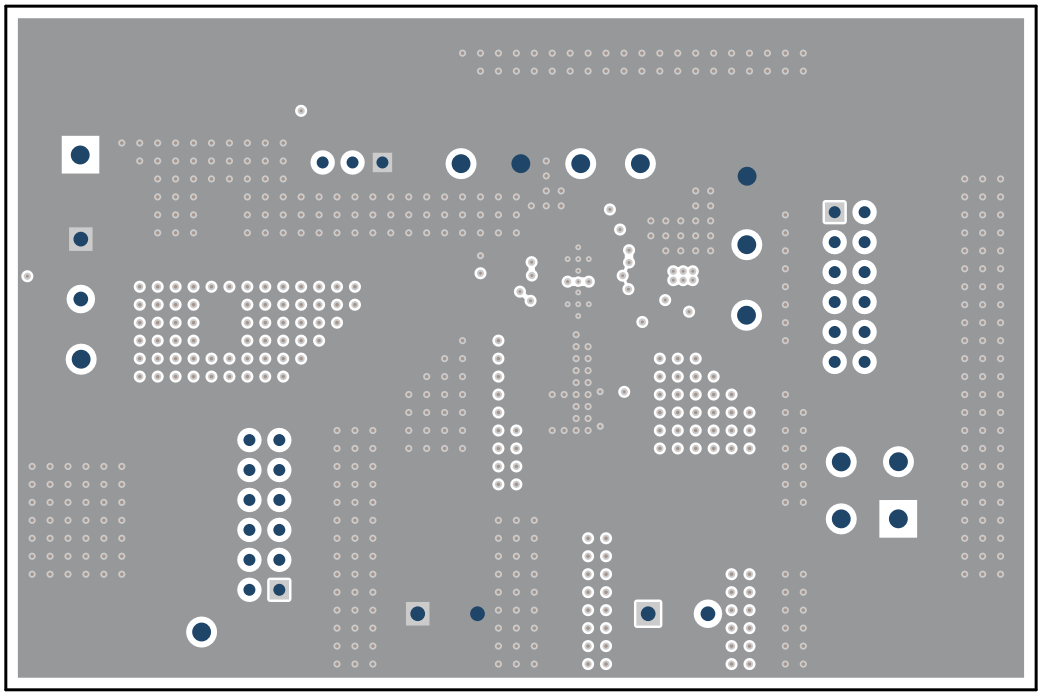


Figure 7-4. TPSM8A29EVM Inner Layer 1 Copper, Top-Down View

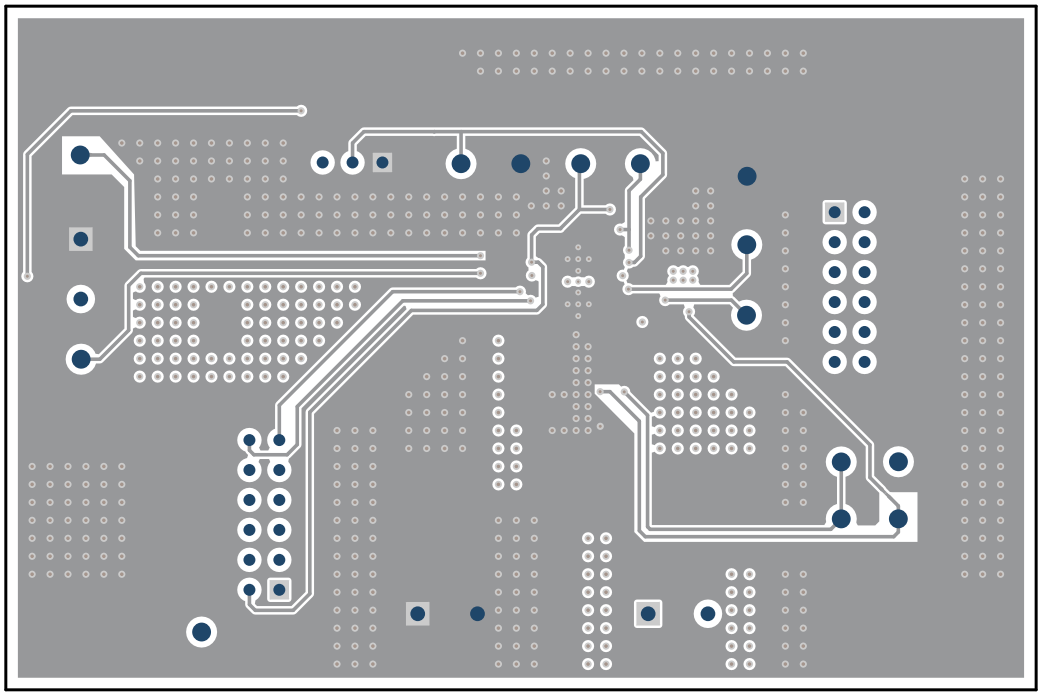


Figure 7-5. TPSM8A29EVM Inner Layer 2 Copper, Top-Down View

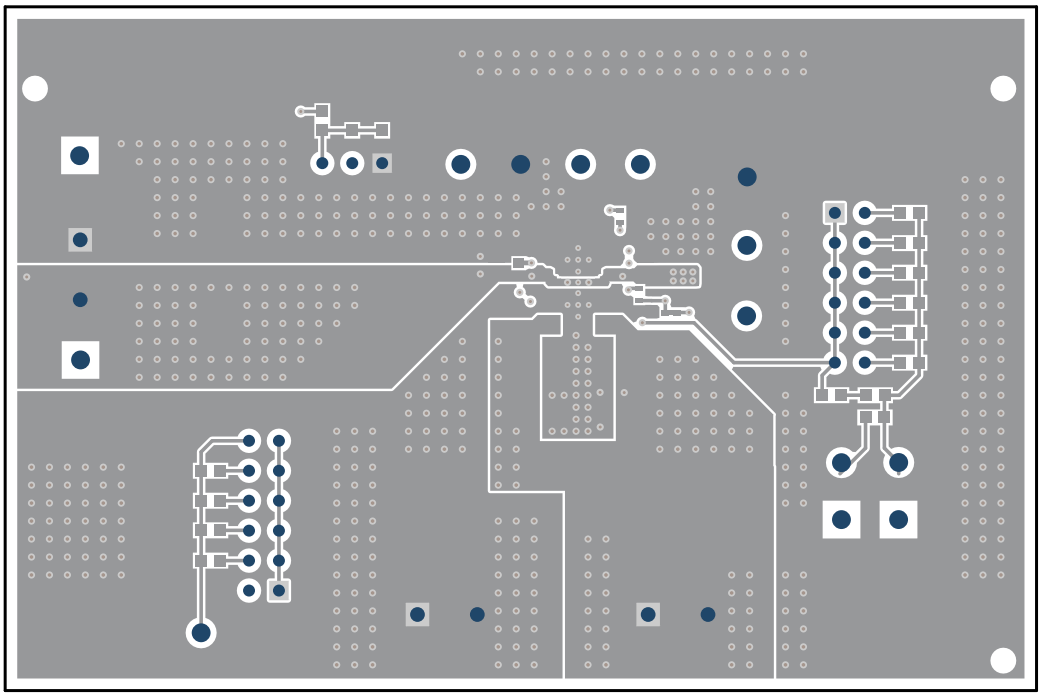


Figure 7-6. TPSM8A29EVM Bottom Layer Copper, Top-Down View

8 TPSM8A29EVM Bill of Materials

A complete bill of materials (BOM) is shown in TPSM8A29EVM Bill of Materials. Resistors may be substituted as required so long as tolerance and temperature coefficients are considered. Capacitors may be substituted as required so long as dielectric, voltage ratings, and derating are considered. TI makes no guarantees about component availability.

Table 8-1. TPSM8A29EVM Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		BSR136	Any
C3	1	330uF	CAP, AL, 330 uF, 25 V, +/- 20%, 0.15 ohm, SMD	SMT Radial G	EEE-FC1E331P	Panasonic
C5, C6	2	22uF	CAP, CERM, 22 uF, 25 V, +/- 20%, X5R, 0805	0805	GRM21BR61E226ME44L	MuRata
C15, C16, C17, C19	4	47uF	CAP, CERM, 47 uF, 6.3 V, +/- 10%, X6S, 1206	1206	GRM31CC80J476KE18L	MuRata
H1, H2, H3, H4	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
J1, J4, J7	3		Terminal Block, 5.08 mm, 2x1, Brass, TH	2x1 5.08 mm Terminal Block	ED120/2DS	On-Shore Technology
J2	1		Header, 100mil, 3x1, Gold, TH	Header, 100mil, 3x1, TH	HTSW-103-07-G-S	Samtec
J5, J6	2		Header, 100mil, 6x2, Gold, TH	6x2 Header	TSW-106-07-G-D	Samtec
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
R2	1	20.0k	RES, 20.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060320K0FKEA	Vishay-Dale
R3	1	10.0k	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310K0FKEA	Vishay-Dale
R5	1	3.32k	RES, 3.32 k, 1%, 0.1 W, 0603	0603	RC0603FR-073K32L	Yageo
R6	1	4.02k	RES, 4.02 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04024K02FKED	Vishay-Dale

Table 8-1. TPSM8A29EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R10	1	10.0k	RES, 10.0 k, 1%, 0.063 W, 0402	0402	RC0402FR-0710KL	Yageo America
R12	1	30.1k	RES, 30.1 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060330K1FKEA	Vishay-Dale
R13	1	60.4k	RES, 60.4 k, 1%, 0.1 W, 0603	0603	RC0603FR-0760K4L	Yageo
R14	1	121k	RES, 121 k, 1%, 0.1 W, 0603	0603	RC0603FR-07121KL	Yageo
R15	1	243k	RES, 243 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603243KFKEA	Vishay-Dale
R16	1	30.1k	RES, 30.1 k, 1%, 0.063 W, 0402	0402	RC0402FR-0730K1L	Yageo America
R18	1	6.65k	RES, 6.65 k, 1%, 0.1 W, 0603	0603	RC0603FR-076K65L	Yageo
R19	1	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo
R22	1	20.0k	RES, 20.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0720KL	Yageo
R24	1	45.3k	RES, 45.3 k, 1%, 0.1 W, 0603	0603	RC0603FR-0745K3L	Yageo
R25	1	73.2k	RES, 73.2 k, 1%, 0.1 W, 0603	0603	RC0603FR-0773K2L	Yageo
R27	1	10.0	RES, 10.0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310R0FKEA	Vishay-Dale
SH-J1, SH-J2, SH-J3	3	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TP1, TP2, TP7, TP11, TP19	5		Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint	5011	Keystone
TP4, TP14, TP18	3		Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint	5010	Keystone
TP5, TP12, TP13	3		Test Point, Compact, Yellow, TH	Yellow Compact Testpoint	5009	Keystone

Table 8-1. TPSM8A29EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
TP15, TP16, TP17	3		Test Point, Multipurpose, Orange, TH	Orange Multipurpose Testpoint	5013	Keystone
U1	1		Justin Junior Power Module, 16V, 12A, DC-DC buck converter	QFN-FCMOD	TPSM8A29RDGR	Texas Instruments
C2	0	0.01uF	CAP, CERM, 0.01 uF, 16 V, +/- 10%, X7R, 0603	0603	885012206040	Wurth Elektronik
C4, C7	0	22uF	CAP, CERM, 22 uF, 25 V, +/- 20%, X5R, 0805	0805	GRM21BR61E226ME44L	MuRata
C8, C10	0		CAP CER 1UF 25V X6S 0402	0402	GRM155C81E105KE11D	Murata
C12, C13, C14	0	0.1uF	CAP, CERM, 0.1 uF, 6.3 V, +/- 10%, X7R, 0402	0402	GRM155R70J104KA01D	MuRata
C18, C20, C21, C23, C24, C25	0	47uF	CAP, CERM, 47 uF, 6.3 V, +/- 10%, X6S, 1206	1206	GRM31CC80J476KE18L	MuRata
C22	0	2.2uF	CAP, CERM, 2.2 uF, 10 V, +/- 10%, X7R, 0603	0603	GRM188R71A225KE15D	MuRata
C27	0	220pF	CAP, CERM, 220 pF, 100 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C2A221JA01D	MuRata
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
R28	0	1.00k	RES, 1.00 k, 1%, 0.1 W, 0603	0603	RC0603FR-071KL	Yageo

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2021) to Revision A (January 2022)	Page
• Updated user's guide title	3

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