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eFuse, 4 Channel, 60 V, 2.5 A

NIS3071, NIV3071

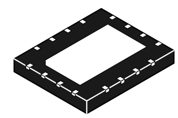
The NIS/NIV3071 is a 4−channel, 60 V, 2.5 A per channel eFuse which protects downstream loads from output shorts, overloads and overcurrent events. Each channel is in a high−side configuration, and is independently controlled by its corresponding enable pins. The NIS/NIV3071 communicates status via a common active−low fault pin. This eFuse features an internal soft start delay, trip time control, and an adjustable current limit setting common to all channels. The NIS3071 is well suited for industrial and telecom applications while the NIV3071 is for automotive applications.

Features

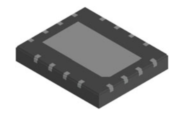
- 4 Independent Channels with 2.5 A Current Capability Each
- Power Device Thermally Protected for Each Channel
- No External Current Shunt Required
- Active−High Digital Enable Pin
- Open−Drain Common Fault Pin
- Adjustable Overcurrent Limit for All Channels
- Adjustable Turn−on Time Control
- NIV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Automotive Body Control Modules
- Power Distribution Box
- Automotive Zonal Controllers
- Load/Harness Protection
- Automotive Low−Medium Power Loads
- General Purpose High−Side Load Switch
- Power Amplifier Protection
- Motor Drive Protection
- Telecomm Equipment
- 8 V to 60 V Industrial

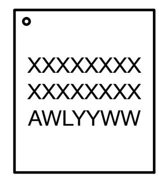


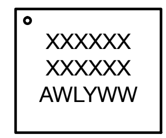
WQFN16, 6x5
CASE 510CM



WQFNW16, 6x5
CASE 512AN

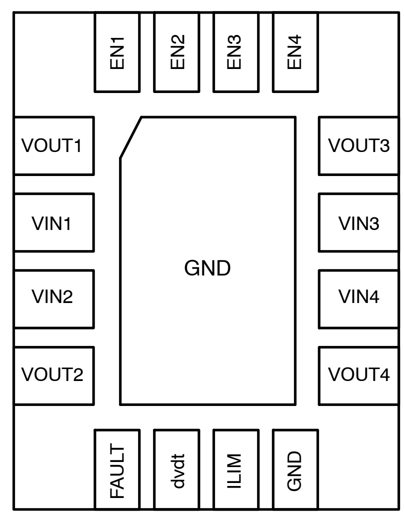
MARKING DIAGRAMS





XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

Table 1. PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	OUT1	Output voltage for channel 1
2	IN1	Input voltage for channel 1
3	IN2	Input voltage for channel 2
4	OUT2	Output voltage for channel 2
5	FAULT	Active Low Open−Drain FAULT pin (Pull up to 5 V, 3.3 V or 1.8 V external logic supply with 15 kΩ resistor)
6	dvdt	Turn−on Time/inrush current control (connect capacitor to ground to control output slew rate)
7	ILIM	Connect R_{LIM} resistor to GND to set current limit for all channels
8	GND	Ground
9	OUT4	Output voltage for channel 4
10	IN4	Input voltage for channel 4
11	IN3	Input voltage for channel 3
12	OUT3	Output voltage for channel 3
13	EN4	Channel 4 Enable, Active High, Internal Pull−up
14	EN3	Channel 3 Enable, Active High, Internal Pull−up
15	EN2	Channel 2 Enable, Active High, Internal Pull−up
16	EN1	Channel 1 Enable, Active High, Internal Pull−up
PAD	GND	Ground

Table 2. ABSOLUTE MAXIMUM RATINGS AND THERMAL RATINGS

Rating	Symbol	Value	Unit
IN1,2,3,4 Pins Input Voltage, operating, steady−state (V_{INx}, V_{OUTx} to GND, Note 1)	$V_{IN(Max)}$	−0.3 to 60	V
Absolute Maximum Transient voltage on IN1,2,3,4 pins (Note 2)	$V_{IN(Tran)}$	65	V
Maximum DC voltage on EN pin	$V_{EN(Max)}$	−0.3 to 6	V
Thermal Resistance, Junction−to−Air JEDEC JESD51−5 JEDEC JESD51−7 0.5 in^2 copper (Note 3)	θ_{JA}	 32.1 56.8 24.0	°C/W
Thermal Resistance, Junction−to−Lead	θ_{JL}	0.5	°C/W
Operating Junction Temperature Range (Note 4)	T_J	−40 to 150	°C
Non−operating Junction Temperature Range	T_J	−50 to 155	°C
Lead Temperature, Soldering (10 sec)	T_L	260	°C
ESD Human Body Model ANSI/ESDA/JEDEC JS−001 Class 2	ESD_{HBM}	2.0	kV
ESD Charged Device Model AEC Standard Q100−01 (JESD22−C101E)	ESD_{CDM}	1.0	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Negative voltage will not damage device provided that the power dissipation is limited to the rated allowable power for the package.
2. Transient Voltage pulse duration ≤ 100 μs.
3. Based on thermal models using the NIS/NIV3071 EVB.
4. Thermal limit is set above the maximum thermal rating. It is not recommended to operate this device at temperatures greater than maximum ratings for extended periods of time.

Table 3. ELECTRICAL CHARACTERISTICS
(Unless otherwise noted: V_{IN} = 48 V, C_{IN} = 100 μF, C_{OUT} = 100 μF, dV/dt pin open, R_{LIM} = 20 kΩ, T_A = 25°C)

Characteristics	Symbol	Min	Typ	Max	Unit
POWER FET					
ON Resistance per channel, T_J = 25°C	$R_{DS(ON)}$		80	92	mΩ
ON Resistance per channel, T_J = 150°C	$R_{DS(ON)}$		135	155	
Continuous Current per channel (T_A = 100°C, single channel)	$I_{D(Cont)}$		2.5*		A
Off State Leakage per channel (V_{IN} = 48 V, V_{EN} = 0 V)	I_{OFF}		1.0		μA
THERMAL LATCH					
Shutdown Temperature	T_{SD}		175		°C
Thermal Hysteresis (Decrease in die temperature for turn on)	T_{Hyst}		27		°C
OVERCURRENT PROTECTION					
Minimum Settable Current Limit (R_{LIM} = 130 kΩ) MTW3, MTW4 versions	$I_{TH(Min)}$		0.5		A
Minimum Settable Current Limit (R_{LIM} = 300 kΩ) MTW5, MTW6 versions	$I_{TH(Min)}$		0.2		A
Maximum Settable Current Limit (R_{LIM} = 62 kΩ) MTW5, MTW6 versions	$I_{TH(Max)}$		1.0		A
Threshold Current Level (R_{LIM} = 30 kΩ)	I_{TH}	1.9	2.0	2.1	A
Circuit Breaker Current Level	I_{CB}		2 x I_{TH}		A
Circuit Breaker Response Time	t_{CB}		6		μs
Overcurrent Trip Timer	t_{TRIP}	1.5			ms
UNDERVOLTAGE LOCKOUT					
Undervoltage Lockout Level Rising	V_{UVLO}	5.0	6.0	7.0	V
Undervoltage Lockout Hysteresis	$UVLO_{hyst}$		0.3		V
Undervoltage Lockout Response Time (Time from Vin reaching UVLO to enabling/disabling)	t_{UVLO}		5.0	10	μs
TURN−ON TIME					
Output On Delay Time (C_{IN} = 100 μF, C_{OUT} = none, V_{IN} = 48 V) (Note 5)	$t_{DLY(On)}$		350		μs
Turn−On Time (C_{IN} = 100 μF, C_{OUT} = none, V_{IN} = 48 V, C_{dvdt} = none) (Note 5)	$t_{RAMP(On)}$		1.5		ms
LOGIC INPUT/OUTPUT					
LOW Level Input; EN	V_{IL}			0.4	V
HIGH Level Input; EN	V_{IH}	1.2			V
LOW Level Output; FAULT, 0.5 mA	V_{OL}			0.3	V
Output Sink Current; FAULT	I_{OL}			0.5	mA
EN Sink Ground Current; EN (V_{IN} = 48, ENx = 0 V)	$I_{EN(sink)}$		3		μA
EN Pull−up Current (EN = 5 V)	$I_{EN(pull-up)}$			1	μA
TOTAL DEVICE CURRENT					
Off State Bias Current (All channels Off)	$I_{bias(Off)}$		85	175	μA
On State Bias Current (All channels On, No Load)	$I_{bias(On)}$		850	1200	μA
On State Bias Current (All channels On, 2.5 A load per channel)	$I_{bias(On,Max)}$		5.0		mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
*Application is to have $R_{\theta JA} \leq$ 14°C/W when driving 2.5 A on each channel.
5. 1 A load connected to output.

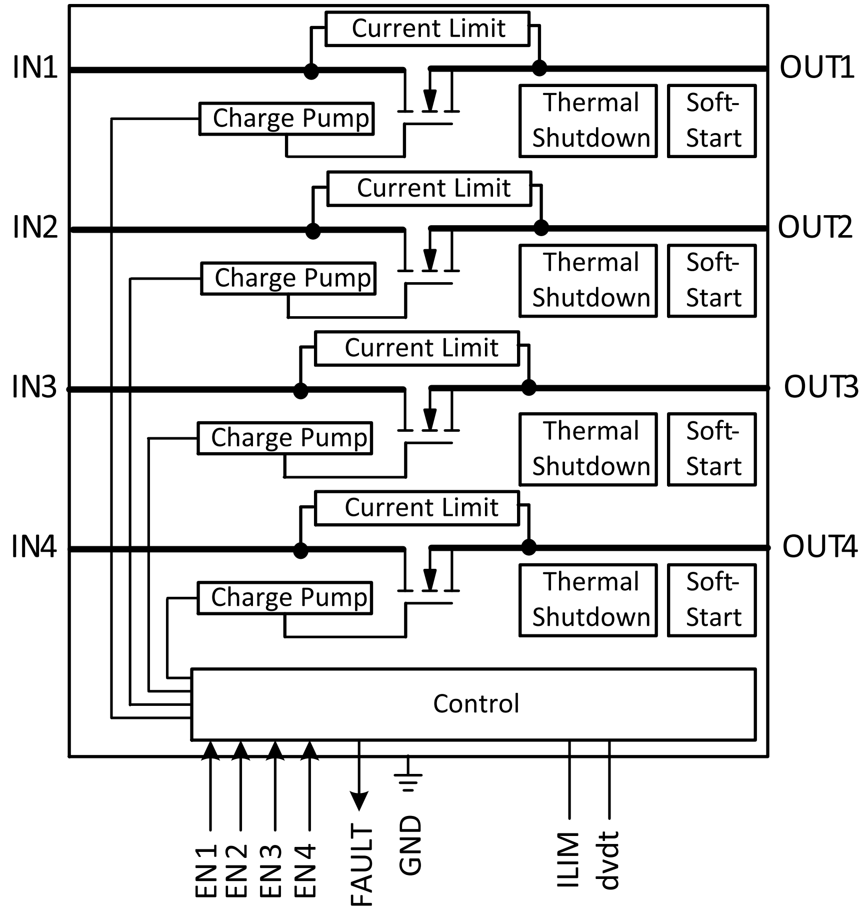


Figure 1. Block Diagram

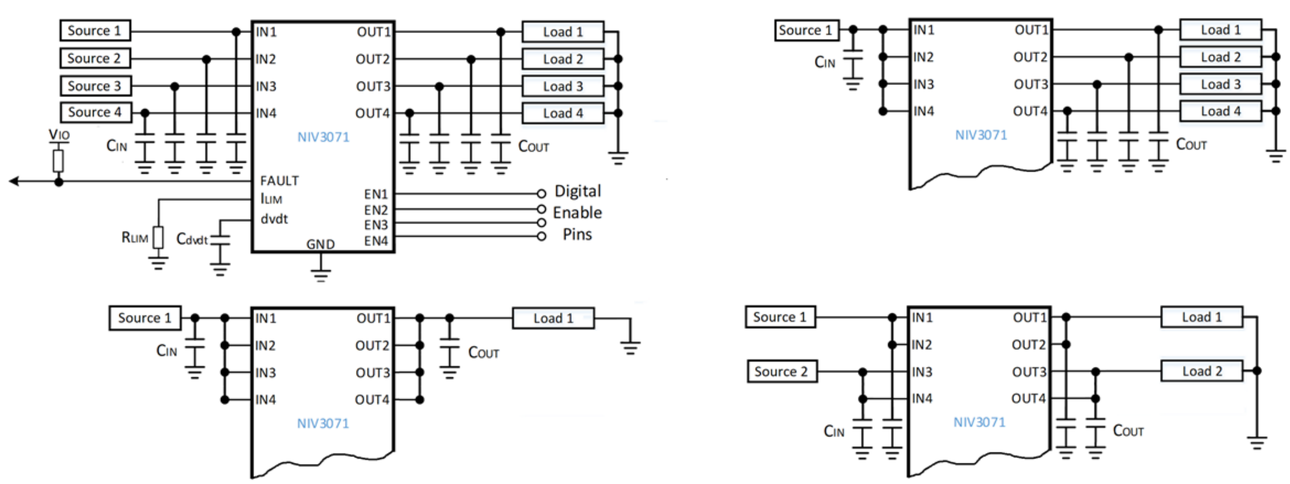


Figure 2. Application Diagrams

APPLICATIONS INFORMATION

Basic Operation

The NIS/NIV3071 is an eFuse with four self−protected channels in a high−side configuration. It contains circuits to monitor the output current and die temperature for each channel independently.

Once the input voltage is applied to any INx pin, the device will apply the input voltage to the load connected to OUTx pin based on the restrictions of the controlling circuits. It is also possible to operate this eFuse with common inputs and common outputs, thus paralleling the channels for higher total output current. When a channel is not in use connect the INx and ENx pins to ground.

Each channel of the device will remain on as long as the temperature of the channel FET does not exceed the 175°C limit that is programmed into the chip.

The overcurrent protection circuit will allow for a load to draw the current for that channel within the allowable overcurrent limit defined by I_{TH} and I_{CB}. If the load current in one channel exceeds limits defined by I_{TH} and I_{CB} it will subsequently turn off, while other channels can continue the normal operation.

An internal charge pump provides bias for the gate voltage of the internal power FET structures and also for the current limit circuit. The remainder of the control circuitry operates between the input voltage at INx pins and ground.

Overcurrent Protection

The Overcurrent protection circuit monitors the load current and allows the load to draw current as long as its level is within an allowable overcurrent range defined by I_{TH} and I_{CB}. The I_{TH} is the overcurrent limit set by the R_{LIM} resistor, and ICB is a circuit breaker level which is 2x of I_{TH}; as long as the load is drawing current not exceeding the I_{CB} level the FET is on, if the current level exceeds the I_{CB} level the FET is turned off for that specific channel. If during the overcurrent mode the internal temperature for the channel FET exceeds the threshold level, that specific channel will be shut off. Additional device options offer a overcurrent trip timer which starts counting right after the load current exceeds the I_{TH} level, once the predetermined amount of time has elapsed the channel will be shut off. Examples of a typical operation for such scheme is shown in Figure 4. Figure 5 shows typical values of I_{TH} with respect to the R_{LIM} resistor.

Turn−on Time Control

The Turn−on Time circuit brings the output voltage up under a linear controlled rate in order to limit peak inrush current. The default ramp time is approximately 1.5 ms. This can be modified by adding an external capacitor at the dvdt pin.

The diagram showing the typical turn−on time and enable delay is shown in Figure 3. The value of capacitor connected to dvdt pin defines the $t_{RAMP(On)}$ turn on times as shown in a Figures 9, 10 and 11. It is recommended to use a ceramic or other low leakage capacitor.

Enable

The active high Enable pins provides a digital interface to control the state of the channels. When ENx pin is pulled low by external circuitry, the specific channel will be turned off. When ENx pin is driven high or left floating, the corresponding channel is enabled. In applications with high inductances on the output, it is recommended to pull the ENx pins high. Protection circuits such as the overcurrent limit function override the function of the enable pin. The EN pin has an internal high impedance pull−up resistor.

Fault

The FAULT pin is an open−drain active low pin signaling the system controller about an overcurrent event on any of the channels. If a thermal shutdown or overcurrent trip timer runout event occurs, the FAULT pin will be pulled low. After the fault is cleared the pin will be floating or pulled up by an external pull−up resistor. The pin can be left unconnected if not used.

Table 4. FAULT PIN TRUTH TABLE

Condition	Fault Pin Status (With external pull up)
Thermal Shutdown	Low
I_{CB} Overcurrent Event	Low
I_{TH} Overcurrent Event (t > tTrip)	Low
Normal Operation	High
Input < UVLO	High

Thermal Protection

The NIS/NIV3071 series device includes an independent internal temperature sensing circuit for each channel that senses the temperature of the power FETs on the die. If the FET temperature reaches 175°C for any of the channels, the device will shut down that specific channel while other channels will continue normal operation. The disabled channel will be automatically turned on once the channel FET temperature has been reduced by 27°C. (for auto−retry version, latched version must be reset) The thermal limit has been set high intentionally, to increase the trip time during high power transient events. It is not recommended to operate this device above 150°C in normal operating conditions.

Transient Protection

In the event of a short circuit or overcurrent fault, the device will interrupt the flow of current by becoming an open circuit. If there is inductance in the system, specifically on the input or output pins of the eFuse, the resulting transients could exceed the datasheet maximum voltage ratings. Input inductance will generate a positive voltage spike on the INx pin(s) and output inductance will generate a negative voltage spike on the OUTx pin(s). Some applications may require large inductances on the input or output, in such a case a Transient Voltage Suppressor (TVS) can placed between the input and ground pins and a Schottky diode can be placed between the output and ground pins to maintain the datasheet absolute maximum voltage ratings. Additionally, capacitors can be used to help absorb transients as well.

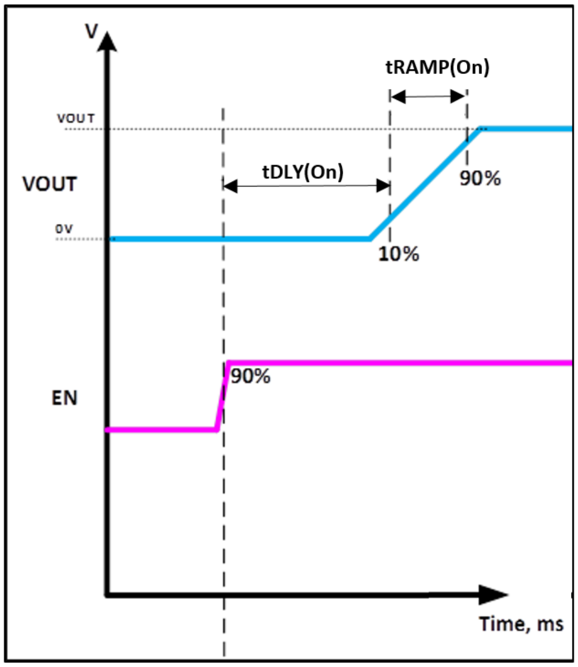
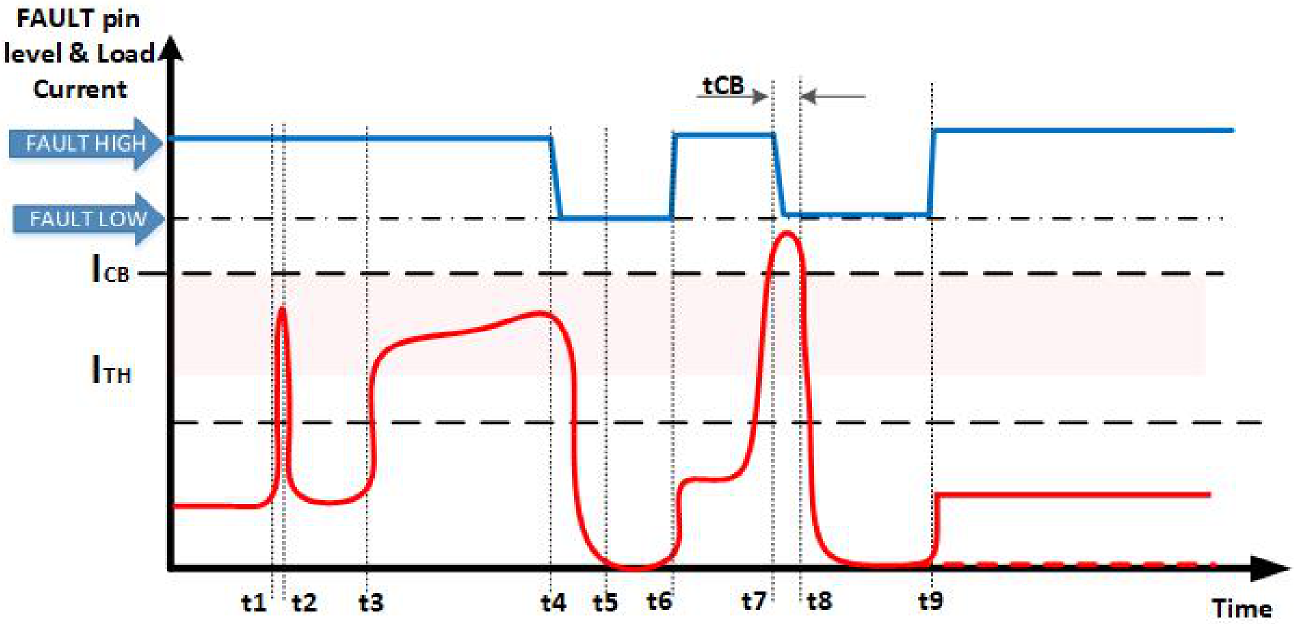


Figure 3. Turn On Delay and Turn−on Time



t1: Current is above I_{TH} (but below I_{CB}); t_{TRIP} counter is started.
t2: Current goes below I_{TH} before t_{TRIP} timer expires. t_{TRIP} counter is reset and normal operation continues.
t3: Current is above I_{TH} (but below I_{CB}); t_{TRIP} counter is started. Note that the load continues to draw current as long as it is below I_{CB} and device remains below the thermal shutdown temperature (T_{SD}).
t4: Device begins shut down due to A) t_{TRIP} timer has expired, OR B) device has reached the thermal shutdown temperature (T_{SD}). FAULT pin is pulled low.
t5: Device shuts down in t_{TSD} after t4.
t6: Device is restarted when temperature is reduced by 27°C (Auto−Retry version only; Latched version will require manual restart with EN pin).
t7: Device output has been shorted (or a severe current overload condition).
t8: Device Output current has exceeded I_{CB}. The device is immediately shut down within the I_{CB} shutdown time t_{CB}. FAULT pin is pulled low.
t9: Device restarts after auto−retry time is exceeded (Auto−Retry only, Latch version will require a manual restart with EN).
Note: dotted line shows device remains off for latched version (until restarted using EN pin).

Figure 4. Overcurrent Protection Diagram

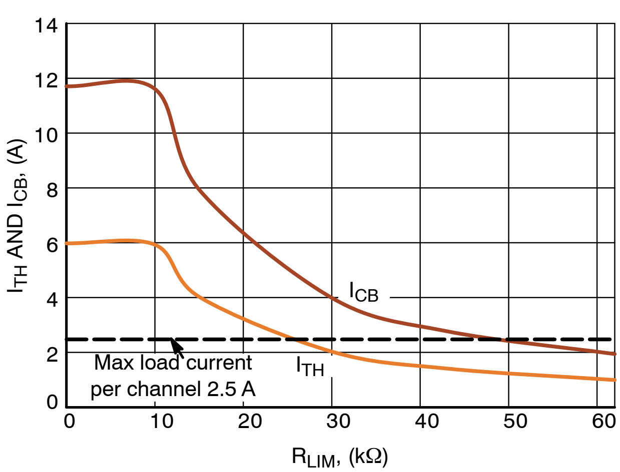


Figure 5. Current Limit Setting vs. R_{LIM} (MT3, MT4 versions)

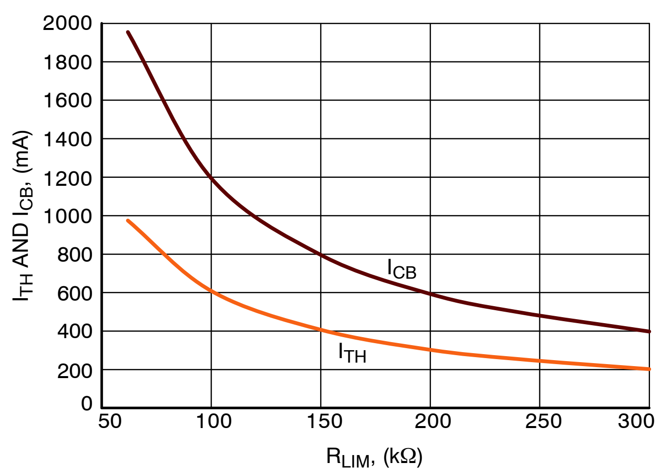


Figure 6. Current Limit Setting vs. R_{LIM} (MT5, MT6 versions)

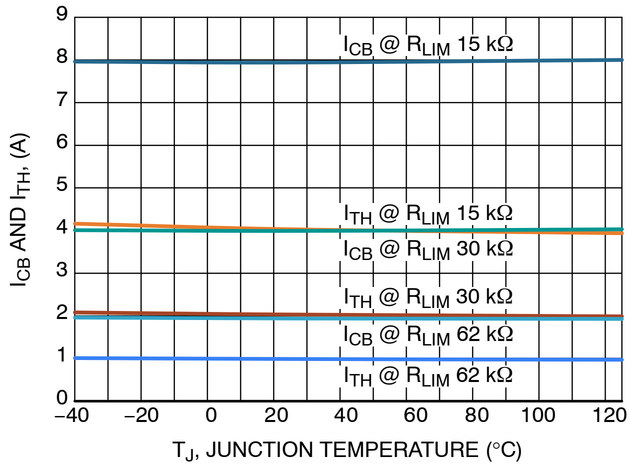


Figure 7. Junction Temperature vs. I_{TH} & I_{CB} (MT3, MT4 versions)

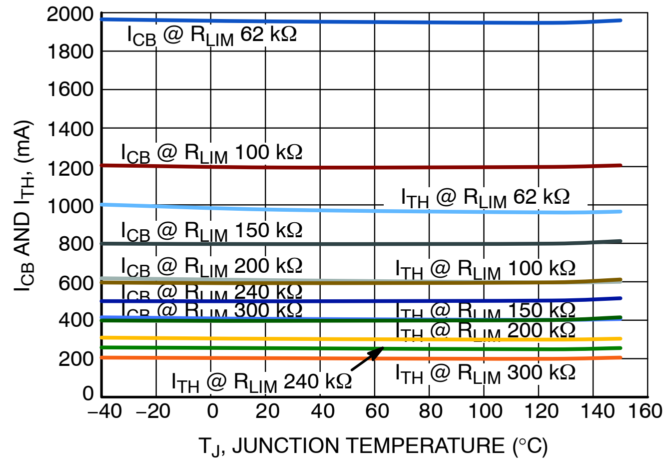


Figure 8. Junction Temperature vs. I_{TH} & I_{CB} (MT5, MT6 versions)

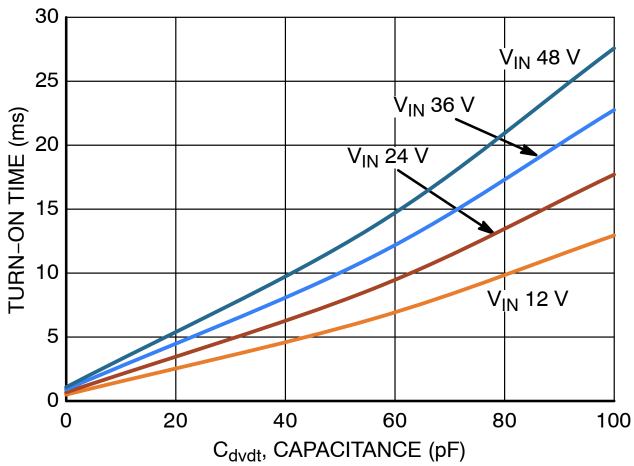


Figure 9. Turn−on Time vs. C_{dvdt} Capacitance at T_J = −40°C

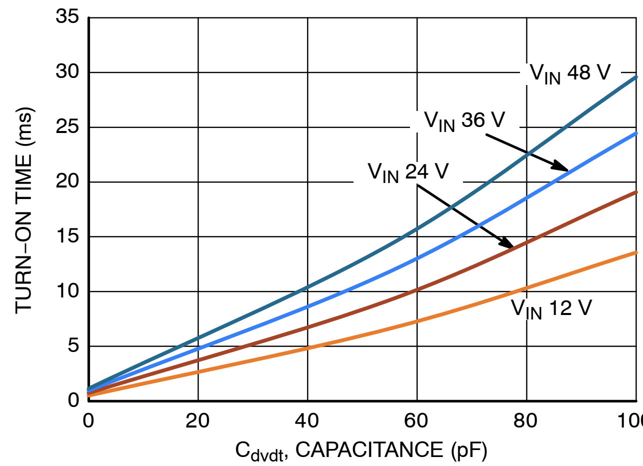


Figure 10. Turn−on Time vs. C_{dvdt} Capacitance at T_J = 25°C

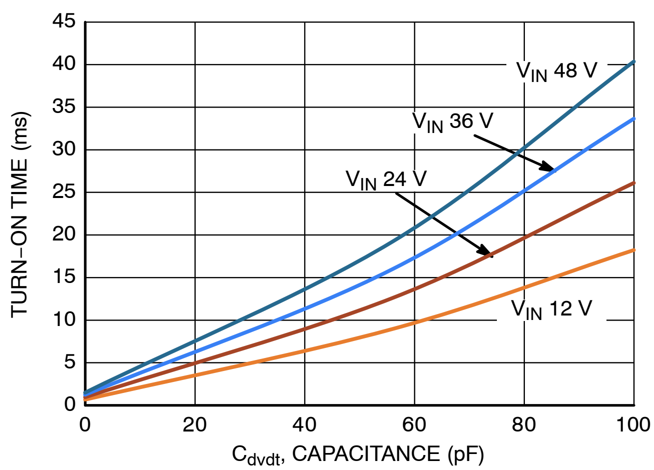


Figure 11. Turn−on Time vs. C_{dvdt} Capacitance at T_J = 125°C

Figure 12. Turning on a Single Output with EN Pin

Figure 13. Turning on a Single Output with the EN Pin While Another Output Pin is On

Figure 14. Turning on a Single Output with the Input Voltage (EN pin pull−up or floated)

Figure 15. Turning on a Single Output with the Input Voltage While Another Output is On (EN pin pull−up or floated)

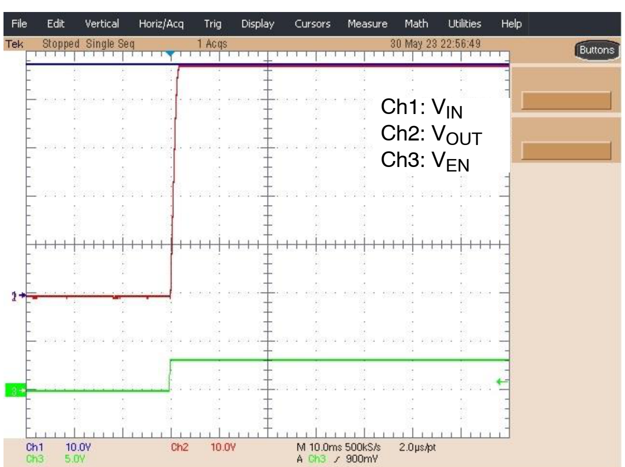


Figure 16. Turn On with EN Pin with C_{dvdt} Open

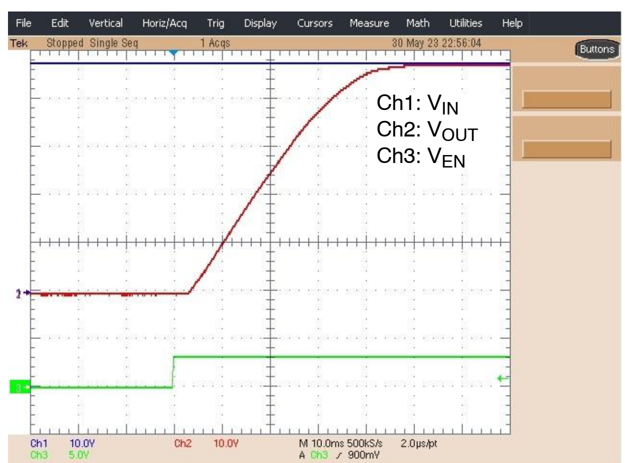


Figure 17. Turn On with EN Pin with C_{dvdt} 56 pF

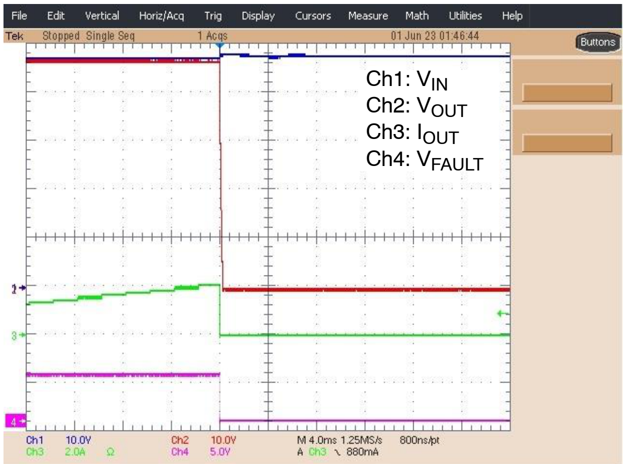


Figure 18. I_{TH} Overcurrent Event on Latching Device

Figure 19. I_{TH} Overcurrent Event on Auto−retry Device

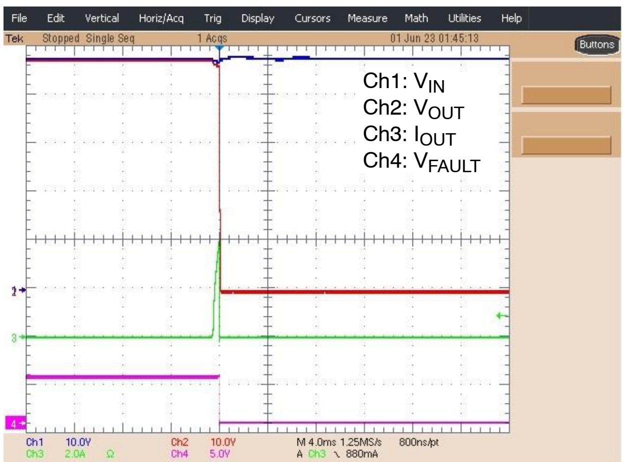


Figure 20. I_{CB} Overcurrent Event on Latching Device

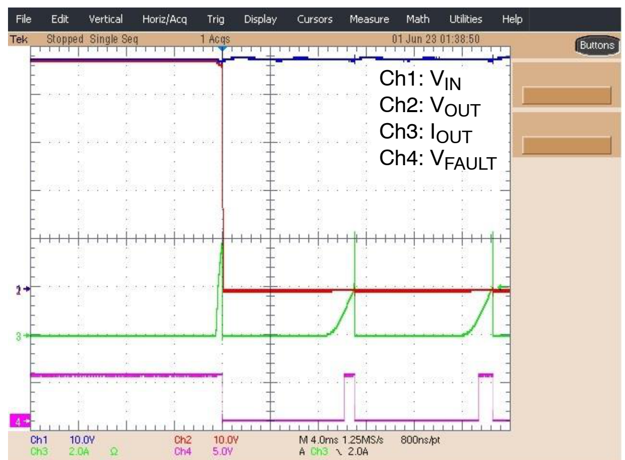


Figure 21. I_{CB} Overcurrent Event on Auto−retry Device

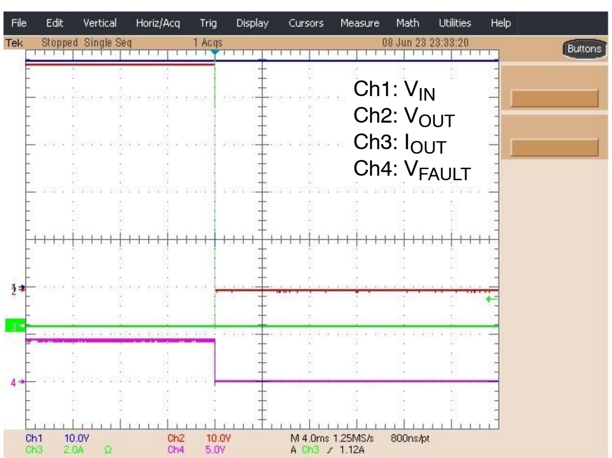


Figure 22. Short Circuit Event on Latching Device

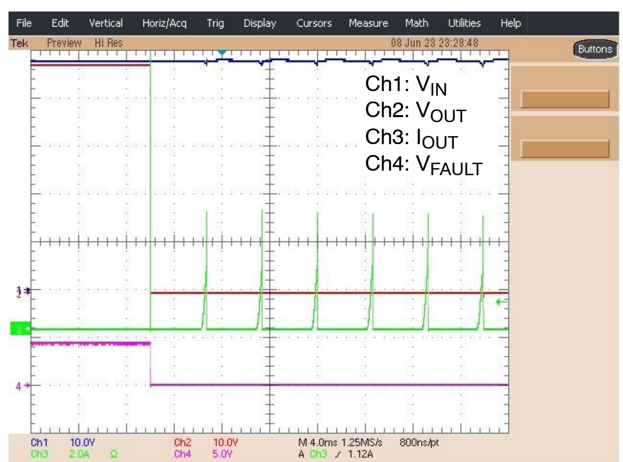


Figure 23. Short Circuit Event on Auto−retry Device

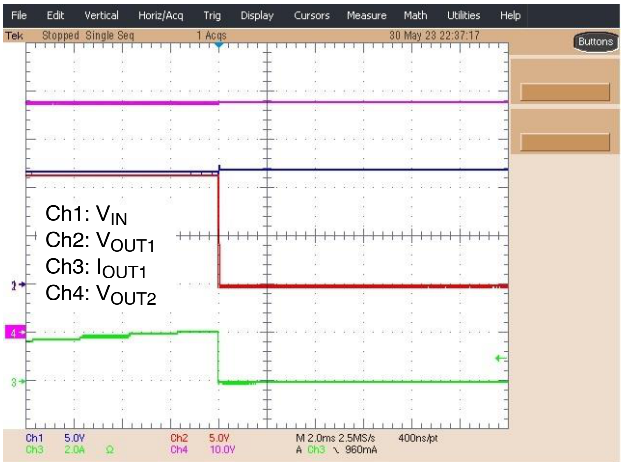


Figure 24. I_{TH} Overcurrent Event While Another Output is On

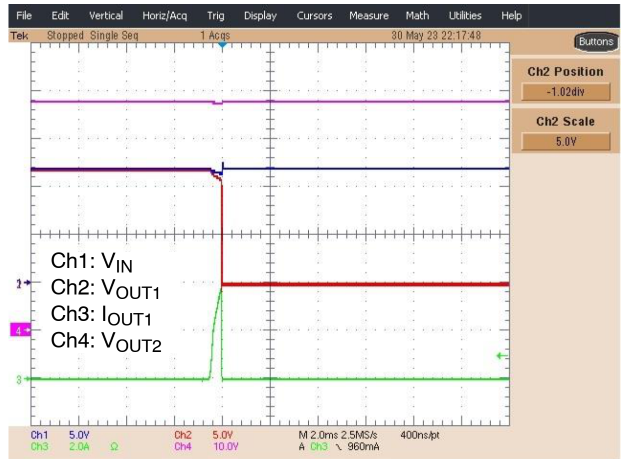


Figure 25. I_{CB} Overcurrent Event While Another Output is On

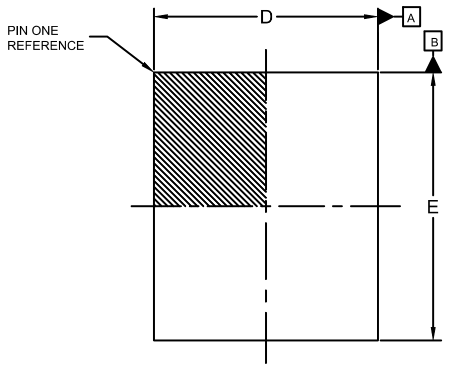
ORDERING INFORMATION

Part Number	Shutdown Version	Package	Shipping†
NIS3071MT3TWG	Latch	WQFN16 5x6 mm (Pb−Free)	5000 / Tape & Reel
NIS3071MT4TWG	Auto−R	WQFN16 5x6 mm (Pb−Free)	5000 / Tape & Reel
NIS3071MTW3TWG	Latch	WQFN16 5x6 mm (Pb−Free) (Wettable Flank)	5000 / Tape & Reel
NIS3071MTW4TWG	Auto−R	WQFN16 5x6 mm (Pb−Free) (Wettable Flank)	5000 / Tape & Reel
NIV3071MTW3TWG*	Latch	WQFNW16 5x6 mm (Pb−Free) (Wettable Flank)	5000 / Tape & Reel
NIV3071MTW4TWG*	Auto−R	WQFNW16 5x6 mm (Pb−Free) (Wettable Flank)	5000 / Tape & Reel
NIS3071MTW5TWG	Latch	WQFN16 5x6 mm (Pb−Free) (Wettable Flank)	5000 / Tape & Reel
NIS3071MTW6TWG	Auto−R	WQFN16 5x6 mm (Pb−Free) (Wettable Flank)	5000 / Tape & Reel
NIV3071MTW5TWG*	Latch	WQFNW16 5x6 mm (Pb−Free) (Wettable Flank)	5000 / Tape & Reel
NIV3071MTW6TWG*	Auto−R	WQFNW16 5x6 mm (Pb−Free) (Wettable Flank)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NIV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable.

WQFN16 5x6, 1.05P
CASE 510CM
ISSUE O

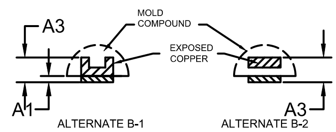
DATE 14 JUN 2019



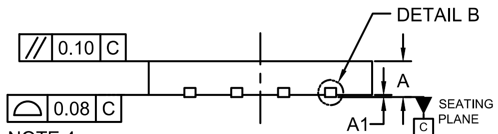
TOP VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINALS AND IS MEASURED BETWEEN 0.20 AND 0.25 FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE PLATED TERMINALS.

DIM	MILLIMETERS MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.025	0.05
A3	0.15	0.20	0.25
b	0.20	0.25	0.30
D	4.90	5.00	5.10
D1	2.65	2.70	2.75
E	5.90	6.00	6.10
E1	4.55	4.60	4.65
e	1.05 BSC		
k	0.40 REF		
k1	0.85 REF		
L	0.25	0.30	0.35
L1	0.05 REF		

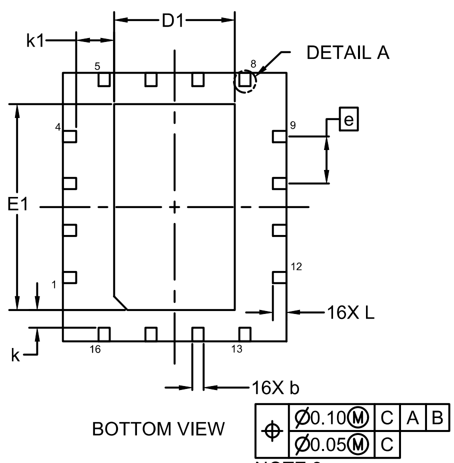


DETAIL B
ALTERNATE CONSTRUCTION

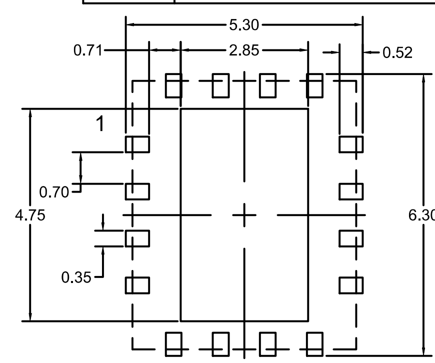


SIDE VIEW

DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



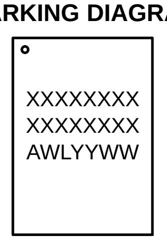
BOTTOM VIEW



RECOMMENDED MOUNTING PATTERN

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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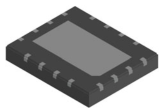
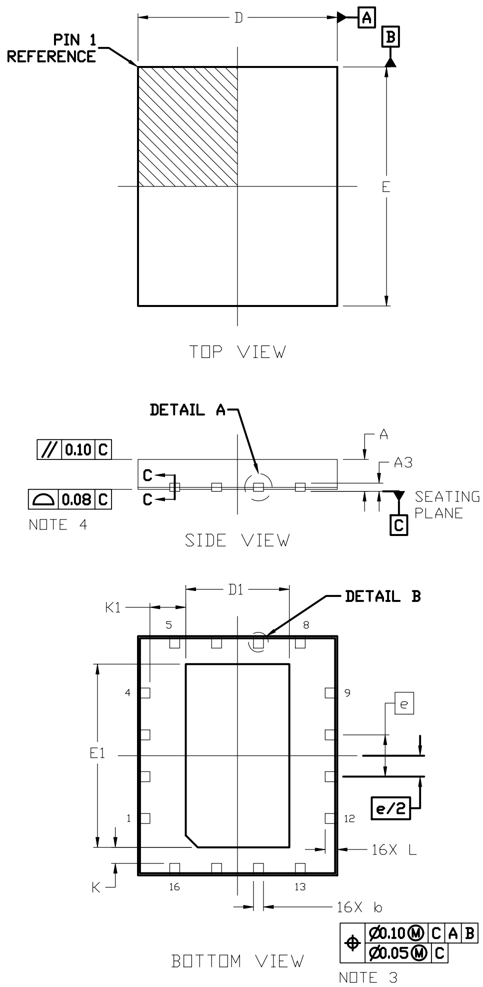
DESCRIPTION:	**WQFN16 5x6, 1.05P**	**PAGE 1 OF 1**

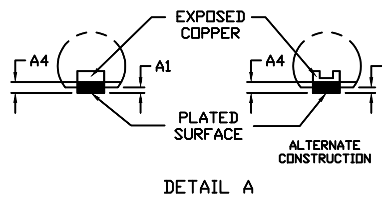


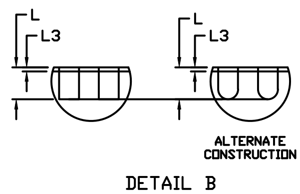
WQFNW16 5x6, 1.05P
CASE 512AN
ISSUE O

DATE 30 JUL 2021

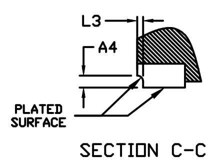


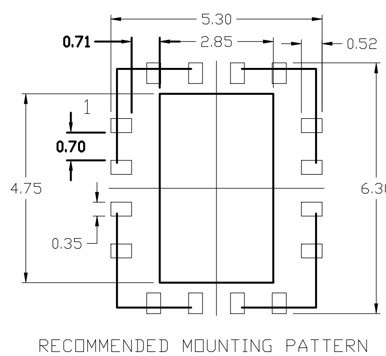
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DIMENSIONS DO NOT INCLUDE BURRS. MOLD FLASH OR BURRS DO NOT EXCEED 0.10MM..
6. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURE TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.





DIM	MILLIMETERS MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	---	0.05
A3		0.20 REF	
A4	0.10	---	---
b	0.20	0.25	0.30
D	4.90	5.00	5.10
D1	2.60	2.70	2.80
E	5.90	6.00	6.10
E1	4.50	4.60	4.70
e		1.05 BSC	
K		0.40 REF	
K1		0.85 REF	
L	0.25	0.30	0.35
L3	---	---	0.09





* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXXXX
XXXXXX
AWLYWW

XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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