NVT4858

SD, SDIO, mini SD, micro SD and SIM card voltage level translator with EMI filter and ESD protection

Rev. 2.1 — 12 November 2021 Product data sheet

1 General description

The device is an SD 3.0-compliant bidirectional dual voltage level translator with auto-direction control. It is designed to interface between a memory or SIM card operating between 1.62 V to 3.6 V signal levels and a host with a supply voltage of 1.08 V to 1.98 V.

The device supports SD 3.0 SDR104, SDR50, DDR50, SDR25, SDR12 and SD 2.0 High-Speed (50 MHz) and Default-Speed (25 MHz) modes. The device has an auto-enable/disable function connected to the V_{CCB} supply pin, built-in EMI filters and robust ESD protections (IEC 61000-4-2, level 4) on V_{CCB} or any of the card side pins. External ESD diodes are not required.

This device also supports SIM card voltage level translator using CLK and two of the data lines for SD and SIM card combo sockets.

2 Features and benefits

- Supports up to 208 MHz clock rate
- SD 3.0 specification-compliant voltage translation to support SDR104, SDR50, DDR50, SDR25, SDR12, High-Speed and Default-Speed modes
- Compliant with all ETSI, IMT-2000 and ISO-7816 SIM/Smart Card interface requirements
- Support SD/SIM card supply voltages with range of 1.62 V to 3.6 V
- Host microcontroller operating voltage range: 1.08 V to 1.98 V
- Feedback channel for clock synchronization
- Low power consumption by push-pull output stage with break-before-make architecture
- Automatic enable and disable through V_{CCB}
- Integrated pull-up and pull-down resistors: no external resistors required
- Integrated EMI filters suppress higher harmonics of digital I/Os
- Integrated 8 kV ESD protection according to IEC 61000-4-2, level 4 on on V_{CCB} or any of the card side pins. External ESD diodes are not required.
- Level shifting buffers keep ESD stress away from the host (zero-clamping concept)
- Available in XQFN16 with 0.4 mm pitch and WLCSP16 with 0.35 mm pitch

3 Applications

- Smart phones
- Mobile handsets
- Digital cameras
- Tablet PCs
- Laptop computers
- SD, MMC or microSD card readers

4 Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
NVT4858UK	N858	WLCSP16	wafer level chip scale package; 16 bumps (4 x 4), body 1.41 x 1.41 x 0.525 mm, 0.35 mm pitch	SOT2127-1
NVT4858HK	N58	XQFN16	plastic, extremely thin quad flat package; no leads; 16 terminals; 2.6 mm x 1.8 mm x 0.50 mm body with 0.4 mm pitch	SOT1161-2

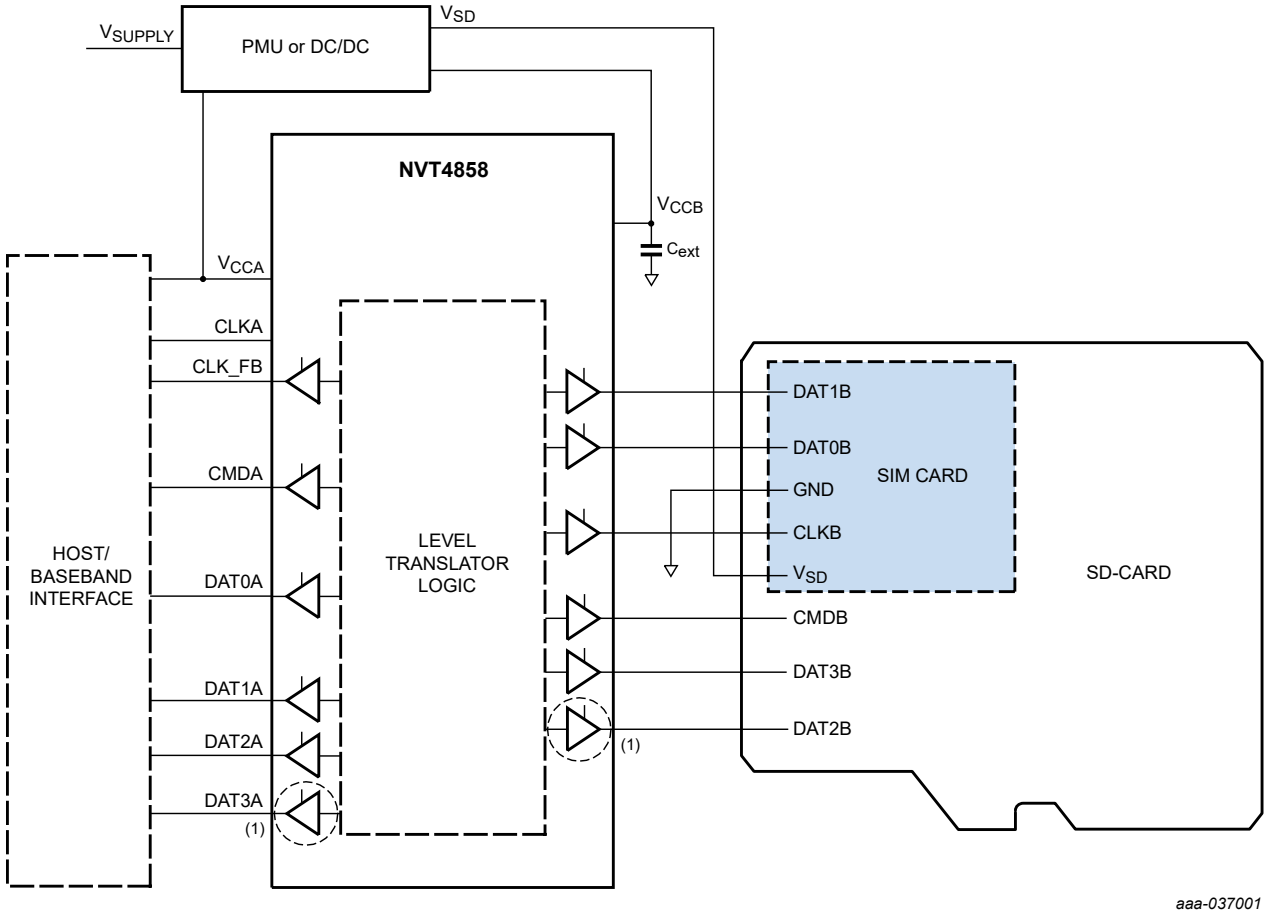
4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
NVT4858UK	NVT4858UKZ	WLCSP16	REEL 7" Q1/T1 [1]	3000	T_{amb} = -40 °C to +85 °C
NVT4858HK	NVT4858HKZ	XQFN16	REEL 7" Q1/T1 SSB [2] [3]	4000	T_{amb} = -40 °C to +85 °C

[1] Find packing information at www.nxp.com/docs/en/packing/SOT2127-1_012.pdf
[2] This packing method uses a Static Shielding Bag (SSB) solution. Material is to be kept in the sealed bag between uses.
[3] Find packing information at www.nxp.com/docs/en/packing/SOT1161-2_471.pdf

5 Block diagram



(1) See Figure 10 for more details.

Figure 1. Application diagram

6 Functional diagram

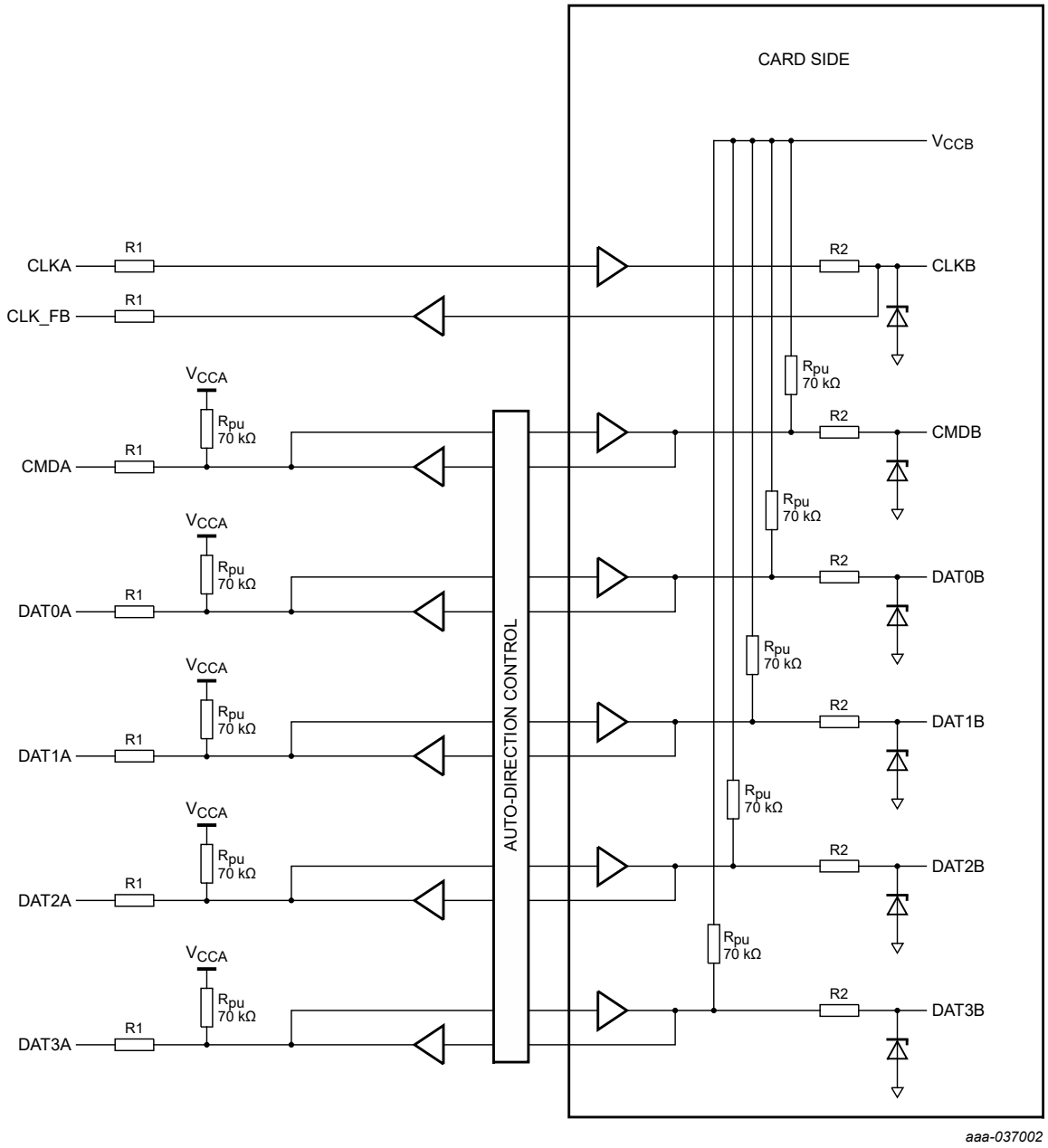


Figure 2. Functional diagram

7 Pinning information

7.1 Pinning

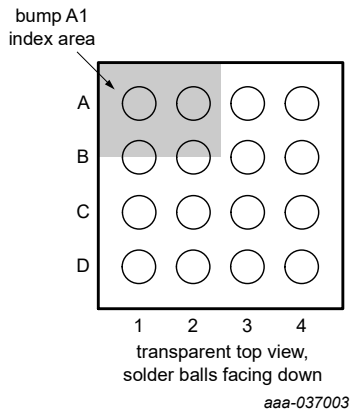


Figure 3. Pin configuration WLCSP16

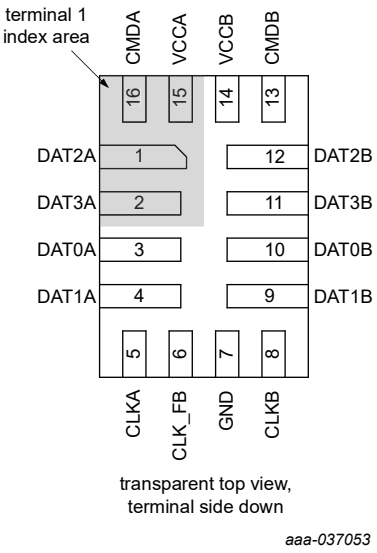


Figure 4. Pin configuration XQFN16

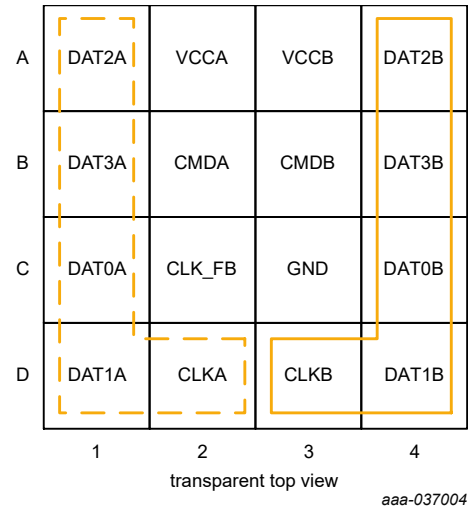


Figure 5. NVT4858UK pinout

Table 3. Pin allocation table WLCSP16

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
A1	DAT2A	A2	V_{CCA}	A3	V_{CCB}	A4	DAT2B
B1	DAT3A	B2	CMDA	B3	CMDB	B4	DAT3B
C1	DAT0A	C2	CLK_FB	C3	GND	C4	DAT0B
D1	DAT1A	D2	CLKA	D3	CLKB	D4	DAT1B

7.2 Pin description

Table 4. Pin description

Symbol [1]	WLCSP16 pinout	XQFN16 pinout	Type [2]	Description
DAT2A	A1	1	I/O	data 2 input or output on host side
V_{CCA}	A2	15	S	supply voltage from host side
V_{CCB}	A3	14	S	supply voltage for card side
DAT2B	A4	12	I/O	data 2 input or output on memory card side or for SIM card reset
DAT3A	B1	2	I/O	data 3 input or output on host side
CMDA	B2	16	I/O	command input or output on host side
CMDB	B3	13	I/O	command input or output on memory card side
DAT3B	B4	11	I/O	data 3 input or output on memory card side or for SIM card IO
DAT0A	C1	3	I/O	data 0 input or output on host side
CLK_FB	C2	6	O	clock feedback output on host side
GND	C3	7	S	supply ground
DAT0B	C4	10	I/O	data 0 input or output on memory card side

Table 4. Pin description...*continued*

Symbol [1]	WLCSP16 pinout	XQFN16 pinout	Type [2]	Description
DAT1A	D1	4	I/O	data 1 input or output on host side
CLKA	D2	5	I	clock signal input on host side
CLKB	D3	8	O	clock signal output on memory or SIM card side
DAT1B	D4	9	I/O	data 1 input or output on memory card side

[1] The pin names relate particularly to SD memory cards, but also apply to microSD and MMC memory cards.
[2] I = input, O = output, I/O = input and output, S = power supply

8 Functional description

Table 5. Function table

Supply Voltage		Supply Status change	Input/Out		Operational Mode
V_{CCA}	V_{CCB}		Host	SD Card	
1.08 V to 1.98 V	1.62 V to 3.6 V	V_{CCA} > 1.0 V and V_{CCB} raising > 1.62 V	HOST = SD Card	SD Card = HOST	Active
1.08 V to 1.98 V	1.62 to 3.6 V	V_{CCA} > 1.0 V and V_{CCB} lower < 0.8V	See Table 6, Condition A		Shutdown Mode
GND	1.62 to 3.6 V	X [1]	See Table 6, Condition A		Shutdown Mode
1.08 V to 1.98 V	GND	X [1]	See Table 6, Condition A		Shutdown Mode
GND	GND	X [1]	See Table 6, Condition A		Shutdown Mode

[1] X = don't care

Table 6. Pin condition

Pin condition	Condition A
CLKA	High Z
CLK_FB	High Z
CMDA and DATxA	70 kΩ pull to V_{CCA}
CLKB	High Z
CMDB and DATxB	70 kΩ pull to V_{CCB}

8.1 Level translator

The bidirectional level translator shifts the data between the I/O supply levels of the host and the memory card. The voltage translator has to support several clock and data transfer rates at the signaling levels specified in the SD 3.0 standard specification.

Table 7. Supported modes

Bus speed mode	Signal level (V)	Clock rate (MHz)	Data rate (MB/s)
Default-Speed	3.0	25	12.5
High-Speed	3.0	50	25
SDR12	1.8	25	12.5
SDR25	1.8	50	25
SDR50	1.8	100	50
SDR104	1.8	208	104
DDR50	1.8	50	50

8.2 Enable and direction control

The device contains an auto-enable feature. If V_{CCB} rises above V_{CCBen}, the level translator logic is enabled automatically. As soon as V_{CCB} drops below the $V_{CCBdisable}$, as specified in Section 11, the card side drivers and the level translator logic is disabled. All host side pins excluding CLKA [1] are configured as inputs with a 70 kΩ resistor pulled up to V_{CCA}.

8.3 Feedback clock channel

The clock is transmitted from the host to the memory card side. The voltage translator and the Printed-Circuit Board (PCB) tracks introduce some amount of delay. It reduces timing margin for data read back from memory card, especially at higher data rates. Therefore, a feedback path is provided to compensate the delay. The reasoning behind this approach is the fact that the clock is always delivered by the host, while the data in the timing critical read mode comes from the card.

Float the node (e.g., leave CLK-FB pin as no connect) for designs that don't need to use the CLK_FB signal.

8.4 EMI filter

All input/output driver stages are equipped with EMI filters to reduce interferences towards sensitive mobile communication.

8.5 ESD protection

The device has robust ESD protections on all memory card pins as well as on the V_{CCB} pin . The architecture prevents any stress for the host: the voltage translator discharges any stress to supply ground.

1 CLKA is a pure high-ohmic input. Please refer to Section 6 for more detail.

9 Limiting values

Table 8. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	4 ms transient			
		on pin V_{CCA}	-0.5	+2.4	V
		on pin V_{CCB}	-0.5	+4.0	V
V_I	input voltage	4 ms transient			
		at I/O pins supplied by V_{CCA}	-0.5	V_{CCA} + 0.3	V
		at I/O pins supplied by V_{CCB}	-0.5	V_{CCB} + 0.3	V
P_{tot}	total power dissipation	T_{amb} = -40 °C to +85 °C	-	1000	mW
T_{stg}	storage temperature		-55	+150	°C
T_{amb}	ambient temperature		-40	+85	°C
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4, all memory card-side pins, and V_{CCB} [1]			
		contact discharge	-8	+8	kV
		air discharge [2]	-15	+15	kV
		Human Body Model (HBM) JEDEC JESD22-A114F; all pins	-2000	+2000	V
		Charge Device Model (CDM) JEDEC JESD22-C101E; all pins	-500	+500	V
$I_{lu(IO)}$	input/output latch-up current	JESD 78B: -0.5 × V_{CC} < V_I < 1.5 × V_{CC}; T_j < 125 °C	-100	+100	mA

[1] All system level tests are performed with the application-specific capacitors connected to the supply pins V_{SUPPLY}, V_{LDO} and V_{CCA}.

[2] The IEC 61000-4-2 standards are defined so that each level is considered equivalent – a Level 4 contact discharge of 8 kV is considered equivalent to a 15 kV air discharge. Air discharge is provided for information only and was not tested. Per IEC61000-4-2: Contact discharge is the preferred test method, air discharges shall be used where contact discharge cannot be applied. Please refer to AN10897: A guide to designing for ESD and EMC and AN11267: EMC and system level ESD design guidelines for LCD drivers for more information on ESD testing and ESD design techniques.

10 Recommended operating conditions

Table 9. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	on pin V_{CCA}	1.08	-	1.98	V
		on pin V_{CCB}	1.62	-	3.6	V
V_I	input voltage	host side [1]	-0.3	-	V_{CCA} + 0.3	V
		memory and sim card side	-0.3	-	V_{CCB} + 0.3	V
C_{ext}	external capacitance	recommended capacitor at pin V_{CCA} (NVT4858HK)	-	100	-	pF
		recommended capacitor at pin V_{CCB} (NVT4858HK)	-	100	-	pF
		recommended capacitor at pin V_{CCA} (NVT4858UK)	-	220	-	pF
		recommended capacitor at pin V_{CCB} (NVT4858UK)	-	220	-	pF

[1] The voltage must not exceed 1.98 V steady state.

Table 10. Integrated resistors

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{pu}	pull-up resistance	all data lines and CMDx	49	70	91	kΩ
R_s	series resistance	host side; R1; tolerance ±30 % [1]	-	22.5	-	Ω
		card side; R2; tolerance ±30 % [1]	-	15	-	Ω

[1] Guaranteed by design.

11 Static characteristics

Table 11. Static characteristics

At recommended operating conditions; T_{amb} = -40 °C to +85 °C; voltages are referenced to GND (ground = 0 V); C_{ext} = 2.2 µF at pin V_{CCB}; unless otherwise specified; Guaranteed by design and characterization.

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
Automatic enable feature: V_{CCB}						
V_{CCBen}	device enable voltage level	V_{CCA} ≥ 1.0 V, V_{CCB} rising edge	1.62	-	-	V
$V_{CCBdisable}$	device disable voltage level	V_{CCA} ≥ 1.0 V, V_{CCB} falling edge	-	-	0.8	V
Host-side input signals: CMDA and DAT0A to DAT3A, CLKA; 1.08 V ≤ V_{CCA} ≤ 1.98 V						
V_{IH}	HIGH-level input voltage		0.7 × V_{CCA}	-		V
V_{IL}	LOW-level input voltage			-	0.3 × V_{CCA}	V
Host-side output signals: CLK_FB, CMDA and DAT0A to DAT3A; 1.08 V ≤ V_{CCA} ≤ 1.98 V						
V_{OH}	HIGH-level output voltage for CLK_FB	I_O = -2 mA; V_I = V_{IH} (card side)	0.8 × V_{CCA}	-	V_{CCA}	V
	HIGH-level output voltage for CMDA, DATxA	I_O = -2 µA; V_I = V_{IH} (card side)	0.8 × V_{CCA}	-	V_{CCA}	V
V_{OL}	LOW-level output voltage	I_O = 2 mA; V_I = V_{IL} (card side)	-	-	0.15 × V_{CCA}	V
Card-side input signals: CMDB and DAT0B to DAT3B						
V_{IH}	HIGH-level input voltage		0.625 × V_{CCB}	-		V
V_{IL}	LOW-level input voltage			-	0.35 × V_{CCB}	V
Card-side output signal: CMDB and DAT0B to DAT3B, CLKB						
V_{OH}	HIGH-level output voltage for CLKB only	I_O = -4 mA; V_I = V_{IH} (host side); V_{CCB} = 3.0 V card interface	0.85 × V_{CCB}	-	V_{CCB}	V
		I_O = -2 mA; V_I = V_{IH} (host side); V_{CCB} = 1.8 V card interface	0.85 × V_{CCB}	-	V_{CCB}	V
	HIGH-level output voltage for CMDB, DATxB	I_O = -2 µA; V_I = V_{IH} (host side); V_{CCB} = 1.8 V card interface	0.85 × V_{CCB}	-	V_{CCB}	V
V_{OL}	LOW-level output voltage	I_O = 4 mA; V_I = V_{IL} (host side); V_{CCB} = 3.0 V card interface	-0.3	-	0.125 × V_{CCB}	V
		I_O = 2 mA; V_I = $V_{I\ card\ L}$ (host side); V_{CCB} 1.8 V interface	-0.3	-	0.125 × V_{CCB}	V
Bus signal equivalent capacitance						
C_{ch}	channel capacitance	V_I = 0 V; f_i = 1 MHz; V_{CCB} = 3.0 V; V_{CCA} = 1.8 V [2]				
		host side	-	7	-	pF
		card side	-	15	-	pF
Current consumption						

Table 11. Static characteristics...*continued*

At recommended operating conditions; T_{amb} = -40 °C to +85 °C; voltages are referenced to GND (ground = 0 V); C_{ext} = 2.2 µF at pin V_{CCB}; unless otherwise specified; Guaranteed by design and characterization.

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
$I_{CC(stat)}$	static supply current	$V_{CCB} \geq V_{CCBen}$ (active mode); all inputs = HIGH	-	-	15	µA
$I_{CC(stb)}$	standby supply current	$V_{CCB} \leq V_{CCBen}$ and $V_{CCA} \geq 1.0$ V (inactive mode); all host side inputs = HIGH	-	-	7	µA

[1] Typical values are measured at T_{amb} = 25 °C.
[2] EMI filter line capacitance per data channel from I/O driver to pin; C_{ch} is guaranteed by design.

12 Dynamic characteristics

12.1 Level translator

Table 12. Level translator dynamic characteristics

At recommended operating conditions; V_{CCA} = 1.2 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Host side transition times							
t_r	rise time	V_{CCB} = 1.8 V card interface; V_{CCA} = 1.8 V	[1]	-	0.4	1.0	ns
t_f	fall time		[1]	-	0.4	1.0	ns
t_r	rise time	V_{CCB} = 1.8 V card interface; V_{CCA} = 1.2 V	[1]	-	0.4	1.0	ns
t_f	fall time		[1]	-	0.4	1.0	ns
Card side transition times							
t_r	rise time	V_{CCB} = 1.8 V card interface; -40 °C ≤ T_{amb} ≤ +85 °C	[2]	0.4	0.88	1.32	ns
t_f	fall time		[2]	0.4	0.88	1.32	ns
Card input transition times							
t_r	rise time	V_{CCB} = 1.8 V card interface; -40 °C ≤ T_{amb} ≤ +85 °C	[3]	0.2	0.5	0.96	ns
t_f	fall time		[3]	0.2	0.45	0.96	ns
Host to card propagation delay							
t_{pd}	trailing edge	V_{CCB} = 1.8 V card interface; V_{CCA} = 1.2 V		-	2.5	5.0	ns
t_{pd}	rising edge	V_{CCB} = 1.8 V card interface; V_{CCA} = 1.2 V		-	2.9	5.0	ns
t_{pd}	trailing edge	V_{CCB} = 3.3 V card interface; V_{CCA} = 1.2 V		-	1.9	5.0	ns
t_{pd}	rising edge	V_{CCB} = 3.3 V card interface; V_{CCA} = 1.2 V		-	2.3	5.0	ns
t_{pd}	trailing edge	V_{CCB} = 1.8 V card interface; V_{CCA} = 1.8 V		-	1.9	5.0	ns
t_{pd}	rising edge	V_{CCB} = 1.8 V card interface; V_{CCA} = 1.8 V		-	2.1	5.0	ns
t_{pd}	trailing edge	V_{CCB} = 3.3 V card interface; V_{CCA} = 1.8 V		-	1.2	5.0	ns
t_{pd}	rising edge	V_{CCB} = 3.3 V card interface; V_{CCA} = 1.8 V		-	1.5	5.0	ns
Card to host propagation delay							
t_{pd}	trailing edge	V_{CCB} = 1.8 V card interface; V_{CCA} = 1.2 V		-	2.9	5.0	ns
t_{pd}	rising edge	V_{CCB} = 1.8 V card interface; V_{CCA} = 1.2 V		-	3.0	5.0	ns
t_{pd}	trailing edge	V_{CCB} = 3.3 V card interface; V_{CCA} = 1.2 V		-	2.6	5.0	ns
t_{pd}	rising edge	V_{CCB} = 3.3 V card interface; V_{CCA} = 1.2 V		-	2.6	5.0	ns
t_{pd}	trailing edge	V_{CCB} = 1.8 V card interface; V_{CCA} = 1.8 V		-	2.2	5.0	ns
t_{pd}	rising edge	V_{CCB} = 1.8 V card interface; V_{CCA} = 1.8 V		-	2.2	5.0	ns
t_{pd}	trailing edge	V_{CCB} = 3.3 V card interface; V_{CCA} = 1.8 V		-	2.0	5.0	ns
t_{pd}	rising edge	V_{CCB} = 3.3 V card interface; V_{CCA} = 1.8 V		-	1.8	5.0	ns
CLKA to CLK_FB propagation delay							
t_{pd}	trailing edge	V_{CCB} = 1.8 V card interface; V_{CCA} = 1.2 V		-	6.3	10	ns
t_{pd}	rising edge	V_{CCB} = 1.8 V card interface; V_{CCA} = 1.2 V		-	6.3	10	ns
t_{pd}	trailing edge	V_{CCB} = 3.3 V card interface; V_{CCA} = 1.2 V		-	5.5	10	ns
t_{pd}	rising edge	V_{CCB} = 3.3 V card interface; V_{CCA} = 1.2 V		-	5.5	10	ns
t_{pd}	trailing edge	V_{CCB} = 1.8 V card interface; V_{CCA} = 1.8 V		-	4.8	10	ns
t_{pd}	rising edge	V_{CCB} = 1.8 V card interface; V_{CCA} = 1.8 V		-	4.8	10	ns

Table 12. Level translator dynamic characteristics...*continued*

At recommended operating conditions; V_{CCA} = 1.2 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{pd}	trailing edge	V_{CCB} = 3.3 V card interface; V_{CCA} = 1.8 V	-	3.9	10	ns
t_{pd}	rising edge	V_{CCB} = 3.3 V card interface; V_{CCA} = 1.8 V	-	3.9	10	ns

[1] transition between V_{OL} = 0.35 * V_{CCA} and V_{OH} = 0.65 * V_{CCA}
[2] transition between V_{OL} = 0.45 V and V_{OH} = 1.4 V
[3] Guaranteed by design; transition between V_{IL} = 0.58 V and V_{IH} = 1.27 V with C_{trace} = 3.5 pF and $C_{card+CRADLE}$ = 12 pF, trace length = 11 mm

Table 13. SD card level translator skew - NVT4858HK (QFN)

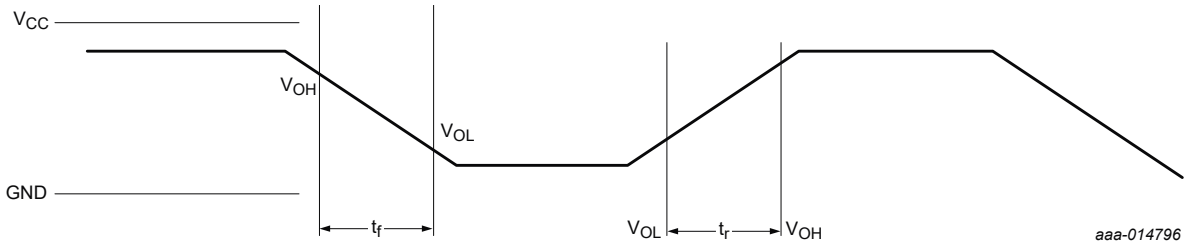
Over -40 °C to +85 °C

Item	Condition	Direction	V_{DD} condition (±10 %)	Min	Typ	Max	Unit
skew	clk/cmdb to data (clk to data2)	host to card	V_{CCA} = 1.2 V; V_{CCB} = 3 V	-	-	200	ps
skew (data to data)	data to data	host to card	V_{CCA} = 1.2 V; V_{CCB} = 3 V	-	-	200	ps
skew	clk/cmdb to data	card to host	V_{CCA} = 1.2 V; V_{CCB} = 3 V	-	-	200	ps
skew (data to data)	data to data	card to host	V_{CCA} = 1.2 V; V_{CCB} = 3 V	-	-	200	ps
skew	clk/cmdb to data	host to card	V_{CCA} = 1.2 V; V_{CCB} = 1.8 V	-	-	200	ps
skew (data to data)	data to data	host to card	V_{CCA} = 1.2 V; V_{CCB} = 1.8 V	-	-	200	ps
skew	clk/cmdb to data	card to host	V_{CCA} = 1.2 V; V_{CCB} = 1.8 V	-	-	200	ps
skew (data to data)	data to data	card to host	V_{CCA} = 1.2 V; V_{CCB} = 1.8 V	-	-	200	ps

Table 14. SD card level translator skew - NVT4858UK (WLCSP)

Over -40 °C to +85 °C

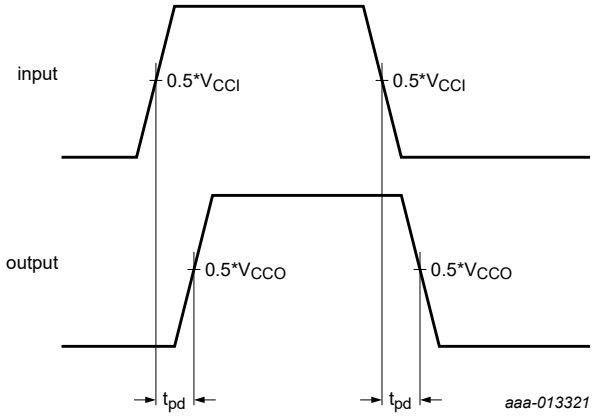
Item	Condition	Direction	V_{DD} condition (±10 %)	Min	Typ	Max	Unit
skew	clk/cmdb to data (clk to data2)	host to card	V_{CCA} = 1.2 V; V_{CCB} = 3 V	-	-	200	ps
skew (data to data)	data to data	host to card	V_{CCA} = 1.2 V; V_{CCB} = 3 V	-	-	200	ps
skew	clk/cmdb to data	card to host	V_{CCA} = 1.2 V; V_{CCB} = 3 V	-	-	200	ps
skew (data to data)	data to data	card to host	V_{CCA} = 1.2 V; V_{CCB} = 3 V	-	-	200	ps
skew	clk/cmdb to data	host to card	V_{CCA} = 1.2 V; V_{CCB} = 1.8 V	-	-	200	ps
skew (data to data)	data to data	host to card	V_{CCA} = 1.2 V; V_{CCB} = 1.8 V	-	-	200	ps
skew	clk/cmdb to data	card to host	V_{CCA} = 1.2 V; V_{CCB} = 1.8 V	-	-	200	ps
skew (data to data)	data to data	card to host	V_{CCA} = 1.2 V; V_{CCB} = 1.8 V	-	-	200	ps



V_{OH} and V_{OL} are specified in Table 12 as [1] and [2]

Figure 6. Output rise and fall times

[1] transition between V_{OL} = 0.35 * V_{CCA} and V_{OH} = 0.65 * V_{CCA}
[2] transition between V_{OL} = 0.45 V and V_{OH} = 1.4 V



Output delay is for every single channel, from input to output, 0.5*V_{CCI} to 0.5*V_{CCO}, in which V_{CCI} and V_{CCO} are the input and output voltage domain.

Figure 7. Output delay timing

13 Application information

The application circuit for NVT4858, which shows the typical interface with a SD or SIM card, is shown below.

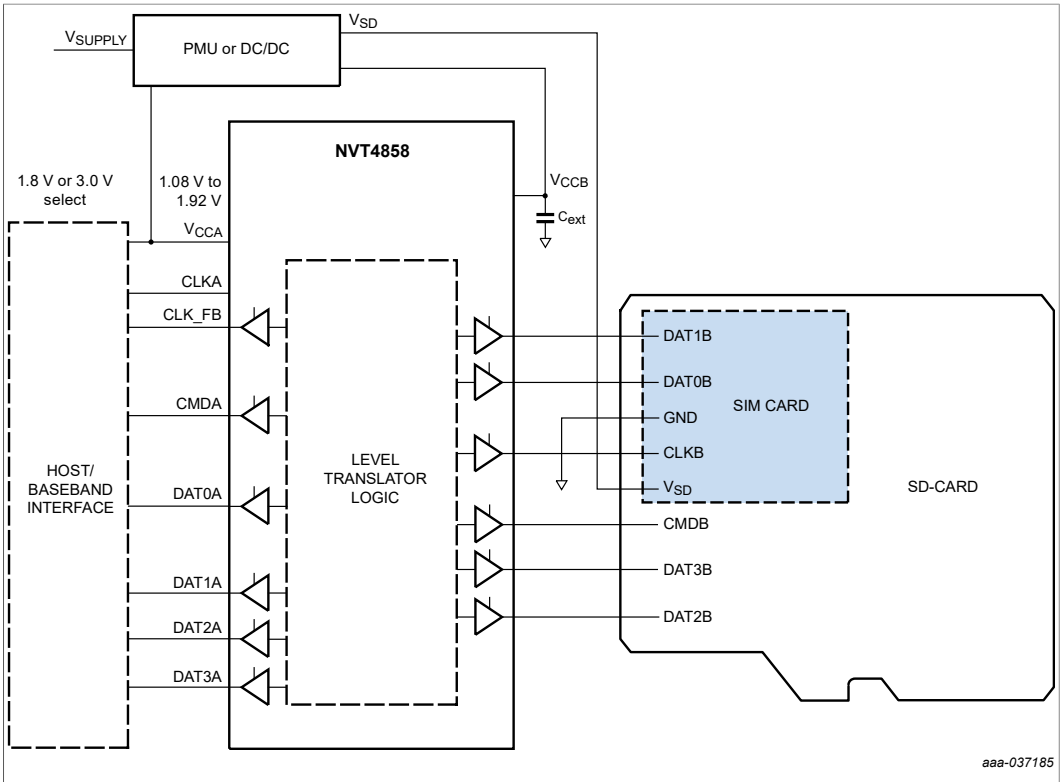


Figure 8. Application circuit interfacing with typical SD or SIM card

13.1 SD card pin assignment

Figure 9 shows the general shape and interface contacts of the SD Memory Card and Table 15 defines the card contacts.

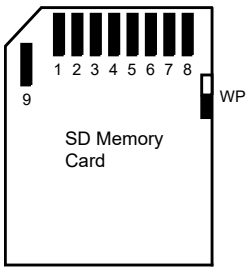


Figure 9. SD memory card shape and interface (top view)

Table 15. SD memory card pad assignment

Pin #	Name	Type	Description
SD mode			
1	CD/DAT3	I/O/PP	Card detect/data line (Bit 3)

Table 15. SD memory card pad assignment*...continued*

Pin #	Name	Type	Description
2	CMD	I/O/PP	Command/response
3	VSS1	S	Supply voltage ground
4	VDD	S	Supply voltage
5	CLK	I	Clock
6	VSS2	S	Supply voltage ground
7	DAT0	I/O/PP	Data line (Bit 0)
8	DAT1	I/O/PP	Data line (Bit 1)
9	DAT2	I/O/PP	Data line (Bit 2)

13.2 Input/output capacitor considerations

It is recommended that a 1 µF and 100 nF (NVT4858HK) or 220 nF (NVT4858UK) capacitors having low Equivalent Series Resistance (ESR) are used respectively at V_{CCA} and V_{CCB} input terminals of the device. X5R and X7R type multi-layer ceramic capacitors (MLCC) are preferred because they have minimal variation in value and ESR over temperature. The maximum ESR should be < 500 mΩ (50 mΩ typical).

13.3 Layout consideration

The capacitors should be placed directly at the terminals and ground plane. It is recommended to design the PCB so that the V_{CCA} and V_{CCB} pins are bypassed with a capacitor with each ground returning to a common node at the GND pin of the device such that ground loops are minimized.

13.4 Level translator stage

The architecture of the device I/O channel is shown below. The device does not require an extra input signal to control the direction of data flow from host to SD/SIM card or from SD/SIM to host. As a change of driving direction is just possible when both sides are in HIGH state, the control logic is recognizing the first falling edge granting it control about the other signal side. During a rising edge signal, the non-driving output is driven by a one-shot circuit to accelerate the rising edge. In case of a communication error or some other unforeseen incident that would drive both connected sides to be drivers at the same time, the internal logic automatically prevents stuck-at situation, so both I/Os will return to HIGH level once released from being driven LOW.

The channels CLK and CLK_FB just contain single direction drivers without the holding mechanism of the I/O channel, as these are just driven from the host to the card side.

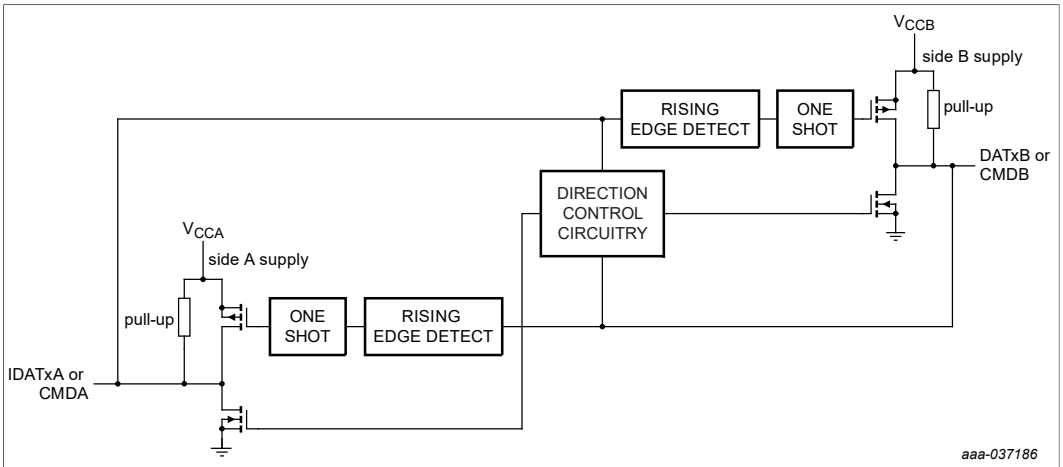
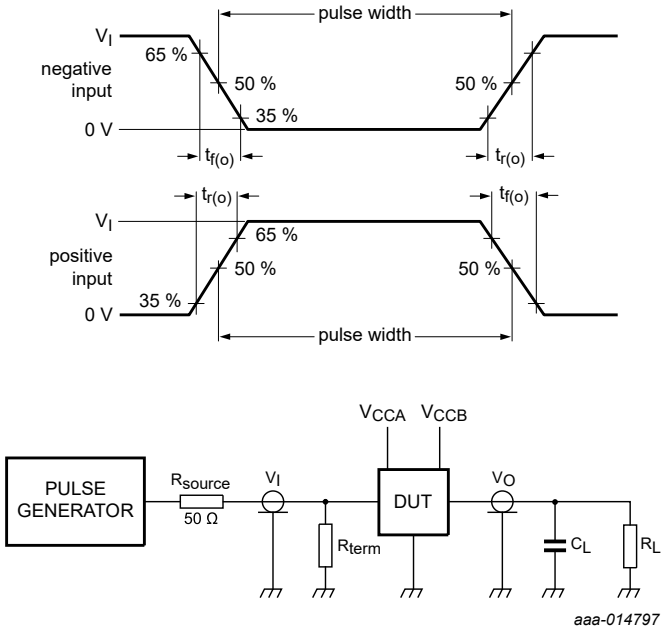


Figure 10. Automatic direction control level translator for HIGH-level direction change interfaces

14 Test information



Definitions test circuit:

R_{source} = source resistance of pulse generator.

R_{term} = termination resistance should be equal to output impedance Z_o of pulse generator.

C_L = load capacitance including jig and probe capacitance.

R_L = load resistance.

Figure 11. Load circuitry for measuring switching time

15 Package outline

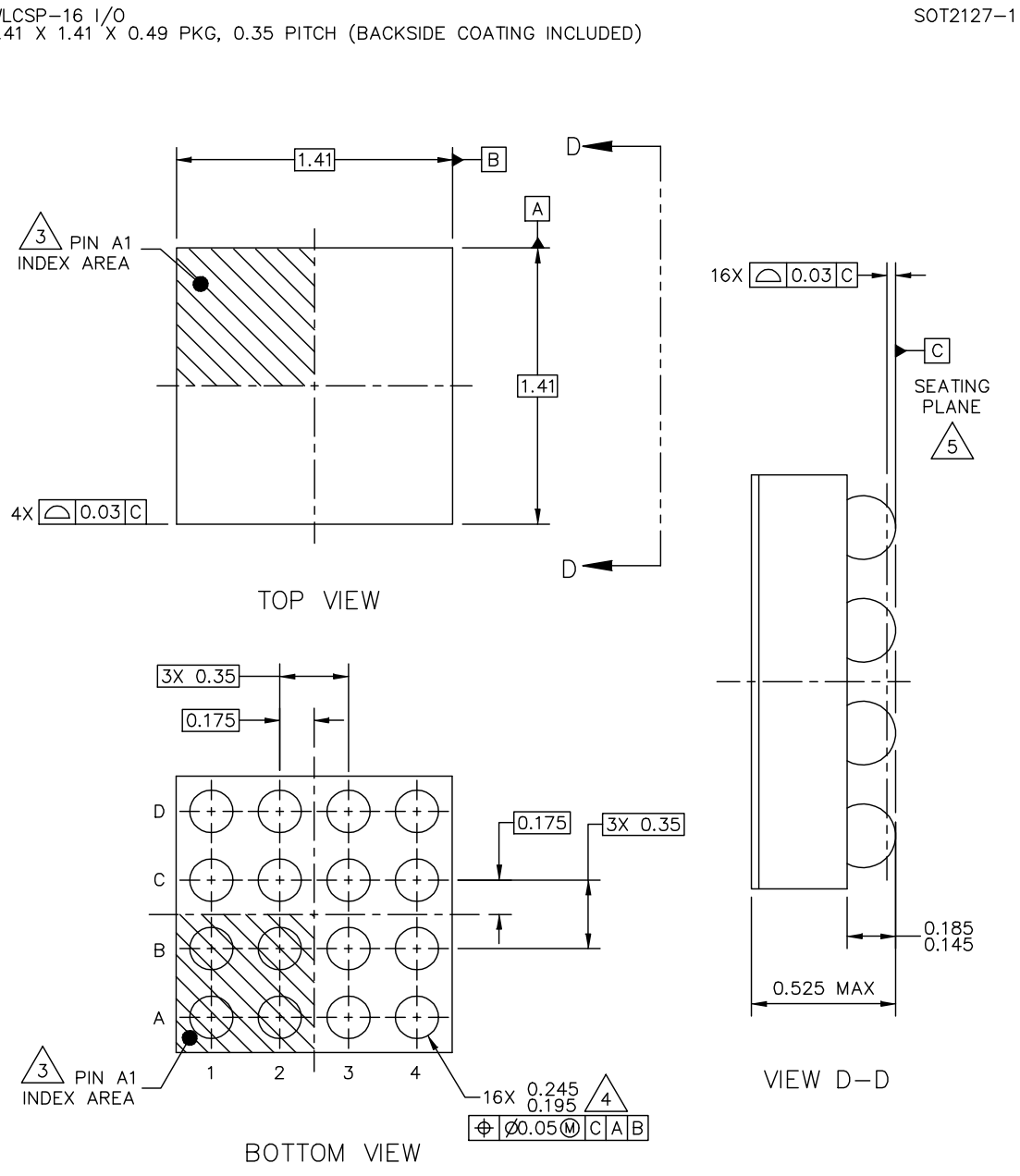


Figure 12. Package outline SOT2127-1 (WLCSP16)

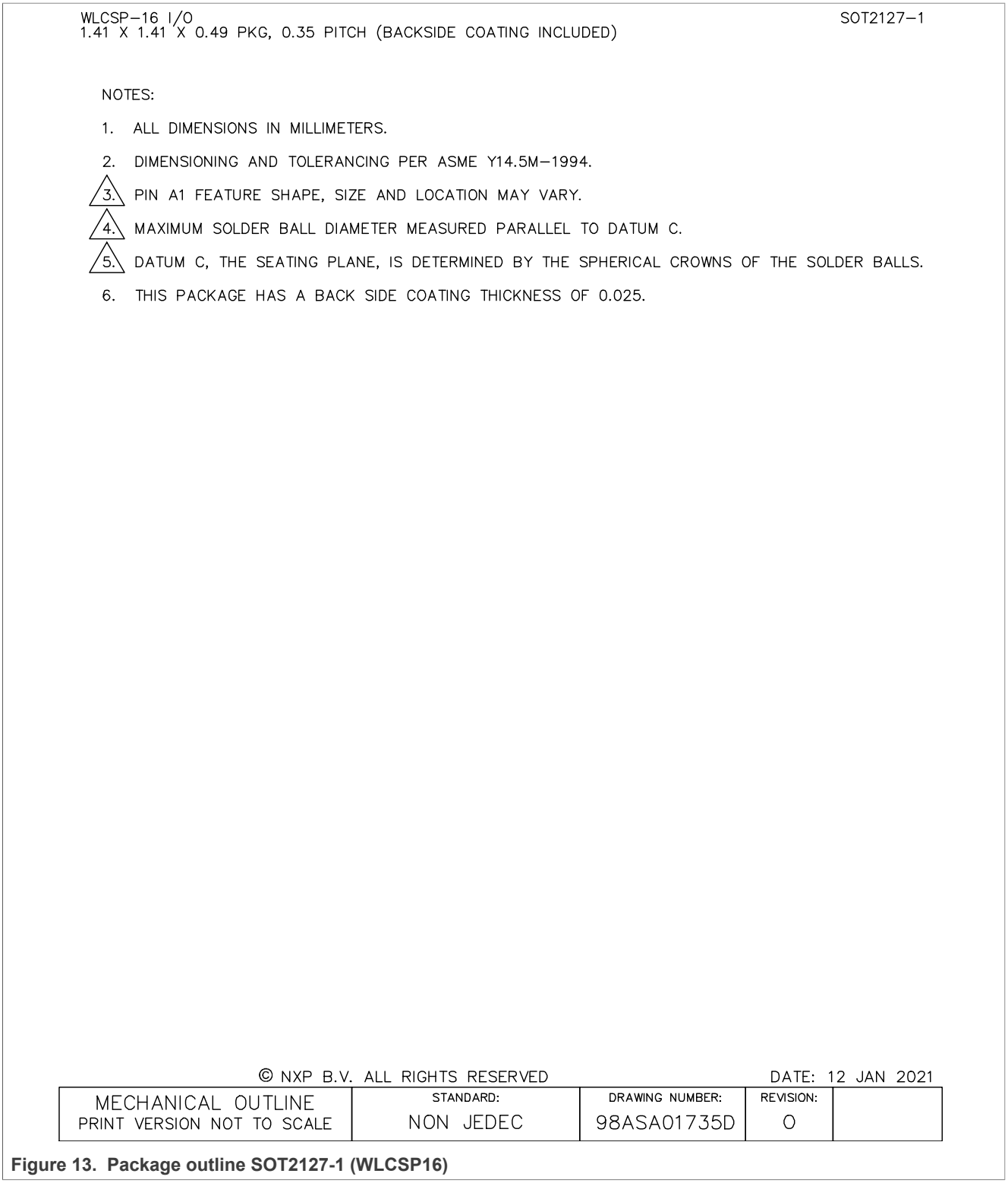
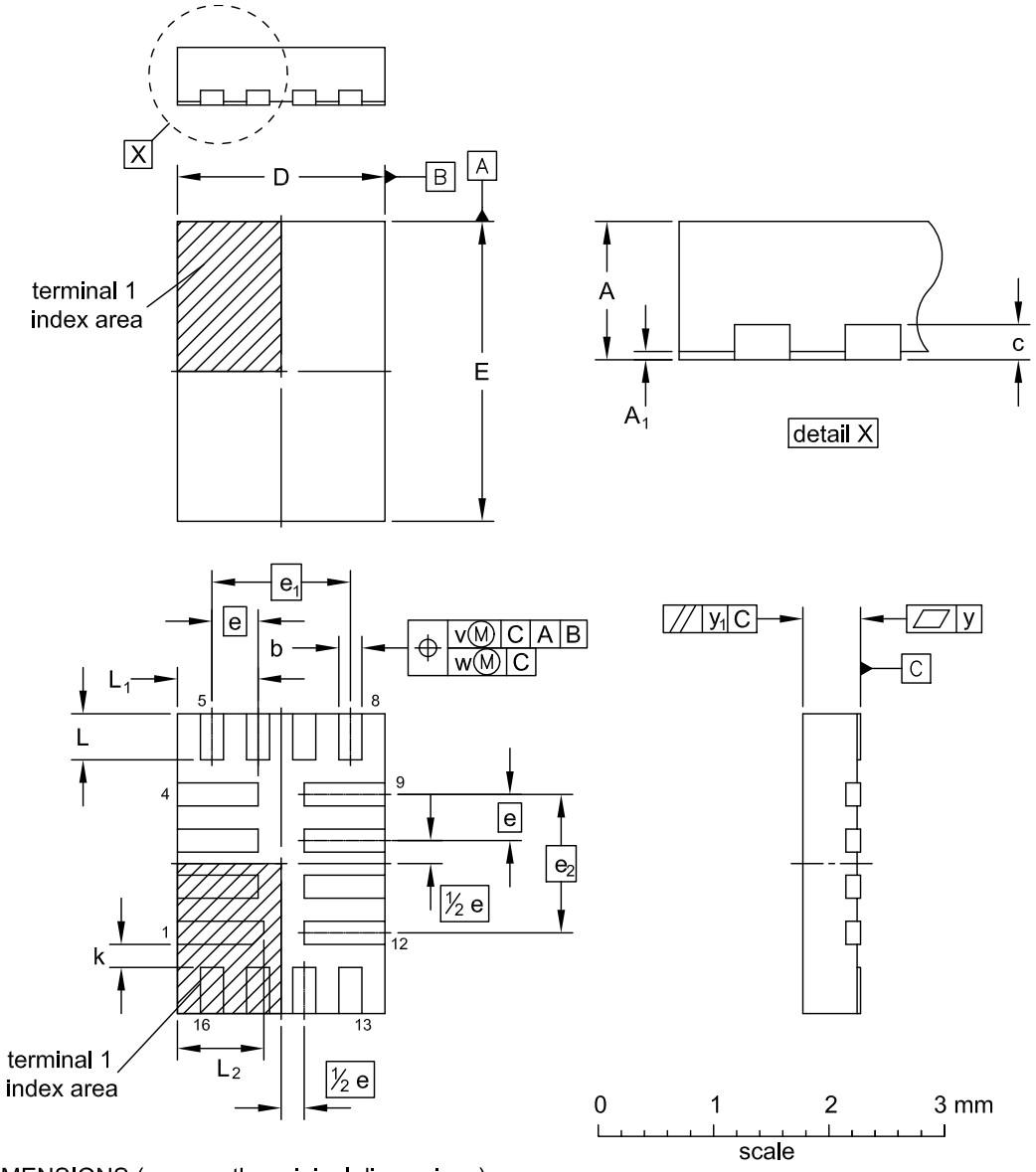


Figure 13. Package outline SOT2127-1 (WLCSP16)



DIMENSIONS (mm are the original dimensions)

UNIT		$A^{(1)}$	A_1	b	c	$D^{(1)}$	$E^{(1)}$	e	e_1	e_2	k	L	L_1	L_2	v	w	y	y_1
mm	MAX	0.50	0.05	0.25		1.90	2.70					0.45	0.75	0.80				
	NOM			0.20	0.127	1.80	2.60	0.40	1.20	1.20	0.2	0.40	0.70	0.75	0.1	0.05	0.05	0.1
	MIN		0.00	0.15		1.70	2.50					0.35	0.65	0.70				

Notes
1. Plastic or metal protrusions of 0.075 maximum per side are not included.

Figure 14. Package outline SOT1161-2 (XQFN16)

16 PCB layout

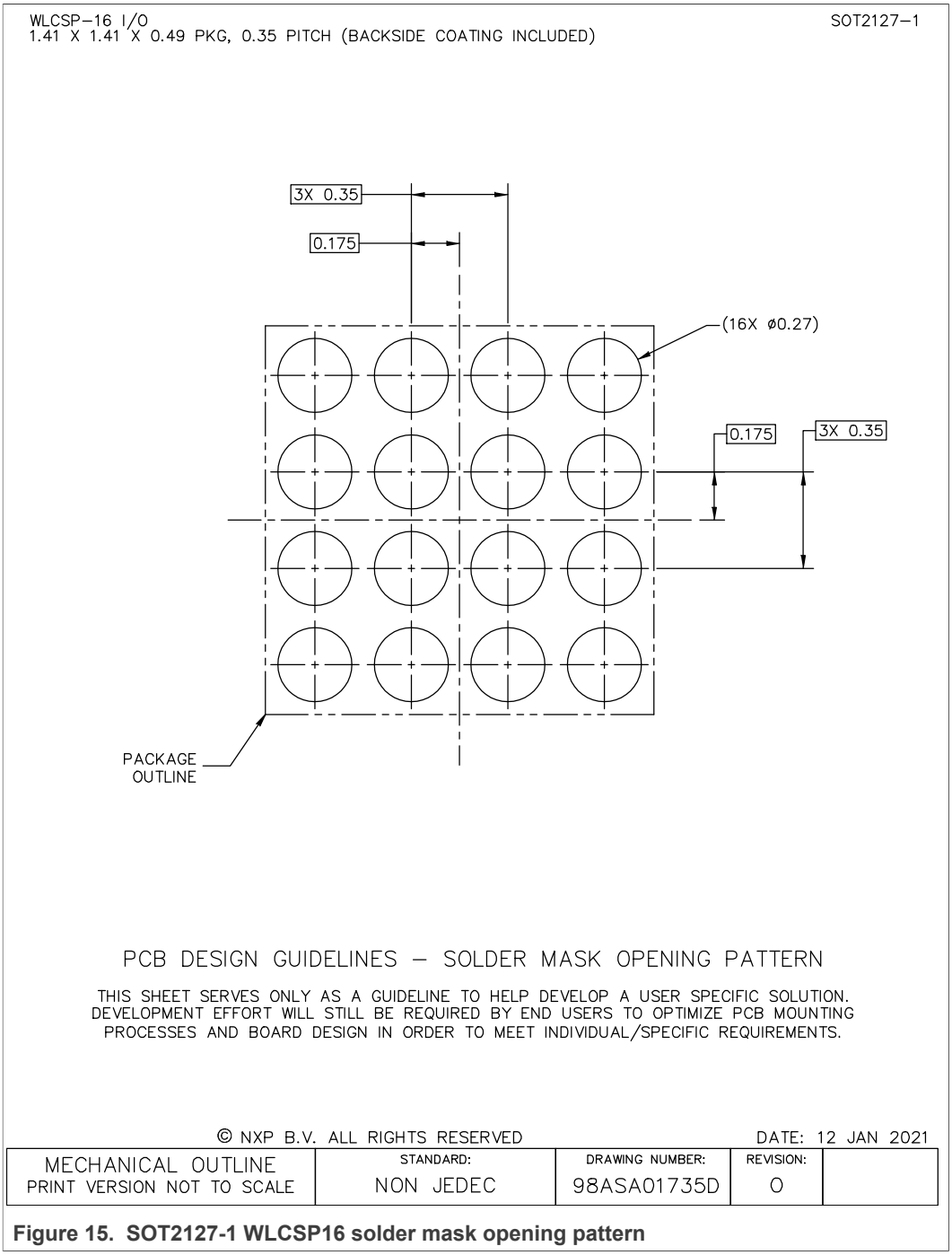


Figure 15. SOT2127-1 WLCSP16 solder mask opening pattern

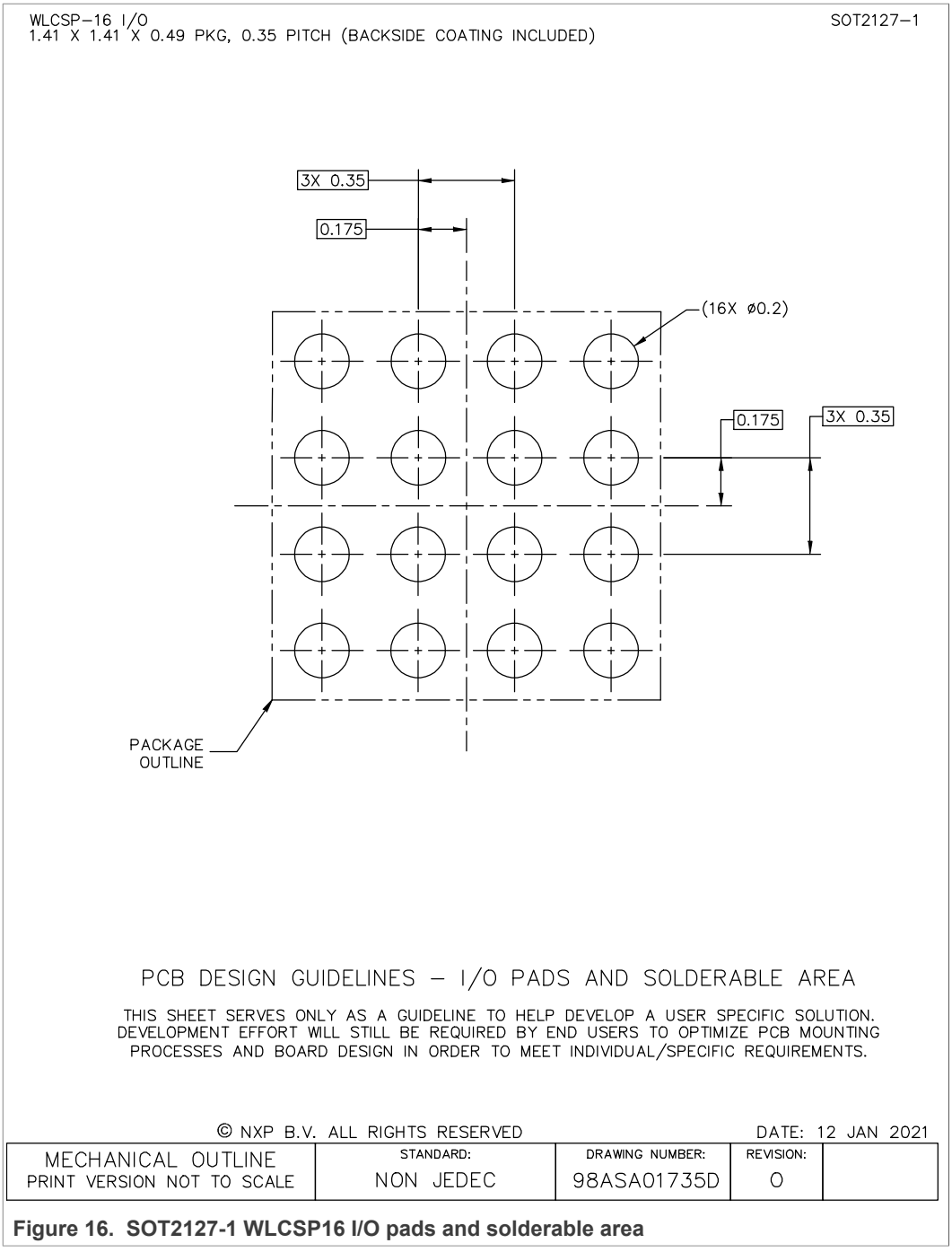


Figure 16. SOT2127-1 WLCSP16 I/O pads and solderable area

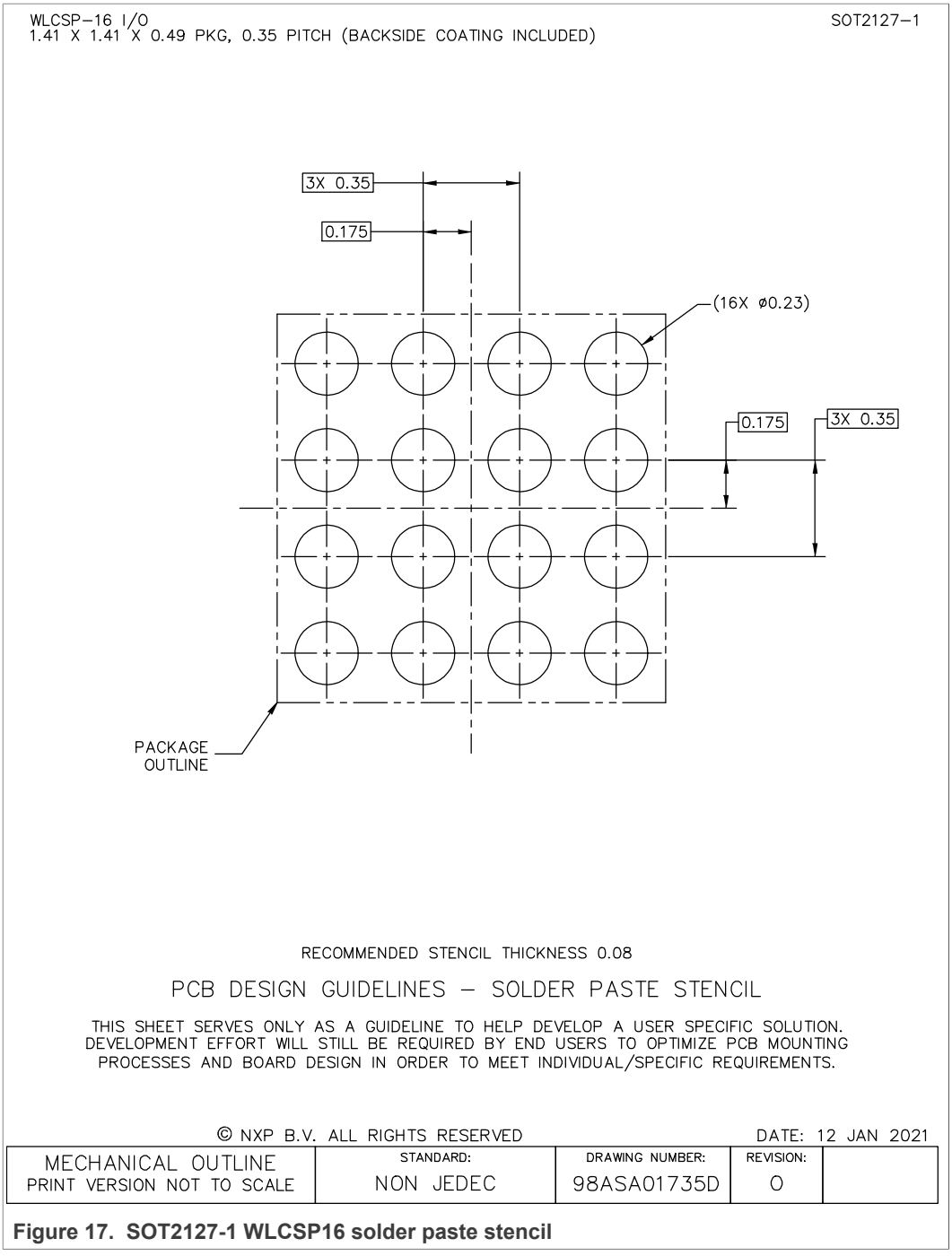


Figure 17. SOT2127-1 WLCSP16 solder paste stencil

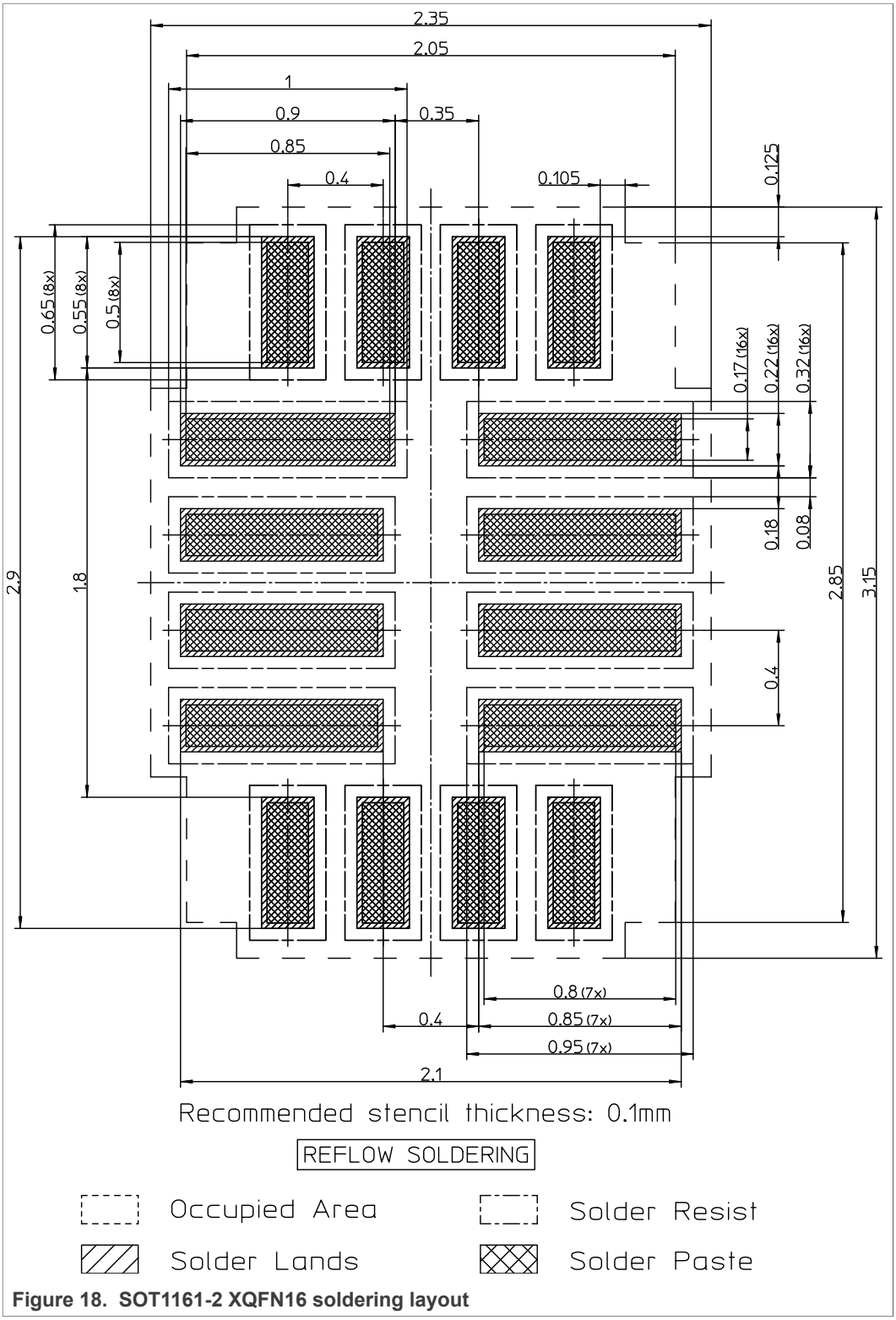


Figure 18. SOT1161-2 XQFN16 soldering layout

17 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 19) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 16 and Table 17

Table 16. SnPb eutectic process (from J-STD-020D)

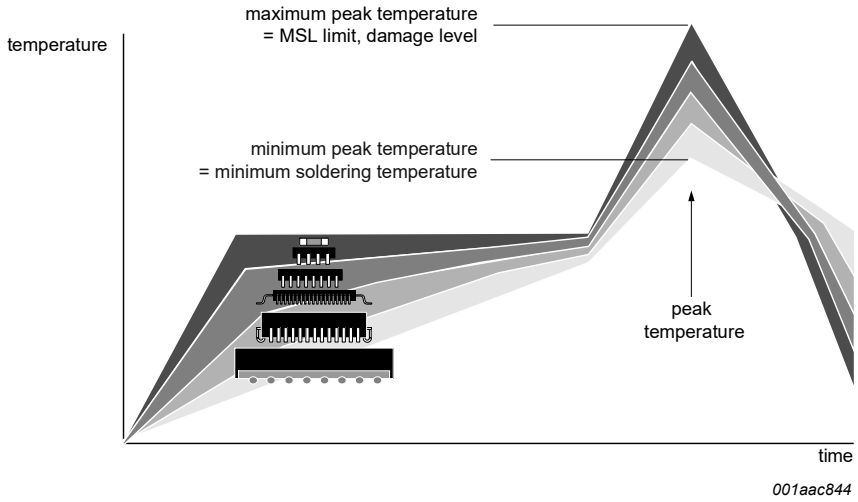
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 17. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 19.



MSL: Moisture Sensitivity Level

Figure 19. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

18 Abbreviations

Table 18. Abbreviations

Acronym	Description
DUT	Device Under Test
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
MMC	MultiMedia Card
PCB	Printed-Circuit Board
RoHS	Restriction of Hazardous Substances
SD	Secure Digital
WLCSP	Wafer-Level Chip-Scale Package

19 Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NVT4858 v.2.1	20211112	Product data sheet	202111014I	NVT4858 v.2.0
Modifications:	• Changed 1.95 V to 1.98 V and 1.65 V to 1.62 V throughout the data sheet • Table 11: Removed hysteresis voltage from "Automatic enable feature: V_{CCB}" • Table 13 and Table 14: Added skew information for NVT4858HK (QFN) and NVT4858UK (WLCSP)			
NVT4858 v.2.0	20210915	Product data sheet	-	NVT4858 v.1.0
NVT4858 v.1.0	20210421	Product data sheet	-	-

20 Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

20.2 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

20.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

20.4 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Tables

Figures

Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 12 November 2021
Document identifier: NVT4858