

SN75ALS165 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

SLLS023B – JUNE 1986 – REVISED AUGUST 1989

MEETS IEEE STANDARD 488-1978 (GPIB)

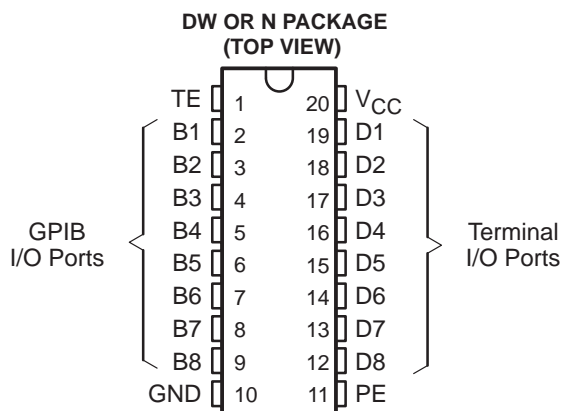
- 8-Channel Bidirectional Transceiver
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation . . . 46 mW Max Per Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance PNP Inputs
- Receiver Hysteresis . . . 650 mV Typ
- No Loading of Bus When Device Is Powered Down ($V_{CC} = 0$)
- Power-Up/Power-Down Protection (Glitch Free)
- Driver and Receiver Can Be Disabled Simultaneously

description

The SN75ALS165 eight-channel general-purpose interface bus transceiver is a monolithic, high-speed, advanced low-power Schottky device designed for two-way data communications over single-ended transmission lines. It is designed to meet the requirements of IEEE Standard 488-1978. The transceiver features driver outputs that can be operated in either the passive-pullup or 3-state mode. If talk enable (TE) is high, these ports have the characteristics of passive-pullup outputs when pullup enable (PE) is low and of 3-state outputs when PE is high. Taking TE low places these ports in the high-impedance state. Taking TE and PE low places both the drivers and receivers in the high-impedance state. The driver outputs are designed to handle loads up to 48 mA of sink current.

An active turn-off feature is incorporated into the bus-terminating resistors so that the device exhibits a high impedance to the bus when $V_{CC} = 0$. When combined with the SN75ALS161 or SN75ALS162 management bus transceiver, the pair provides the complete 16-wire interface for the IEEE 488 bus.

The SN75ALS165 is manufactured in a 20-pin package and is characterized for operation from 0°C to 70°C.



NOT RECOMMENDED FOR NEW DESIGN

Function Tables

EACH DRIVER				EACH RECEIVER			
INPUTS			OUTPUT	INPUTS			OUTPUT
D	TE	PE	B	B	TE	PE	D
H	H	H	H	L	L	H	L
L	H	X	L	H	L	H	H
H	X	L	Z†	X	H	X	Z
X	L	X	Z†	X	X	L	Z

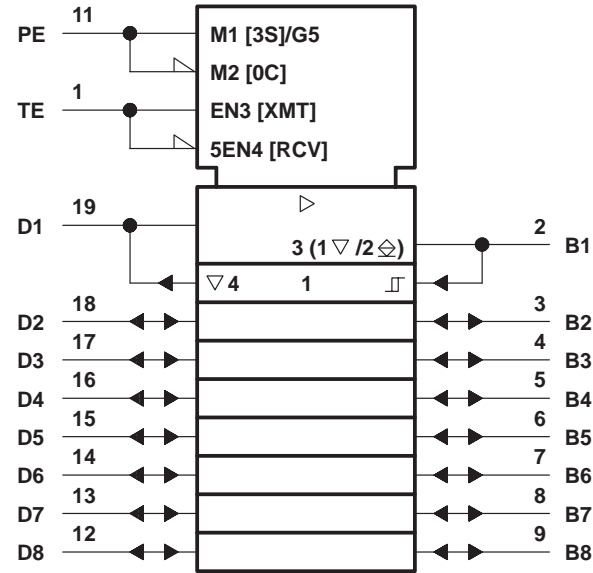
H = high level, L = low level, X = irrelevant,
Z = high-impedance state

† This is the high-impedance state of a normal 3-state output modified by the internal resistors to V_{CC} and GND.

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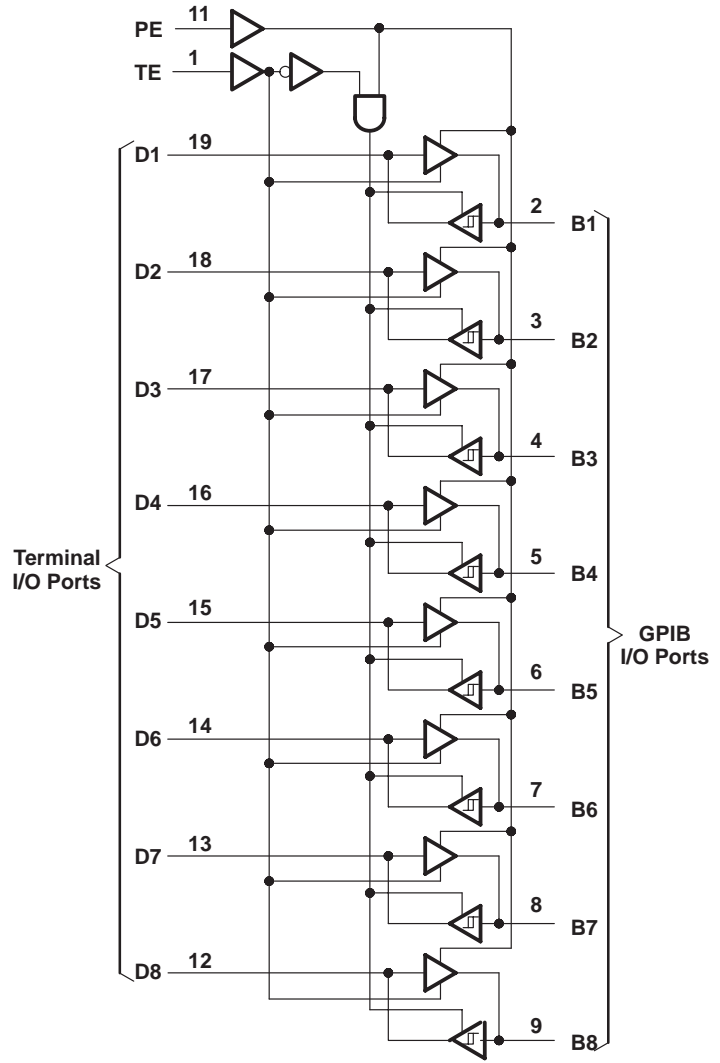
logic symbol†



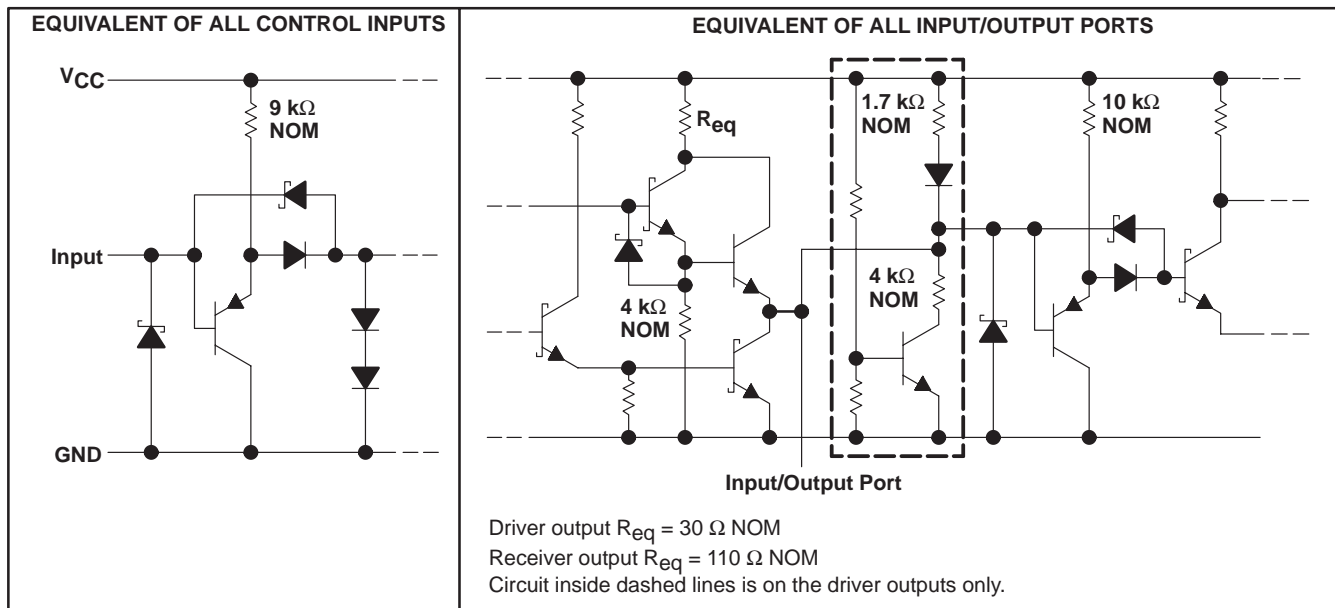
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

- ▽ Designates 3-state outputs
- ◇ Designates passive-pullup outputs

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Low-level driver output current	100 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds	260°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with pullups active			-5.2	mA
	Terminal ports			-800	μA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	mA
Operating free-air temperature, T_A		0		70	°C

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18 \text{ mA}$		-0.8	1.5		V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus		0.4	0.65		V
$V_{OH}‡$	High-level output voltage	Terminal	$I_{OH} = -800 \mu\text{A}$, TE at 0.8 V	2.7	3.5		V
		Bus	$I_{OH} = -5.2 \text{ mA}$, PE and TE at 2 V	2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	$I_{OL} = 16 \text{ mA}$, TE at 0.8 V	0.3	0.5		V
		Bus	$I_{OL} = 48 \text{ mA}$, TE at 2 V	0.35	0.5		
I_I	Input current at maximum input voltage	Terminal	$V_I = 5.5 \text{ V}$		0.2	100	μA
I_{IH}	High-level input current	Terminal and control inputs	$V_I = 2.7 \text{ V}$		0.1	20	μA
I_{IL}	Low-level input current		$V_I = 0.5 \text{ V}$		-10	-100	μA
$V_{I/O(\text{bus})}$	Voltage at bus port	Driver disabled	$I_I(\text{bus}) = 0$	2.5	3	3.7	V
			$I_I(\text{bus}) = -12 \text{ mA}$			-1.5	
$I_{I/O(\text{bus})}$	Current into bus port	Power on	Driver disabled	$V_I(\text{bus}) = -1.5 \text{ V to } 0.4 \text{ V}$	-1.3		mA
				$V_I(\text{bus}) = 0.4 \text{ V to } 2.5 \text{ V}$	0	-3.2	
				$V_I(\text{bus}) = 2.5 \text{ V to } 3.7 \text{ V}$		2.5 -3.2	
				$V_I(\text{bus}) = 3.7 \text{ V to } 5 \text{ V}$	0	2.5	
				$V_I(\text{bus}) = 5 \text{ V to } 5.5 \text{ V}$	0.7	2.5	
		Power off	$V_{CC} = 0$, $V_I(\text{bus}) = 0 \text{ to } 2.5 \text{ V}$		40	μA	
I_{OS}	Short-circuit output current	Terminal		-15	-35	-75	mA
		Bus		-25	-50	-125	
I_{CC}	Supply current	No load	Terminal outputs low and enabled		42	65	mA
			Bus outputs low and enabled		52	80	
$C_{I/O(\text{bus})}$	Bus-port capacitance	$V_{CC} = 5 \text{ V to } 0$, $V_{I/O} = 0 \text{ to } 2 \text{ V}$, $f = 1 \text{ MHz}$			30		pF

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ V_{OH} applies for 3-state outputs only.



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switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), $V_{CC} = 5\text{ V}$

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
tPLH	Propagation delay time, low-to-high-level output	Terminal	Bus	$C_L = 30\text{ pF}$, See Figure 1		7	20	ns
tPHL	Propagation delay time, high-to-low-level output					8	20	
tPLH	Propagation delay time, low-to-high-level output	Bus	Terminal	$C_L = 30\text{ pF}$, See Figure 2		7	14	ns
tPHL	Propagation delay time, high-to-low-level output					9	14	
tPZH	Output enable time to high level	TE	Bus	$C_L = 15\text{ pF}$, See Figure 3		19	30	ns
tPHZ	Output disable time from high level					5	12	
tPZL	Output enable time to low level					16	35	
tPLZ	Output disable time from low level					9	20	
tPZH	Output enable time to high level	TE	Terminal	$C_L = 15\text{ pF}$, See Figure 4		13	30	ns
tPHZ	Output disable time from high level					12	20	
tPZL	Output enable time to low level					12	20	
tPLZ	Output disable time from low level					11	20	
t _{en}	Output pullup enable time	PE	Terminal	$C_L = 15\text{ pF}$, See Figure 5		11	22	ns
t _{dis}	Output pullup disable time					6	12	

† All typical values are at $T_A = 25^\circ\text{C}$.

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PARAMETER MEASUREMENT INFORMATION

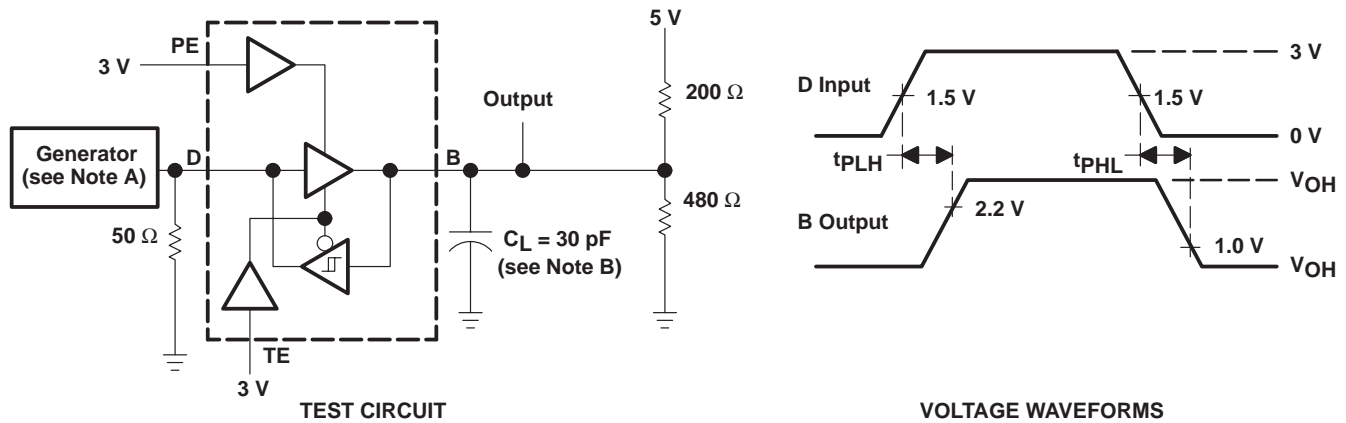


Figure 1. Terminal-to-Bus Test Circuit and Voltage Waveforms

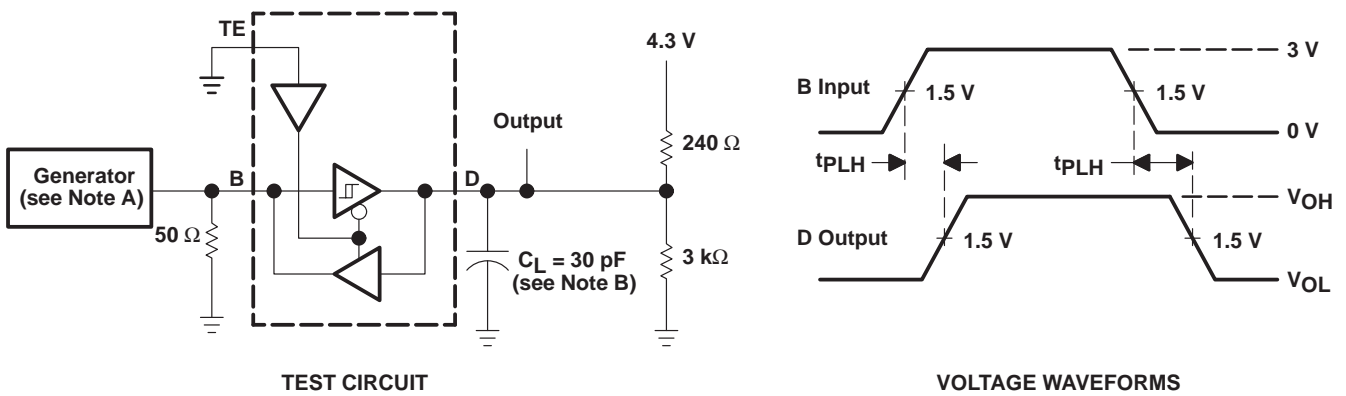


Figure 2. Bus-to-Terminal Test Circuit and Voltage Waveforms

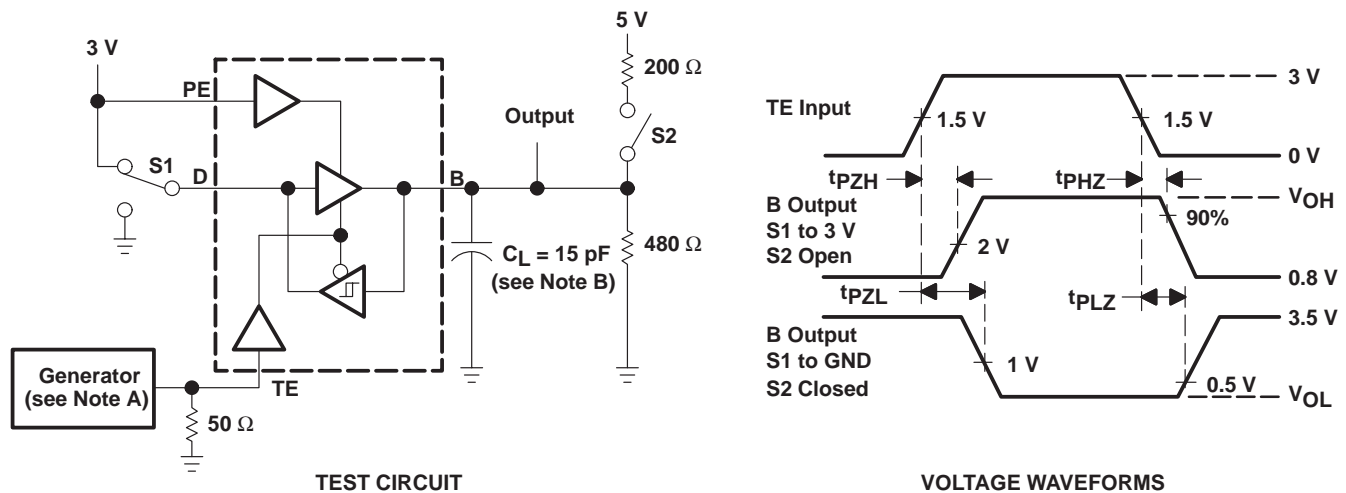


Figure 3. TE-to-Bus Test Circuit and Voltage Waveforms

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_0 = 50 \Omega$.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

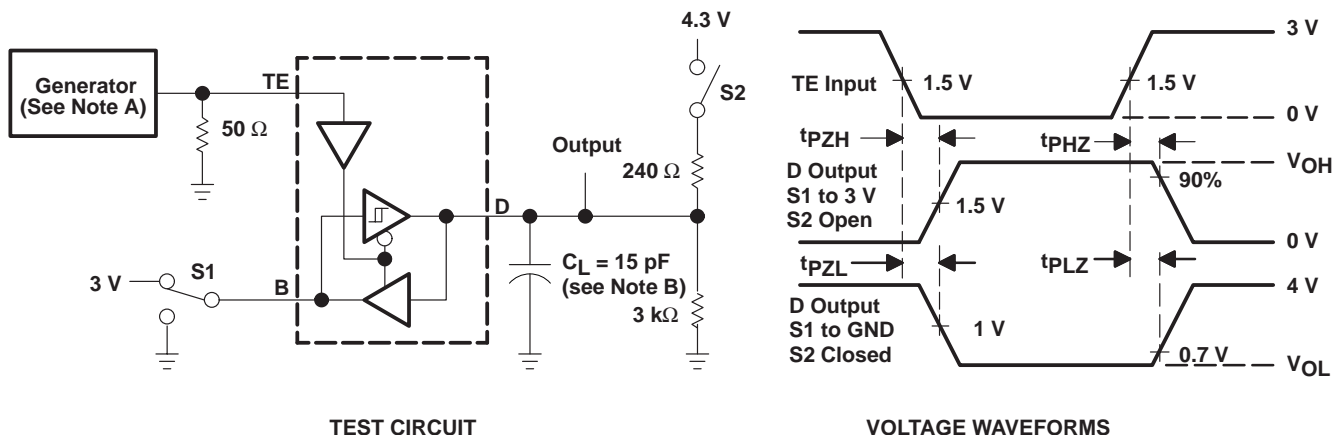


Figure 4. TE-to-Terminal Test Circuit and Voltage Waveforms

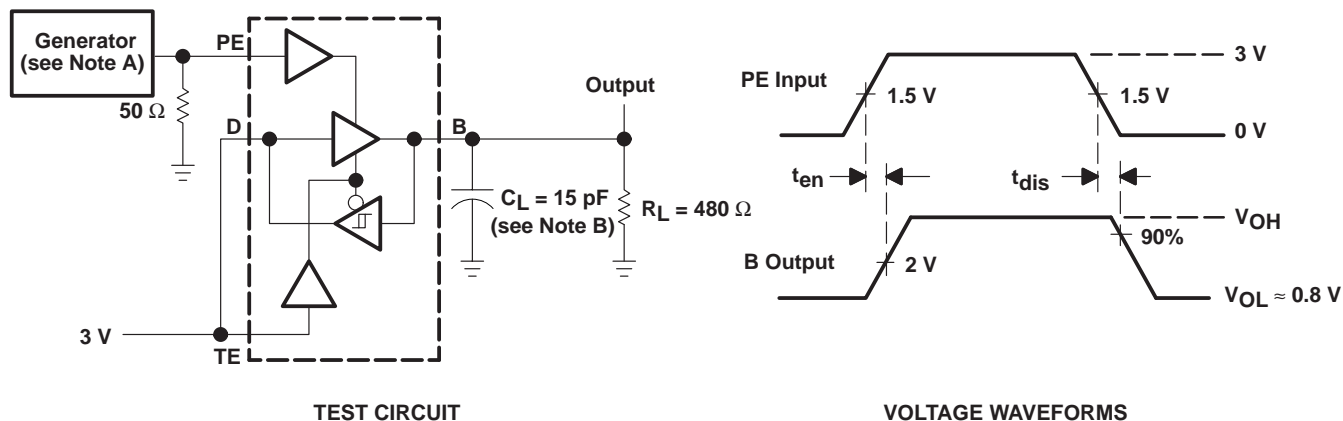


Figure 5. PE-to-Bus Test Circuit and Voltage Waveforms

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_O = 50 \Omega$.
B. C_L includes probe and jig capacitance.

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TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

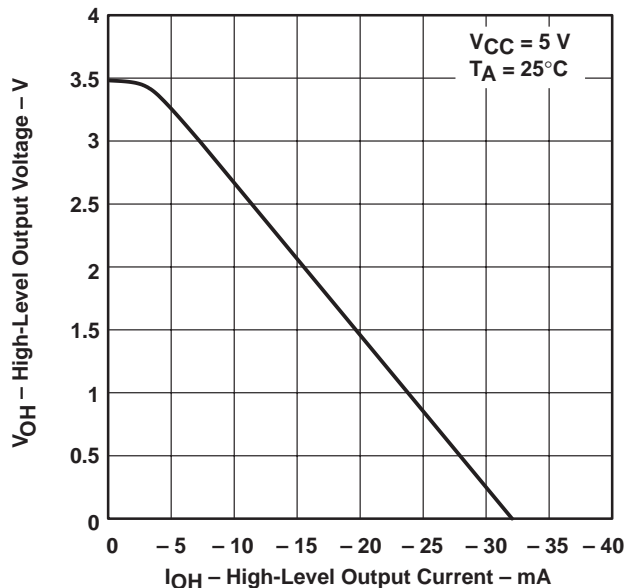


Figure 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

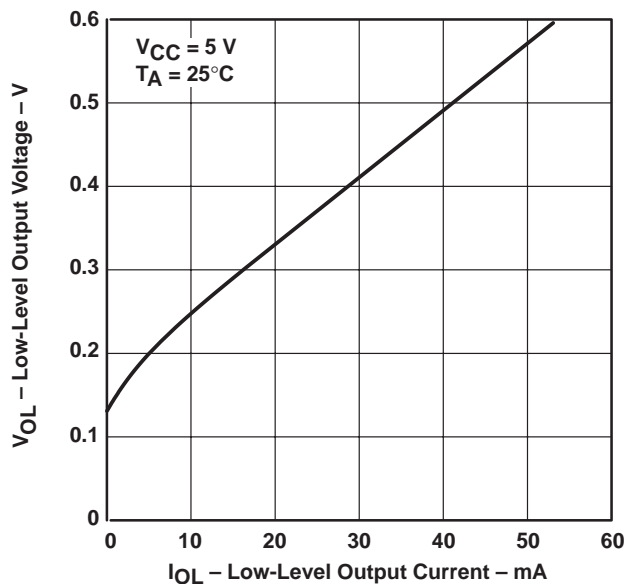


Figure 7

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

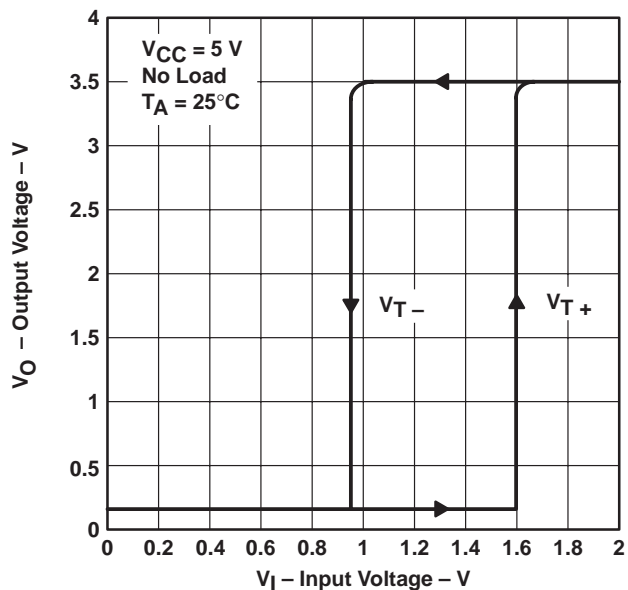


Figure 8

TYPICAL CHARACTERISTICS

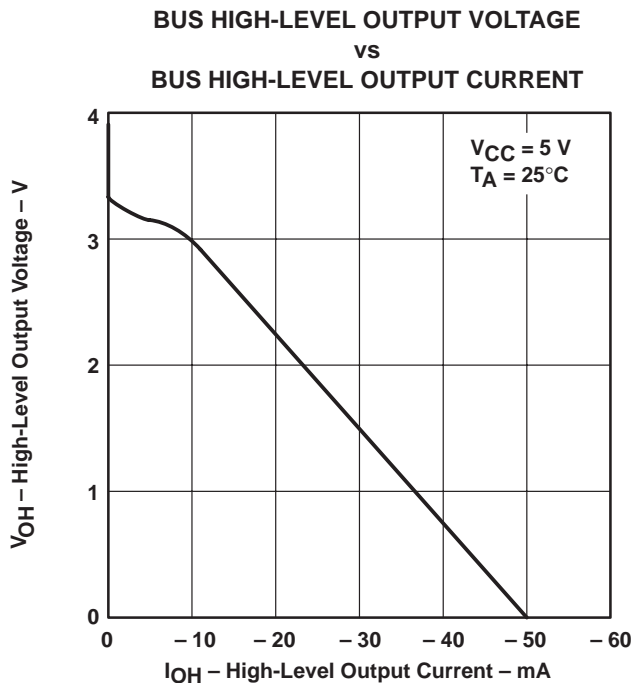


Figure 9

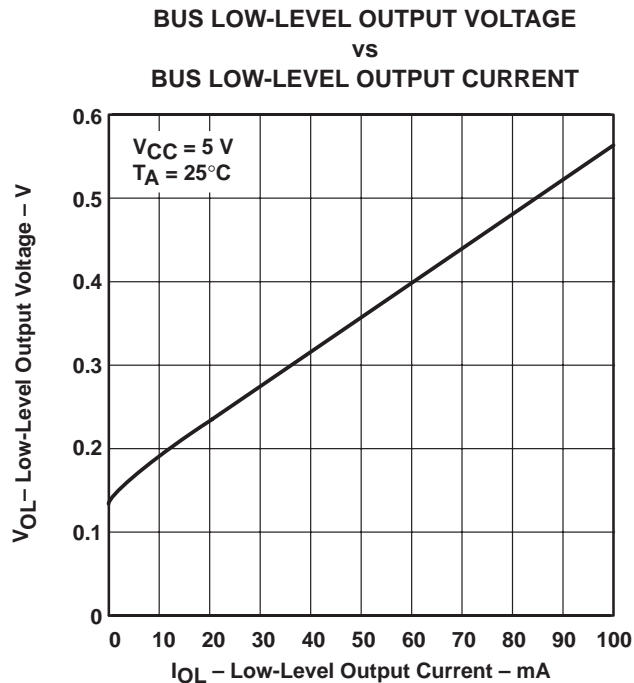


Figure 10

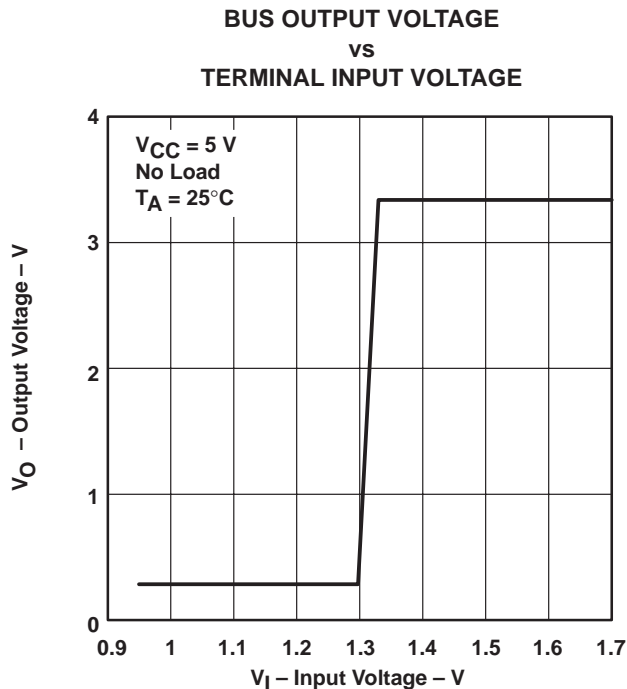


Figure 11

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN75ALS165DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN75ALS165N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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