PI3HDX1204E

HDMI 2.0 6Gbps Linear ReDriver with High EQ, Low Jitter and DP++ Level Shifter

Features

- ➔ HDMI 2.0 Compliant TMDS Linear Redriver™ with 2x Improved Jitter Performance than conventional technology
- ➔ DP++ Level Shifting for HDMI output
- ➔ Linear Redriver increases TMDS Link Margin supporting Sink-side DFE (Decision Feedback Equalizers) receiver
- ➔ Every Channel's Equalizations, Swings and Gains are programmable Independently
- ➔ Supports Pin- strap and I2C Programming
- ➔ Flexible 4-bit I2C address selectable (42-pin, ZH package)
- ➔ Power supply: 3.3V
- ➔ Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- ➔ Halogen and Antimony Free. "Green" Device (Note 3)
- ➔ For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.

  https://www.diodes.com/quality/product-definitions/
- ➔ Package (Pb-Free & Green):
  - ♦ 32-pin TQFN (3x6mm)
  - ♦ 42-pin TQFN (3.5x9mm)

Applications

- ➔ TVs and Monitors

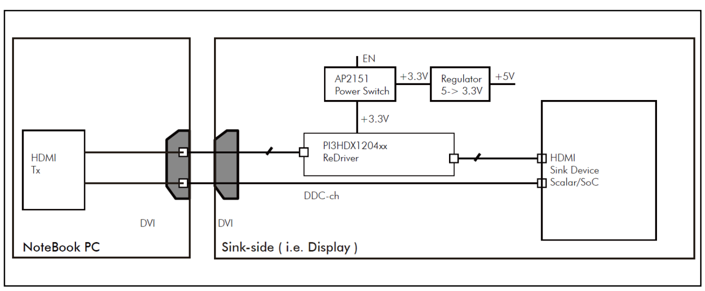

Figure 1-1 HDMI Sink-side Application

Description

PI3HDX1204E is a HDMI 2.0 Linear ReDriver with built-in Level Shifter, supporting minimal additive jitters. The linear ReDriver allows easy handling of the signal integrity issues known in the component placement and the setting parameters of Equalization and Flat Gain compensation between the Source-side and Sink-side link system.

The advantage of Linear ReDriver does not block the original source differential signals to maximize the Sink-side Receiver Digital Feedback Equalization (DFE) circuits to improve signal quality of the high-speed link. The output swing range can be set by Swing control for the power saving.

The device uses pin-strapping or I2C programming to optimize the signal quality over a variety of physical media by reducing Inter-symbol Interference (ISI) jitters.

Ordering Information

Ordering Number	Package Code	Package Description
PI3HDX1204EZLEX	ZL	32-Contact, Very Thin Quad Flat No-Lead (TQFN)
PI3HDX1204EZHEX	ZH	42-Contact, Very Thin Quad Flat No-Lead (TQFN)

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green, I=Industrial
5. X suffix = Tape/Reel

ReDriver is a trademark of Diodes Incorporated.

2. General Information

2.1 Revision History

Date	Revision	Description
Mar 2016	-	Pin-out (p8): FGx(x=0,1) Pin name typo fixed.
Apr 2016	-	Electrical(p17): tSK_INTRA_OUT changed 5 typ, 10 max ps
May 2016	-	Application(p30): More informative system EE contents added. DDC source-side pull-up changed to 10 kΩ from 2 kΩ
Jun 2016	-	Mechanical (p39): EPAD outline changed
Oct 2016	-	Diodes Disclaimer added
Aug 2017	-	Clarified Output Swing range control in functional description. PI3HDX1204B1 limiting and PI3HDX1204E linear pin-out comparison added in generic information session
Dec 2017	1	Updated package mechanical drawing with latest (p46). Change to whole Revision number
Feb 2021	2	Updated Description Updated Feature Updated Part Marking Updated Part Numbers Information Updated Pin Configuration Updated Pin Description Updated Features
Sept 2021	3	Delete PI3HDX1204D to PI3HDX1204E PDN Notice Section Updated Section Feature Updated Section 2.2 Similar Products Comparison Updated Section 6.3.4 Switching I/O Characteristics Updated Section 7.4.1 Trace Card Loss Informations Updated Figure 7.7 Frequency Response vs EQ Remove Pin-out Co-layout Comparison Remove Section 7.2 Sink-side ReDriver Application and move the image to the first page

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3. Pin Configuration

3.1 Pin Configuration

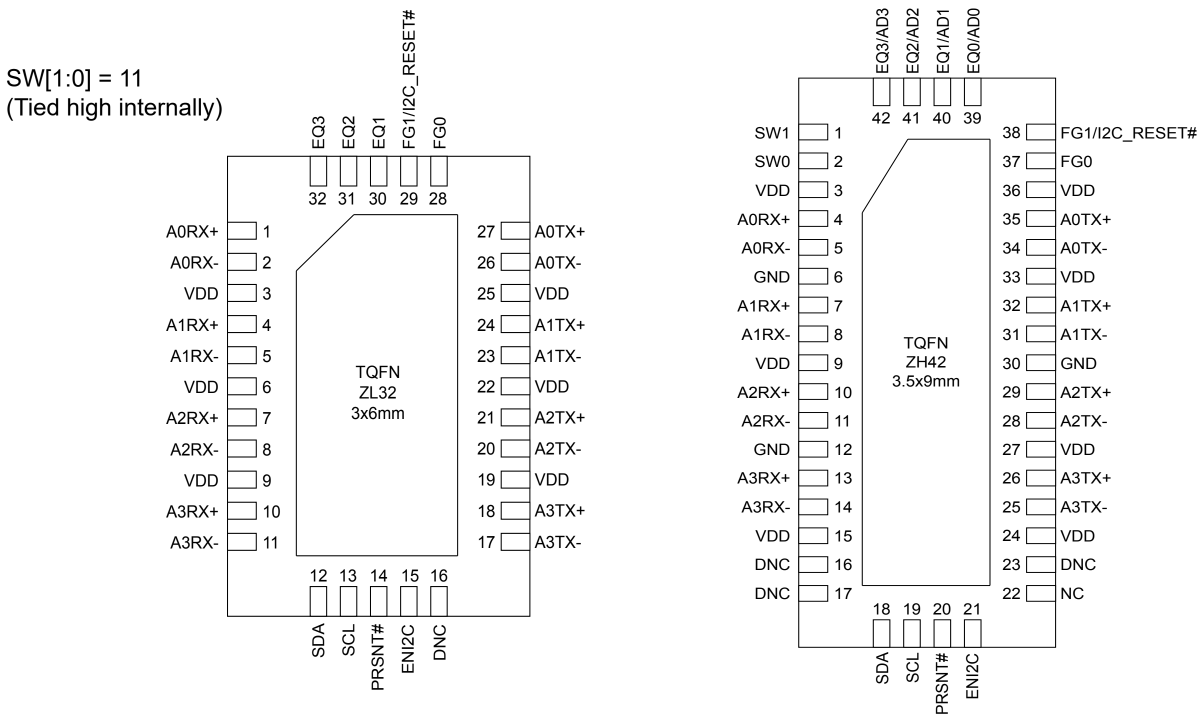


Figure 3-1 32/42-pin package pin-out

Note: In TMDS Data and Clock Differential Pairs of Input and Output, the polarity (+/- or P/N) of each pairs and high-speed data channels A[3:0] can use interchangeably. Output pins of polarity and data channel will always follow the input polarity and data channel assignment changes.

3.1 Pin Description

3.1.1 32-ZL Pin Package

Pin #	Pin Name	Type	Description
Data Signals			
1, 2	A0RX+ A0RX-	I	TMDS differential positive/negative input for Channel A0, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
27, 26	A0TX+, A0TX-	O	TMDS differential positive/negative outputs for Channel A0, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
4, 5	A1RX+, A1RX-	I	TMDS differential positive/negative inputs for Channel A1, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
24, 23	A1TX+, A1TX-	O	TMDS differential positive/negative outputs for Channel A1, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
7, 8	A2RX+, A2RX-	I	TMDS differential positive/negative inputs for Channel A2, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
21, 20	A2TX+, A2TX-	O	TMDS differential positive/negative outputs for Channel A2, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
10, 11	A3RX+, A3RX-	I	TMDS differential positive/negative inputs for Channel A3, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
18, 17	A3TX+, A3TX-	O	TMDS differential positive/negative outputs for Channel A3, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
Control Signals			
13	SCL	I/P	I^2C Serial Clock line
12	SDA	I/O	I^2C Serial Data line
14	PRSNT#	I	Cable Present Detect input. This pin has internal 100KΩ pull-up. The pin is active when both PIN mode (ENI2C = LOW) and I2C mode (ENI2C = HIGH). When High, a cable is not present, and the device is put in lower power mode. When Low, the device is enabled and in normal operation.
15	ENI2C	I	I2C Enable pin. When LOW, each channel is programmed by the external pin voltage. When HIGH, each channel is programmed by the data stored in the I2C bus.
32, 31, 30	EQ[3:1]	I	EQ Control pin. Inputs with internal 100kΩ pull-up. This pins set the amount of Equalizer Boost in all channels when ENI2C is low.
	AD[3:1]	I	Address bits control pins for I2C programming with internal 100kΩ pullup.
29	FG1/I2C_ RESET#	I	Shared pin for Gain Control bit-1 and I2C Reset pin. Inputs with internal 100kΩ pullup resistor. (1) Sets the output flat gain level bit-1 on all channels when ENI2C is Low. (2) I2C Reset pin. Active Low to reset the registers to default state.

Pin #	Pin Name	Type	Description
28	FG0	I	Flat Gain control bit-0 pin. Inputs with internal 100kΩ pull up resistor. Sets the output flat gain level on all channels when ENI2C is low.
Power Pins			
3, 6, 9, 19, 22, 25	VDD	PWR	3.3V Power supply pins
Center Pad	GND	GND	Exposed Ground pad.
16	DNC		Do Not Connect

3.1.2 42-ZH Pin Package

Pin #	Pin Name	Type	Description
Data Signals			
4, 5	A0RX+ A0RX-	I	TMDS differential positive/negative input for Channel A0, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
35, 34	A0TX+, A0TX-	O	TMDS differential positive/negative outputs for Channel A0, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
7, 8	A1RX+, A1RX-	I	TMDS differential positive/negative inputs for Channel A1, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
32, 31	A1TX+, A1TX-	O	TMDS differential positive/negative outputs for Channel A1, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
10, 11	A2RX+, A2RX-	I	TMDS differential positive/negative inputs for Channel A2, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
29, 28	A2TX+, A2TX-	O	TMDS differential positive/negative outputs for Channel A2, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
13, 14	A3RX+, A3RX-	I	TMDS differential positive/negative inputs for Channel A3, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
26, 25	A3TX+, A3TX-	O	TMDS differential positive/negative outputs for Channel A3, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
Control Signals			
19	SCL	I	I^2C Serial Clock line
18	SDA	I/O	I^2C Serial Data line
20	PRSNT#	I	Cable Present Detect input. This pin has internal 100KΩ pull-up. The pin is active when both PIN mode (ENI2C = LOW) and I2C mode (ENI2C = HIGH). When High, a cable is not present, and the device is put in lower power mode. When Low, the device is enabled and in normal operation.
21	ENI2C	I	I2C Enable pin. When LOW, each channel is programmed by the external pin voltage. When HIGH, each channel is programmed by the data stored in the I2C bus.
39, 40, 41, 42	EQ[3:1]	I	EQ Control pin. Inputs with internal 100kΩ pull-up. This pins set the amount of Equalizer Boost in all channels when ENI2C is low.
	AD[3:1]	I	Address bits control pins for I2C programming with internal 100kΩ pullup.
1, 2	SW[1:0]	I	Output Swing control pins. Inputs with internal 100kΩ pull-up. This pin sets the output Voltage Level in all channel when ENI2C is LOW.
38	FG1/I2C_ RESET#	I	Shared pin for Gain Control bit-1 and I2C Reset pin. Inputs with internal 100kΩ pullup resistor. (1) Sets the output flat gain level bit-1 all channels when ENI2C is Low. (2) I2C Reset pin. Active Low to reset the registers to default state.
37	FG0	I	Flat Gain control bit-0 pin. Inputs with internal 100kΩ pull up resistor. Sets the output flat gain level on all channels when ENI2C is low.

Pin #	Pin Name	Type	Description
22	NC	NC	No Connect
Power Pins			
3, 9, 15, 24, 27, 33, 36	VDD	PWR	3.3V Power supply pins
6, 12, 30, Center Pad	GND	GND	Exposed Ground pad.
16, 17, 23	DNC		Do Not Connect

4. Functional Description

4.1 Functional Block

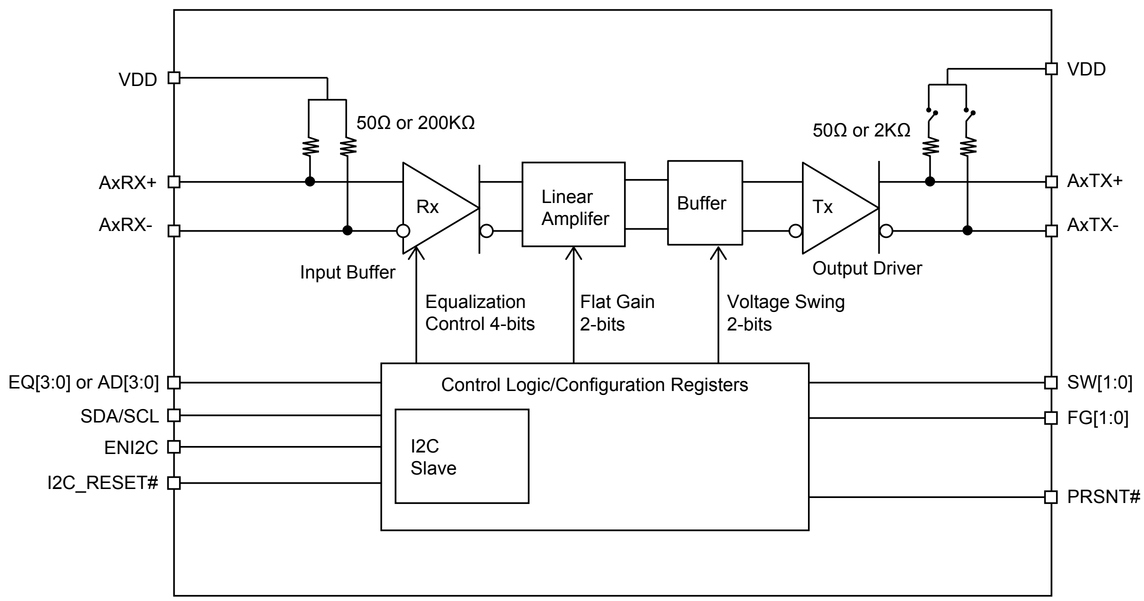


Figure 4-1 Functional Block Diagram

4.2 Function Description

4.2.1 Pin Strap or I2C Control

Pin Strap or I2C mode is enabled thru ENI2C pin. When ENI2C pin is LOW, the chip operates in Pin Control Mode. In Pin control mode, for 42 pin package EQ[3:0] pins control the 16 equalizer settings for all channels (see table) from 3.6dB for 0000 setting to 8.9dB for 1111 setting. For 32 pin package, there are 8 settings from 4dB for 000 to 8.9dB for 111. FG[1:0} controls the 4 output Flat Gain settings for all channels (see table) from -3.5dB to 2.5dB. SW[1:0] control the 4 output voltage levels (see table) from 1100mV to 1400mV. When ENI2C pin is HIGH, he chip operates in I2C mode. In this mode, EQ[2:0}, FG[1:0} and SW1 powerup values are derived from the corresponding input pins. Later thru I2C programming, those values can be changed.

4.2.2 Power-Down/Enable

When PRSNT# is set to "1", device enter to the power-down mode. When Input 200kΩ and Output High Impedance (HIZ) termination resisters set, each individual channels Ax(x=0,1,2,3) can program the I2C register.

4.2.3 Input Equalization Setting

The EQx(x=0,1,2,3) pins are the pin-strap option for each Ax(x=0,1,2,3) channels. It can also be programmable by the I2C mode.

Table 4-1. Equalization Setting for 42-pin

EQ3	EQ2	EQ1	EQ0	6Gbps Input (dB)
0	0	0	0	3.6
0	0	0	1	4.0
0	0	1	0	4.4
0	0	1	1	4.7
0	1	0	0	5.1
0	1	0	1	5.5
0	1	1	0	5.9
0	1	1	1	6.2
1	0	0	0	6.6
1	0	0	1	6.9
1	0	1	0	7.3
1	0	1	1	7.6
1	1	0	0	8.0
1	1	0	1	8.2
1	1	1	0	8.6
1	1	1	1	8.9

Table 4-2. Equalization Setting for 32-pin

EQ3	EQ2	EQ1	6Gbps Input (dB)	Notes
0	0	0	4.0	(1) EQ0 pin always tied to "1" internally in 32-pin package.
0	0	1	4.7	
0	1	0	5.5	
0	1	1	6.2	
1	0	0	6.9	
1	0	1	7.6	
1	1	0	8.2	
1	1	1	8.9	

4.2.4 Output -1 dB Compression Swing setting

SWx(x=0,1) affects the linearity of the output when input amplitude changes.

Table 4-3. SW[1:0] Output Swing Setting

SW1	SW0	Voltage Swing mVpp @100MHz	Voltage Swing mVpp @ 6Gbps	Notes
0	0	920	1100	
0	1	1040	1200	
1	0	1280	1300	
1	1	1370	1400	Default Setting. Internally 100kΩ pull-up.

Note: (1) SW[1:0]=11 setting support by I2C programming in 32-pin package

4.2.5 Flat Gain Setting

FGx(x=0,1) two pins are the selection 2 bits for the DC Flat Gain value.

Table 4-4. Flat Gain FG[1:0] Control

FG1	FG0	Gain (dB)
0	0	-3.5
0	1	-1.5
1	0	+0.5
1	1	+2.5

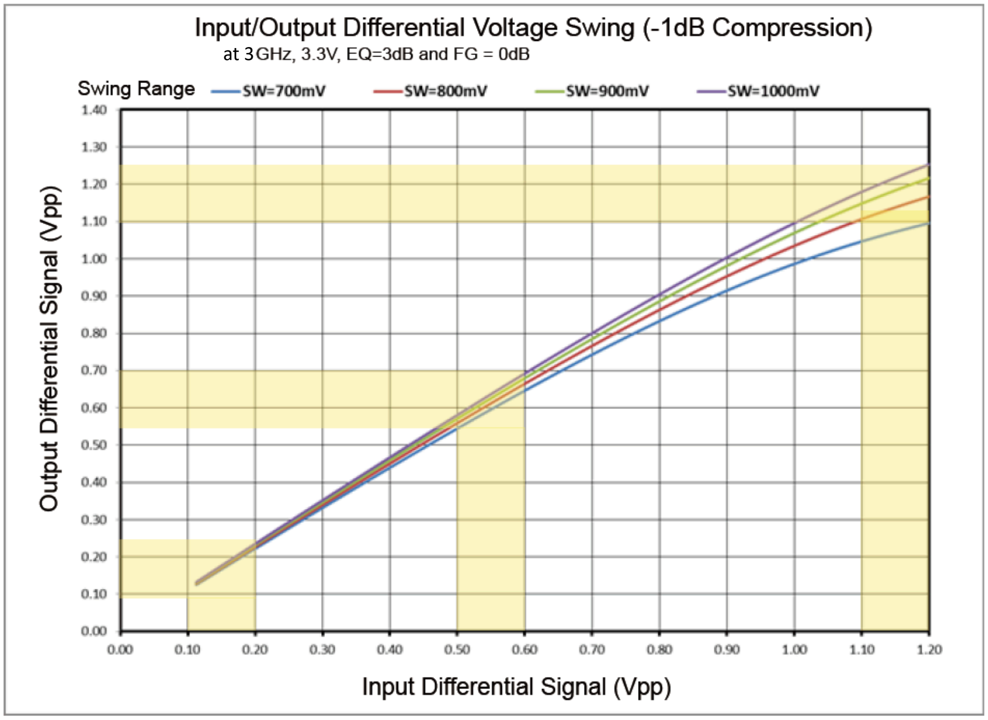


Figure 4-2 Example of Output voltage swing with different SW setting

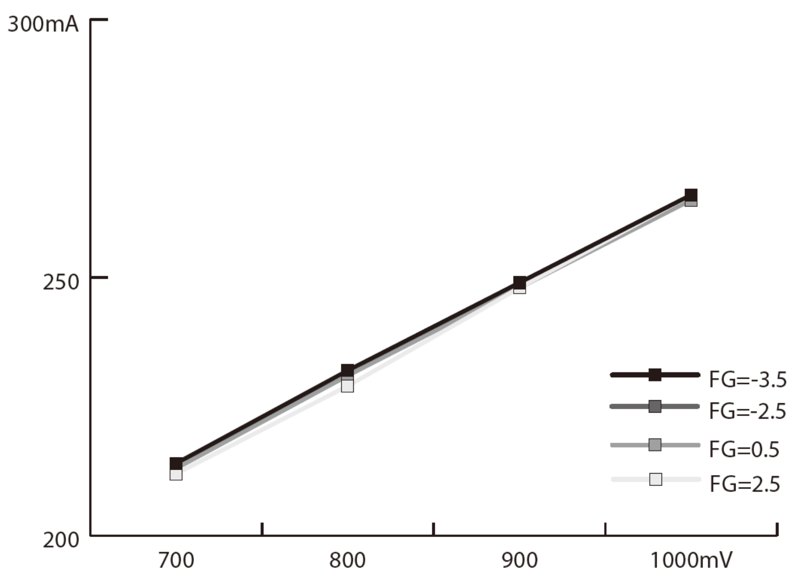


Figure 4-3 Power dissipation mA vs. SW[1:0] setting

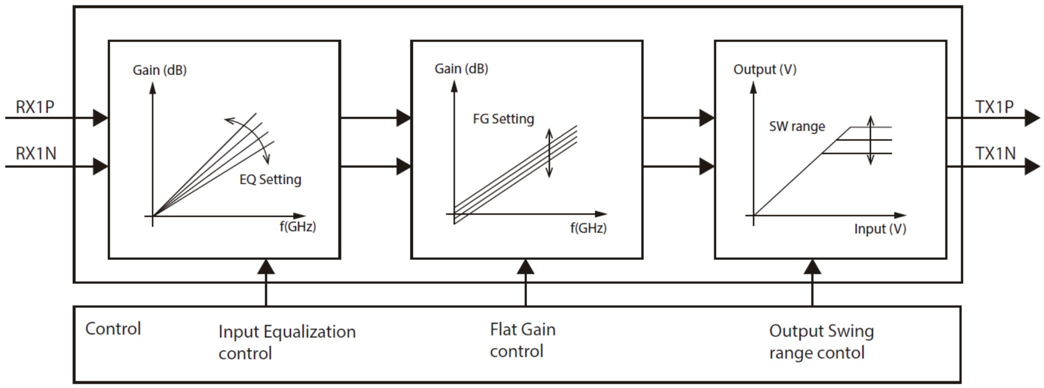


Figure 4-4 Illustration of EQ, Gain and Swing setting

5. I2C Programming

5.1 Programming Registers

5.1.1 I2C address

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	1	AD3	AD2	AD1	AD0	1=R, 0=W

Note: (1) Address A0 is always "1" tied high for 32-pin package.

5.1.2 Configuration Registers

BYTE 0

Bit	Type	Power up condition	Description	Control Affected	Comment
7:0	R		Reserved		

BYTE 1

Bit	Type	Power up condition	Description	Control Affected	Comment
7:0	R		Reserved		

BYTE 2

Bit	Type	Power up condition	Description	Control Affected	Comment
7	R/W	0		A3 Power down	1 = Power down
6	R/W	0		A2 Power down	
5	R/W	0		A1 Power down	
4	R/W	0		A0 Power down	
3	R/W	0		Reserved	
2	R/W	0		Reserved	
1	R/W	0		Reserved	
0	R/W	0		Reserved	

BYTE 3

Bit	Type	Power up condition	Description	Control Affected	Comment
7	R/W	0	Channel A0 configuration	EQ3	Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	0		SW0	

BYTE 4					
Bit	Type	Power up condition	Description	Control Affected	Comment
7	R/W	0	Channel A1 configuration	EQ3	Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	0		SW0	

BYTE 5					
Bit	Type	Power up condition	Description	Control Affected	Comment
7	R/W	0	Channel A2 configuration	EQ3	Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	0		SW0	

BYTE 6					
Bit	Type	Power up condition	Description	Control Affected	Comment
7	R/W	0	Channel A3 configuration	EQ3	Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	0		SW0	

BYTE 7					
Bit	Type	Power up condition	Description	Control Affected	Comment
7:0	R/W		Reserved		

BYTE 8-15					
Bit	Type	Power up condition	Description	Control Affected	Comment
Power up condition : "0"					

5.2 I²C Operation

The integrated I2C interface operates as a slave device mode. Standard I2C mode (100 Kbps) is supported with 7-bit addressing and data byte format 8-bit.

The device supports Read/Write. The bytes must be accessed in sequential order from the lowest to the highest byte with the ability to stop after any complete byte has been transferred. Address bits A3 to A0 are programmable to support multiple chips environment.

The Data is loaded until a Stop sequence is issued.

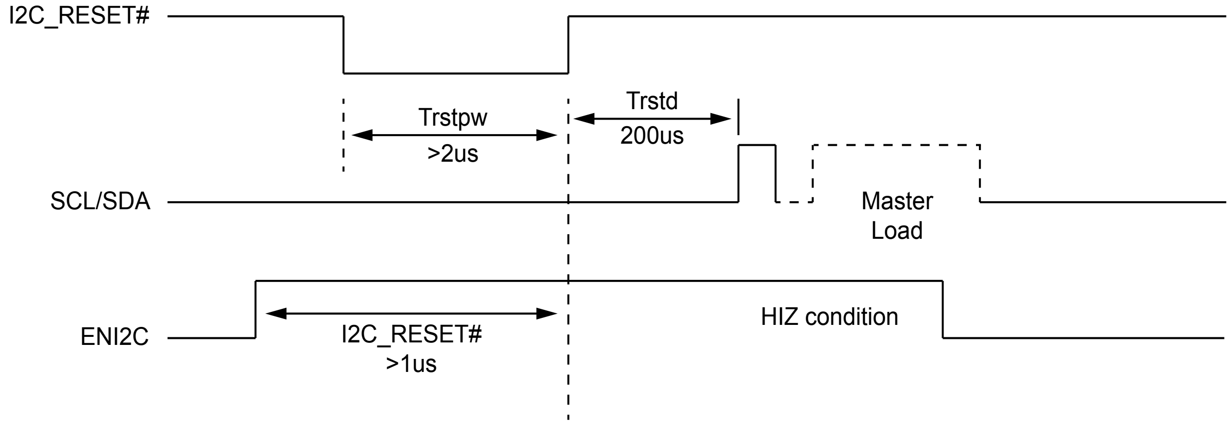


Figure 5-1 I2C Reset, Enable and SCL/SDA Timing Diagram

6. Electrical Specification

6.1 Absolute Maximum Ratings

Supply Voltage to Ground Potential . . . . . −0.5V to +4.6V
DC SIG Voltage . . . . . −0.5V to V_{DD} + 0.5V
Output Current . . . . . −25mA to +25mA
Power Dissipation Continuous 2.1W
ESD, HBM . . . . . –2kV to +2kV
Storage Temperature . . . . . −65°C to +150°C

Note
(1) Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

6.2 Recommended Operation Conditions

Parameter	Min.	Typ.	Max	Units
Power supply voltage (VDD to GND)(1)	3.0	3.3	3.6	V
I2C (SDA, SCL)			3.6	V
Supply Noise Tolerance up to 25 MHz (2)			100	mVp-p
Ambient Temperature	-40	25	85	°C

Note
(1) Typical parameters are measured at VDD = 3.3 ± 0.3V, TA = 25°C. They are for the reference purposes, and are not production-tested
(2) Allow supply noise (mVp-p sine wave) under typical condition

6.3 Electrical Characteristics

Over recommend operating supply and temperature range unless otherwise specified.

6.3.1 LVCMOS DC Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
V_{IH}	DC input logic high		$V_{DD}/2 + 0.7$		$V_{DD} + 0.3$	V
V_{IL}	DC input logic low		-0.3		$V_{DD}/2 - 0.7$	V
V_{OH}	At I_{OH} = -200µA		$V_{DD} + 0.2$			V
V_{OL}	At I_{OL} = -200µA				0.2	V
V_{hys}	Hysteresis of Schmitt trigger input		0.8			V

6.3.2 Power Dissipation

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{DD}	Supply current	PRSNT#=0 , SW=1000mVdiff, FG=2.5		265	290	mA
		PRSNT#=0, SW=900mVdiff, FG=2.5		240	290	mA
		PRSNT#=0, SW=800mVdiff, FG=2.5		233	290	mA
I_{DDQ}	Quiescent Supply Current	PEN=0, TMDS Output Disable		2.0	4.2	mA

6.3.3 Package Power Ratings

Package	Theta Ja(still air) (°C/W)	Theta Jc (°C/W)	Max. Power Dissipation Rating (Ta ≤ 70°)
32-pin TQFN (ZL32)	37.05	11.3	1.48W
42-pin TQFN (ZH42)	33.69	15.17	1.63W

6.3.4 Switching I/O Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{RX\text{-}DIFFp\text{-}p}$	Peak to peak differential input voltage			200		mV
T_R	Rise Time	Input signal with 30ps rise time, 20% to 80%		31		ps
T_F	Falling Time	Input signal with 30ps rise time, 20% to 80%		31		ps
T_{PLH}	Low-to-High Propagation Delay			65		ps
T_{PHL}	High-to-Low Propagation Delay			65		ps
$T_{SK\_IN\text{-}TRA\_IN}$	Input Intra-pair Differential Skew tolerance				0.15	IU
$T_{SK\_INTRA\_OUT}$	Output Intra-pair Differential Skew			5	10	ps
TSK_INTER_OUT	Output Inter-pair Differential Skew			8		ps
R_J	Add-in Random Jitter	at 6Gbps		0.57		RMS ps
D_J	Add-in Deterministic Jitter	at 6Gbps		6.57		ps
T_{SX}	Select to Switch Output				10	ns
S_{22}	Output return loss	10Mhz to 3GHz differential		-13		dB
		10Mhz to 3GHz common mode		-8		
R_{IN}	DC single-ended input impedance			50		Ω
	DC Differential Input Impedance			100		
R_{OUT}	DC single-ended output impedance			50		Ω
	DC Differential output Impedance			100		
$Z_{RX\text{-}HIZ}$	DC input CM input impedance during reset or power down			200		kΩ
$V_{RX\text{-}DIFFPP}$	Differential Input Peak-to-peak Voltage	Operational			1.4	Vppd
$V_{CMNOISE}$	Input source common-mode noise	DC – 200MHz			150	mVppd
TTX-IDLE-SET-TOIDLE	Max time to electrical idle after sending an EIOS			4	8	ns
TTX-IDLETO-DIFFDATA	Max time to valid differential signal after leaving electrical idle			4	8	ns

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
T_{PD}	Latency	From input to output		0.5		ns
G_P	Peaking gain (Compensation at 6Gbps, relative to 100MHz, 100mVp-p sine wave input)	EQ<3:0> = 1111 EQ<3:0> = 1000 EQ<3:0> = 0000		8.9 6.6 3.6		dB
		Variation around typical	-3		+3	dB
G_F	Flat gain (100MHz, EQ<3:0> = 1000, SW<1:0> = 10)	FG<1:0> = 11 FG<1:0> = 10 FG<1:0> = 01 FG<1:0> = 00		-3.5 -1.5 0.5 2.5		dB
		Variation around typical	-3		+3	dB
V_{1dB_100M}	-1dB compression point of output swing (at 100MHz)	SW<1:0> = 11 SW<1:0> = 10 SW<1:0> = 01 SW<1:0> = 00		1400 1300 1200 1100		mVppd
V_{1dB_6G}	-1dB compression point of output swing (at 6 Gbps)	SW<1:0> = 11 SW<1:0> = 10 SW<1:0> = 01 SW<1:0> = 00		1300 1200 1100 1000		mVppd
V_{Coup}	Channel isolation	100MHz to 3GHz		-40		dB
V_{noise_input}	Input-referred noise[2]	100MHz to 3GHz, FG<1:0> = 11, EQ<3:0> = 0000		0.5		mV_{RMS}
		100MHz to 3GHz, FG<1:0> = 11, EQ<3:0> = 1010		0.4		
V_{noise_output}	Output-referred noise[2]	100MHz to 3GHz, FG<1:0> = 11, EQ<3:0> = 0000		0.7		mV_{RMS}
		100MHz to 3GHz, FG<1:0> = 11, EQ<3:0> = 1010		0.8	1.6	

Note:

(1) Measured using a vector-network analyzer (VNA) with -15dBm power level applied to the adjacent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50Ω.

(2) Guaranteed by design.

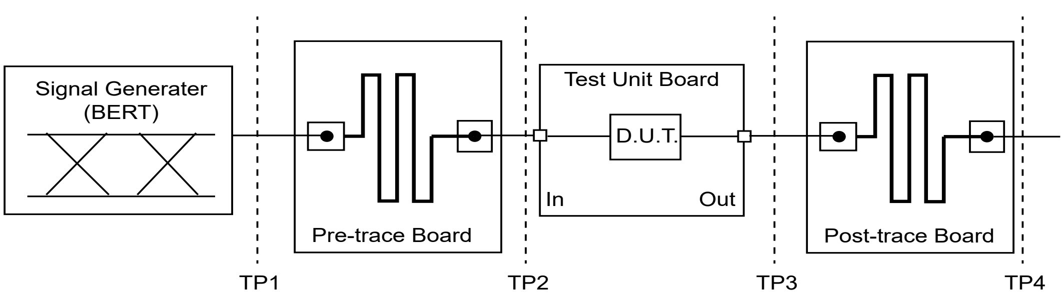


Figure 6-1 Electrical Parameter Test Setup

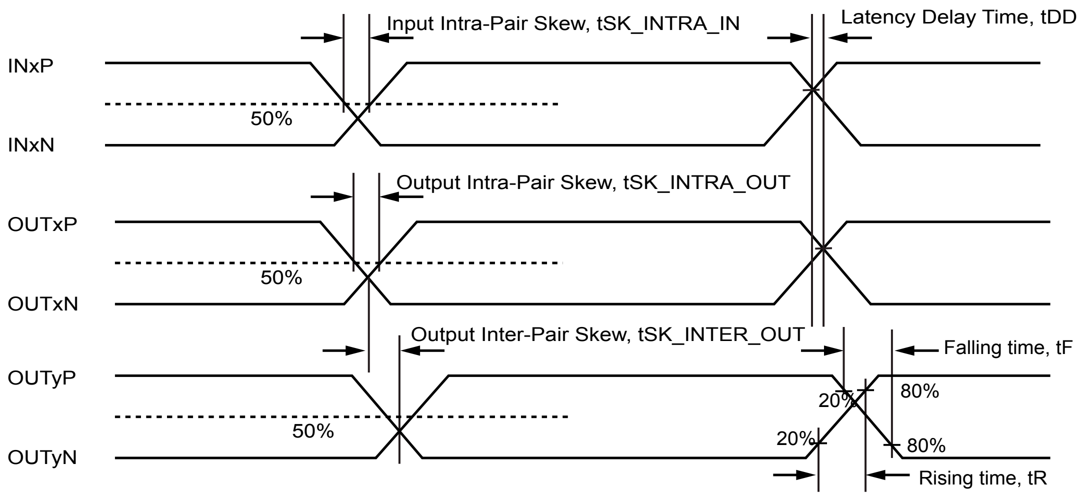


Figure 6-2 Intra and Inter-pair Differential Skew Definition

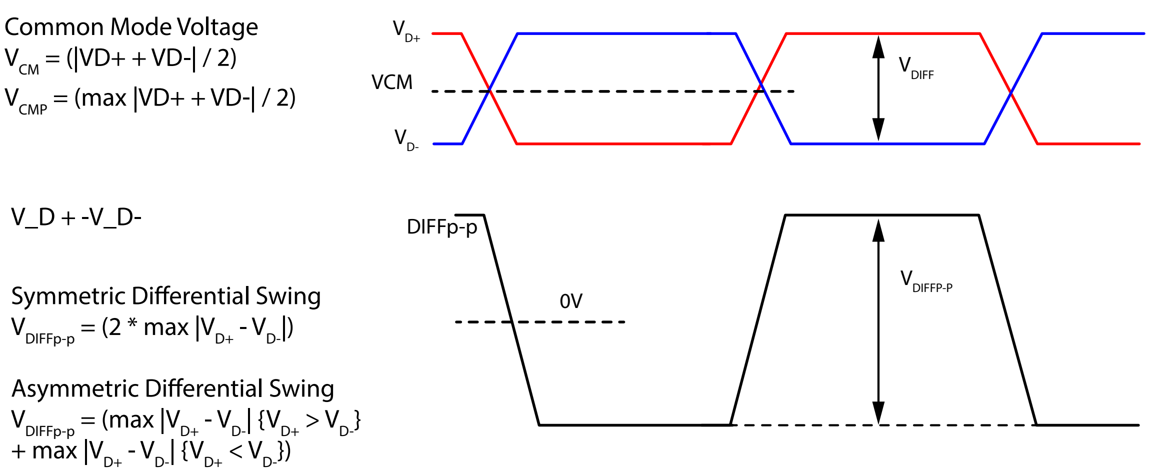


Figure 6-3 Definition of Peak-to-peak Differential Voltage

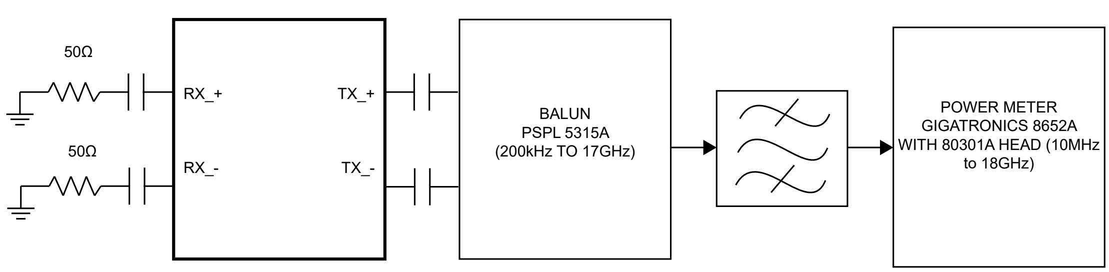


Figure 6-4 Noise Test Configuration

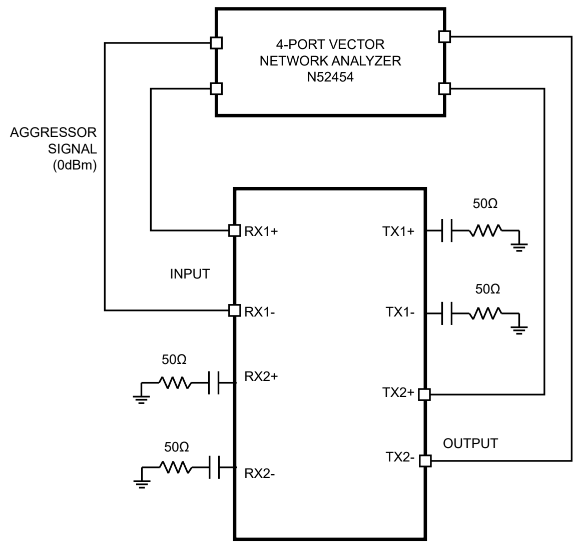


Figure 6-5 Channel-isolation Test Configuration

6.4 I2C Bus

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
VDD	Nominal Bus Voltage		3.0		3.6	V
Freq	Bus Operation Frequency				400	kHz
V_{IH}	DC input logic high		$V_{DD}/2 + 0.7$		$V_{DD} + 0.3$	V
V_{IL}	DC input logic low		-0.3		$V_{DD}/2 - 0.7$	V
V_{OL}	DC output logic low	I_{OL} = 3mA			0.4	V
Ipullup	Current Through Pull-Up Resistor or Current Source	High Power specification	3.0		3.6	mA
Ileak-bus	Input leakage per bus segment		-200		200	uA
Ileak-pin	Input leakage per device pin			-15		uA
CI	Capacitance for SDA/SCL				10	pF
tBUF	Bus Free Time Between Stop and Start condition		1.3			us
tHD:STA	Hold time after (Repeated) Start condition. After this period, the first clock is generated.	At pull-up, Max	0.6			us
TSU:STA	Repeated start condition setup time		0.6			us
TSU:STO	Stop condition setup time		0.6			us
THD:DAT	Data hold time		0			ns
TSU:DAT	Data setup time		100			ns
tLOW	Clock low period		1.3			us
tHIGH	Clock high period		0.6		50	us
tF	Clock/Data fall time				300	ns
tR	Clock/Data rise time				300	ns
tPOR	Time in which a device must be operation after power-on reset				500	ms

Note:
(1) Recommended maximum capacitance load per bus segment is 400pF.
(2) Compliant to I2C physical layer specification.
(3) Ensured by Design. Parameter not tested in production.

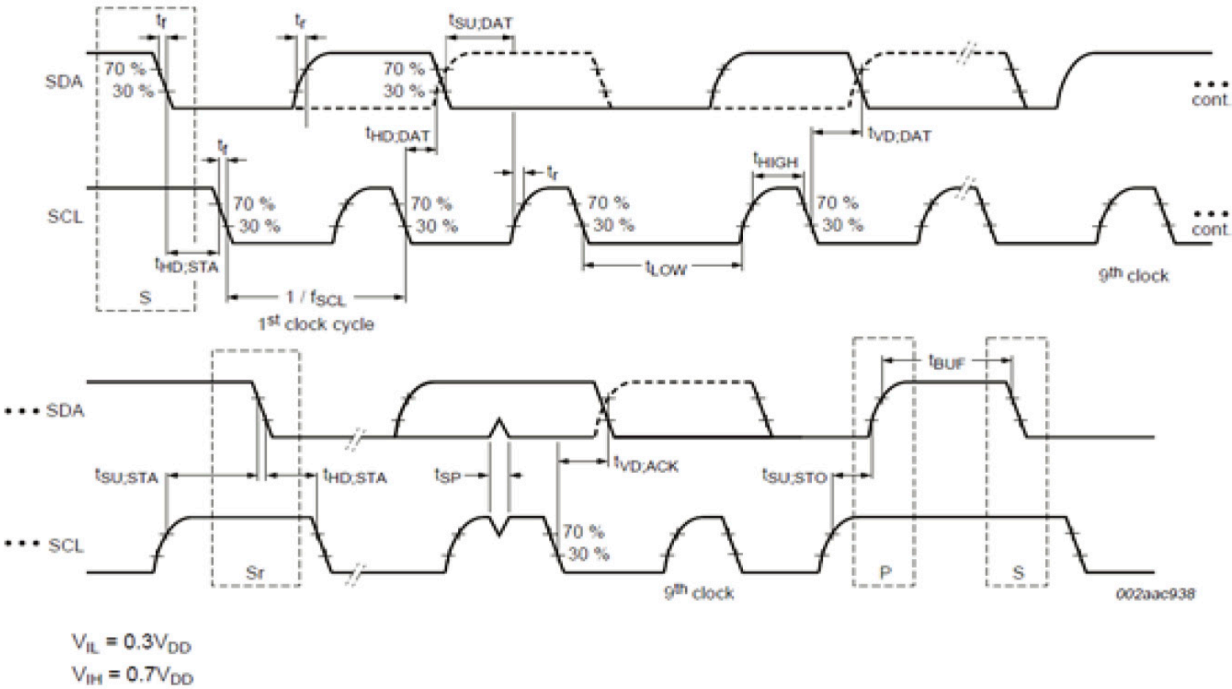
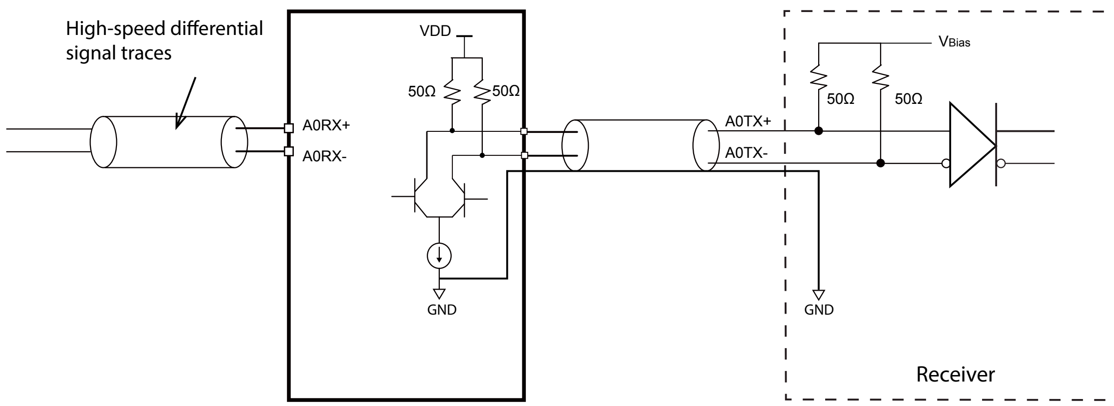


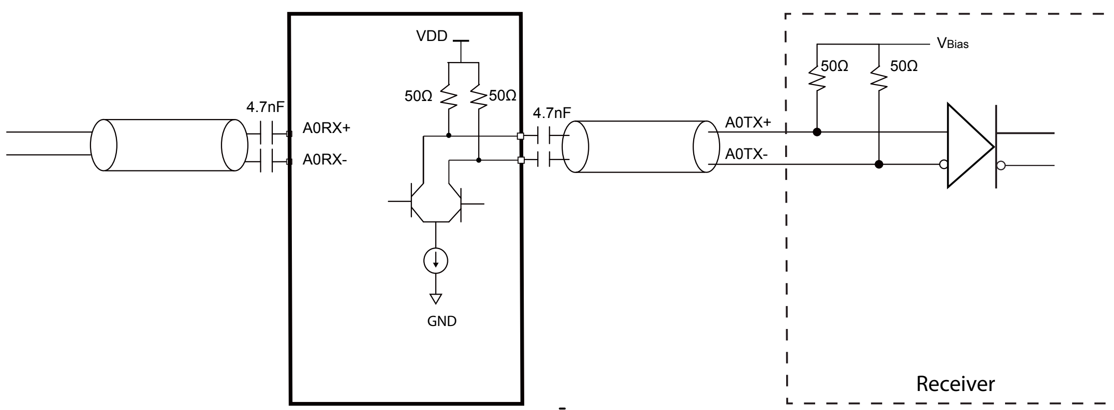
Figure 6-6 I2C Timing Definition

7. Applications

7.1 DC/AC-coupled Application



DC-Coupled Differential Signaling Application Circuits



AC-Coupled Differential Signaling Application Circuits

Figure 7-1 DC/AC-coupled Application Diagram

7.2 Channels/Polarity Swap

Linear Redriver does not have built-in internal channel/polarity switch. Transmitter can send swapped polarity signal to the Redriver.

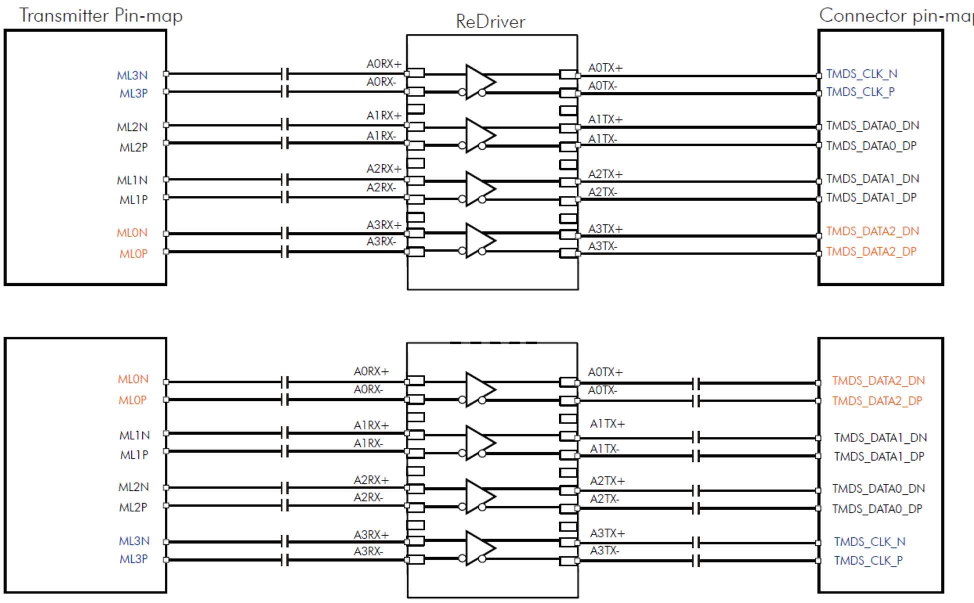


Figure 7-2 Polarity Swap Connection

7.3 Output Eye Diagram

7.3.1 Trace Card Loss Informations

Frequency	3 GHz	Units
6 inch Input Trace	-1.43	dB
12 inch Input Trace	-6.1	dB
18 inch Input Trace	-8.34	dB
30 inch Input Trace	-10.14	dB
36 inch Input Trace	-12.13	dB
48 inch Input Trace	-16.42	dB

Table 7-1. Characterization Trace Card dB Loss Information

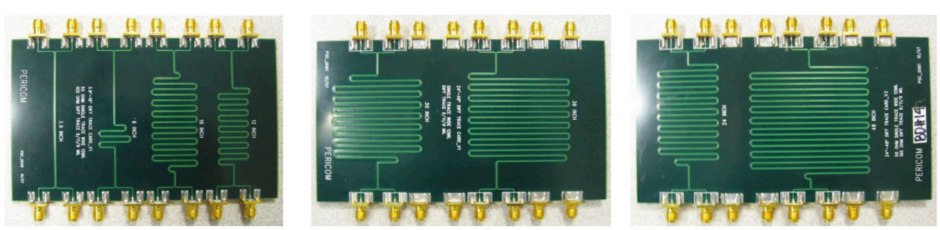


Figure 7-3 Trace Board Photo

7.3.2 Output Eye Diagram Measurement

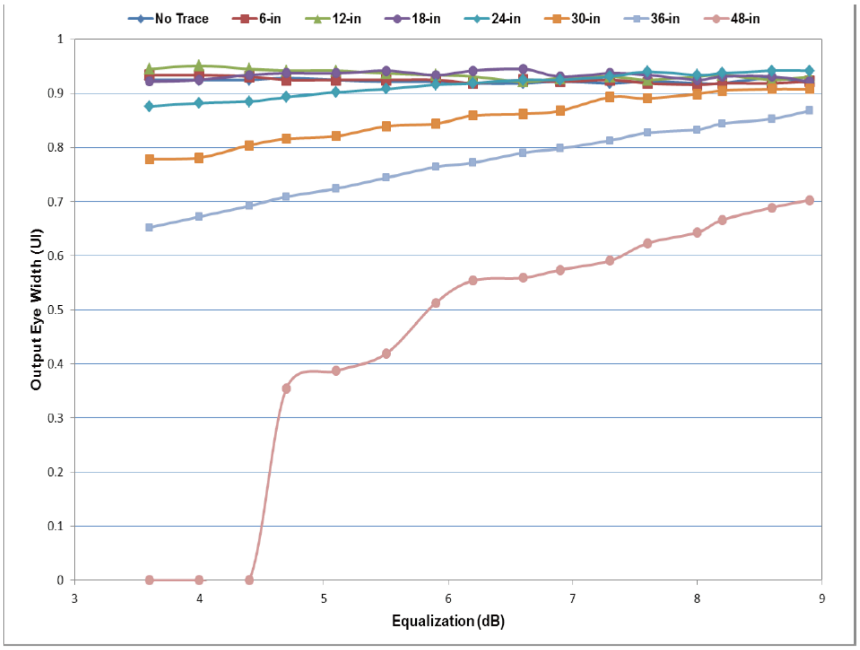


Figure 7-4 Eye Width vs. EQ plots at 6 Gbps, PRBS2^23-1, FG=11 (Gain +2.5dB)
Eye Width vs EQ, FG =1000mV, Gain=+2.5dB (Input Swing=800mVd)

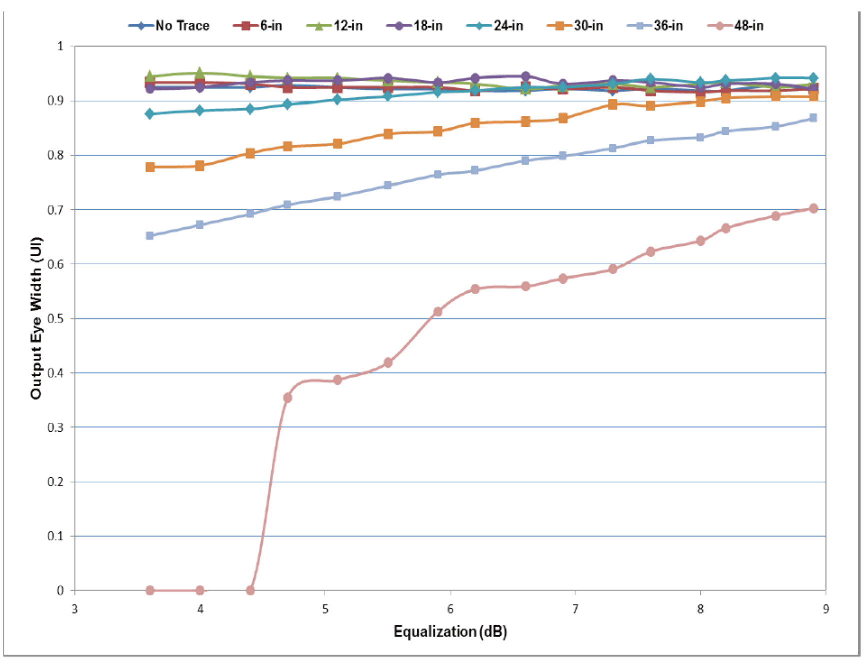


Figure 7-5 Eye Width vs. EQ plots at 6 Gbps, PRBS2^23-1, FG=10 (Gain +0.5dB)
Eye Height vs EQ, FG=1000mV, Gain=+2.5dB (input swing=800mVd)

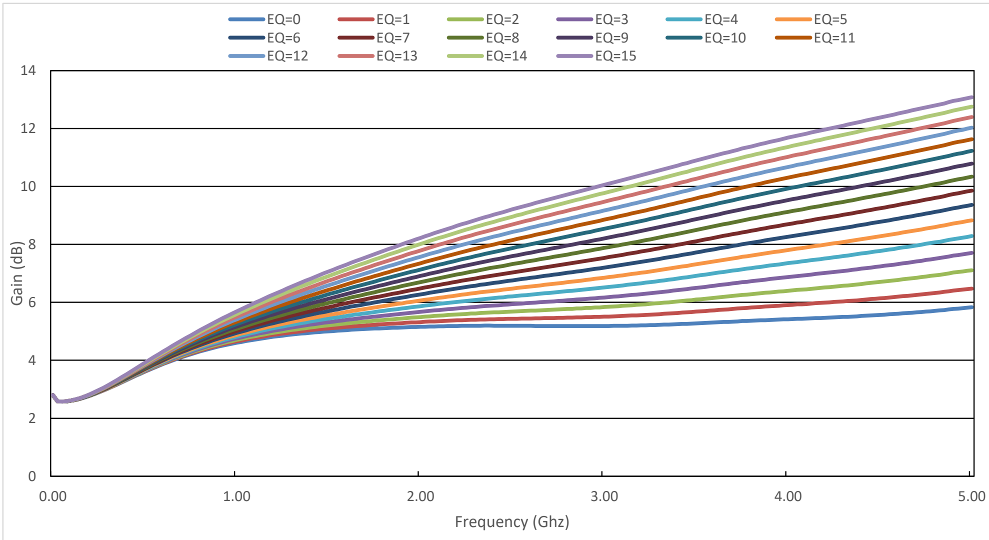


Figure 7-6 Frequency Response vs EQ

with FG=11(+2.5dB), Output Swing=1000mV, Vdd=3.0V, 25C, Input Power=-15dBm, No Input Trace

7.3.3 Output Eye Diagram

Condition: PRBS 2^23-1 pattern, Input Swing=800mVdiff, Output Swing= 1000mVdiff

Table 7-2. Output Eye diagram by EQ changes at FG 0.5dB

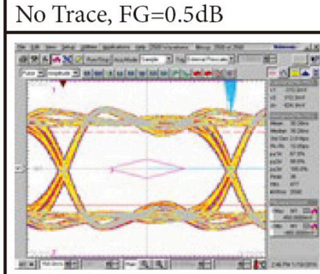
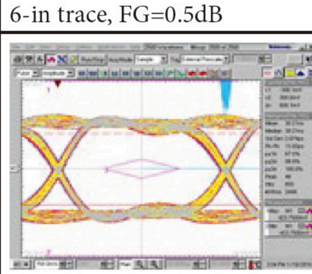
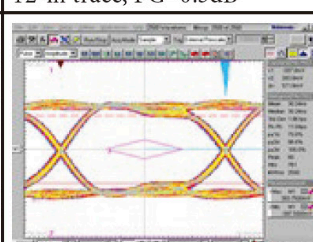
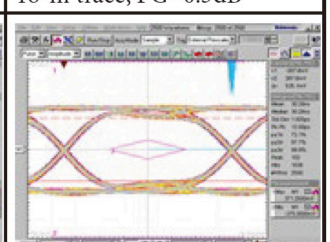
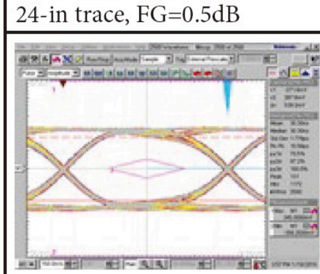
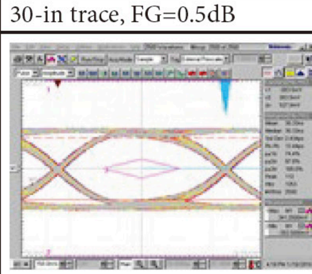
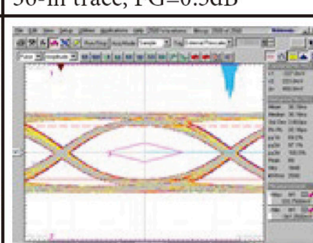
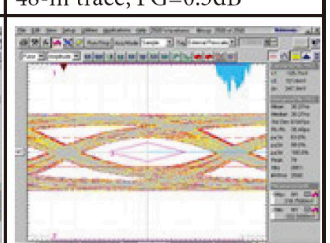
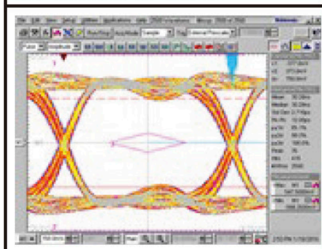
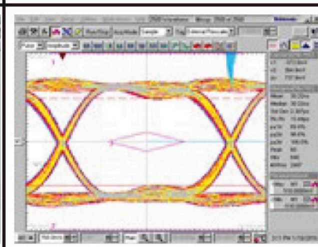
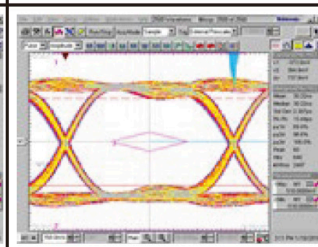
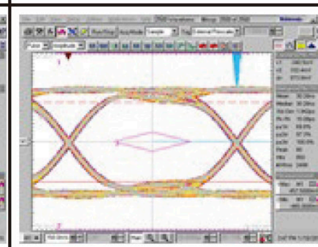
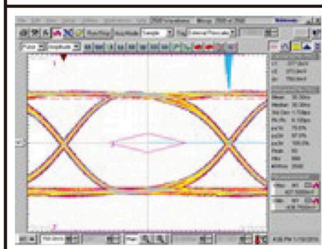
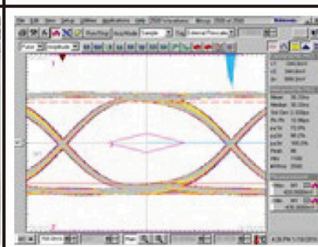
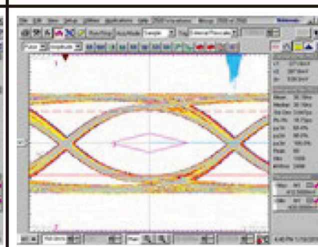
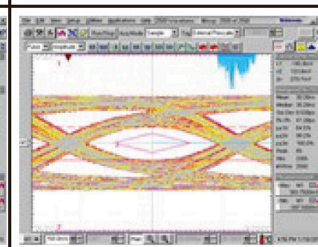
No Trace, FG=0.5dB	6-in trace, FG=0.5dB	12-in trace, FG=0.5dB	18-in trace, FG=0.5dB
			
EQ=3dB	EQ=3dB	EQ=5dB	EQ=6dB
24-in trace, FG=0.5dB	30-in trace, FG=0.5dB	36-in trace, FG=0.5dB	48-in trace, FG=0.5dB
			
EQ=10dB	EQ=13.3dB	EQ=14.5dB	EQ=15dB

Table 7-3. Output Eye Diagram by EQ changes at FG 2.5dB

No Trace, FG=2.5dB	6-in trace, FG=2.5dB	12-in trace, FG=2.5dB	18-in trace, FG=2.5dB
			
EQ=3dB	EQ=3dB	EQ=5dB	EQ=8dB
24-in trace, FG=2.5dB	30-in trace, FG=2.5dB	36-in trace, FG=2.5dB	48-in trace, FG=2.5dB
			
EQ=13dB	EQ=15dB	EQ=15dB	EQ=15dB

7.4 Layout Guideline

As transmission data rate increases rapidly, any flaws and/or mis-matches on PCB layout are amplified in terms of signal integrity. Layout guideline for high-speed transmission is highlighted in this application note.

7.4.1 Power and Ground

To provide a clean power supply for Diodes high-speed device, few recommendations are listed below:

- Power (VDD) and ground (GND) pins should be connected to corresponding power planes of the printed circuit board directly without passing through any resistor.
- The thickness of the PCB dielectric layer should be minimized such that the VDD and GND planes create low inductance paths.
- One low-ESR 0.1uF decoupling capacitor should be mounted at each VDD pin or should supply bypassing for at most two VDD pins. Capacitors of smaller body size, i.e. 0402 package, is more preferable as the insertion loss is lower. The capacitor should be placed next to the VDD pin.
- One capacitor with capacitance in the range of 4.7uF to 10uF should be incorporated in the power supply decoupling design as well. It can be either tantalum or an ultra-low ESR ceramic.
- A ferrite bead for isolating the power supply for Diodes high-speed device from the power supplies for other parts on the printed circuit board should be implemented.
- Several thermal ground vias must be required on the thermal pad. 25-mil or less pad size and 14-mil or less finished hole are recommended.

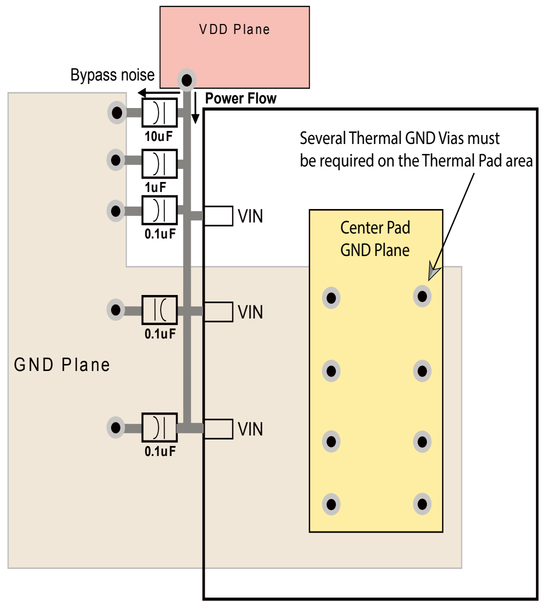
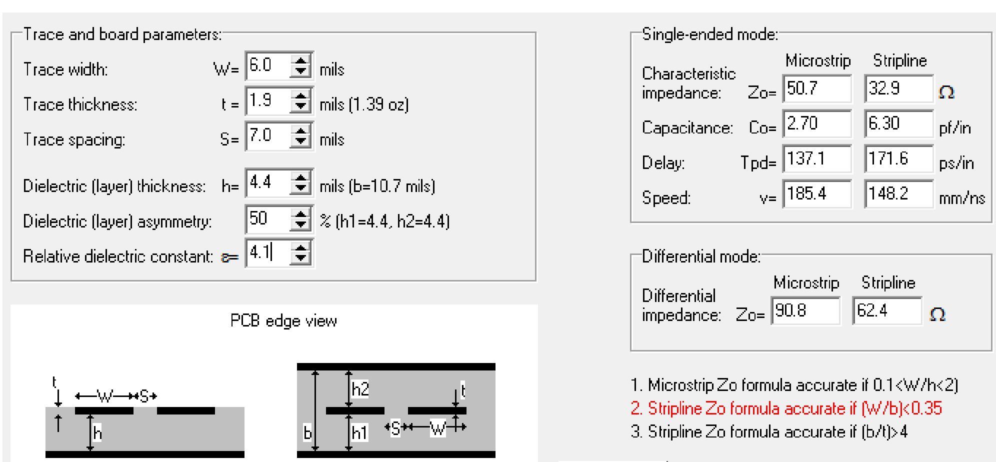


Figure 7-7 Decoupling Capacitor Placement Diagram

7.4.2 High-speed signal Routing

Well-designed layout is essential to prevent signal reflection:

- For 90Ω differential impedance, width-spacing-width micro-strip of 6-7-6 mils is recommended; for 100Ω differential impedance, width-spacing-width micro-strip of 5-7-5 mils is recommended.
- Differential impedance tolerance is targeted at ±15%.



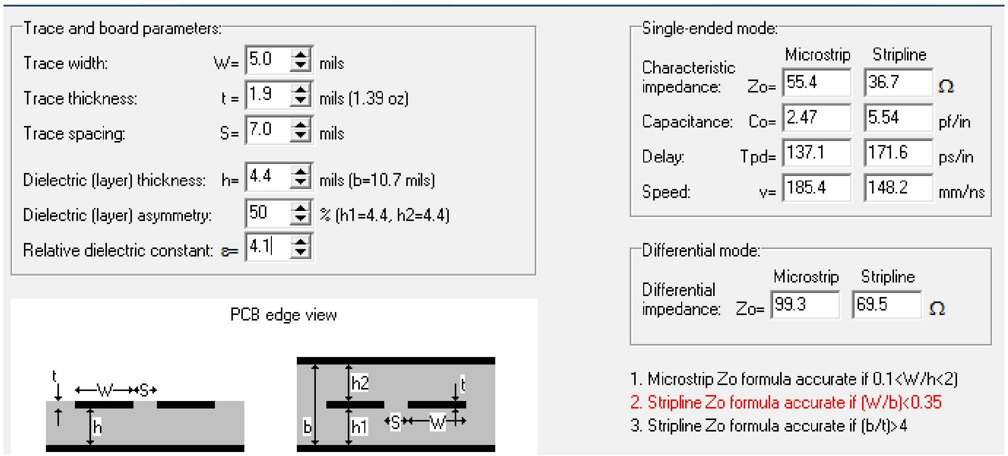


Figure 7-8 Trace Width and Clearance of Micro-strip and Strip-line

- For micro-strip, using 1/2oz Cu is fine. For strip-line in 6+ PCB layers, 1oz Cu is more preferable.

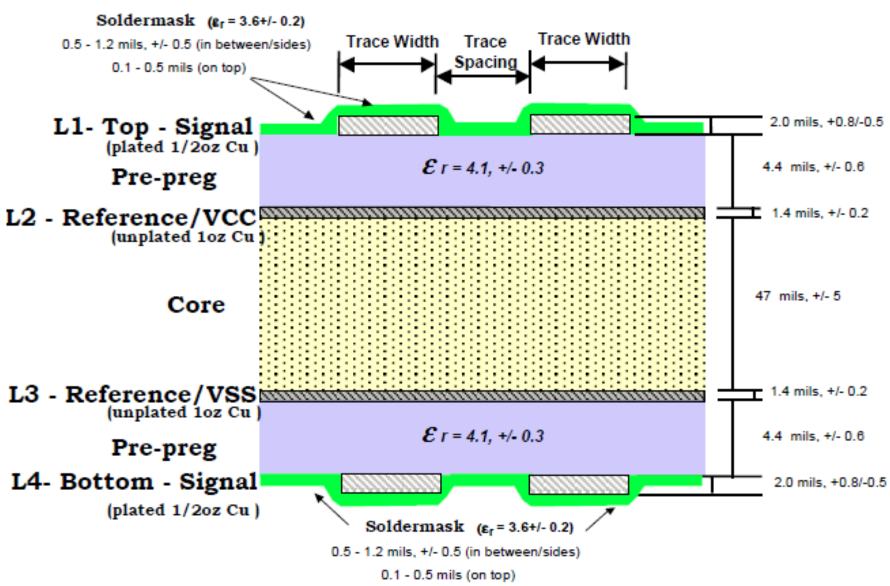


Figure 7-9 4-Layer PCB Stack-up Example

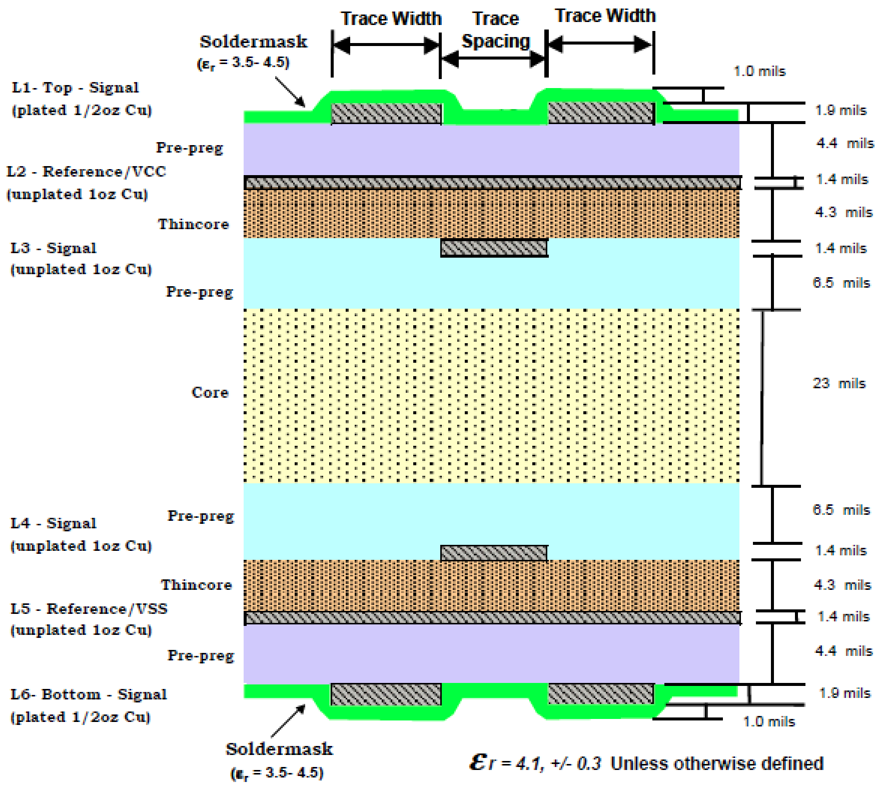


Figure 7-10 6-Layer PCB Stack-up Example

- Ground referencing is highly recommended. If unavoidable, stitching capacitors of 0.1uF should be placed when reference plane is changed.

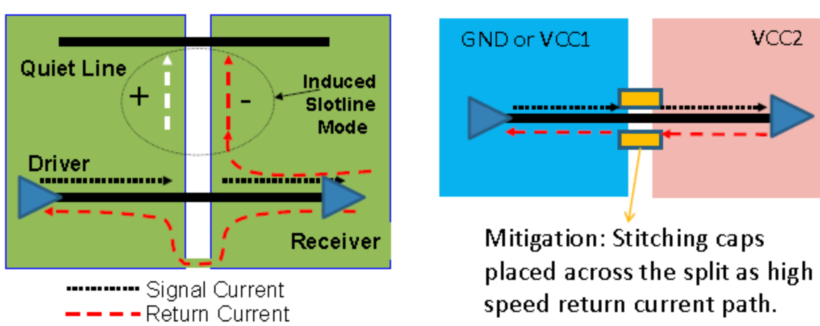


Figure 7-11 Stitching Capacitor Placement

- To keep the reference unchanged, stitching vias must be used when changing layers.
- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew of micro-strip should be less than 5 mils.

- To keep the reference unchanged, stitching vias must be used when changing layers.
- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew of micro-strip should be less than 5 mils.

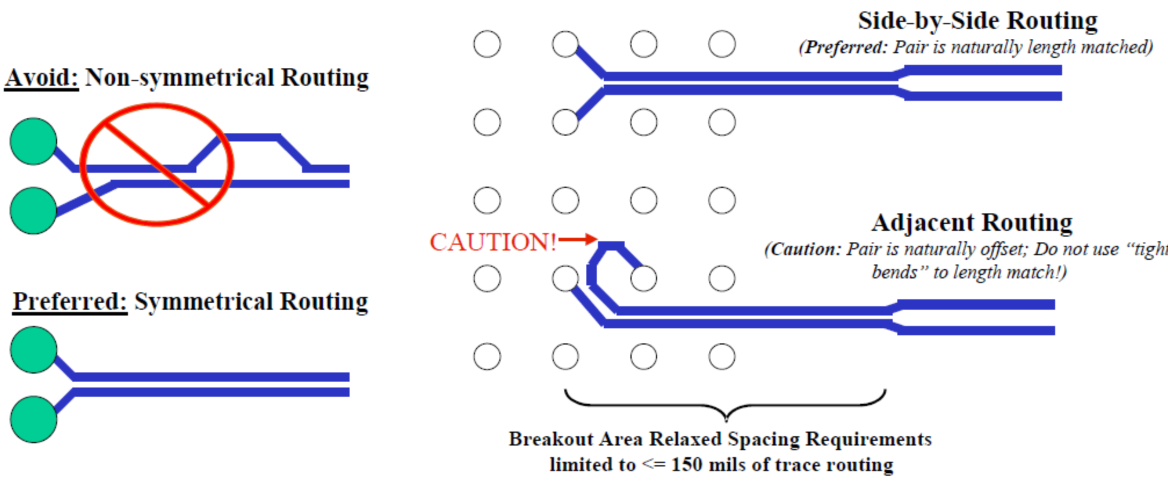


Figure 7-12 Layout Guidance of Matched Differential Pair

- For minimal crosstalk, inter-pair spacing between two differential micro-strip pairs should be at least 20 mils or 4 times the dielectric thickness of the PCB.
- Wider trace width of each differential pair is recommended in order to minimize the loss, especially for long routing. More consistent PCB impedance can be achieved by a PCB vendor if trace is wider.
- Differential signals should be routed away from noise sources and other switching signals on the printed circuit board.
- To minimize signal loss and jitter, tight bend is not recommended. All angles α should be at least 135 degrees. The inner air gap A should be at least 4 times the dielectric thickness of the PCB.

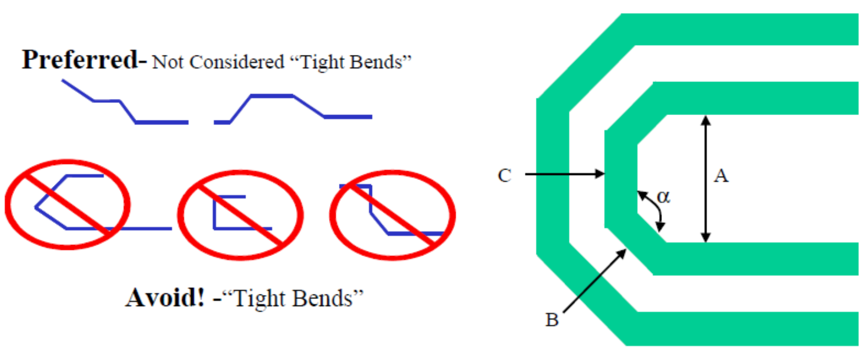


Figure 7-13 Layout Guidance of Bends

- Stub creation should be avoided when placing shunt components on a differential pair.

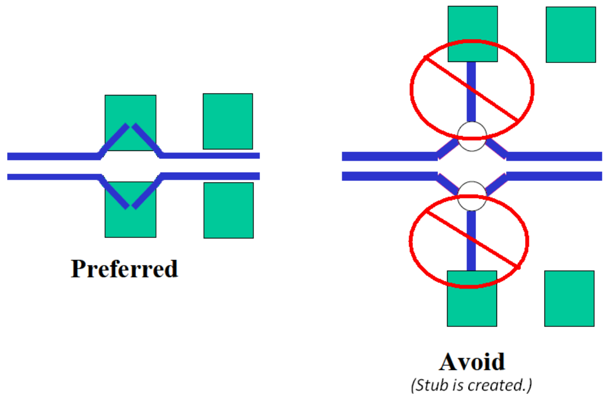


Figure 7-14 Layout Guidance of Shunt Component

- Placement of series components on a differential pair should be symmetrical.

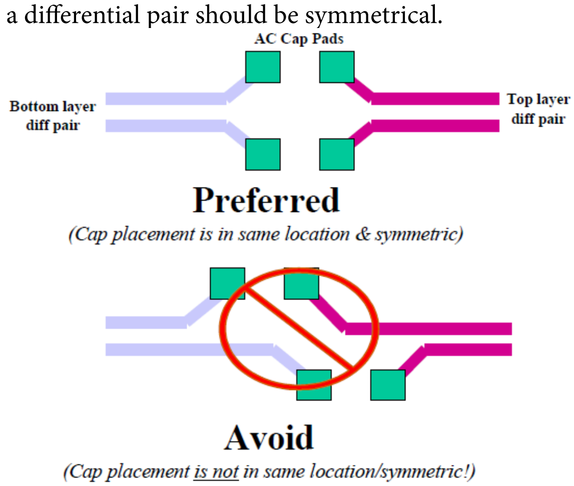


Figure 7-15 Layout Guidance of Series Component

- Stitching vias or test points must be used sparingly and placed symmetrically on a differential pair.

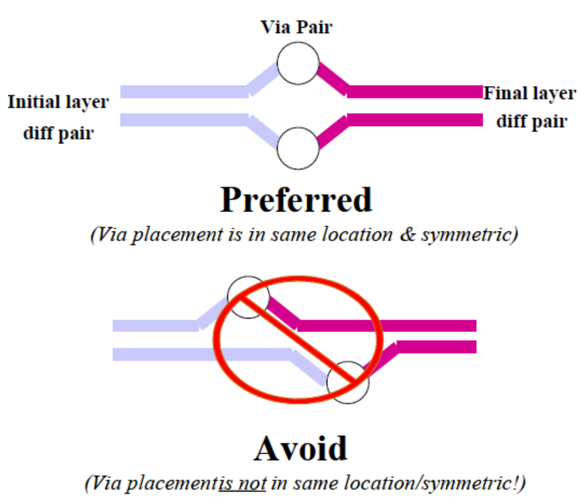


Figure 7-16 Layout Guidance of Stitching Via

7.5 HDMI 2.0 Compliance Test

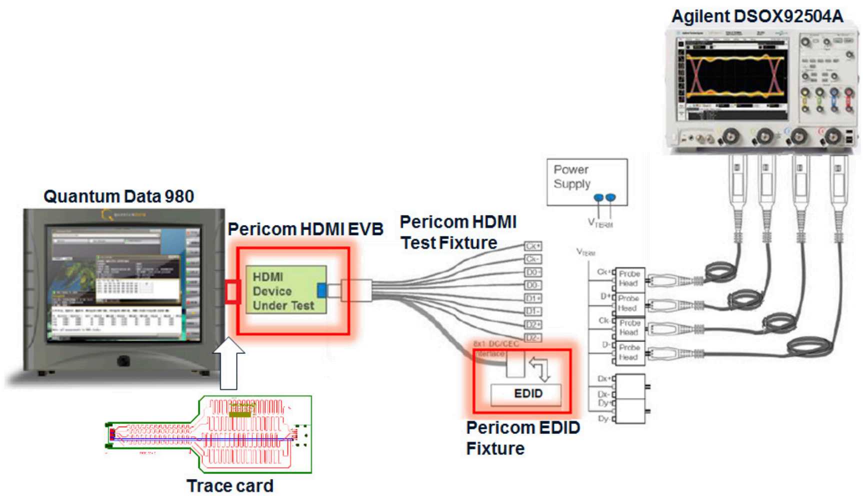


Figure 7-17 HDMI 2.0 CTS test setup

Note: Application Trace Card Information for CTS test

Table 7-4. Application Trace Card Information for CTS test

HDMI FR4 trace	0 in	6 in	12 in	18 in	24 in	30 in	36 in
Insertion loss @ 6Gbps	-5.91 dB	-9.75 dB	-10.47 dB	-13.05 dB	-15.87 dB	-16.97 dB	-21.20 dB

HDMI Test Report

Overall Result: PASS

Test Configuration Details	
Device Description	
Device ID	Transmitter
Fixture Type	Other
Probe Connection	4 Probes
Probe Head Type	N5444A
Lane Connection	1 Data Lane
HDMI Specification	2.0
HDMI Test Type	TMDS Physical Layer Tests
Test Session Details	
Infiniium SW Version	05.20.0013
Infiniium Model Number	DSOX92504A
Infiniium Serial Number	MY54410104
Application SW Version	2.11
Debug Mode Used	No
Probe (Channel 1)	Model: N2801A Serial: US54094067 Head: N5444A Atten: Calibrated (18 FEB 2015 11:16:48), Using Cal Atten (5.7831E+000) Skew: Calibrated (18 FEB 2015 11:16:56), Using Cal Skew
Probe (Channel 2)	Model: N2801A Serial: US54094054 Head: N5444A Atten: Calibrated (18 FEB 2015 11:19:29), Using Cal Atten (5.5882E+000) Skew: Calibrated (18 FEB 2015 11:13:57), Using Cal Skew
Probe (Channel 3)	Model: N2801A Serial: US54094059 Head: N5444A Atten: Calibrated (18 FEB 2015 11:15:19), Using Cal Atten (5.7320E+000) Skew: Calibrated (18 FEB 2015 11:15:29), Using Cal Skew
Probe (Channel 4)	Model: N2801A Serial: US54094057 Head: N5444A Atten: Calibrated (18 FEB 2015 11:11:30), Using Cal Atten (5.5123E+000) Skew: Calibrated (18 FEB 2015 11:12:12), Using Cal Skew
Last Test Date	2016-01-21 16:43:22 UTC +08:00

Figure 7-18 HDMI 2.0 CTS Test Report

Summary of Results

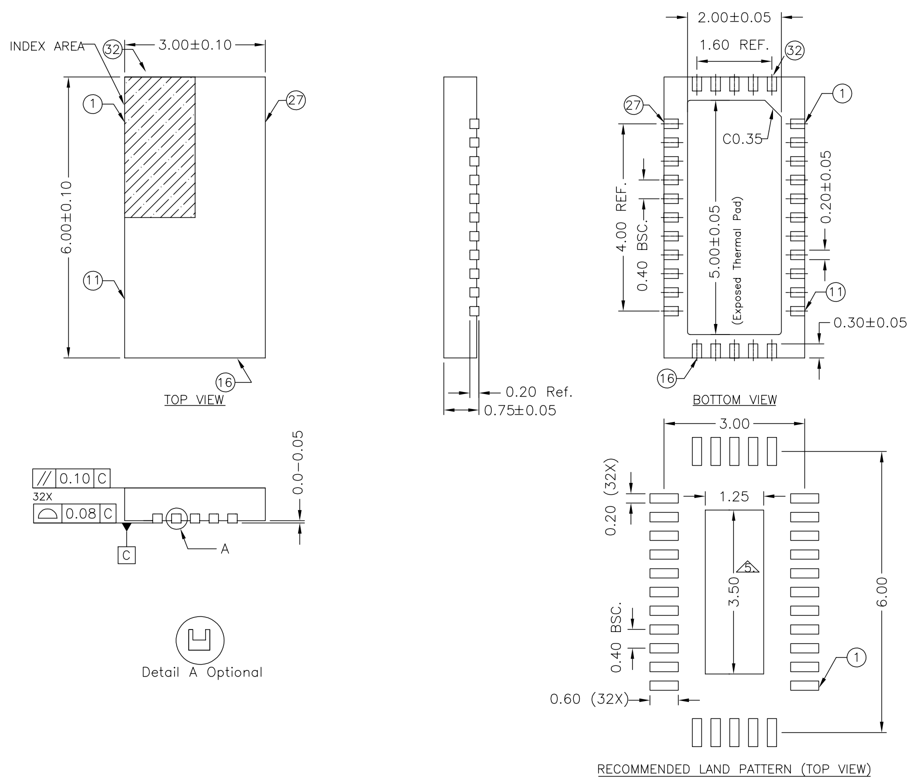
Test Statistics	
Failed	0
Passed	24
Total	24

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	HF1-2: Clock Rise Time	151.367 ps	101.8 %	VALUE >= 75.000 ps
✓	0	1	HF1-2: Clock Fall Time	150.838 ps	101.1 %	VALUE >= 75.000 ps
✓	0	1	HF1-6: Clock Duty Cycle(Minimum)	49.780	24.5 %	>=40%
✓	0	1	HF1-6: Clock Duty Cycle(Maximum)	50.330	16.1 %	<=60%
✓	0	1	HF1-6: Clock Rate	148.513500000 MHz	2.3 %	85.000000000 MHz <= VALUE <= 150.000000000 MHz
✓	0	1	HF1-7: Differential Clock Voltage Swing, Vs (TP1)	997 mV	25.4 %	400 mV < VALUE < 1.200 V
✓	0	1	HF1-7: Clock Jitter (TP2_EQ with Worst Case Positive Skew)	250 mTbit	16.7 %	VALUE <= 300 mTbit
✓	0	1	HF1-7: Clock Jitter (TP2_EQ with Worst Case Negative Skew)	225 mTbit	25.0 %	VALUE <= 300 mTbit
✓	0	1	HF1-5: D0 Maximum Differential Voltage	542 m	30.5 %	VALUE <= 780 m
✓	0	1	HF1-5: D0 Minimum Differential Voltage	-564 m	27.7 %	VALUE >= -780 m
✓	0	1	HF1-2: D0 Rise Time	135.000 ps	217.6 %	VALUE >= 42.500 ps
✓	0	1	HF1-2: D0 Fall Time	134.370 ps	216.2 %	VALUE >= 42.500 ps
✓	0	1	HF1-8: D0 Mask Test (TP2_EQ with Worst Case Positive Skew)	0.000	50.0 %	No Mask Failures
✓	0	1	HF1-8: D0 Mask Test (TP2_EQ with Worst Case Negative Skew)	0.000	50.0 %	No Mask Failures
✓	0	1	HF1-1: VL Clock +	2.684 V	48.0 %	2.300 V <= VALUE <= 3.100 V
✓	0	1	HF1-1:Clock + VSwing	513 mV	21.8 %	200 mV <= VALUE <= 600 mV
✓	0	1	HF1-1: VL Clock -	2.678 V	47.3 %	2.300 V <= VALUE <= 3.100 V
✓	0	1	HF1-1:Clock - VSwing	513 mV	21.8 %	200 mV <= VALUE <= 600 mV
✓	0	1	HF1-4: Intra-Pair Skew - Clock	51 mTbit	33.0 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	1	HF1-1: VL D0+	2.706 V	32.3 %	2.300 V <= VALUE <= 2.900 V
✓	0	1	HF1-1: D0+ VSwing	459 mV	29.5 %	400 mV <= VALUE <= 600 mV
✓	0	1	HF1-1: VL D0-	2.718 V	30.3 %	2.300 V <= VALUE <= 2.900 V
✓	0	1	HF1-1: D0- VSwing	450 mV	25.0 %	400 mV <= VALUE <= 600 mV
✓	0	1	HF1-4: Intra-Pair Skew - Data Lane 0	36 mTbit	38.0 %	-150 mTbit <= VALUE <= 150 mTbit

8. Mechanical/Packaging Information

8.1 Mechanical

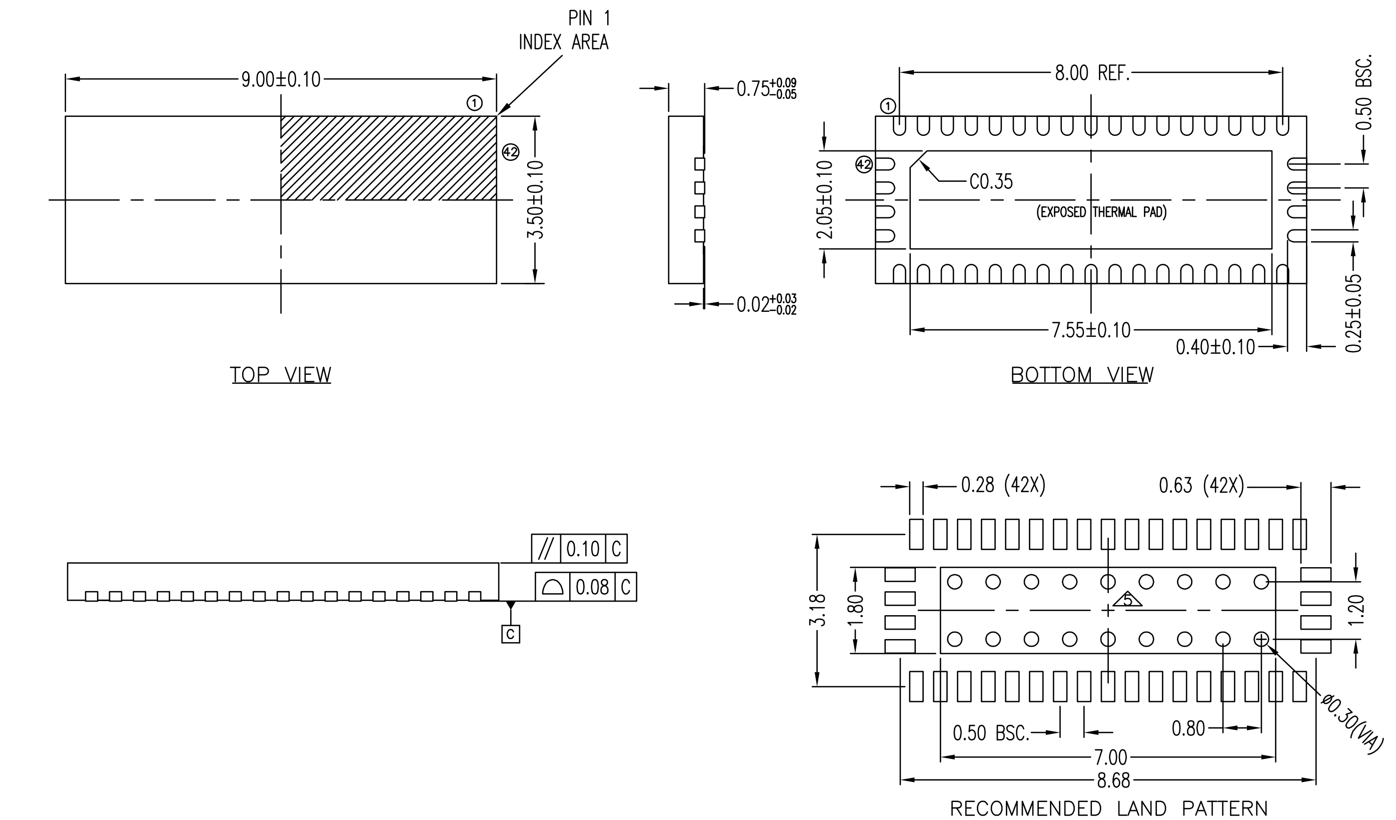


NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED).

	DATE: 04/01/20
DESCRIPTION: 32-Contact, Very Thin Quad Flat No-Lead (TQFN)	
PACKAGE CODE: ZL (ZL32)	
DOCUMENT CONTROL #: PD-2044	**REVISION: D**

20-1240

Figure 8-1 32-pin TQFN Package Mechanical



NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL IS RECOMMENDED).

DIODES INCORPORATED / PERICOM A PRODUCT LINE OF DIODES INCORPORATED / ENABLING SERIAL CONNECTIVITY	DATE: 04/25/17
DESCRIPTION: 42-Contact, Very Thin Quad Flat No-Lead (TQFN)	
PACKAGE CODE: ZH (ZH42)	
DOCUMENT CONTROL #: PD-2035	REVISION: G

17-0266

Figure 8-2 42-pin TQFN Package Mechanical

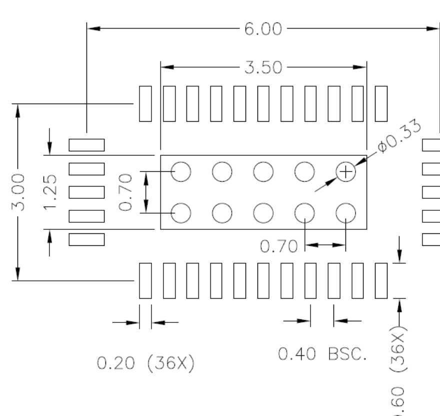


Figure 8-3 42-pin TQFN Package Mechanical

8.2 Part Marking Information

Our standard product mark follows our standard part number ordering information, except for those products with a speed letter code. The speed letter code mark is placed after the package code letter, rather than after the device number as it is ordered. After electrical test screening and speed binning has been completed, we then perform an "add mark" operation which places the speed code letter at the end of the complete part number.

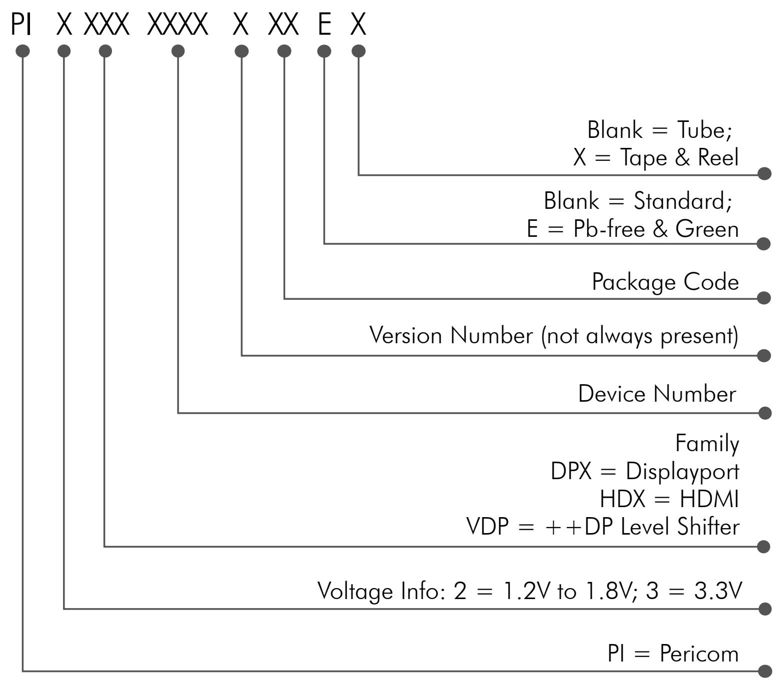
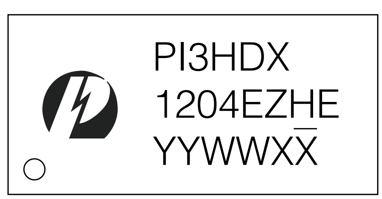


Figure 8-4 Part Numbers Information



YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

Figure 8-5 Part Marking Information

8.3 Tape & Reel Materials and Design

8.3.1 Carrier Tape

The Pocketed Carrier Tape is made of Conductive Polystyrene plus Carbon material (or equivalent). The surface resistivity is 10^6Ohm/sq. maximum. Pocket tapes are designed so that the component remains in position for automatic handling after cover tape is removed. Each pocket has a hole in the center for automated sensing if the pocket is occupied or not, thus facilitating device removal. Sprocket holes along the edge of the center tape enable direct feeding into automated board assembly equipment. See Figures 3 and 4 for carrier tape dimensions.

8.3.2 Cover Tape

Cover tape is made of Anti-static Transparent Polyester film. The surface resistivity is 10^7Ohm/Sq. Minimum to 10^{11}Ohm sq. maximum. The cover tape is heat-sealed to the edges of the carrier tape to encase the devices in the pockets. The force to peel back the cover tape from the carrier tape shall be a MEAN value of 20 to 80gm (2N to 0.8N).

8.3.3 Reel

The device loading orientation is in compliance with EIA-481, current version (Figure 2). The loaded carrier tape is wound onto either a 13-inch reel, (Figure 4) or 7-inch reel. The reel is made of Antistatic High-Impact Polystyrene. The surface resistivity 10^7Ohm/sq. minimum to 10^{11}Ohm/sq. max.

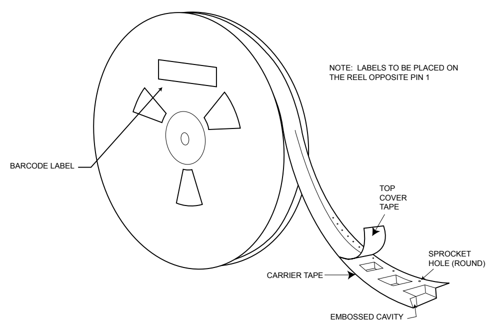


Figure 8-6 Tape & Reel Label Information

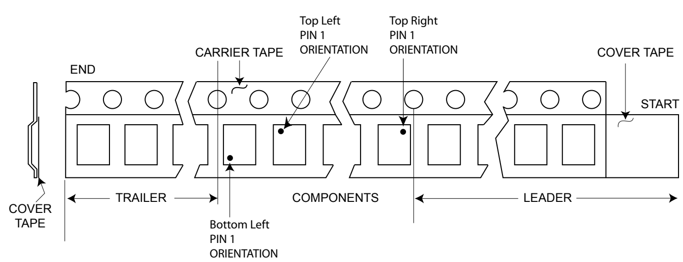


Figure 8-7 Tape Leader and Trailer pin 1 Orientations

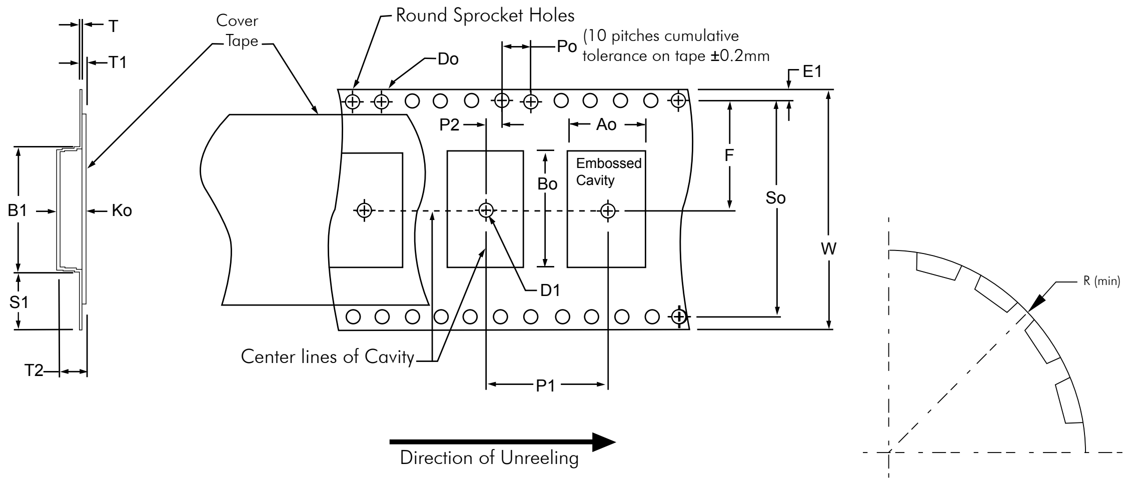


Figure 8-8 Standard Embossed Carrier Tape Dimensions

Table 8-1. Constant Dimensions

<table>
<tr><th>Tape Size</th><th>D0</th><th>D1 (Min)</th><th>E1</th><th>P0</th><th>P2</th><th>R (See Note 2)</th><th>S1 (Min)</th><th>T (Max)</th><th>T1 (Max)</th></tr>
<tr><td>8mm</td><td rowspan="6">1.5 +0.1 -0.0</td><td>1.0</td><td rowspan="6">1.75 ± 0.1</td><td rowspan="6">4.0 ± 0.1</td><td rowspan="2">2.0 ± 0.05</td><td>25</td><td rowspan="4">0.6</td><td rowspan="6">0.6</td><td rowspan="6">0.1</td></tr>
<tr><td>12mm</td><td rowspan="3">1.5</td><td rowspan="3">30</td></tr>
<tr><td>16mm</td><td rowspan="3">2.0 ± 0.1</td></tr>
<tr><td>24mm</td></tr>
<tr><td>32mm</td><td rowspan="2">2.0</td><td rowspan="2">50</td><td rowspan="2">N/A (See Note 3)</td></tr>
<tr><td>44mm</td><td>2.0 ± 0.15</td></tr>
</table>

Table 8-2. Variable Dimensions

<table>
<tr><th>Tape Size</th><th>P_1</th><th>B_1 (Max)</th><th>E_2 (Min)</th><th>F</th><th>So</th><th>T_2 (Max.)</th><th>W (Max)</th><th>A_0, B_0, & K_0</th></tr>
<tr><td>8mm</td><td rowspan="6">Specific per package type. Refer to FR-0221 (Tape and Reel Packing Information)</td><td>4.35</td><td>6.25</td><td>3.5 ± 0.05</td><td rowspan="4">N/A (see note 4)</td><td>2.5</td><td>8.3</td><td rowspan="6">See Note 1</td></tr>
<tr><td>12mm</td><td>8.2</td><td>10.25</td><td>5.5 ± 0.05</td><td>6.5</td><td>12.3</td></tr>
<tr><td>16mm</td><td>12.1</td><td>14.25</td><td>7.5 ± 0.1</td><td>8.0</td><td>16.3</td></tr>
<tr><td>24mm</td><td>20.1</td><td>22.25</td><td>11.5 ± 0.1</td><td rowspan="2">12.0</td><td>24.3</td></tr>
<tr><td>32mm</td><td>23.0</td><td>N/A</td><td>14.2 ± 0.1</td><td>28.4± 0.1</td><td>32.3</td></tr>
<tr><td>44mm</td><td>35.0</td><td>N/A</td><td>20.2 ± 0.15</td><td>40.4 ± 0.1</td><td>16.0</td><td>44.3</td></tr>
</table>

NOTES:
1. A0, B0, and K0 are determined by component size. The cavity must restrict lateral movement of component to 0.5mm maximum for 8mm and 12mm wide tape and to 1.0mm maximum for 16,24,32, and 44mm wide carrier. The maximum component rotation within the cavity must be limited to 20o maximum for 8 and 12 mm carrier tapes and 10o maximum for 16 through 44mm.
2. Tape and components will pass around reel with radius "R" without damage.
3. S1 does not apply to carrier width ≥32mm because carrier has sprocket holes on both sides of carrier where Do≥S1.
4. So does not exist for carrier ≤32mm because carrier does not have sprocket hole on both side of carrier.

Table 8-3. Reel Dimensions by Tape Size

Tape Size	A	N (Min) See Note A	W1	W2 (Max)	W3	B (Min)	C	D (Min)
8mm	178 ±2.0mm or 330±2.0mm	60 ±2.0mm or 100±2.0mm	8.4 +1.5/-0.0 mm	14.4 mm	Shall Accommodate Tape Width Without Interference	1.5mm	13.0 +0.5/-0.2 mm	20.2mm
12mm			12.4 +2.0/-0.0 mm	18.4 mm				
16mm	330 ±2.0mm	100 ±2.0mm	16.4 +2.0/-0.0 mm	22.4 mm				
24mm			24.4 +2.0/-0.0 mm	30.4 mm				
32mm			32.4 +2.0/-0.0 mm	38.4 mm				
44mm			44.4 +2.0/-0.0 mm	50.4 mm				

NOTE:
A. If reel diameter A=178 ±2.0mm, then the corresponding hub diameter (N(min)) will by 60 ±2.0mm. If reel diameter A=330±2.0mm, then the corresponding hub diameter (N(min)) will by 100±2.0mm.

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