IQS323 DATASHEET

3 Channel Self-Capacitive / 3 Channel Mutual-Capacitive / 2 Channel Inductive sensing controller with Touch and Proximity user interfaces. The device features an I²C communications interface, low power options, wear detection, metal detection and a slider with on-chip gesture recognition

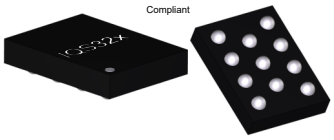
1 Device Overview

The IQS323 ProxFusion® IC is a sensor fusion device for various single and dual-channel sensing requirements. Applications include proximity and touch buttons, sliders, metal sensors and wear detection pairs. The sensor is fully I²C compatible and on-chip calculations enable the IC to respond effectively even in lowest power modes.

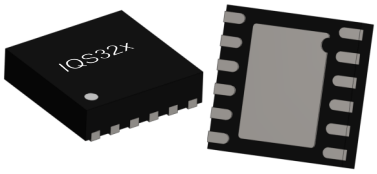
1.1 Main Features

- Highly flexible ProxFusion® device
- 3 external sensor pad connections
- Configure multiple channels on external pins (Self/Mutual/Inductive).
- External sensor options:
  - 3 self-capacitive buttons
  - Up to 2 wear detection pairs (with shared physical reference)
  - 3 mutual capacitive touch/proximity sensors
  - 2 inductive mode sensors
- Built-in basic functions:
  - Automatic tuning
  - Noise filtering
  - Differential measurements (reference channels)
  - Debounce & Hysteresis
  - Dual direction trigger indication
  - Halt Mode
- Built-in Signal processing options:
  - Touch/Proximity output
  - Slider output
  - Gesture output
  - Reference User Interface
  - Release User Interface (For order codes with Release UI)
  - Movement User Interface (For order codes with Movement UI)
- Design simplicity
  - PC Software for debugging & optimal setup for performance
- Automated system power modes for optimal response vs consumption
  - Distributed ultra low power (ULP) mode
- I²C communication interface with Ready Indicator(up to fast plus -1MHz)
- Event and streaming modes
- Supply Voltage 1.71V to 3.5V
- Package options
  - WLCSP11 (1.48 x 1.08 x 0.345 mm) - interleaved 0.35mm x 0.35mm ball pitch
  - DFN12 (3 x 3 x 0.75 mm) - 0.5mm pitch
  - QFN20 (3 x 3 x 0.55 mm) - 0.4mm pitch

RoHS2 Compliant



WLCSP11, DFN12 & QFN20 packages



Representation only

1.2 Applications

- TWS earphones
- Wear Detection
- Waterproof Buttons (Inductive)
- Low power Wake-up Buttons / Proximity
- Watches and fitness bands
- SAR Safety Sensor

1.3 Block Diagram

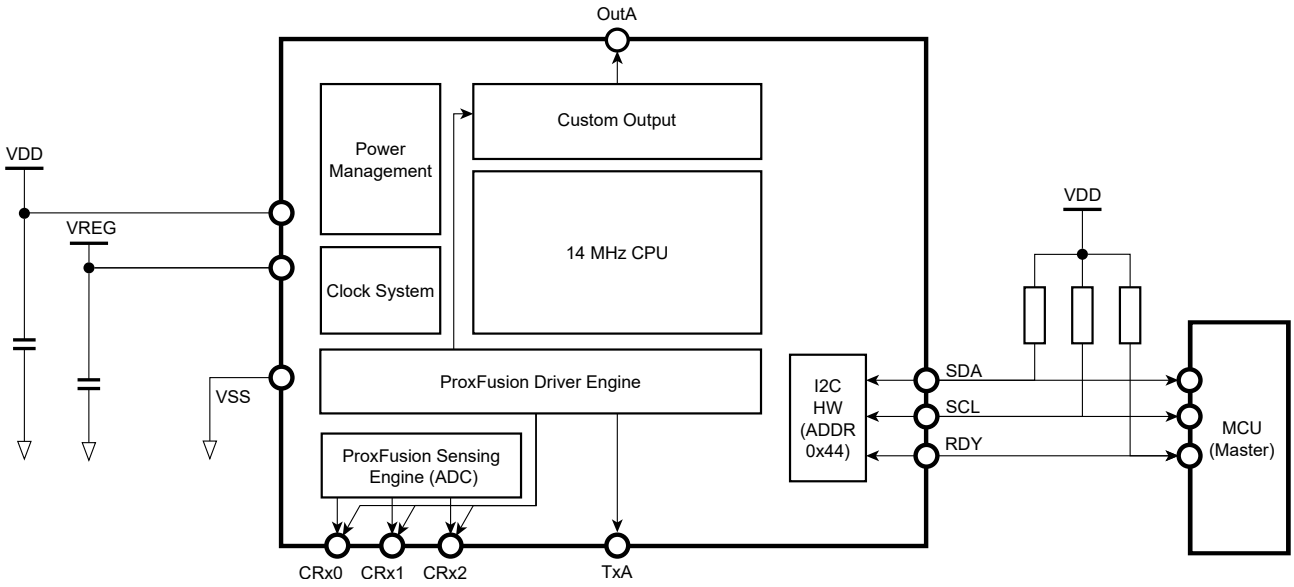


Figure 1.1: Functional Block Diagram

Contents

2 Hardware Connection

2.1 WLCSP11 Pin Diagram

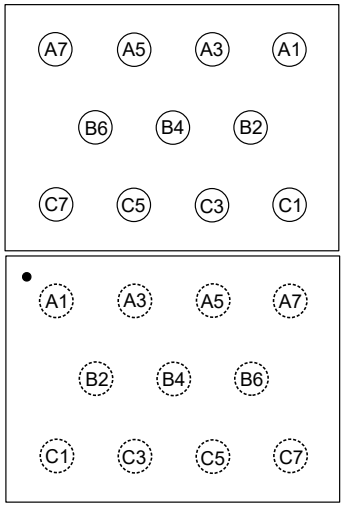


Table 2.1: 11-pin WLCSP11 Package

Pin no.	Signal
A7	VSS
A5	SDA
A3	VREG
A1	CRx1/CTx1
B6	TxA
B4	OutA
B2	CRx0/CTx0
C7	RDY/MCLR
C5	VDD
C3	SCL
C1	CRx2/CTx2/Bias

2.2 DFN12 Pin Diagram

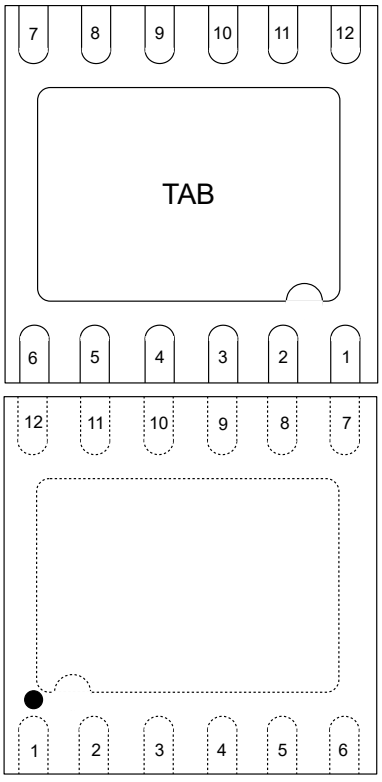
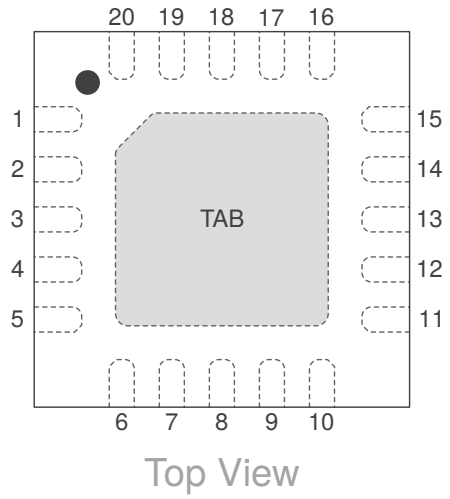


Table 2.2: 12-pin DFN Package

Pin no.	Signal
1	TxA
2	SDA
3	VDD
4	VREG
5	SCL
6	CRx2/CTx2/Bias
7	CRx0/CTx0
8	NC
9	CRx1/CTx1
10	OutA
11	RDY/MCLR
12	VSS

2.3 QFN20 Pin Diagram

Table 2.3: 20-pin QFN Package (Top View)



Top View

Pin no.	Signal	Pin no.	Signal
1	CRx2/CTx2/Bias	11	NC
2	CRx0/CTx0	12	NC
3	CRx1/CTx1	13	NC
4	NC	14	NC
5	NC	15	NC
6	VREG	16	NC
7	OutA	17	RDY/MCLR
8	VDD	18	TxA
9	VSS	19	SDA
10	NC	20	SCL

Area name	Signal
TAB[i]	Thermal pad (floating)

2.4 Signal Descriptions

Table 2.4: Signal Descriptions

Function	Signal Name	Signal Type	Pin Type[ii]	Description
ProxFusion®	CRx0/CTx0	Analog	IO	ProxFusion® channel
	CRx1/CTx1	Analog	IO	
	CRx2/CTx2/Bias	Analog	IO	
	TxA	Digital	O	TxA pad
	OutA	Digital	O	OutA pad
GPIO	RDY/MCLR	Digital	IO	Active pull-up, 200k resistor to VDD. Pulled low during POR, and MCLR function enabled by default. VPP input for OTP
I^2C	SDA	Digital	IO	I^2C Data
	SCL	Digital	IO	I^2C Clock
Power	VDD	Power	P	Power supply input voltage
	VREG	Power	P	Internal regulated supply output
	VSS	Power	P	Analog/Digital Ground

[i] It is recommended to connect the thermal pad (TAB) to VSS.
[ii] Pin Types: I = Input, O = Output, I/O = Input or Output, P = Power

2.5 Reference Schematic

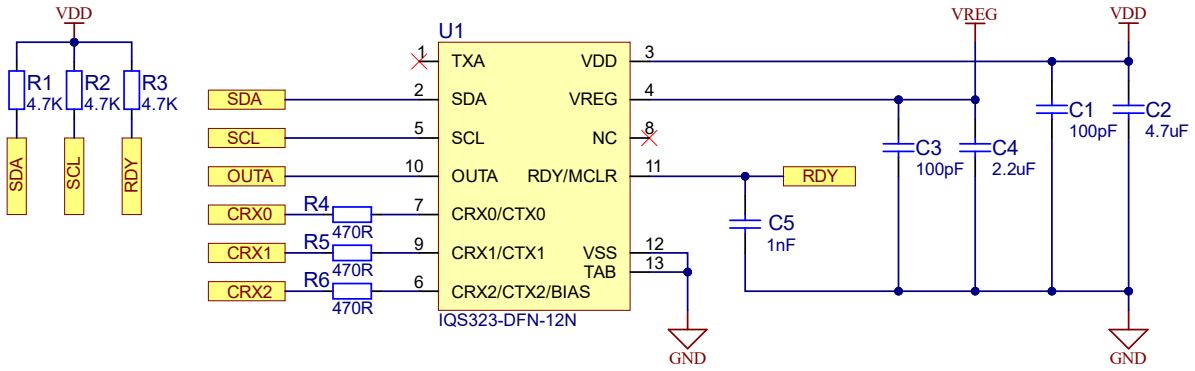


Figure 2.1: 3 Button Self Capacitance Reference Schematic

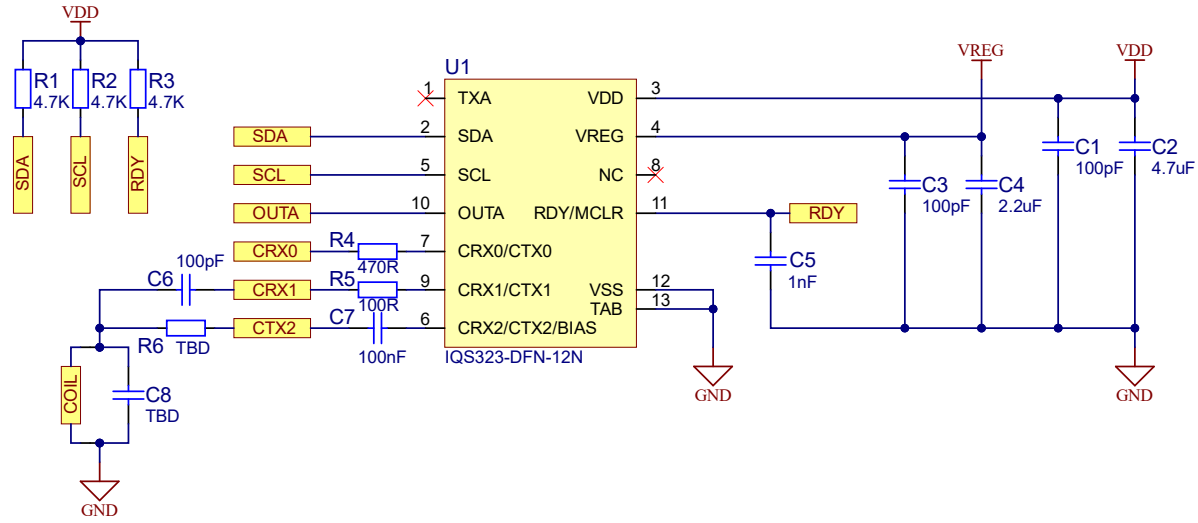


Figure 2.2: Single Proximity/Touch Key and Inductive Sensing Reference Schematic

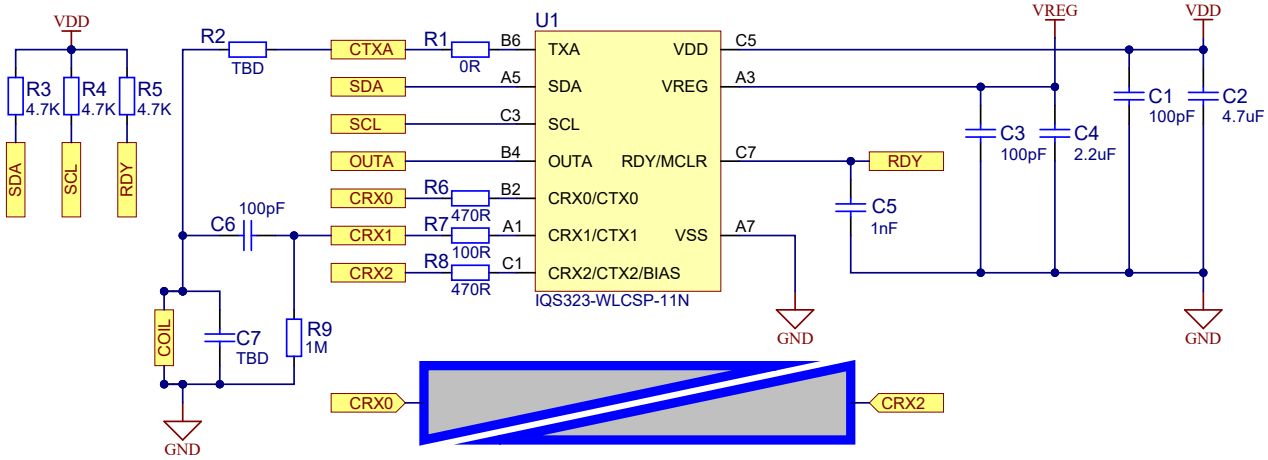


Figure 2.3: Self Capacitive Slider and Inductive Sensing Reference Schematic

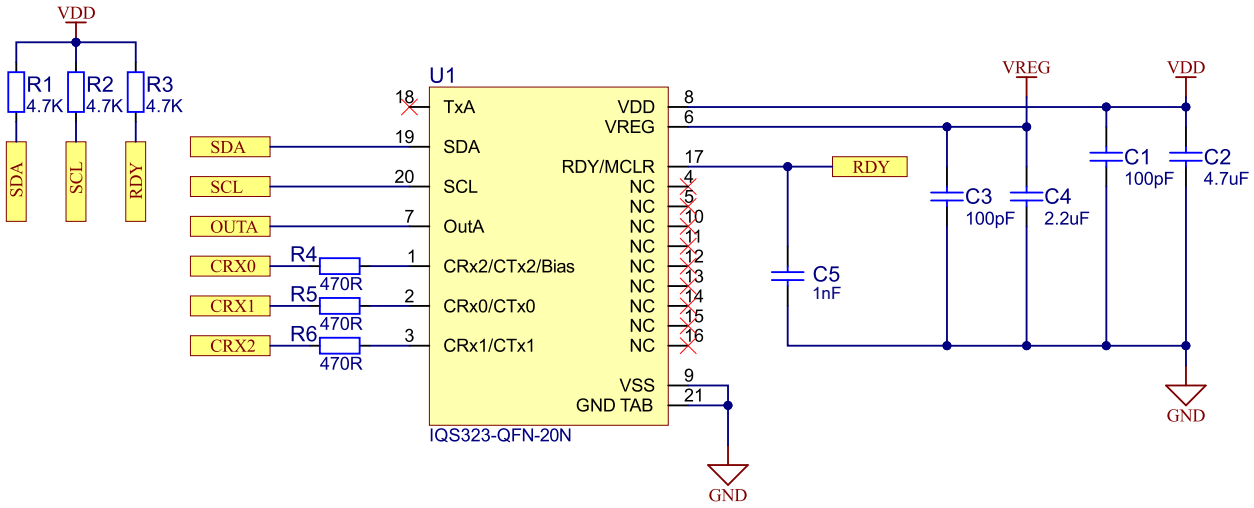


Figure 2.4: 3 Button Self Capacitance Reference Schematic

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

	Min	Max	Unit
Voltage applied at VDD pin to VSS	1.71	3.5	V
Voltage applied to any ProxFusion® pin	-0.3	VREG	V
Voltage applied to any other pin (referenced to VSS)	-0.3	VDD + 0.3 (3.5V max)	V
Storage temperature, T_{stg}	-40	85	°C

3.2 Recommended Operating Conditions

Recommended operating conditions		Min	Nom	Max	Unit
VDD	Supply voltage applied at VDD pin	1.71		3.5	V
VREG	Internal regulated supply output for analog domain		1.53		V
VSS	Supply voltage applied at VSS pin	0	0	0	V
T_A	Operating free-air temperature	-40	25	85	°C
C_{VDD}	Recommended capacitor at VDD	$2*C_{VREG}$	$3*C_{VREG}$		µF
C_{VREG}	Recommended external buffer capacitor at VREG, ESR≤ 200mΩ	2[i]	5	13	µF
$Cx_{\_SELF-VSS}$	Maximum capacitance of all external electrodes on all ProxFusion® blocks (self-capacitance mode)	-	-	400	pF
$Cm_{\_CTX-CRX}$	Capacitance of all external electrodes on all ProxFusion® blocks (mutual-capacitance mode)	0.1	-	9	pF
$Cx_{\_CRX-VSS-1M}$	Maximum capacitance of all external electrodes on all ProxFusion® blocks (mutual-capacitance mode @f_{xfer}=1MHz)			100	pF
$Cx_{\_CRX-VSS-4M}$	Maximum capacitance of all external electrodes on all ProxFusion® blocks (mutual-capacitance mode @ f_{xfer}=4MHz sensing)			25	pF
$\frac{Cx_{CRX-VSS}}{Cm_{CTX-CRX}}$	Capacitance ratio for optimal SNR in mutual capacitance mode	10		20	n/a
$RCx_{\_CRX/CTX}$	Series (in-line) resistance of all mutual capacitance pins (Tx & Rx pins) in mutual capacitance mode	0[ii]	0.47	10[iii]	kΩ
$RCx_{\_SELF}$	Series (in-line) resistance of all self capacitance pins in self capacitance mode	0[ii]	0.47	10[iii]	kΩ

3.3 ESD Rating

		Value	Unit
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[iv]	± 2000	V

[i] Absolute minimum allowed capacitance value is 1 µF, after taking derating, temperature, and worst-case tolerance into account. Please refer to the AZD004 application note for more information regarding capacitor derating.

[ii] Nominal series resistance of 470Ω is recommended to prevent received and emitted EMI effects. Typical resistance also adds additional ESD protection.

[iii] Series resistance limit is a function of f_{xfer} and the circuit time constant, RC. R_{max} x C_{max} = $\frac{1}{(6xf_{xfer})}$ where "C" is the pin capacitance to Vss.

[iv] JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.

3.4 Current Consumption

Inductive Mode Setup: ATI Target = 256, F_{OSC} = 14MHz
Self-capacitive Mode Setup: ATI Target = 512, F_{xfer} = 500kHz
Mutual capacitive Mode Setup: ATI Target = 512, F_{xfer} = 500kHz
Interface Selection: Event mode

Power mode	Active channels	Report rate [ms]	Typical Current [µA]	
			1.8V	3.3V
Normal Power	Inductive (1 coil)	10	128	129
	Self-capacitive (3 channels)	16	125	125
	Mutual Capacitive (2 channels)	16	171	172
Low Power	Inductive (1 coil)	80	11.0	11.5
	Self-capacitive (3 channels)	60	37.0	37.5
	Mutual Capacitive (2 channels)	60	50.0	50.5
Ultra Low Power	Inductive (1 coil)	200	6.50	7.00
	Self-capacitive (3 channels)	160	4.00	4.00
	Mutual Capacitive (2 channels)	160	9.00	9.00
Halt	NA	3000	2.00	2.00

4 Timing and Switching Characteristics

4.1 Reset Levels

Table 4.1: Reset Levels

Parameter		Min	Max	Unit
V_{VDD}	Rising edge (Reset release) - slope >100V/s	-	1.65	V
	Falling edge (Reset trigger) - slope >100V/s	0.90	-	V

4.2 MCLR Pin Levels and Characteristics

Table 4.2: MCLR Pin Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
$V_{IL(MCLR)}$	MCLR Input low level voltage	VDD = 3.3V	VSS – 0.3	-	1.05	V
		VDD = 1.7V			0.75	
$V_{IH(MCLR)}$	MCLR Input high level voltage	VDD = 3.3V	2.25	-	VDD + 0.3	V
		VDD = 1.7V	1.05			
$R_{PU(MCLR)}$	MCLR pull-up equivalent resistor		180	210	240	kΩ
$t_{PULSE(MCLR)}$	MCLR input pulse width – no trigger	VDD = 3.3V	-	-	15	ns
		VDD = 1.7V			10	
$t_{TRIG(MCLR)}$	MCLR input pulse width – ensure trigger		250	-	-	ns

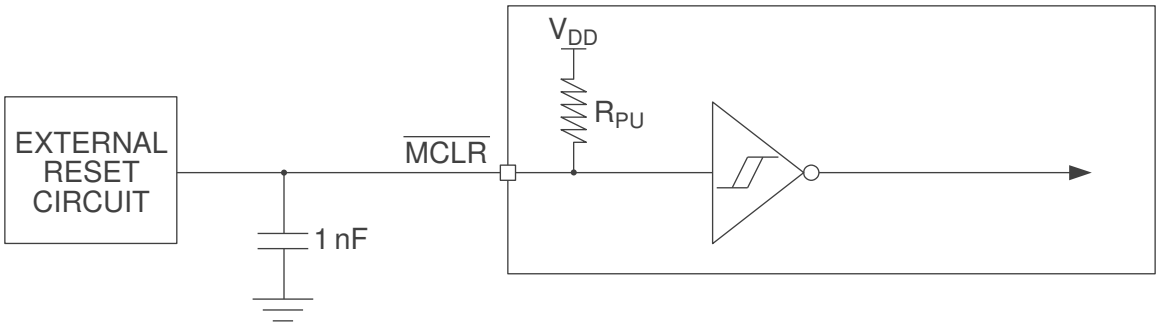


Figure 4.1: MCLR Pin Diagram

4.3 Digital I/O Characteristics

Table 4.3: Digital I/O Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{OL}	SDA & SCL Output low voltage	I_{sink} = 20mA			0.3	V
V_{OL}	TxA Output low voltage OutA Output low voltage RDY/MCLR Output low voltage	I_{sink} = 10mA			0.15	V
V_{OH}	Output high voltage	I_{source} = 20mA	VDD - 0.2			V
V_{IL}	Input low voltage		VDD * 0.3			V
V_{IH}	Input high voltage				VDD * 0.7	V
C_{b_max}	SDA & SCL maximum bus capacitance				550	pF

4.4 I²C Characteristics

Table 4.4: I²C Characteristics

Parameter		Test Conditions	VDD	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency		1.8V, 3.3V			1000	kHz
$t_{HD,STA}$	Hold time (repeated) START		1.8V, 3.3V	0.26			µs
$t_{SU,STA}$	Setup time for a repeated START		1.8V, 3.3V	0.26			µs
$t_{HD,DAT}$	Data hold time		1.8V, 3.3V	0			ns
$t_{SU,DAT}$	Data setup time		1.8V, 3.3V	50			ns
$t_{SU,STO}$	Setup time for STOP		1.8V, 3.3V	0.26			µs
t_{SP}	Pulse duration of spikes suppressed by input filter		1.8V, 3.3V	0		50	ns

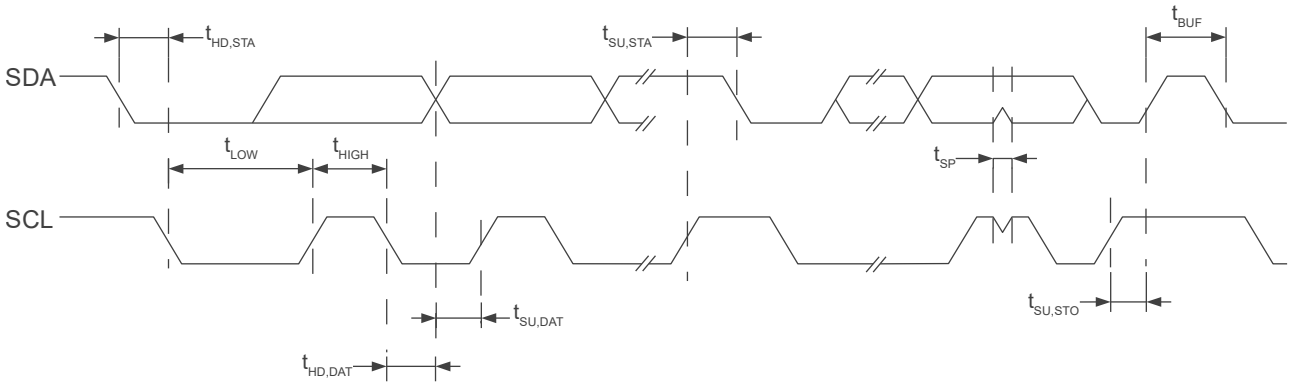


Figure 4.2: I²C Mode Timing Diagram

5 ProxFusion® Module

The IQS323 contains a single ProxFusion® module that uses patented technology to measure and process the sensor data.

5.1 Channel Options

Self-capacitive, mutual-capacitive, reference tracking and inductive designs are possible with the IQS323.

The below application notes provide background and information on applications where the IQS323 would be a suitable choice.

- Azoteq Sensing Technologies: AZD004
- Capacitive Sensing Design Guide: AZD125
- Inductive Design Layout Guide: AZD115

5.2 Low Power Options

The IQS323 offers 4 power modes:

- Normal power mode (NP)
- Low power mode (LP)
  - Typically set to a slower rate than NP
- Ultra-low power mode (ULP)
  - Optimized firmware setup
  - Intended for rapid wake-up from deep sleep on a single channel (e.g. distributed proximity event), enabling immediate button response for an approaching user
  - Other sensor channels are sampled at a slower rate in order to optimize power consumption
- Halt mode
  - Deep sleep in which no conversions or processing are done

The NP, LP and ULP power modes are described in the AZD004 application note.

In Halt mode, the IQS323 will remain in a deep sleep state. To exit Halt Mode, a force communications request must be made(see Section 8.13), and the power mode must be changed in the following communications window. For lowest power consumption it is recommended to set the *Halt Mode Report Rate* to 3000ms by writing ’3000’ to the *Halt Mode Report Rate* register.

The currently active power mode is reported in the *System Status* register.

5.3 Power Mode Selection

The power mode is selected by writing the appropriate value to the *Power Mode* field in the *System Control* register.

In order to optimize power consumption, power modes are stepped when the power mode is set to ’Automatic’. This moves the device to more power efficient modes when no interaction has been detected for a certain configurable time specified by the *Power Mode Timeout* register. Setting the power mode timeout to ’0x00’ will prevent the chip from lowering the power mode.

In addition to ’Automatic’ power mode, the IQS323 power mode switching can also be set to ’Automatic

No ULP'. This functions identically to 'Automatic' mode except the device will never enter Ultra Low Power (ULP) mode.

While the power mode switching is set to either 'Automatic' or 'Automatic No ULP', the IQS323 will return to normal power mode regardless of the current power mode if any events are triggered. Thereafter, the automatic power mode switching will take effect.

5.4 Count Value

The sensing measurement returns a counts value for each channel. The counts value is the raw measured signal for a channel. Count values are inversely proportional to capacitance and inductance, and all other outputs are derived from this.

Counts are reported in the *Filtered Counts* registers.

5.4.1 Linearise Counts

If the *Linearise Counts* bit in the *Sensor Setup* register is set, the IQS323 linearises the counts before reporting them. If this option is set, the counts are inverted and the *Invert* bit must be appropriately set to ensure correct channel logic.

It is recommended to linearise the counts, especially when using the Release UI (Section 7.4).

5.4.2 Max Counts

Each channel is limited to having a count value smaller than some limit. The limit is set by the *Max Counts* setting in the *Prox Control* register. If the ATI settings or hardware causes measured count values higher than the limit, the conversion will be stopped, and the maximum value will be read. Limiting the counts prevents the IQS323 from getting stuck under error conditions. The smallest maximum count setting that is above the expected maximum counts under normal operating conditions should be selected.

If the *Linearise Counts* bit in the *Sensor Setup* register is set, it is possible that a counts value greater than the maximum counts will be reported. This is because linearisation of the counts occurs after the maximum counts setting is enforced.

5.5 Reference Value/Long-Term Average (LTA)

User interaction is detected by comparing the measured count values to some reference value called the Long Term Average (LTA). The LTA of a sensor is slowly updated to track changes in the environment. During a touch or proximity event, the LTA is frozen.

Channel LTA's are reported in the *Channel X LTA* registers.

5.5.1 Reseed

It is possible that there are situations which would call for a manual reseed of the LTA. A reseed takes the latest measured counts, and seeds the LTA with this value. This updates the LTA to match the latest conditions in the external environment.

A reseed command is given by setting the *Reseed* bit in the *System Control* register. The *Reseed* bit is automatically cleared once the reseed has been completed.

5.6 Filter Betas

An Infinite Impulse Response(IIR) filter is applied to the digitized raw input for both the counts value and the LTA.

Damping options for the counts and LTA filters are defined in the *Counts Filter Betas*, *LTA Filter Betas* and *LTA Fast Filter Betas* registers.

Damping factor = Beta/256

The NP filter betas are used when the *Current Power Mode* in the *System Status* register is 'Normal Power'. When the *Current Power Mode* is 'Low Power' or 'Ultra Low Power', the LP filter betas are used.

The *Fast Filter Band* determines when the fast beta filters are used. Fast filtering is applied to the LTA if the channel counts drift away from the LTA in the opposite direction to the sensing direction by more than the *Fast Filter Band*. Once the difference between the counts and LTA is less than the fast filter band the normal filters are used again.

5.7 Proximity and Touch Thresholds

Each channel has its own independently settable proximity and touch thresholds. These thresholds, along with the channel's counts and LTA, determine whether a channel is in a proximity or touch state. Once a channel enters a proximity or touch state, the relevant *CHx Prox* or *CHx Touch* bits will be set in the *System Status* register, and will remain set until the channel leaves its proximity or touch state.

With non-inverted channel logic and dual direction sensing disabled, a channel will enter the proximity state if

(LTA-Counts) > Prox Threshold

for more than the number of consecutive samples specified by the *Prox Debounce Enter* field in the Prox Settings register. The channel will exit the proximity state if the above condition is not met for more than the number of consecutive samples specified by the *Prox Debounce Exit* field. The *Prox Threshold* is set in the *Prox Settings* register.

A channel will enter the touch state if

(LTA-Counts) > Touch Threshold

and exit the touch state if

(LTA-Counts) < (Touch Threshold - Touch Hysteresis)

The *Touch Threshold* and *Touch Hysteresis* are set in the *Touch Settings* register.

Setting a channel's *Invert* bit in the *Sensor Setup* register will invert the logic above. This setting is required because counts increase with user interaction when sensing mutual capacitance and inductance, and decrease when sensing self capacitance.

If the *Dual Direction* bit in the *Sensor Setup* register is set, the proximity and touch thresholds will be applied in both directions, meaning that a channel will be in a proximity or touch state if

Counts > (LTA + Threshold) or Counts < (LTA - Threshold)

5.8 Channel Timeouts

A channel will be reseeded and therefore exit a proximity or touch state if it has been in a proximity or touch state for longer than the relevant time specified by the timeouts in the *Event Timeouts* register[i].

The times specified by the event timeouts apply to all channels. They can be disabled on a per channel basis using the *CHx Timeout Disable* bits in the *System Control* register.

5.9 Automatic Tuning Implementation (ATI)

The ATI is a sophisticated technology implemented in ProxFusion® devices to provide optimal performance over a wide range of sensing electrode capacitances and inductance, without modification of external components.

The choice of ATI parameters has a significant impact on channel performance. The ATI algorithm is responsible for selecting each channel's dividers, multipliers and compensation.

[i] If channel prox and touch timeouts are used then ULP mode should not be used. For automatic power mode switching set the mode to 'Automatic No ULP'.

When the *ATI Mode* in the *ATI Setup* register is set to 'Full', the *Coarse Fractional Divider*, *Fine Fractional Divider*, *Coarse Fractional Multiplier* and *Fine Fractional Multiplier* fields in the *ATI Multipliers and Dividers* register are set by the ATI algorithm using the value in the *ATI Base* register as an input to the algorithm. The coarse parameters are set before the fine parameters. Generally, a lower base value will increase sensitivity.

Each channel's *Compensation Value* and *Compensation Divider* in the channel's *Compensation* register are set by the ATI algorithm using the *ATI Resolution Factor* in the *ATI Setup* register. A higher resolution factor will generally increase sensitivity.

When an ATI is triggered, the algorithm will first adjust the dividers and multipliers so that the counts are as close to the *ATI Base* as possible. The *Compensation Value* and *Compensation Divider* are then adjusted until the counts are as close as possible to the ATI Target, where:

ATI Target = (Counts after dividers and multipliers have been set) $\times$ (ATI Resolution Factor / 16)

In certain cases it is desirable to fix some or all of the dividers and multipliers at design time. For these cases, the *ATI Mode* can be set to 'ATI from Fine Fractional Divider', 'ATI from Compensation Divider' or 'Compensation Only'.

For measurements where the conversion frequency is greater than 2MHz, the *Compensation Value* should be minimised and the *Compensation Divider* should be maximised, or both the *Compensation Value* and the *Compensation Divider* should be set to '0'. This is achieved by setting the *ATI Resolution Factor* to '16' with ATI enabled, or disabling ATI and setting both the *Compensation Value* and *Compensation Divider* to '0'.

It is recommended to set the *ATI Mode* to 'Full' and to allow the ATI algorithm to select the dividers, multipliers and compensation.

The ATI algorithm executes in a short time, and therefore goes unnoticed by the user.

5.10 Automatic Re-ATI

The IQS323 automatically detects when a channel drifts out of it's design time operating range. To place the channel back into it's expected operating range, a re-ATI is automatically triggered.

When a re-ATI occurs the *ATI Event* bit in the *System Status* register will be set. It is cleared when read by the master through I^2C.

A re-ATI is executed when the LTA of a channel drifts outside of the *ATI Band*. The band is centered around the ATI Target. The *ATI Band* for all channels is configured in the *ATI Setup* register.

Re-ATI Boundary = ATI Target $\pm$ ATI Band

For example, suppose that the ATI Target is 800 and that the *ATI Band* selection is 1/8. The ATI band would then be $\frac{1}{8} \times 800 = 100$ counts. If ATI is enabled, it will be run when:

LTA > 900 or LTA < 700

5.11 ATI Error

After the ATI algorithm is executed, a check is done to see if there are any errors. The *ATI Error* bit in the *System Status* register is set if the following is true for any channel after the ATI has completed:

- Counts are outside the **Re-ATI Boundary** upon completion of the ATI algorithm

A re-ATI will not be automatically triggered if an ATI Error occurs. If an ATI Error occurs the master should manually trigger a re-ATI by setting the *Re-ATI* bit in the *System Control* register. The *Re-ATI* bit is automatically cleared by the IQS323.

5.12 Sensor Setup

5.12.1 Self Capacitance, Mutual Capacitance and Inductive Measurements

All channels in use must be enabled by setting the *Enable Channel* bit in the channel's *Sensor Setup* register.

To perform a measurement the IQS323 must be configured to output the correct waveform on it's Tx pins. The *PXS Mode* in the *Prox Control* register must be selected for the required type of measurement and the correct Rxs and Txs must be selected in the *Prox Input and Control* and *Sensor Setup* registers. For a self-capacitive measurement, the same CRx and CTx must be selected. For example, if the sensing electrode is connected to CRx0/CTx0, both the *CRx0* bit in the *Prox Input and Control* register and the *CTx0* bit in the *Sensor Setup* register must be set.

When not using the Reference UI, the *Channel Mode* in the *Channel Setup* register must be set to 'Independent'.

For all measurement types an appropriate conversion frequency must be selected. Section 6.5 provides information on setting the conversion frequency.

For inductive measurements dead time must be disabled by clearing the *Dead Time Enable* bit in the *Prox Input and Control* register, and it is recommended to enable the *FOSC Tx Frequency* option in the *Sensor Setup* register and set the *Conversion Frequency Period* in the *Conversion Frequency Setup* register to '0'.

Wav Pattern 0 and *Wav Pattern 1* in the *Pattern Definitions* register define the waveforms to be output on the CTx pins. *Wav Pattern Select* in the *Pattern Selection and Engine Bias Current* register selects whether *Wav Pattern 0* or *Wav Pattern 1* is output on each CTx pin.

Writing a '0' to a bit in the *Wav Pattern Select* field will output the pattern defined by *Wav Pattern 0* on the corresponding Tx. Likewise, writing a '1' will output the waveform defined by *Wav Pattern 1*. Table 5.1 how the bits in the *Wav Pattern Select* register map to the Txs.

Table 5.1: Wav Pattern Select

Bit3	Bit2	Bit1	Bit0
TxA	CTx2	CTx1	CTx0

Table 5.2 shows the values to be written to *Wav Pattern 0* and *Wav Pattern 1* for each measurement type. In all cases *Wav Pattern Select* should be set to '0x00'.

Table 5.2: Recommended Pattern Values

Measurement Type	Wav Pattern 0	Wav Pattern 1
Self Capacitance	0x03	0x00
Mutual Capacitance	0x0E	0x00
Inductive	0x0B	0x00

5.12.2 Temperature/Current Measurement

The IQS323 is capable of measuring the external temperature or an external current. The measurement is not very accurate. Depending on the hardware, there are some fringe cases where this type of measurement may be useful.

In most cases, the temperature/current measurement should be disabled by clearing the *Internal Reference* bit in the *Prox Input and Control* register.

5.12.3 Calibration Capacitor

The IQS323 has an internal calibration capacitor (CalCap). The calibration capacitor can be connected to the input of the ProxFusion® module and used as a load for a conversion. Typically, the calibration capacitor is used for debugging and characterisation.

When not using the CalCap, the *Calibration Capacitor* field in the *Pattern Definitions* register should be set to '0pF', the *CalCap Rx* and *CalCap Tx* bits in the *Sensor Setup* register should be cleared and *Calibration Capacitor Select* in the *Prox Input and Control* register should be cleared.

6 Hardware Settings

6.1 Inactive Rxs

The *Inactive Rxs* in the *Pattern Definitions* register sets the state of any Rxs that are not selected for the currently executing conversion.

For best noise rejection, the *Inactive Rxs* option should be set to 'VSS'.

6.2 Prox Control Settings

The *Prox Control* register contains various configuration options for the ProxFusion® module. Some of the configuration settings apply to all measurement types.

0v5 Discharge

During a conversion, the reference capacitor (Cs) is charged until the voltage over it reaches some threshold. Once the conversion has completed, the Cs capacitor is fully discharged in preparation for the next conversion.

Setting the *0v5 Discharge* bit will discharge the Cs capacitor to 0.5V instead of 0V. With the *0v5 Discharge* bit set, the charging curve is more linear. However, this can introduce some noise.

For most applications it is recommended to fully discharge the Cs capacitor.

Cs Size

The size of the Cs capacitor is selected using the *Cs Size* option.

The Cs capacitor can be either 40pF or 80pF. Selecting between the 40pF and 80pF options puts the measurement into different operating regions.

For most applications, using the 80pF *Cs Size* option is appropriate.

S/H Bias Select

A mutual capacitance conversion makes use of Sample and Hold (S/H) circuitry. The *S/H Bias Select* option selects how aggressively the S/H circuit holds after sampling.

The *S/H Bias Select* setting should be set to 10uA.

6.3 Engine Bias Current

A constant bias current can be applied at the input to the ProxFusion® module during conversions. The bias current is enabled by setting the *Prox Engine Bias Current* bit in the *Prox Input and Control* register. The current is selected using the *Engine Bias Current* and *Engine Bias Current Trim* values in the *Patten Selection and Engine Bias Current* register.

In certain cases, the bias current can be used to bias a measurement setup. This moves the operating point of the measurement. It is recommended to disable the bias current for all measurements unless otherwise advised by an Azoteq engineer.

6.4 Dead Time

Setting the *Dead Time Enable* bit in the *Prox Input and Control* register will add a period of dead time between the charge and transfer phases in every conversion. This allows the ProxFusion® module time to switch in and out its measurement circuitry.

Dead time should always be enabled for capacitance measurements, and disabled for inductive measurements.

6.5 Conversion Frequency

The charge transfer frequency (f_{xfer}) is set using the *Conversion Frequency Fraction* and *Conversion Frequency Period* fields in the *Conversion Frequency Setup* register. For high resistance sensors, it might be needed to decrease f_{xfer}.

It is recommended to always set the *Conversion Frequency Fraction* to '127' and to select the conversion frequency with the *Conversion Frequency Period*.

The *Dead Time Enable* option in the *Prox Input and Control* register must be considered when setting the conversion frequency. See the description for the *Conversion Frequency Setup* register in the memory map for details.

6.6 Reset

6.6.1 Reset Indication

After a reset, the *Reset Event* bit in the *System Status* register will be set to indicate a reset event occurred. The *Reset Event* bit is cleared when the master sets the *ACK Reset* bit in the *System Control* register. Under a reset condition communication windows will continuously be opened by the IQS323.

After a reset event, the chip's settings revert to their start-up values. To recover, the master must first acknowledge the reset event by setting the *ACK Reset* bit, and then re-write all the application settings to the IQS323 over I^2C.

While the *Reset Event* bit is set:

- The device will not be able to enter I^2C event mode
- ATI will take much longer to complete, since communication windows are continuously being opened

6.6.2 Software Reset

The IQS323 can be forced to reset by setting the *Soft Reset* bit in the *System Control* register.

6.6.3 Hardware Reset

Pulling the Ready / Master Clear (RDY/MCLR) pin low will hard reset the device. When a communications window is open, the IQS323 disables MCLR functionality and pulls RDY/MCLR low. Therefore, the master cannot hard reset the IQS323 when RDY/MCLR is low.

For MCLR reset levels see Section 4.2.

7 Additional Features

7.1 OutA Functionality

OutA is a push-pull output pin and can be used either as a general purpose output pin or as an event indicator. The *OutA Mask* register controls the behaviour of OutA.

7.1.1 OutA as a General Purpose Output

Writing a value of '0x0000' to *OutA Mask* will set the state of OutA to low (0V). Writing a value of '0x7FFF' to *OutA Mask* will set the state of OutA to high (VDD). Any other value will result in the behaviour outlined in Section 7.1.2.

7.1.2 OutA as an Event Indicator

If the *Total Channels* field in the *Slider Setup and Calibration* register is set to zero, the *OutA Mask* register selects which event in the *System Status* register controls OutA.

If *Total Channels* is greater than zero, the slider is enabled and the *OutA Mask* register selects which event in the *Gesture Status* register controls OutA.

In both cases OutA can be configured as either active high or active low using the most significant bit (bit 15) in the *OutA Mask* register. Setting the most significant bit to '1' will configure OutA as an active low pin while setting it to '0' will configure it as active low.

For example, suppose OutA is required to be low during a HOLD slider event and low otherwise. With the slider configured, the *OutA Mask* register selects from the events in the *Gesture Status* register. Since OutA should go low during a HOLD event and high otherwise, OutA must be configured to be active low and the HOLD event should be selected by setting the fifth bit in the *OutA Mask* register. Therefore the value '0x8020' should be written to the *OutA Mask* register.

7.2 Slider

The IQS323 is capable of processing a slider with on chip gesture recognition. A single channel slider can be used to do on chip tap and hold recognition for a single channel.

Slider events can be indicated using OutA. For more details on configuring this functionality, see Section 7.1.2.

Enabled gestures are reported in the *Gesture Status* register. The position of the touch on the slider is reported in the *Slider Position* register.

7.2.1 Setup

Any channels used for the slider must be set up as described in Section 5.12. If 3 mutual capacitance channels are used in a slider, TxA must be used as a shared Tx.

The slider is enabled by setting the *Total Channels* field in the *Slider Setup and Calibration* register to a non-zero value and enabling the slider channels by setting the *Channel X Enable* bits in the *Enable Mask* register.

The *Enable Status Pointer* register must be set correctly. This activates the slider when any of the enabled channels are in touch. Take note of the different status pointers for the different order codes.

The *Delta Links* registers determine the order in which the channels are processed. For example, if channel 1 is the first element in the slider, the *Delta Link 0* register must be set to '0x472' (for order codes with the Release UI).

The *Slider Resolution* register defines the output range of the slider position. The gesture setup registers must be set in accordance with the *Slider Resolution*. The touch position ranges from 0 to the *Slider Resolution*, where 0 is the start of the first slider element and the *Slider Resolution* is the end of the last slider element.

The *Upper Calibration Value* field in the *Slider Calibration and Bottom Speed* register and the *Lower Calibration Value* field in the *Slider Setup and Calibration* register are used to offset the end-points of the slider position so that they match the end-points of the physical slider.

The slider output position is dynamically filtered based on the *Slow/Static Beta* in the *Slider Setup and Calibration* register, the *Bottom Speed* field in the *Calibration and Bottom Speed* register and the value in the *Slider Top Speed* register. The *Slider Top Speed* and *Bottom Speed* are specified in pixels per sample period. Figure 7.1 shows the behaviour of the dynamic filter.

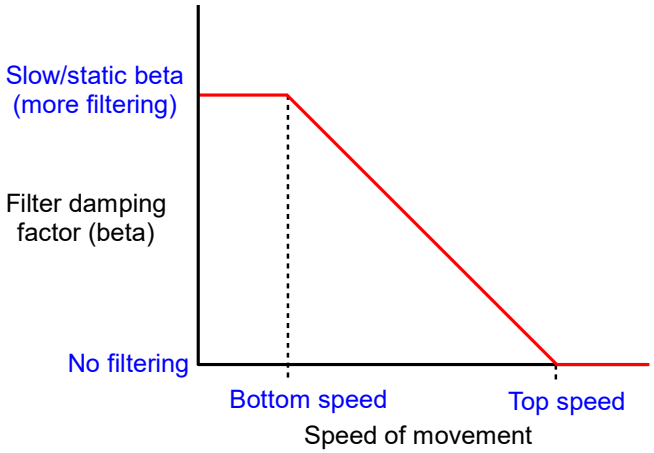


Figure 7.1: Slider filtering when the Static Filter bit is not set

If the *Static Filter* bit in the *Slider Setup and Calibration* register is set, the *Slow/Static Beta* is used to filter the slider position regardless of the touch's movement speed.

7.2.2 Gestures

The IQS323 does on chip gesture recognition when a slider is enabled.

All gestures are configurable and can be individually enabled using the *Gesture Enable* register. Gestures are reported in the *Gesture Status* register.

The recognised gestures are:

- Single Tap
- Swipe
- Flick
- Hold

Gesture parameters are specified in pixels and milliseconds.

For any gesture to be reported, a touch must be registered for at least as long as the value in the *Minimum Time* register. This prevents false touches from triggering the gestures.

Tap and Hold

A tap gesture will be reported if the touch lasts longer than the *Minimum Time* but less than the time specified in the *Maximum Tap Time* register, and the touch does not move further than the value in the *Maximum Tap Distance* register from its starting point. The tap will be reported only for the cycle in which it is detected.

Similarly, a hold will be reported if the touch lasts longer than both the *Minimum Time* and the time specified in the *Minimum Hold Time* register, and the touch does not move more than the *Maximum Tap Distance* from its starting point. Once a hold is detected, it will be continuously reported until the touch is released.

Swipe and Flick

Swipe and flick gestures are reported if there is a touch lasting longer than the *Minimum Time*, and the touch moves further from its starting point than the value in the *Minimum Swipe Distance* register. Given that the above conditions have been met, if the touch is released before the time specified in the *Maximum Swipe Time* register, a flick is reported. Otherwise, a swipe is reported.

Swipes and flicks are reported only in the cycle in which they are detected.

7.3 Reference UI

The IQS323 implements a Reference User Interface (Reference UI).

A reference channel adjusts the LTA of the primary sensing channel by subtracting the change in LTA of the reference channel from the LTA of the primary sensing channel. This subtraction is done when the primary sensing channel is in a touch or proximity state. The Reference UI eliminates the effect of count drift on the measurement.

For example, in wear detect applications the dielectric parameters of the PCB and sensor elements are likely to change over time, resulting in poor sensor performance. By using the Reference UI, the drift in counts due to temperature and/or humidity is accounted for and the sensor performance is not affected by the temperature change.

The reference channel sensor should be exposed to the same conditions as the sensing channel, and the user should not be able to affect the counts of the reference channel.

A single reference channel can be configured to have multiple follower channel's. However, a follower channel cannot have multiple references.

See the AZD125 application note for details on designing a reference channel.

7.3.1 Setting Descriptions

The *Channel Setup* register contains the parameters *Channel Mode*, *Reference Sensor ID* and *Follower Event Mask*. The *Follower Weight* is defined in the *Follower Weight* register.

Table 7.1 describes these settings.

Table 7.1: Reference UI Setting Descriptions

Setting	Description	Options
Channel mode	Configure channel as reference or follower	Independent Reference Follower
Reference Sensor ID	If a channel is selected as a follower then its *Reference Sensor ID* should be set to select which channel acts as a reference for it.	Set to the channel number of the desired reference channel.
Follower Event Mask	The reference channel should not ATI if the follower is in a proximity or touch state. This mask must be set to select the follower's *Prox* and *Touch* flags in the *System Status* register so that ATI is disabled for the reference channel when the follower is in a proximity or touch state. The *Follower Event Mask* only needs to be set if the channel is setup as a reference channel.	
Follower Weight	If the channel is set as a follower channel, this value determines how aggressively it will track the reference channel adjustment.	Register value/4096

7.3.2 Example Setup

In an example Reference UI setup Channel 0 is set as the follower and Channel 1 is configured as a reference.

Since Channel 0 is the follower and Channel 1 is the reference, the *Reference Sensor ID* for Channel 0 should be set to '0x01'. This selects Channel 1 as a reference for Channel 0.

The *Reference Sensor ID* is not used if the *Channel Mode* is set to 'Reference'. Therefore Channel 1's *Reference Sensor ID* is not used and must be set to '0x00'.

Since Channel 1 is the reference, its *Follower Event Mask* must be set to disable ATI on Channel 1 when Channel 0 is in a proximity or touch state. Channel 0's *Prox* and *Touch* flags are the first and second bits of the upper byte of the *System Status* register. To select them, the first and second bits of the *Follower Event Mask* should be set to 1. Therefore, 0x03 should be written to *Follower Event Mask* for Channel 1.

The *Follower Event Mask* is not used if the *Channel Mode* is set to 'Follower'. Therefore Channel 0's *Follower Event Mask* is not used and must be set to '0x00'.

A *Follower Weight* must be set for the follower channel. Its value is application specific. Setting the register value to '4096' will result in the follower channel directly tracking the reference. A value greater than 4096 will cause the follower to track the reference aggressively while a value less than 4096 results in slower tracking. The AZD125 application note describes the process of selecting an appropriate *Follower Weight*.

Table 7.2: Reference UI Example Settings

Setting	Channel 0	Channel 1
Channel mode	Follower	Reference
Reference Sensor ID	0x01	0x00
Follower Event Mask	0x00	0x03
Follower Weight	Bit value/4096	0x00

7.4 Release UI

The Release User Interface (Release UI) allows for the detection and release of long term touch and proximity events. In order to do this, the Release UI makes use of an additional LTA, called the Activation LTA. The Activation LTA for a channel can be read from the *Channel X Activation LTA* registers. Unlike the standard LTA, the Activation LTA is continuously updated, even when the channel is in a proximity or touch state. The Activation LTA is filtered using an IIR beta filter. The filter parameters are defined in the *Activation LTA Filter Betas* register.

When a touch or proximity event is detected the LTA is frozen but the Activation LTA is still updated. When the difference between the counts and Activation LTA is smaller than the value of the *Activation Settling Threshold* in the *Events Enable and Activation Settling Threshold* register for more than number of consecutive samples specified by the *Delta Snapshot Sample Delay* field in the *Release UI Settings* register, the absolute delta between the LTA and counts values is recorded and stored in the channel's *Delta Snapshot* register.

A percentage of the Delta Snapshot, as defined by the *Release Delta Percentage* in the *Release UI Settings* register, is used to exit the touch and proximity states.

If

$$\textbf{(Counts - Activation LTA) > (Delta Snapshot} \times \frac{\textbf{Release Delta Percentage}}{128}\textbf{)}$$

the channel is reseeded and therefore any touch or proximity states are exited.

The Release UI implementation allows for the detection of long term touch events by exiting a touch or proximity state based on the rate at which counts change rather than by comparing the counts to a fixed threshold.

For order codes implementing the Release UI, the Release UI is enabled by setting the *Release UI Enable* bit in the *Sensor Setup* register.

7.5 Movement UI

The Movement User Interface (Movement UI) is designed to detect movement[i]. This is useful in wear detection applications where there is a distinction between long term touch events in which movement is seen on the channel and long term touch events in which no movement is seen on the channel.

For example, a watch worn on a user's wrist will experience variation in counts while in touch. The same watch left on a table could also be in touch but no variation in counts will be seen.

A channel with the Movement UI enabled tracks an additional LTA called the Movement LTA. The

[i] ULP mode must not be used with the Movement UI. For automatic power mode switching set the mode to 'Automatic No ULP'.

Movement LTA for a channel can be read from the *Channel X Movement LTA* registers. The Movement LTA is continuously updated even when the channel is in a proximity or touch state.

When the difference between the counts and Movement LTA is greater than the *Movement Threshold* in the *Movement UI Settings* register for more than the number of consecutive samples set by the *Movement Debounce Enter* setting, the *Channel X Movement Status* bits in the *Movement Status* register are set.

When the difference between the counts and Movement LTA is less than the *Movement Threshold* for more than the number of consecutive samples set by the *Movement Debounce Exit* setting, the *Channel X Movement Status* bits in the *Movement Status* register are cleared.

Movement is indicated by there being significant variation in counts. When movement is occurring, the *Channel X Movement Status* bits will constantly be set and cleared as the difference between the counts and Movement LTA continuously changes. When movement stops, the Movement LTA will eventually reach the counts value and the *Channel X Movement Status* bits will be cleared.

If a channel's *Movement Status* bit has been cleared for longer than the time specified by the *Movement Timeout* register, the channel is reseeded and its touch and proximity states are cleared.

A channel with the Movement UI enabled will remain in a touch state while there is movement, and will exit the touch state and re-calibrate itself to the external environment if there is no movement.

The Movement LTA is filtered using an IIR beta filter. The filter beta values are set in the *Movement LTA Filter Betas* register.

Together with the *Movement Threshold*, the Movement LTA Betas can be adjusted to set how much movement is required to prevent a touch state from timing out and reseeding.

For order codes implementing the Movement UI, the Movement UI is enabled by setting the *Movement UI Enable* bit in the *Sensor Setup* register.

7.6 Watchdog Timer

The IQS323 implements a hardware watchdog timer. The watchdog timer is set to expire after 255ms if not kicked and will trigger a software reset upon expiration.

During I^2C communication the IQS323 kicks the watchdog timer whenever a byte level read or write occurs. Therefore, if the master initiates communication by sending an I^2C START condition and does not complete the I^2C transaction, the IQS323 will reset after 255ms.

The I^2C transaction is completed either when an I^2C STOP notification is sent by the master or when the master ends the communication as described in Section 8.9.

Outside of a communications window, the IQS323 will automatically kick the watchdog every cycle. The master is not required to manually kick the watchdog.

8 I²C Interface

8.1 I²C Module Specification

The device supports a standard two wire I²C interface with the addition of a ready (RDY) line. Byte level clock stretching is allowed. The communications interface of the IQS323 supports the following:

- *Fast-mode-plus* standard I²C up to 1MHz.
- Streaming data as well as event mode.

The IQS323 implements 8-bit addressing with 2 bytes at each address.

8.2 I²C Address

The 7 bit I²C address is determined by the order code. For available I²C addresses, see Section 10.

For every order code, the IQS323 will also acknowledge an additional debug I²C address. The debug address is for debugging purposes only and should not be used during normal operation. The debug address is the primary address with the least significant bit inverted. For example, the primary address for IQS323-001 is 0x44 and its debug address is 0x45.

8.3 I³C Compatibility

This device is not compatible with an I³C bus due to clock stretching allowed for data retrieval.

8.4 Communication During ATI

Provided the *Reset Event* bit in the *System Status* register is not set, I²C communications are disabled for the duration of the ATI process.

8.5 Memory Map Addressing and Data

The memory map implements 8-bit addressing. Data is formatted as 16-bit words meaning that two bytes are stored at each address. For example, address 0x10 will provide two bytes. The next two bytes read will be from address 0x11.

The 16-bit data is sent in little endian byte order (least significant byte first).

8.6 Ready (RDY) Indicator

The IQS323 has an open-drain active low RDY signal to inform the master that updated data is available. It is optimal for the master to use this as an interrupt input and initiate I²C communication only when the RDY signal is low.

The RDY line also serves as an reset pin. Reset functionality is described in Section 6.6.3.

8.7 Communications Window

When the device has data for the master, it will pull the RDY line low. This indicates that the device has opened its communications window and is expecting the master to address it. When the communication window is closed the IQS323 releases the RDY line. For information on when the communications window is closed see section 8.9.

Transfer of data between the master and slave must occur during the communications window (RDY is low). If the master wishes to initiate communication outside of a communications window (RDY is high), a force communications request must be made. Section 8.13 describes the force communications request sequence.

8.8 I²C Transaction Timeout

If the communication window is not serviced within the time specified in milliseconds by the *I²C Transaction Timeout* register, the communications window is closed (RDY goes high) and processing continues as normal. This allows the system to continue and keep reference values up to date even if the master is not responsive. However, the data for the closed window will be lost. The default *I²C Transaction Timeout* is set to 200ms. The *I²C Transaction Timeout* must be between 2ms and 230ms. The *I²C Transaction Timeout* is measured from the start of the communications window (RDY goes low).

Once communication between the master and the IQS323 has begun (START condition on I²C lines), the I²C transaction timeout is disabled leaving the watchdog timer in control. For more information on the behaviour of the device under these conditions see Section 7.6.

8.9 Terminate Communication

A standard I²C STOP will close the current communication window.

If the *Stop Bit Disable* bit in the *I2C Settings* register is set, the device will not respond to a standard I²C STOP. The communication window must be terminated using the end communications command (0xFF) shown in figure 8.1.

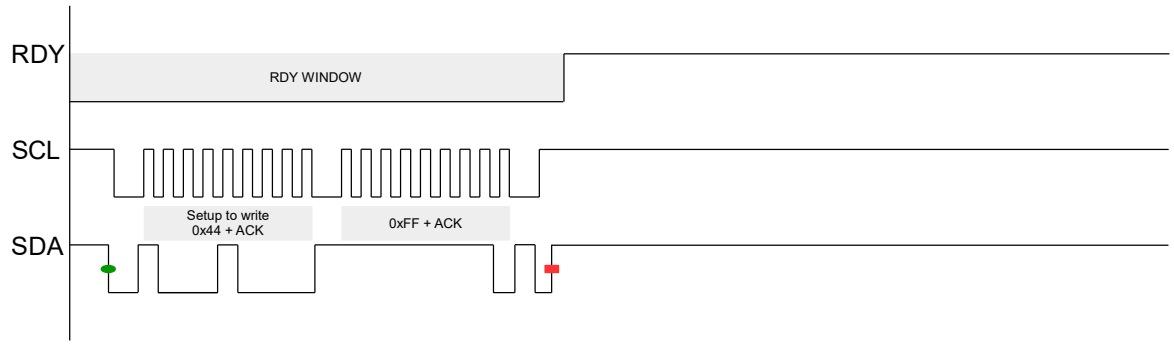


Figure 8.1: Force Stop Communication Sequence

8.10 Invalid Communications Return

The device will give an invalid communication response (0xEE) under the following conditions:

- The host is trying to read from a memory map register that does not exist.
- The host is trying to read from the device outside of a communication window (i.e. while RDY = high)

8.11 I²C Interface

The IQS323 has 2 I²C interface types. The I²C interface is selected using the *Interface Selection* bit in the *System Control* register.

8.11.1 I²C Streaming

In I²C streaming mode data is constantly reported at the relevant power mode report rate specified in milliseconds by the *Normal Power Report Rate*, *Low Power Report Rate* and *Ultra Low Power Report Rate* registers.

In ULP power mode the report rate is

(Auto Prox Cycle Select * Ultra Low Power Report Rate)ms

Where *Auto Prox Cycle Select* is defined in the *Prox Input and Control* register.

See Section 5.2 for a more detailed description of the ULP power mode.

8.11.2 I²C Event Mode

In event mode the RDY line will only go low when one or more of the enabled events are triggered or if the device resets. This is usually enabled since the master does not want to be interrupted unnecessarily during every cycle if no activity occurred.

8.12 Event Mode Communication

To enter event mode, the *Reset Event* bit in the *System Status* register must not be set. Reset behaviour is described in Section 6.6.1.

Enabled events are reported in the *System Status* register when triggered. Global events can be individually enabled by setting the relevant bit in the *Events Enable* register.

The global event flags are cleared when the master reads them via I^2C. When they are set, the IQS323 will continuously provide ready windows.

Table 8.1: Events Descriptions

Event	Trigger Condition
ATI Error	There has been an error during the ATI process
ATI Event	ATI has been triggered
Power	Power mode has changed
Slider	A slider gesture has been detected
Prox	Any channel has entered or exited a proximity state
Touch	Any channel has entered or exited a touch state

8.13 Force Communication

Ideally, communication with the IQS323 should only be initiated in a RDY window. In event mode RDY windows are only provided when an event is reported. In event mode it may be required to change device settings or query the device immediately. A communication request described in the figure below will force a RDY window to open. The minimum and maximum time between the communication request and the opening of a RDY window (t_{wait}) is application specific. The typical values of t_{wait} are $0.1ms \leq t_{wait} \leq 45ms$[i].

The communication request sequence is shown in figure 8.2.

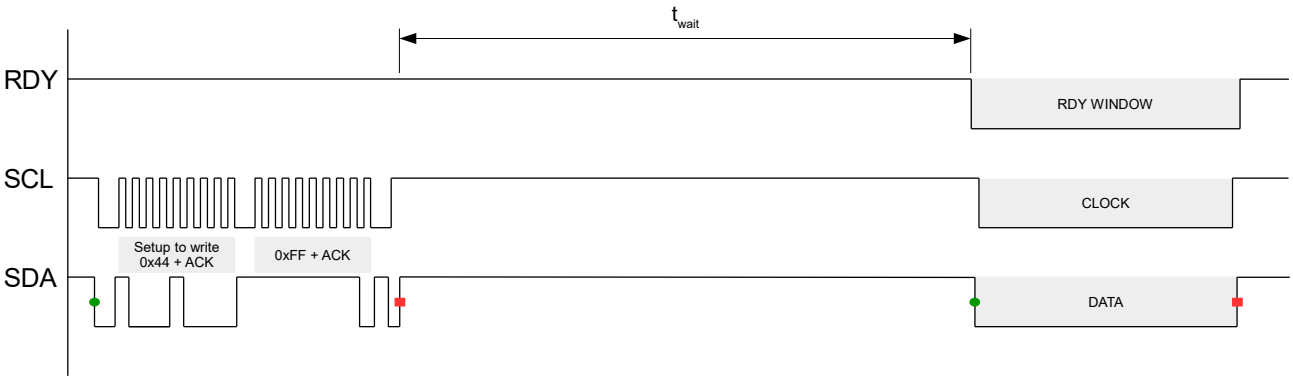


Figure 8.2: Force Communication Sequence

[i] Contact Azoteq for an application specific value of t_{wait}

8.14 Read/Write Check Disable

By default, some registers such as the counts and LTA values are read only. Writing to these registers over I^2C will have no effect. Setting the *Read/Write Check Disable* bit in the *I2C Settings* register will allow the master to write to any register and force its value.

9 Memory Map Register Descriptions

Address	Data (16bit)	Notes
0x00 - 0x09	Version details	See Table A.1
Read Only	**System Information**	
0x10	Systems Status	See Table A.2
0x11	Gestures	See Table A.3
0x12	Slider Position	16-bit value
0x13	Channel 0 Filtered Counts	16-bit value
0x14	Channel 0 LTA	
0x15	Channel 1 Filtered Counts	
0x16	Channel 1 LTA	
0x17	Channel 2 Filtered Counts	
0x18	Channel 2 LTA	
Read Only	**Release UI / Movement UI**	
0x20	Channel 0 Activation LTA / Channel 1 Movement LTA	16-bit value
0x21	Channel 1 Activation LTA / Channel 1 Movement LTA	
0x22	Channel 2 Activation LTA / Channel 2 Movement LTA	
0x23	Channel 0 Delta Snapshot / Movement Status	16 bit value / See Table A.4
0x24	Channel 1 Delta Snapshot / Not applicable for Movement UI	16-bit value
0x25	Channel 2 Delta Snapshot / Not applicable for Movement UI	
Read/Write	**Sensor 0 Setup**	
0x30	Sensor Setup 0	See Table A.5
0x31	Conversion Frequency Setup	See Table A.6
0x32	Prox Control	See Table A.7 / Table A.8
0x33	Prox Input and Control	See Table A.9
0x34	Pattern Definitions	See Table A.10
0x35	Pattern Selection and Engine Bias Current	See Table A.11
0x36	ATI Setup	See Table A.12
0x37	ATI Base	16-bit value
0x38	ATI Multipliers Selection	See Table A.13
0x39	Compensation	See Table A.14
Read/Write	**Sensor 1 Setup**	
0x40	Sensor Setup	See Table A.5
0x41	Conversion Frequency Setup	See Table A.6
0x42	Prox Control	See Table A.7 / Table A.8
0x43	Prox Input and Control	See Table A.9
0x44	Pattern Definitions	See Table A.10
0x45	Pattern Selection and Engine Bias Current	See Table A.11
0x46	ATI Setup	See Table A.12
0x47	ATI Base	16-bit value
0x48	ATI Multipliers and Dividers	See Table A.13
0x49	Compensation	See Table A.14
Read/Write	**Sensor 2 Setup**	
0x50	Sensor Setup	See Table A.5
0x51	Conversion Frequency Setup	See Table A.6
0x52	Prox Control	See Table A.7 / Table A.8
0x53	Prox Input and Control	See Table A.9

0x54	Pattern Definitions	See Table A.10
0x55	Pattern Selection and Engine Bias Current	See Table A.11
0x56	ATI Setup	See Table A.12
0x57	ATI Base	16-bit value
0x58	ATI Multipliers and Dividers	See Table A.13
0x59	Compensation	See Table A.14
Read/Write	**Channel 0 Setup**	
0x60	Channel 0 Setup	See Table A.15
0x61	Prox Settings	See Table A.16
0x62	Touch Settings	See Table A.17
0x63	Follower Weight	See Table A.18
0x64	Movement UI Settings (For order codes with Movement UI)	See Table A.19
Read/Write	**Channel 1 Setup**	
0x70	Channel 1 Setup	See Table A.15
0x71	Prox Settings	See Table A.16
0x72	Touch Settings	See Table A.17
0x73	Follower Weight	See Table A.18
0x74	Movement UI Settings (For order codes with Movement UI)	See Table A.19
Read/Write	**Channel 2 Setup**	
0x80	Channel 2 Setup	See Table A.15
0x81	Prox Settings	See Table A.16
0x82	Touch Settings	See Table A.17
0x83	Follower Weight	See Table A.18
0x84	Movement UI Settings (For order codes with Movement UI)	See Table A.19
Read/Write	**Slider Config**	
0x90	Slider Setup and Calibration	See Table A.20
0x91	Slider Calibration and Bottom Speed	See Table A.21
0x92	Slider Top Speed	16-bit value
0x93	Slider Resolution	
0x94	Enable Mask	See Table A.22
0x95	Enable Status Pointer	See Table A.23
0x96	Delta Link 0	See Table A.24
0x97	Delta Link 1	
0x98	Delta Link 2	
0x99	Reserved	Set to ’0x00’
Read/Write	**Gesture Config**	
0xA0	Gesture Enable	See Table A.25
0xA1	Minimum Time	16-bit value (ms)
0xA2	Maximum Tap Time	
0xA3	Maximum Swipe Time	
0xA4	Mininum Hold Time	
0xA5	Maximum Tap Distance	16-bit value
0xA6	Minimum Swipe Distance	
Read/Write	**Filter Betas**	
0xB0	Counts Filter Betas	See Table A.26
0xB1	LTA Filter Betas	See Table A.27
0xB2	LTA Fast Filter Betas	See Table A.28
0xB3	Activation/Movement LTA Filter Betas	See Table A.29
0xB4	Fast Filter Band	16 bit value
Read/Write	**System Control**	
0xC0	System Control	See Table A.30

0xC1	Normal Power Mode Report Rate	16-bit value (ms) Range: 0 - 3000
0xC2	Low Power Mode Report Rate	
0xC3	Ultra Low Power Mode Report Rate	
0xC4	Halt Mode Report Rate	
0xC5	Power Mode Timeout	16-bit value (ms) Range: 0 - 65000
Read/Write	**General**	
0xD0	OutA Mask	See Section 7.1
0xD1	I^2C Transaction Timeout	16 bit value (ms) Range: 2 - 230
0xD2	Event Timeouts	See Table A.31
0xD3	Events Enable and Activation Settling Threshold	See Table A.32 / Table A.33
0xD4	Release UI Settings / Movement Timeout	See Table A.34 / Table A.35
Read/Write	**I^2C Settings**	
0xE0	I^2C Setup	See Table A.36
0xE1	Hardware ID	See Table A.37

10 Ordering Information

10.1 Ordering Code

IQS323 zzz ppb

IC NAME	IQS323			
DEFAULT CONFIGURATION	zzz	=	001	I^2C address = 0x44. 3 button self capacitance with Release UI, configurable via I^2C.
			002	I^2C address = 0x58. 3 button self capacitance with Release UI, configurable via I^2C.
			A01	I^2C address = 0x44. 3 button self capacitance with Movement UI, configurable via I^2C.
PACKAGE TYPE	pp	=	CS	WLCSP11 package
		=	DN	DFN12 package
		=	QF	QFN20 package
BULK PACKAGING	b	=	R	WLCSP11 Reel (3000pcs/reel) DFN12 Reel (6000pcs/reel) QFN20 Reel (2000pcs/reel)

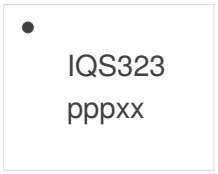
Figure 10.1: Order Code Description

Example : IQS323-001QFR

Throughout this document, generic order codes are referenced by only the device name and default configuration. For example, IQS323-00x refers to all versions with the Release UI, all package types and all bulk packaging options.

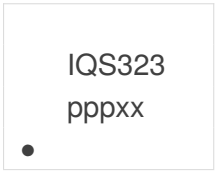
10.2 Top Marking

10.2.1 WLCSP11 Package



Product Name
ppp = product code
xx = batchcode

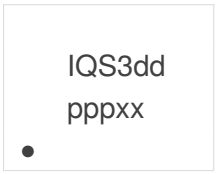
10.2.2 DFN12 Package Marking Option 1



Product Name
ppp = product code
xx = batchcode

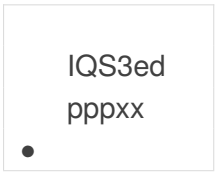
10.2.3 DFN12 Package Marking Option 2

Hardware ID (See Table A.37) = 0xF003



Product Name
ppp = product code
xx = batchcode

Hardware ID (See Table A.37) = 0xF004



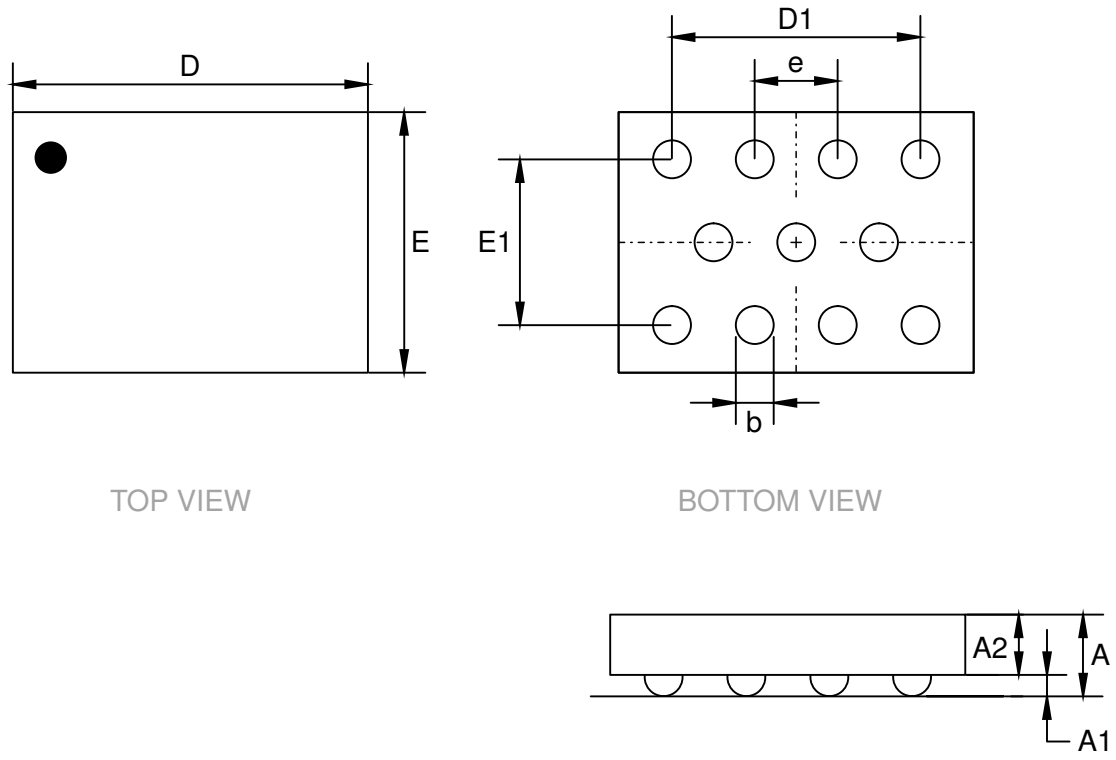
Product Name
ppp = product code
xx = batchcode

10.2.4 QFN20 Package

Product Name
ppp = product code
xx = batchcode

11 Package Specification

11.1 Package Outline Description - WLCSP11



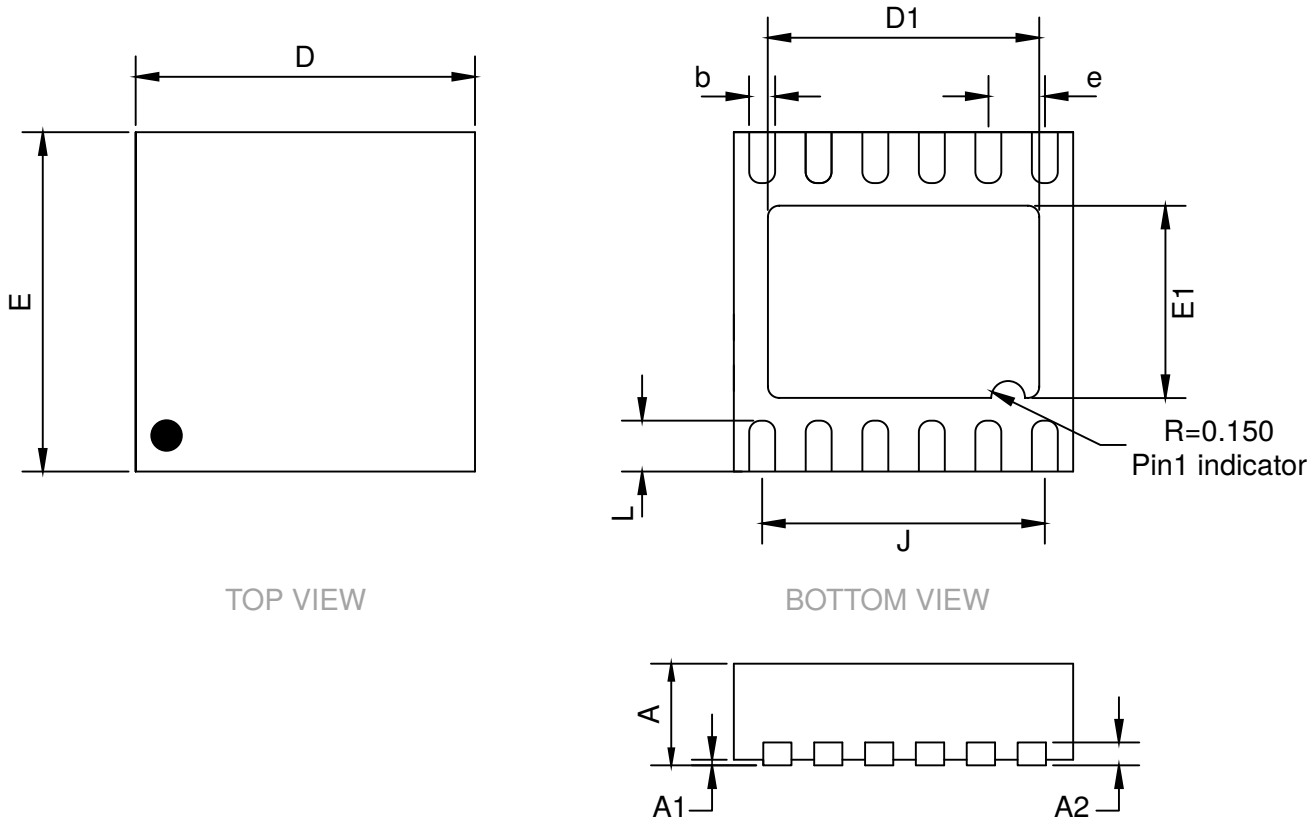
NOTES:
1. Drawing is not to scale.
2. Drawing is subject to change without notice.

Figure 11.1: WLCSP (1.48x1.08) - 11 Package Outline Visual Description

Table 11.1: WLCSP (1.48x1.08) - 11 Package Outline Visual Description (mm)

Dimension	Min	Nom	Max
A	0.303	0.345	0.387
A1	0.076	0.090	0.104
A2	0.227	0.255	0.283
D	1.46	1.48	1.50
E	1.06	1.08	1.10
D1		1.05 BSC	
E1		0.700 BSC	
b	0.136	0.160	0.184
e		0.350 BSC	

11.2 Package Outline Description - DFN12



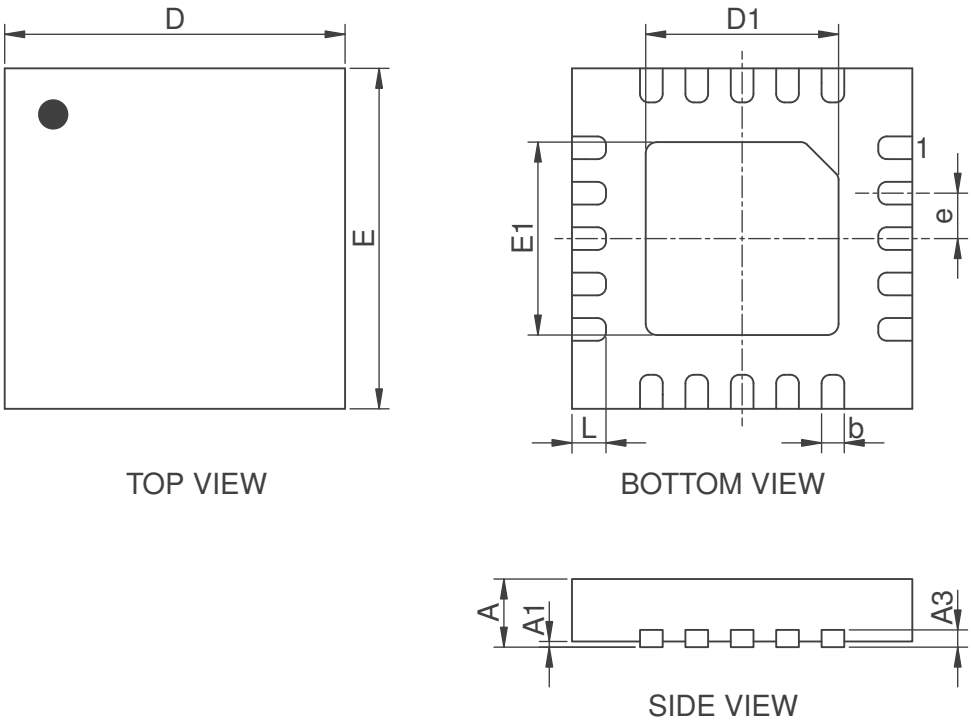
NOTES:
1. Drawing is not to scale.
2. Drawing is subject to change without notice.

Figure 11.2: DFN (3x3)-12 Package Outline Visual Description

Table 11.2: DFN (3x3)-12 Package Outline Visual Description (mm)

Dimension	Min	Nom	Max
A	0.700	0.750	0.800
A1	0.000		0.050
A2		0.203 REF	
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	2.35	2.40	2.45
E1	1.65	1.70	1.75
J		2.50 REF	
L	0.400	0.450	0.500
b	0.180	0.230	0.280
e		0.500 BSC	

11.3 Package Outline Description – QFN20 (QFR)



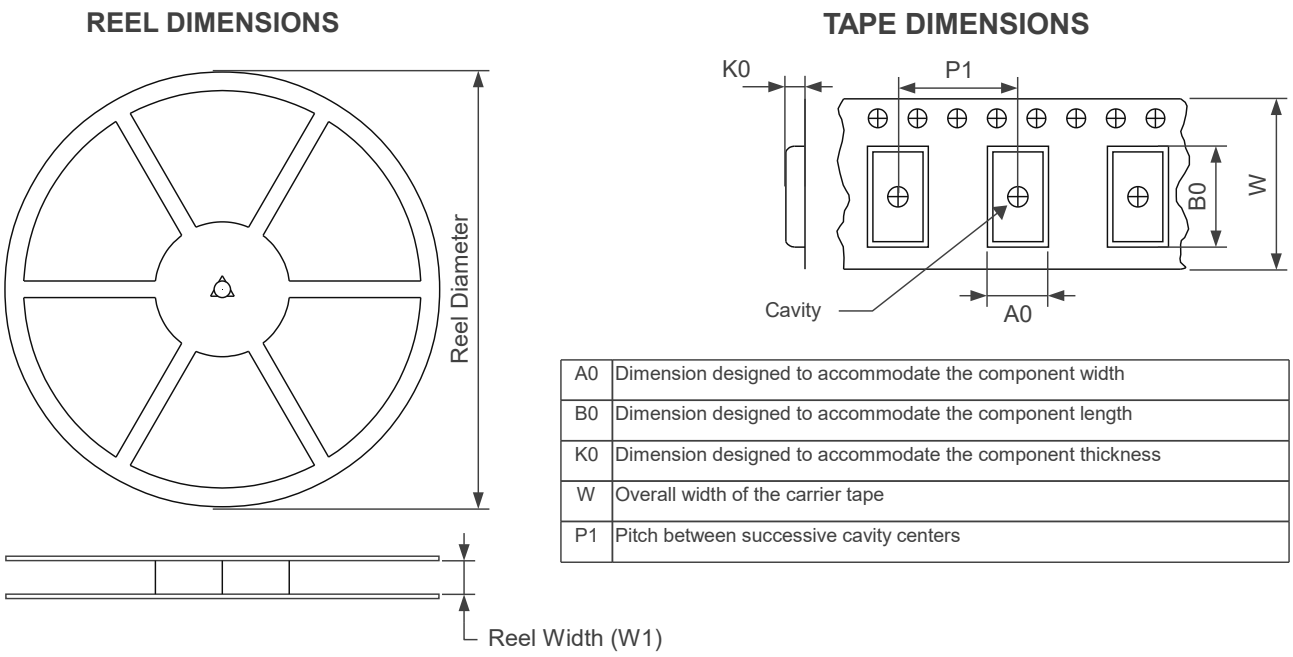
NOTES:
1. Drawing is not to scale.
2. Drawing is subject to change without notice.

Figure 11.3: QFR (3x3)-20 Package Outline Visual Description

Table 11.3: QFR (3x3)-20 Package Outline Dimensions [mm]

Dimension	Min	Nom	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D		3.00 BSC	
E		3.00 BSC	
D1	1.60	1.70	1.80
E1	1.60	1.70	1.80
e		0.40 BSC	
L	0.25	0.30	0.35

11.4 Tape and Reel Specifications



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Figure 11.4: Tape and Reel Specification

Table 11.4: Tape and reel Specifications

Package Type	Pins	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
WLCSP11	11	179	8.4	1.35	1.75	0.5	4	8	Q2
DFN12	12	330	12.4	3.3	3.3	1.1	8	12	Q1
QFN20	20	180	12.4	3.3	3.3	0.8	8	12	Q2

A Memory Map Descriptions

Table A.1: Version Information

Register: 0x00 - 0x09

Address	Category	Name	Value	
			Order Code 00x	Order Code A0x
0x00	Reserved	Product Number	1106	1462
0x01		Major Version	1	
0x02		Minor Version	3	4
0x03		Reserved		
0x04				
0x05 - 0x09		Reserved		

Table A.2: System Status

Register: 0x10

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CHANNEL_FLAGS								SYSTEM_FLAGS							
Current Power mode		CH2 Touch	CH2 Prox	CH1 Touch	CH1 Prox	CH0 Touch	CH0 Prox	Reset Event	ATI Error	ATI Active	ATI Event	Power Event	Slider Event	Touch Event	Prox Event

- Bit 15-14: **Current Power Mode**
  - 00: Normal Power
  - 01: Low Power
  - 10: Ultra Low Power
  - 11: Halt Mode
- Bit 13-8: **CHx Touch and Prox**

  For CHx Touch
  - 0: CHx not in Touch
  - 1: CHx in Touch

  For CHx Prox
  - 0: CHx not in Prox
  - 1: CHx in Prox
- Bit 7: **Reset Event**
  - 0: No Reset Event occurred
  - 1: Reset Event occurred
- Bit 6: **ATI Error**
  - 0: No ATI Error occurred
  - 1: ATI Error occurred
- Bit 5: **ATI Active**
  - 0: ATI not active
  - 1: ATI active
- Bit 4: **ATI Event**
  - 0: No ATI Event occurred
  - 1: ATI Event occurred
- Bit 3: **Power Event**
  - 0: No Power Event occurred
  - 1: Power Event occurred
- Bit 2: **Slider Event**
  - 0: No Slider Event occurred
  - 1: Slider Event occurred
- Bit 1: **Touch Event**
  - 0: No Touch Event occurred
  - 1: Touch Event occurred
- Bit 0: **Prox Event**
  - 0: No Prox Event occurred
  - 1: Prox Event occurred

Table A.3: Gesture Status

Register: 0x11

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RESERVED								**GESTURE_FLAGS**							
Reserved								Busy	Event	Hold	Flick Negative	Flick Positive	Swipe Negative	Swipe Positive	Tap

- Bit 7: **Busy**
  - 0: Gestures Idle
  - 1: Gestures Busy
- Bit 6: **Event**
  - 0: No Gesture Event occurred
  - 1: Gesture Event occurred
- Bit 5: **Hold**
  - 0: No Hold event detected
  - 1: Hold event detected
- Bit 4: **Flick Negative**
  - 0: No Flick Negative event detected
  - 1: Flick Negative event detected
- Bit 3: **Flick Positive**
  - 0: No Flick Positive event detected
  - 1: Flick Positive event detected
- Bit 2: **Swipe Negative**
  - 0: No Swipe Negative event detected
  - 1: Swipe Negative event detected
- Bit 1: **Swipe Positive**
  - 0: No Swipe Positive event detected
  - 1: Swipe Positive event detected
- Bit 0: **Tap**
  - 0: No Tap Event detected
  - 1: Tap Event detected

Table A.4: Movement Status (For order codes with Movement UI)

Register: 0x23

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MOVEMENT_STATUS_1								**MOVEMENT_STATUS_0**							
Reserved													Channel 2 Movement	Channel 1 Movement	Channel 0 Movement

- Bit 2-0: **Channel x Movement Status**
  - 0: No Movement detected on channel x
  - 1: Movement detected on channel x

Table A.5: Sensor Setup

Register: 0x30, 0x40, 0x50

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TX_SELECT								**SENSOR_SETUP**							
Reserved	CalCap Rx	CalCap Tx	Reserved	TxA	CTx2	CTx1	CTx0	Reserved	Release/ Movement UI Enable	FOSC Tx Frequency	Vbias	Invert	Dual Direction	Linearise Counts	Enable Channel

- Bit 14: **CalCap Rx**
  - 0: CalCap Rx not selected
  - 1: CalCap Rx selected
- Bit 13: **CalCap Tx**
  - 0: CalCap Tx not selected
  - 1: CalCap Tx selected
- Bit 11: **TxA**
  - 0: TxA disabled
  - 1: TxA enabled

- Bit 10-8: **CTxx**
  - 0: CTxx disabled
  - 1: CTxx enabled
- Bit 6: **Release/Movement UI Enable**
  - 0: Release/Movement UI disabled
  - 1: Release/Movement UI enabled
- Bit 5: **FOSC Tx Frequency**
  - 0: Tx frequency is set by CONV_FREQ_PERIOD and CONV_FREQ_FRAC (Table A.6)
  - 1: Tx frequency is 14MHz
- Bit 4: **Vbias**
  - 0: Vbias disabled
  - 1: Vbias voltage output on Cx2 (used for some inductive measurement circuits)
- Bit 3: **Invert**
  - 0: Do not invert channel logic
  - 1: Invert channel logic
- Bit 2: **Dual Direction**
  - 0: Single direction thresholds
  - 1: Dual direction thresholds
- Bit 1: **Linearise Counts**
  - 0: Do not Linearise counts
  - 1: Linearise counts
- Bit 0: **Enable Channel**
  - 0: Channel disabled
  - 1: Channel enabled

Table A.6: Conversion Frequency Setup

Register:	0x31, 0x41, 0x51															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CONV_FREQ_PERIOD								**CONV_FREQ_FRAC**							
Conversion Frequency Period								Conversion Frequency Fraction							

- Bit 15-8: **Conversion Frequency Period**
  - The charge transfer frequency f_{xfer} is determined by the values of the Conversion Frequency Fraction and the Conversion Frequency Period. The required value of the Conversion Frequency Period is dependent on the dead time enabled bit (See Table A.9).
  - Dead time disabled $f_{\text{xfer}} = \frac{fosc}{2 \times period + 2}$
  - Dead time enabled $f_{\text{xfer}} = \frac{fosc}{2 \times period + 3}$
  - Range: 0 - 127
- Bit 7-0: **Conversion Frequency Fraction**
  - Set to 127
- With a fixed conversion frequency fraction of 127 and dead time enabled, the following values of the conversion frequency period are recommended and will result in the indicated conversion frequency:
  - 1: 2MHz
  - 5: 1MHz[i]
  - 12: 500kHz
  - 17: 350kHz
  - 26: 250kHz
  - 53: 125kHz

[i] The maximum charge transfer frequency for mutual-capacitance mode (refer to Table A.7) is 1MHz

Table A.7: Prox Control (IQS3dd)

Register: 0x32, 0x42, 0x52

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PROX_CTRL_1								PROX_CTRL_0							
Reserved	0v5 Discharge	Reserved	Cs Size	Reserved	Reserved	S/H Bias Select		Max Counts		PXS Mode					

- Bit 15: **Reserved**
  - Set to 0
- Bit 14: **0v5 Discharge**
  - 0: Disabled
  - 1: Enabled
- Bit 13: **Reserved**
  - Set to 0
- Bit 12: **Cs Size** [ii]
  - 0: Use 40pF reference capacitor (Cs)
  - 1: Use 80pF reference capacitor (Cs)
- Bit 11: **Reserved**
  - Set to 0
- Bit 10: **Reserved**
  - Set to 0
- Bit 9-8: **S/H Bias Select**
  - 00: $2\mu A$
  - 01: $5\mu A$
  - 10: $7\mu A$
  - 11: $10\mu A$
- Bit 7-6: **Max Counts**
  - 00: 1023
  - 01: 2047
  - 10: 4095
  - 11: 16383
- Bit 5-0: **PXS Mode**
  - 0x10: Self-Capacitance
  - 0x13: Mutual-Capacitance
  - 0x1D: Current Measurement
  - 0x3D: Inductive[iii]

Table A.8: Prox Control (IQS3ed)

Register: 0x32, 0x42, 0x52

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PROX_CTRL_1								PROX_CTRL_0							
Reserved	0v5 Discharge	Reserved	Cs Size		Reserved	S/H Bias Select		Max Counts		PXS Mode					

- Bit 15: **Reserved**
  - Set to 0
- Bit 14: **0v5 Discharge**
  - 0: Disabled
  - 1: Enabled
- Bit 13: **Reserved**
  - Set to 0
- Bit 12-11: **Cs Size** [ii]
  - 01: Use 40pF reference capacitor (Cs)
  - 11: Use 80pF reference capacitor (Cs)
- Bit 10: **Reserved**
  - Set to 0

[ii] On IQS3ed hardware bit 11 is read only and always set. Bit 12 enables 80pF Cs on both hardware revisions. Header files generated using the product GUI with IQS3ed should not be used with IQS3dd. Doing this could cause reserved bit 11 in Table A.7 to be set, which will prevent the sensing engine from operating normally.

[iii] If CRx2/CTx2/Bias is used as an Rx for an inductive measurement the PXS Mode should be set to *Current Measurement*

- Bit 9-8: **S/H Bias Select**
  - 00: $2\mu A$
  - 01: $5\mu A$
  - 10: $7\mu A$
  - 11: $10\mu A$
- Bit 7-6: **Max Counts**
  - 00: 1023
  - 01: 2047
  - 10: 4095
  - 11: 16383
- Bit 5-0: **PXS Mode**
  - 0x10: Self-Capacitance
  - 0x13: Mutual-Capacitance
  - 0x1D: Current Measurement
  - 0x3D: Inductive[iii]

Table A.9: Prox Input and Control

Register:		0x33, 0x43, 0x53													
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RX_SELECT								TG_CTRL							
Reserved	Reserved	Internal Reference	Prox Engine Bias Current	Calibration Cap Select	CRx2	CRx1	CRx0	Reserved	Dead Time Enable	Reserved	Reserved	Auto Prox Cycle Select		Reserved	

- Bit 15: **Reserved**
  - Set to 0
- Bit 14: **Reserved**
  - Set to 0
- Bit 13: **Internal Reference**
  - 0: Internal Reference disabled
  - 1: Internal Reference enabled
- Bit 12: **Prox Engine Bias Current**
  - 0: Prox Engine Bias Current disabled
  - 1: Prox Engine Bias Current enabled
- Bit 11: **Calibration Capacitor Select**
  - 0: Calibration Capacitor enabled
  - 1: Calibration Capacitor disabled
- Bit 10-8: **CRxx**
  - 0: CRxx Disabled
  - 1: CRxx Enabled
- Bit 7: **Reserved**
  - Set to 1
- Bit 6: **Dead Time Enable**
  - 0: Dead Time Disabled
  - 1: Dead Time Enabled
- Bit 4: **Reserved**
  - Set to 0
- Bit 3-2: **Auto Prox Cycle Select**
  - Number of conversions before each interrupt is generated in Auto Mode
  - 00: 4
  - 01: 8
  - 10: 16
  - 11: 32
- Bit 1-0: **Reserved**
  - Set to 11

Table A.10: Pattern Definitions

Register:	0x34, 0x44, 0x54															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PATTERN_SETUP								**CALCAP_INACTIVE_RX**							
Wav Pattern 1				Wav Pattern 0				Calibration Capacitor				Inactive Rxs			

- Bit 15-12: **Wav Pattern 1**
  - See Section 5.12
- Bit 11-8: **Wav Pattern 0**
  - See Section 5.12
- Bit 7-4: **Calibration Capacitor**
  - Calibration Capacitor size = 0.5pF x Calibration Capacitor
  - Max value = 7 (Calibration Capacitor size = 3.5pF)
- Bit 3-0: **Inactive Rxs**
  - Selects state of Cx's when not in use
  - 0x00: Floating
  - 0x05: Bias voltage
  - 0x0A: VSS
  - 0x0F: VREG

Table A.11: Pattern Selection and Engine Bias Current

Register:	0x35, 0x45, 0x55															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BIAS_CURRENT								**PATTERN_SELECT**							
Engine Bias Current				Engine Bias Current Trim				Wav Pattern Select							

- Bit 15-12: **Engine Bias Current**
  - Signed value (MSB is sign bit)
  - Bias Current = Engine Bias Current x $3\mu A$ + Engine Bias Current Trim x $200nA$
- Bit 11-8: **Engine Bias Current Trim**
  - 4 bit Engine Bias Current Trim Value
- Bit 7-0: **Wav Pattern Select**
  - Select which pattern is displayed on which Cx
  - See Section 5.12

Table A.12: ATI Setup

Register:	0x36, 0x46, 0x56														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ATI_SETUP_1								**ATI_SETUP_0**							
ATI Resolution Factor												ATI Band	ATI Mode		

- Bit 15-4: **ATI Resolution Factor**
  - ATI TARGET = ACTUAL ATI BASE x $\frac{\text{ATI Resolution Factor}}{16}$
- Bit 3: **ATI Band**
  - 0: Small ATI Band = ($\frac{1}{16}$ x ATI TARGET)
  - 1: Large ATI Band = ($\frac{1}{8}$ x ATI TARGET)
- Bit 2-0: **ATI Mode**
  - 000: Disabled
  - 001: Compensation Only
  - 010: ATI from Compensation Divider
  - 011: ATI from Fine Fractional Divider
  - 100: Full

Table A.13: ATI Multipliers and Dividers

Register:	0x38, 0x48, 0x58														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ATI_FINE								**ATI_COARSE**							
Fine Fractional Multiplier		Fine Fractional Divider						Coarse Fractional Multiplier				Coarse Fractional Divider			

Table A.14: Compensation

Register:	0x39, 0x49, 0x59														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ATI_COMPENSATION_1								**ATI_COMPENSATION_0**							
Compensation Divider					Res-erved	Compensation Value									

Table A.15: Channel Setup

Register:	0x60, 0x70, 0x80														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FOLLOWER_MASK								**REF_UI_SETUP**							
Follower Event Mask								Reference Sensor ID				Channel Mode			

- Bit 15-8: **Follower Event Mask**
  - Masks the events in the upper byte of System Status
- Bit 7-4: **Reference Sensor ID**
  - Select Reference Sensor
- Bit 3-0: **Channel Mode**
  - 00: Independent
  - 01: Follower
  - 10: Reference

Table A.16: Prox Settings

Register:	0x61, 0x71, 0x81														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PROX_DEBOUNCE								**PROX_THRESHOLD**							
Prox Debounce Exit				Prox Debounce Enter				Prox Threshold							

- Bit 15-12: **Prox Debounce Exit**
  - 0000: Prox Debounce Exit disabled
  - Number of debounce conversions on Prox Exit (4-bit value)
- Bit 11-8: **Prox Debounce Enter**
  - 0000: Prox Debounce Enter disabled
  - Number of debounce conversions on Prox Enter (4-bit value)
- Bit 7-0: **Prox Threshold**
  - 8 bit value

Table A.17: Touch Settings

Register:	0x62, 0x72, 0x82														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TOUCH_HYSTERESIS								**TOUCH_THRESHOLD**							
Touch Hysteresis								Touch Threshold							

- Bit 15-12: **Touch Hysteresis**
  - $Touch\ Hysteresis = \frac{Touch\ Hysteresis}{256}$ x $Touch\ Threshold$
- Bit 7-0: **Touch Threshold**
  - $Touch\ Threshold = \frac{Threshold \times LTA}{256}$

Table A.18: Follower Weight

Register:	0x63, 0x73, 0x83														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FOLLOWER_WEIGHT_1								**FOLLOWER_WEIGHT_0**							
Follower Weight															

- Bit 15-0: **Follower Weight**
  - $Follower\ Weight = \frac{Weight}{4096}$

Table A.19: Movement UI Settings (For order codes with Movement UI)

Register:	0x64, 0x74, 0x84														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MOVEMENT_DEBOUNCE								**MOVEMENT_THRESHOLD**							
Movement Debounce Exit				Movement Debounce Enter				Movement Threshold							

- Bit 15-12: **Movement Debounce Exit**
  - 0000: Movement Debounce Exit disabled
  - Number of debounce conversions on Movement Exit (4-bit value)
- Bit 11-8: **Movement Debounce Enter**
  - 0000: Movement Debounce Enter disabled
  - Number of debounce conversions on Movement Enter (4-bit value)
- Bit 7-0: **Movement Threshold**
  - 8 bit value

Table A.20: Slider Setup and Calibration

Register:	0x90														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LOWER_CALIBRATION								**SLIDER_SETUP**							
Lower Calibration Value								Res-erved	Static Filter	Slow/Static Beta			Total Channels		

- Bit 15-8: **Lower Calibration Value**
  - 8-bit value
- Bit 6: **Static Filter**
  - 0: Slider output is dynamically filtered
  - 1: Slider output is filtered using the Slow/Static Beta
- Bit 5-3: **Slow/Static Beta**
  - 3-bit value
- Bit 2-0: **Total Channels**
  - Number of channels to use for slider

Table A.21: Slider Calibration and Bottom Speed

Register:	0x91														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BOTTOM_SPEED								**UPPER_CALIBRATION**							
Bottom Speed								Upper Calibration Value							

- Bit 15-8: **Bottom Speed**
  - 8-bit value
- Bit 7-0: **Upper Calibration Value**
  - 8-bit value

Table A.22: Enable Mask

Register:	0x94														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ENABLE_MASK_1								**ENABLE_MASK_0**							
Reserved													Enable Mask		

- Bit 2: **Channel 2 Enable**
  - 0: Channel 2 disabled for slider
  - 1: Channel 2 enabled for slider
- Bit 1: **Channel 1 Enable**
  - 0: Channel 1 disabled for slider
  - 1: Channel 1 enabled for slider
- Bit 0: **Channel 0 Enable**
  - 0: Channel 0 disabled for slider
  - 1: Channel 0 enabled for slider

Table A.23: Enable Status Pointer

Register:	0x95														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ENABLE_STATUS_POINTER_1								**ENABLE_STATUS_POINTER_0**							
Enable Status Pointer															

- Bit 15-0: **Enable Status Pointer**
  - Enables slider when any channel is in touch

  For order codes with Release UI
  - 0x552: Slider active in touch

  For order codes with Movement UI
  - 0x558: Slider active in touch

Table A.24: Delta Links

Register:	0x96, 0x97, 0x98														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DELTA_LINKX_1								**DELTA_LINKX_0**							
Delta Link X															

- Bit 15-0: **Delta Link X** - Select element order per channel
  - Delta Link number corresponds with slider element order

  For order codes with Release UI
  - 0x000: Disabled
  - 0x430: Channel 0 enabled for element
  - 0x472: Channel 1 enabled for element
  - 0x4B4: Channel 2 enabled for element

  For order codes with Movement UI
  - 0x000: Disabled
  - 0x430: Channel 0 enabled for element
  - 0x474: Channel 1 enabled for element
  - 0x4B8: Channel 2 enabled for element

Table A.25: Gesture Enable

Register:	0xA0														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RESERVED								**GESTURE_ENABLE**							
Reserved								Reserved				Hold Enable	Flick Enable	Swipe Enable	Tap Enable

- Bit 3: **Hold Enable**
  - 0: Hold disabled
  - 1: Hold enabled
- Bit 2: **Flick Enable**
  - 0: Flick disabled
  - 1: Flick enabled
- Bit 1: **Swipe Enable**
  - 0: Swipe disabled
  - 1: Swipe enabled
- Bit 0: **Tap Enable**
  - 0: Tap disabled
  - 1: Tap enabled

Table A.26: Counts Filter Betas

Register:	0xB0														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LP_COUNTS_FILTER								**NP_COUNTS_FILTER**							
Low Power Counts Beta								Normal Power Counts Beta							

Table A.27: LTA Filter Betas

Register:	0xB1														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LP_LTA_FILTER								**NP_LTA_FILTER**							
Low Power LTA Beta								Normal Power LTA Beta							

Table A.28: LTA Fast Filter Betas

Register:	0xB2														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LP_LTA_FAST_FILTER								**NP_LTA_FAST_FILTER**							
Low Power LTA Fast Beta								Normal Power LTA Fast Beta							

Table A.29: Activation/Movement LTA Filter Betas

Register: 0xB3

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LP_ACTIVATION_LTA_FILTER/LP_MOVEMENT_LTA_FILTER								**NP_ACTIVATION_LTA_FILTER/NP_MOVEMENT_LTA_FILTER**							
Low Power Activation/Movement LTA Beta								Normal Power Activation/Movement LTA Beta							

Table A.30: System Control

Register: 0xC0

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH_TIMEOUT_DISABLE								**SYSTEM_CONTROL**							
Reserved					CH2 Time-out Dis-able	CH1 Time-out Dis-able	CH0 Time-out Dis-able	Inter-face Type	Power Mode			Reseed	Re-ATI	Soft Reset	ACK Reset

- Bit 10-8: **CHx Timeout Disable**
  - 0: Global prox and touch timeouts enabled for channel
  - 1: Global prox and touch timeouts disabled for channel
- Bit 7: **Interface Selection**
  - 0: I^2C Streaming
  - 1: I^2C Events
- Bit 6-4: **Power Mode**
  - 000: Normal Power Mode
  - 001: Low Power Mode
  - 010: Ultra Low Power Mode
  - 011: Halt Mode
  - 100: Automatic
  - 101: Automatic No ULP
- Bit 3: **Reseed**
  - 0: No Reseed
  - 1: Trigger Reseed
- Bit 2: **Re-ATI**
  - 0: No Re-ATI
  - 1: Trigger Re-ATI
- Bit 1: **Soft Reset**
  - 0: No Soft Reset
  - 1: Trigger Soft Reset
- Bit 0: **ACK Reset**
  - 0: No ACK Reset
  - 1: ACK Reset

Table A.31: Event Timeouts

Register: 0xD2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TOUCH_EVENT_TIMEOUT								**PROX_EVENT_TIMEOUT**							
Touch Event Timeout								Prox Event Timeout							

- Bit 15-8: **Touch Event Timeout**
  - *Touch Event Timeout* = Touch Event Timeout x 512ms
- Bit 7-0: **Prox Event Timeout**
  - *Prox Event Timeout* = Prox Event Timeout x 512ms

Table A.32: Events Enable and Activation Settling Threshold (For order codes with Release UI)

Register: 0xD3

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ACTIVATION_THRESHOLD								**EVENTS_ENABLE**							
Activation Settling Threshold								Res-erved	ATI Error	Res-erved	ATI Event	Power Event	Slider Event	Touch Event	Prox Event

Table A.33: Events Enable (For order codes with Movement UI)

Register: 0xD3

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RESERVED								**EVENTS_ENABLE**							
Reserved									ATI Error	Res-erved	ATI Event	Power Event	Slider Event	Touch Event	Prox Event

- Bit 15-8: **Reserved**
- Bit 6: **ATI Error**
  - 0: ATI Error disabled
  - 1: ATI Error enabled
- Bit 4: **ATI Event**
  - 0: ATI Event disabled
  - 1: ATI Event enabled
- Bit 3: **Power Event**
  - 0: Power Event disabled
  - 1: Power Event enabled
- Bit 2: **Slider Event**
  - 0: Slider Event disabled
  - 1: Slider Event enabled
- Bit 1: **Touch Event**
  - 0: Touch Event disabled
  - 1: Touch Event enabled
- Bit 0: **Prox Event**
  - 0: Prox Event disabled
  - 1: Prox Event enabled

Table A.34: Release UI Settings (For order codes with Release UI)

Register: 0xD4

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DELTA_SNAP_SAMPLE_DELAY								**RELEASE_DELTA_PERCENTAGE**							
Delta Snapshot Sample Delay								Release Delta Percentage							

- Bit 15-8: **Delta Snapshot Sample Delay**
  - 8-bit value
- Bit 7-0: **Release Delta Percentage**
  - ***Release Delta Percentage*** = $\frac{\text{Release Delta Percentage}}{128}$

Table A.35: Movement Timeout (For order codes with Movement UI)

Register: 0xD4

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MOVEMENT_TIMEOUT_1								**MOVEMENT_TIMEOUT_0**							
Movement Timeout															

- Bit 15-0: **Movement Timeout**
  - *Movement Timeout* = Movement Timeout x 512ms

Table A.36: I2C Settings

Register:	0xE0														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RESERVED								**I2C_SETUP**							
Reserved														R/W Check Dis-able	Stop Bit Dis-able

- Bit 1: **Read/Write Check Disable**
  - 0: Read/Write Check enable
  - 1: Read/Write Check disabled
- Bit 0: **Stop Bit Disable**
  - 0: Stop Bit enabled
  - 1: Stop Bit disabled

Table A.37: Hardware ID

Register:	0xE1														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
HW_ID_1								**HW_ID_0**							
Hardware ID															

- Bit 15-0: **Hardware ID** [iv]
  - 0xF003: IQS3dd
  - 0xF004: IQS3ed

[iv] Take note of Cs Size selection in Table A.7 and Table A.8

B Revision History

Release	Date	Changes
v1.1	August 2022	First public release
v1.2	November 2022	Add slider reference schematic Improve *Cs Size* selection description Update package outlines Add tape and reel specifications
v1.3	October 2023	Update Reset Levels table Change MCLR capacitor recommendation from 0.1uF to 1nF Update reference schematics Improve hyperlinks to memory map Remove Miscellaneous Timings section Fix incorrect WLCSP11 package dimension (A2) Improve clarity in all sections Re-word Movement UI section Add revision history Add descriptions for some ProxFusion® Module settings Add description of gestures Add detailed description of ATI
v1.4	November 2023	Add description for the *Dual Direction* setting Improve Sensor Setup section Correct *FOSC Tx Frequency* description
v1.5	March 2024	Update Release UI section Add I^2C Settings Register and I^2C Lock Up to Known Issues Improve Watchdog Timer section Fix Swipe Enable description Fix pin 1 marking for DFN12 Top Marking Add reserved bits to Enable Mask register description
v1.6	May 2024	Add QFN20 package information Add IQS323-002 order code information Remove Pin Attributes table Remove pin numbers from Signal Descriptions table Add QFN20 schematic
v1.7	May 2024	Add capacitor derating information to Electrical Specifications

C Known Issues

I²C Settings Register
Versions Affected:
IQS323-00x v1.3 and below.

Issue Description:
Once set, the bits in the *I2C Settings* register cannot be cleared.

Recommended Workaround:
Reset the device by following the guidelines in Section 6.6. This will clear the bits in the I²C register, but will require the master to re-write all application settings. Note that with the *Stop Bit Disable* bit set, the master is still able to close a communications window using the terminate communications command as described in Section 8.9.

I²C Lock Up
Versions Affected:
IQS323-00x v1.3 and below.
IQS323-A0x v1.4 and below.

Issue Description:
In certain cases the IQS323 can enter a state in which all bytes read over I²C return a constant value. There is a higher likelihood of this occuring when using the force communications method described in Section 8.13.

Recommended Workaround
At the end of every I²C communication, read one byte from a register that does not exist. If the returned value is not 0xEE, hard reset the IQS323 by following the guidelines in Section 6.6.

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