

N-Channel Enhancement Mode Power MOSFET

<p>Description</p> <p>The GT095N10D5 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.</p> <p>General Features</p> <ul style="list-style-type: none"> ● V_{DS} 100V ● I_D (at $V_{GS} = 10V$) 55A ● $R_{DS(ON)}$ (at $V_{GS} = 10V$) < 11mΩ ● $R_{DS(ON)}$ (at $V_{GS} = 4.5V$) < 15mΩ ● 100% Avalanche Tested ● RoHS Compliant <p>Application</p> <ul style="list-style-type: none"> ● Power switch ● DC/DC converters 	<p>Schematic diagram</p> <p>pin assignment</p> <p>DFN5X6-8L</p>
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Ordering Information			
Device	Package	Marking	Packaging
GT095N10D5	DFN5*6-8L	GT095N10	5000pcs/Reel

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, unless otherwise noted			
Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	100	V
Continuous Drain Current	I_D	55	A
Pulsed Drain Current (note1)	I_{DM}	220	A
Gate-Source Voltage	V_{GS}	± 20	V
Power Dissipation	P_D	74	W
Single pulse avalanche energy (note2)	E_{AS}	73	mJ
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	°C

Thermal Resistance			
Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	55	°C/W
Maximum Junction-to-Case	R_{thJC}	1.7	°C/W

Specifications $T_J = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	100	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = 100\text{V}, V_{\text{GS}} = 0\text{V}$	--	--	1	μA
Gate-Source Leakage	I_{GSS}	$V_{\text{GS}} = \pm 20\text{V}$	--	--	± 100	nA
Gate-Source Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = 250\mu\text{A}$	1	1.8	2.5	V
Drain-Source On-Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10\text{V}, I_D = 35\text{A}$	--	9.5	11	$\text{m}\Omega$
		$V_{\text{GS}} = 4.5\text{V}, I_D = 35\text{A}$	--	13	15	
Forward Transconductance	g_{FS}	$V_{\text{GS}} = 5\text{V}, I_D = 35\text{A}$	--	39	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 50\text{V}, f = 1.0\text{MHz}$	--	1683	--	pF
Output Capacitance	C_{oss}		--	612	--	
Reverse Transfer Capacitance	C_{rss}		--	7	--	
Total Gate Charge	Q_g	$V_{\text{DD}} = 50\text{V}, I_D = 35\text{A}, V_{\text{GS}} = 10\text{V}$	--	54	--	nC
Gate-Source Charge	Q_{gs}		--	10	--	
Gate-Drain Charge	Q_{gd}		--	14	--	
Turn-on Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = 50\text{V}, I_D = 35\text{A}, R_G = 1.6\Omega$	--	13	--	ns
Turn-on Rise Time	t_r		--	10	--	
Turn-off Delay Time	$t_{\text{d}(\text{off})}$		--	30	--	
Turn-off Fall Time	t_f		--	8	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	$T_C = 25^\circ\text{C}$	--	--	55	A
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}, I_{\text{SD}} = 35\text{A}, V_{\text{GS}} = 0\text{V}$	--	--	1.2	V
Reverse Recovery Charge	Q_{rr}	$I_F = \text{A}, V_{\text{GS}} = 0\text{V}$ $dI/dt = 500\text{A}/\mu\text{s}$	--	95	--	nC
Reverse Recovery Time	T_{rr}		--	45	--	ns

Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. EAS condition : $T_J=25^\circ\text{C}$, $V_{\text{DD}}=50\text{V}$, $V_{\text{GS}}=10\text{V}$, $L=0.5\text{mH}$, $R_G=25\Omega$
3. Identical low side and high side switch with identical R_G

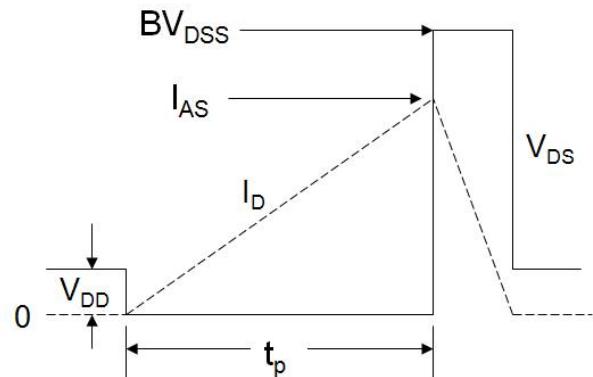
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

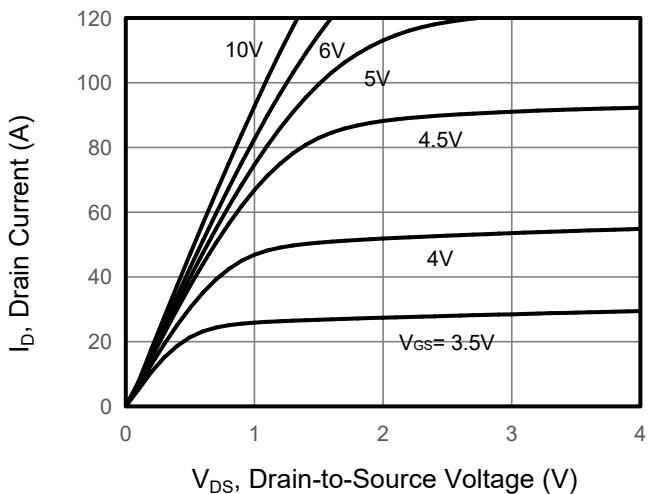


Figure 2. Transfer Characteristics

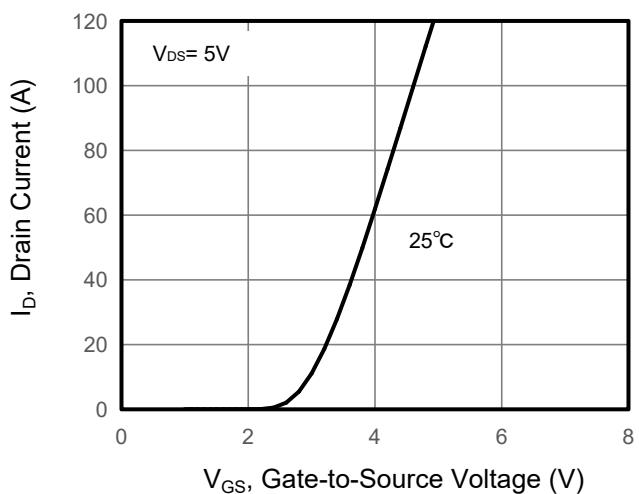


Figure 3. Drain Source On Resistance

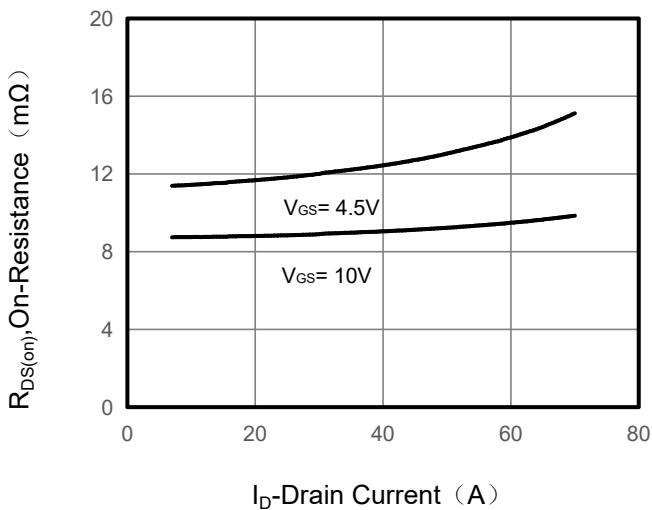


Figure 4. Gate Charge

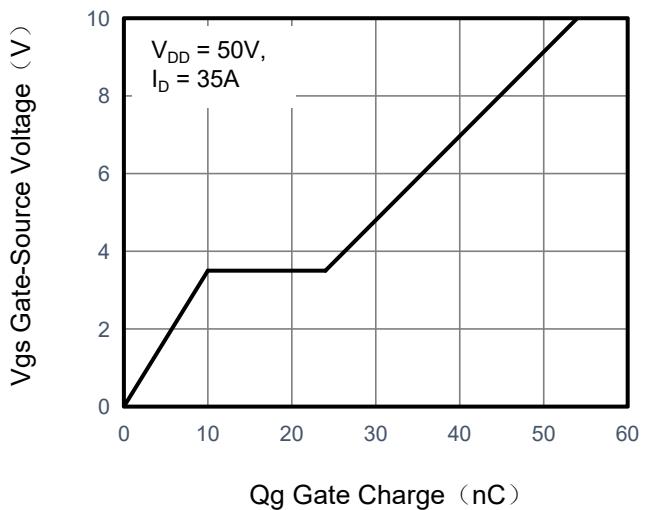


Figure 5. Capacitance

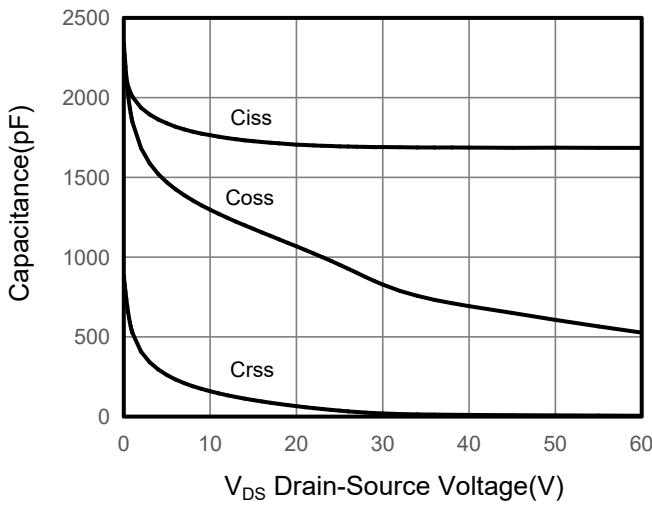
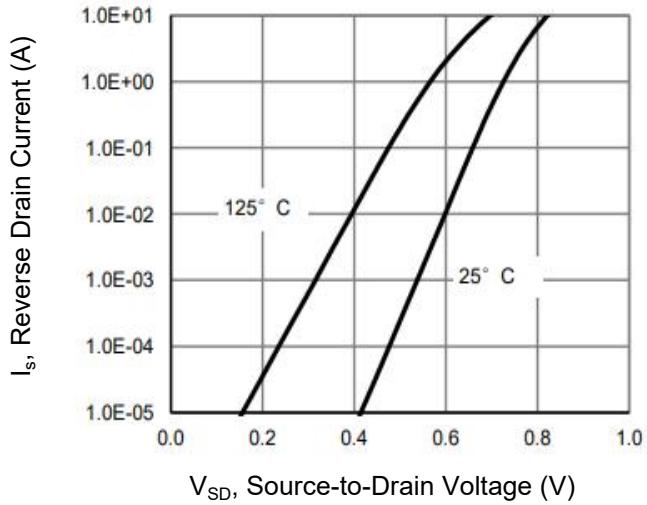


Figure 6. Source-Drain Diode Forward



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. Drain-Source On-Resistance

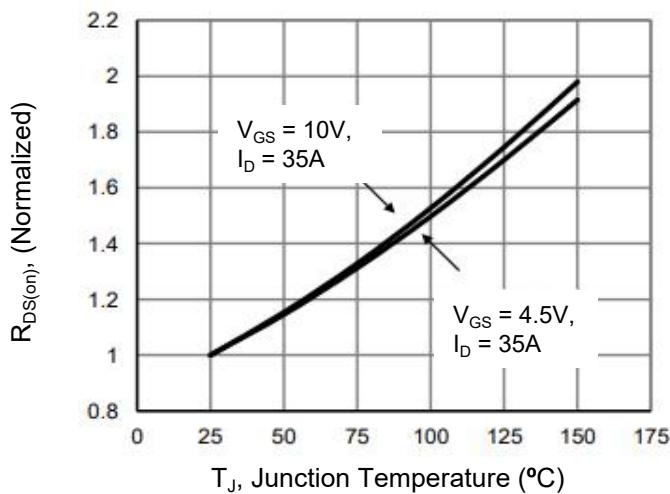


Figure 8. Safe Operation Area

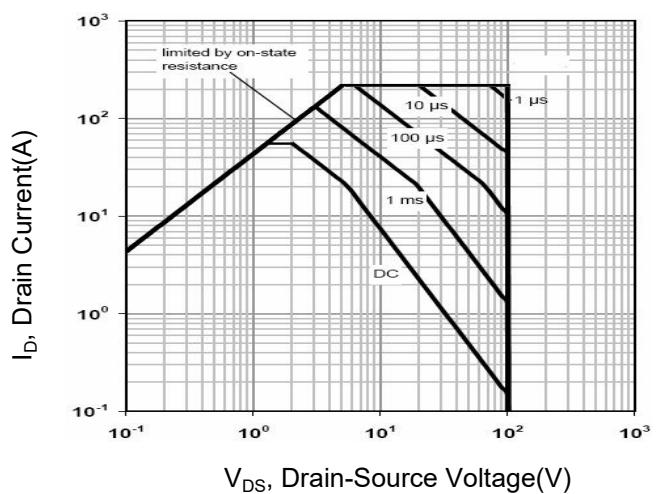
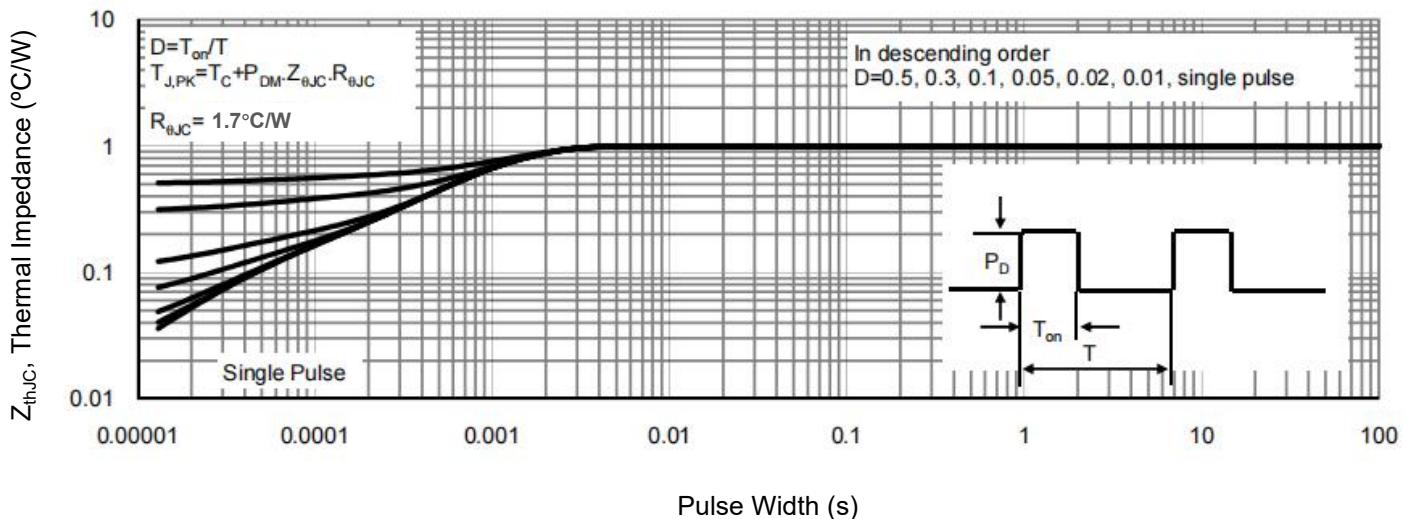
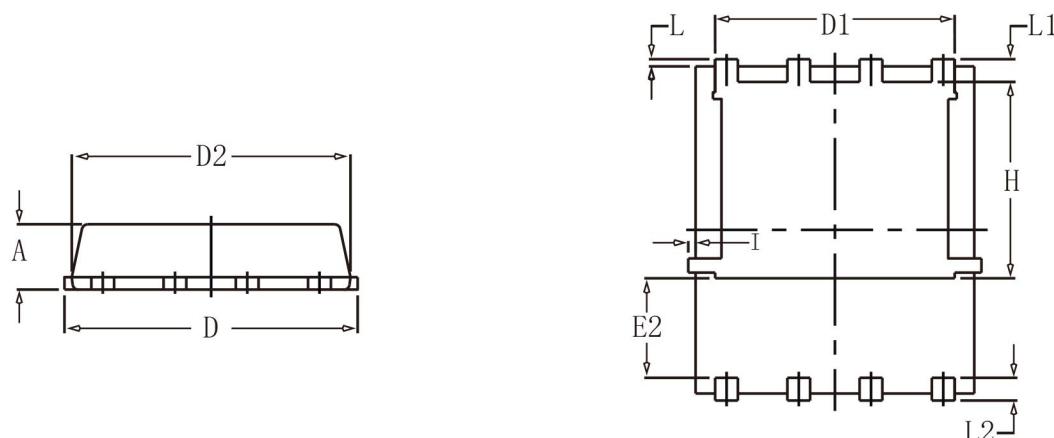
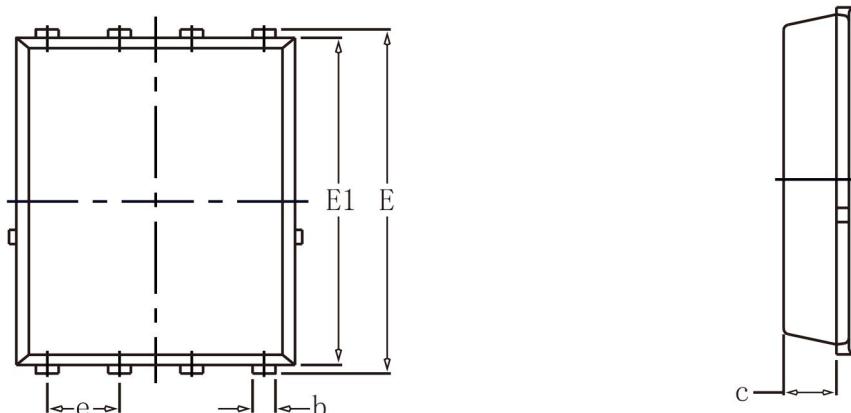


Figure 9. Normalized Maximum Transient Thermal Impedance



DFN5*6-8L Package Information



SYMBOL	COMMON			
	MM		INCH	
	MIN	MAX	MIN	MAX
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.970	0.0324	0.0382
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.59	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	-	0.0630	-
e	1.27	BSC	0.05	BSC
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	-	0.18	-	0.0070