LP3873/LP3876 3A Fast Ultra Low Dropout Linear Regulators

Check for Samples: LP3873, LP3876

FEATURES

- **Ultra Low Dropout Voltage**
- **Low Ground Pin Current**
- **Load Regulation of 0.08%**
- **1µA Quiescent Current in Shutdown Mode**
- **Ensured Output Current of 3A DC**
- **Available in DDPAK/TO-263 and TO-220 Packages**
- **Output Voltage Accuracy ± 1.5%**
- **$\overline{\text{Error}}$ Flag Indicates Output Status**
- **Sense Option Improves Load Regulation**
- **Minimum Output Capacitor Requirements**
- **Overtemperature/overcurrent Protection**
- **−40°C to +125°C Junction Temperature Range**

APPLICATIONS

- **Microprocessor Power Supplies**
- **GTL, GTL+, BTL, and SSTL Bus Terminators**
- **Power Supplies for DSPs**
- **SCSI Terminator**
- **Post Regulators**
- **High Efficiency Linear Regulators**
- **Battery Chargers**
- **Other Battery Powered Applications**

DESCRIPTION

The LP3873/LP3876 series of fast ultra low-dropout linear regulators operate from a +2.5V to +7.0V input supply. Wide range of preset output voltage options are available. These ultra low dropout linear regulators respond very quickly to step changes in load, which makes them suitable for low voltage microprocessor applications. The LP3873/LP3876 are developed on a CMOS process which allows low quiescent current operation independent of output load current. This CMOS process also allows the LP3873/LP3876 to operate under extremely low dropout conditions.

Dropout Voltage: Ultra low dropout voltage; typically 80mV at 300mA load current and 800mV at 3A load current.

Ground Pin Current: Typically 6mA at 3A load current.

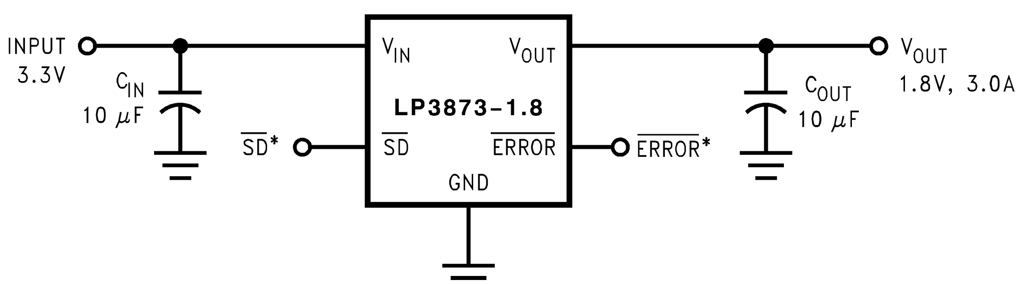
Shutdown Mode: Typically 1µA quiescent current when the shutdown pin is pulled low.

$\overline{\text{Error}}$ Flag: $\overline{\text{Error}}$ flag goes low when the output voltage drops 10% below nominal value.

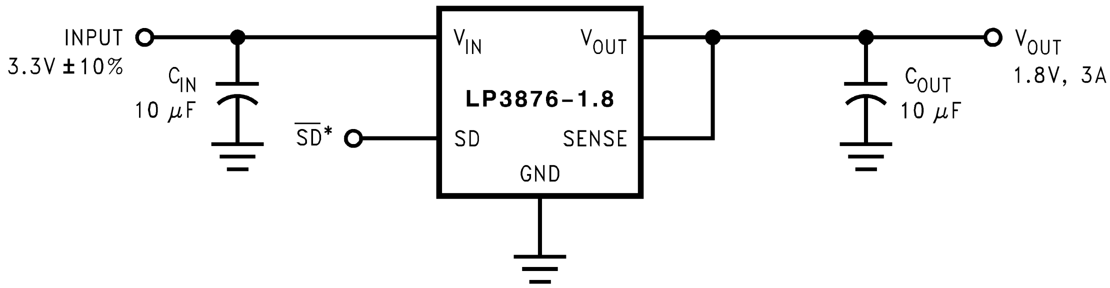
SENSE: Sense pin improves regulation at remote loads.

Precision Output Voltage: Multiple output voltage options are available ranging from 1.8V to 5.0V with an ensured accuracy of ±1.5% at room temperature, and ±3.0% over all conditions (varying line, load, and temperature).

Typical Application Circuits



*$\overline{\text{SD}}$ and $\overline{\text{ERROR}}$ pins must be pulled high through a 10kΩ pull-up resistor. Connect the $\overline{\text{ERROR}}$ pin to ground if this function is not used. See Application Hints for more information.



*SD pins must be pulled high through a 10kΩ pull-up resistor. See Application Hints for more information.

Connection Diagrams

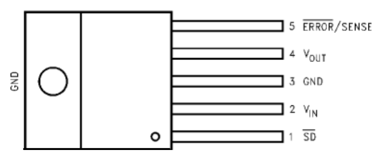


Figure 1. Top View
5-Pin TO-220
See NDH0005D Package

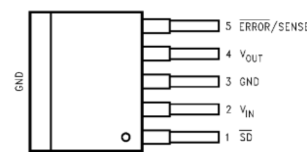
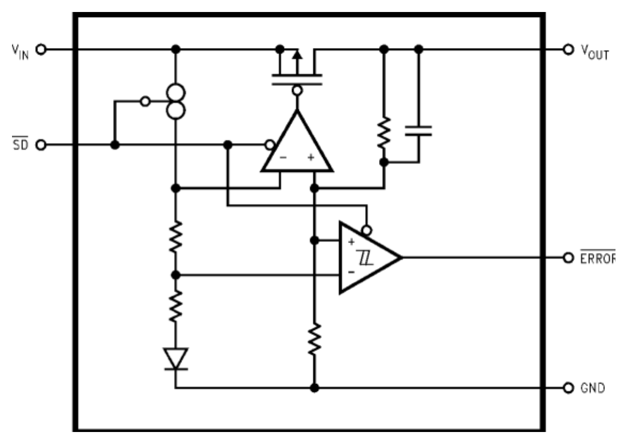


Figure 2. Top View
5-Pin DDPAK/TO-263
See KTT0005B Package

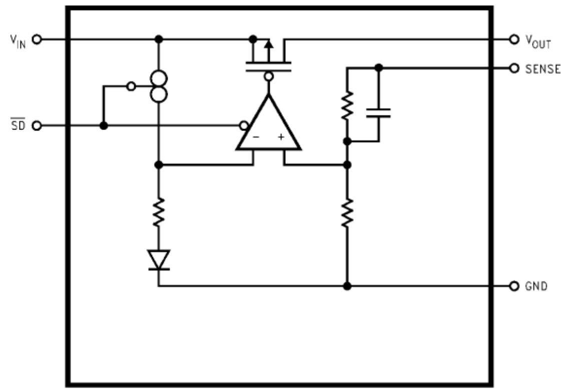
PIN DESCRIPTIONS FOR TO-220 AND DDPAK/TO-263 PACKAGES

Pin #	LP3873		LP3876	
	Name	Function	Name	Function
1	SD	Shutdown	SD	Shutdown
2	V_{IN}	Input Supply	V_{IN}	Input Supply
3	GND	Ground	GND	Ground
4	V_{OUT}	Output Voltage	V_{OUT}	Output Voltage
5	ERROR	ERROR Flag	SENSE	Remote Sense Pin

Block Diagram LP3873



Block Diagram LP3876



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Storage Temperature Range		−65°C to +150°C
Lead Temperature	Soldering, 5 sec.	260°C
ESD Rating(3)		2 kV
Power Dissipation(4)		Internally Limited
Input Supply Voltage (Survival)		−0.3V to +7.5V
Shutdown Input Voltage (Survival)		−0.3V to 7.5V
Output Voltage (Survival)(5)(6)		−0.3V to +6.0V
I_{OUT} (Survival)		Short Circuit Protected
Maximum Voltage for $\overline{\text{ERROR}}$ Pin		V_{IN}
Maximum Voltage for SENSE Pin		V_{OUT}

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and test conditions, see Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.
(4) At elevated temperatures, devices must be derated based on package thermal resistance. The devices in TO-220 package must be derated at θ_{jA} = 50°C/W (with 0.5in^2, 1oz. copper area), junction-to-ambient (with no heat sink). The devices in the TO263 surface-mount package must be derated at θ_{jA} = 60°C/W (with 0.5in^2, 1oz. copper area), junction-to-ambient. See Application Hints.
(5) If used in a dual-supply system where the regulator load is returned to a negative supply, the output must be diode-clamped to ground.
(6) The output PMOS structure contains a diode between the V_{IN} and V_{OUT} terminals. This diode is normally reverse biased. This diode will get forward biased if the voltage at the output terminal is forced to be higher than the voltage at the input terminal. This diode can typically withstand 200mA of DC current and 1Amp of peak current.

Operating Ratings

Input Supply Voltage(1)	2.5V to 7.0V
Shutdown Input Voltage	−0.3V to 7.0V
Maximum Operating Current (DC)	3A
Junction Temperature	−40°C to +125°C

(1) The minimum operating value for V_{IN} is equal to either [$V_{OUT(NOM)}$ + $V_{DROPOUT}$] or 2.5V, whichever is greater.

Electrical Characteristics LP3873/LP3876

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the **full operating temperature range**. Unless otherwise specified: $V_{IN} = V_{O(NOM)}$ + 1.5V, I_L = 10 mA, C_{OUT} = 10µF, V_{SD} = 2V.

Symbol	Parameter	Conditions	Typ (1)	LP3873/6 (2)		Units
				Min	Max	
V_O	Output Voltage Tolerance (3)	V_{OUT} +1.5V ≤ V_{IN} ≤ 7.0V 10 mA ≤ I_L ≤ 3A	0	-1.5 **-3.0**	+1.5 **+3.0**	%
ΔV_{OL}	Output Voltage Line Regulation (3)	V_{OUT} + 1.5V ≤ V_{IN} ≤ 7.0V	0.02 **0.06**			%
$\Delta V_O / \Delta I_{OUT}$	Output Voltage Load Regulation (3)	10 mA ≤ I_L ≤ 3A	0.08 **0.14**			%
$V_{IN} - V_{OUT}$	Dropout Voltage (4)	I_L = 300 mA	80		100 **120**	mV
		I_L = 3A	800		1000 **1200**	
I_{GND}	Ground Pin Current In Normal Operation Mode	I_L = 300 mA	5		9 **10**	mA
		I_L = 3A	6		14 **15**	
I_{GND}	Ground Pin Current In Shutdown Mode	V_{SD} ≤ 0.3V	1		10	µA
		-40°C ≤ T_J ≤ 85°C			**50**	
$I_{O(PK)}$	Peak Output Current	$V_O \geq V_{O(NOM)}$ - 4%	4.5			A
SHORT CIRCUIT PROTECTION						
I_{SC}	Short Circuit Current		6			A
SHUTDOWN INPUT						
V_{SDT}	Shutdown Threshold	Output = High	V_{IN}	**2**		V
		Output = Low	0		**0.3**	
T_{dOFF}	Turn-off delay	I_L = 3A	20			µs
T_{dON}	Turn-on delay	I_L = 3A	25			µs
I_{SD}	$\overline{SD}$ Input Current	$V_{SD} = V_{IN}$	1			nA
$\overline{\text{ERROR}}$ FLAG						
V_T	Threshold	See (5)	10	**5**	**16**	%
V_{TH}	Threshold Hysteresis	See (5)	5	**2**	**8**	%
$V_{EF(Sat)}$	$\overline{\text{Error}}$ Flag Saturation	I_{sink} = 100µA	0.02		**0.1**	V
Td	Flag Reset Delay		1			µs
I_{lk}	$\overline{\text{Error}}$ Flag Pin Leakage Current		1			nA
I_{max}	$\overline{\text{Error}}$ Flag Pin Sink Current	V_{Error} = **0.5V**	1			mA

(1) Typical numbers are at 25°C and represent the most likely parametric norm.
(2) Limits are specified by testing, design, or statistical correlation.
(3) Output voltage line regulation is defined as the change in output voltage from the nominal value due to change in the input line voltage. Output voltage load regulation is defined as the change in output voltage from the nominal value due to change in load current. The line and load regulation specification contains only the typical number. However, the limits for line and load regulation are included in the output voltage tolerance specification.
(4) Dropout voltage is defined as the minimum input to output differential voltage at which the output drops 2% below the nominal value. Dropout voltage specification applies only to output voltages of 2.5V and above. For output voltages below 2.5V, the drop-out voltage is nothing but the input to output differential, since the minimum input voltage is 2.5V.
(5) $\overline{\text{Error}}$ Flag threshold and hysteresis are specified as percentage of regulated output voltage. See Application Hints.

Electrical Characteristics LP3873/LP3876 (continued)

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the **full operating temperature range**. Unless otherwise specified: $V_{IN} = V_{O(NOM)}$ + 1.5V, I_L = 10 mA, C_{OUT} = 10µF, V_{SD} = 2V.

Symbol	Parameter	Conditions	Typ (1)	LP3873/6 (2)		Units
				Min	Max	
AC PARAMETERS						
PSRR	Ripple Rejection	$V_{IN} = V_{OUT}$ + 1.0V C_{OUT} = 10uF V_{OUT} = 3.3V	73			dB
		$V_{IN} = V_{OUT}$ + 0.5V C_{OUT} = 10uF V_{OUT} = 3.3V	57			
$\rho_{n(l/f}$	Output Noise Density	f = 120Hz	0.8			µV
e_n	Output Noise Voltage	BW = 10Hz – 100kHz V_{OUT} = 2.5V	150			µV (rms)
		BW = 300Hz – 300kHz V_{OUT} = 2.5V	100			

Typical Performance Characteristics

Unless otherwise specified: T_J = 25°C, C_{OUT} = 10µF, C_{IN} = 10µF, S/D pin is tied to V_{IN}, V_{OUT} = 2.5V, V_{IN} = $V_{O(NOM)}$ + 1V, I_L = 10mA

Dropout Voltage Vs Output Load Current

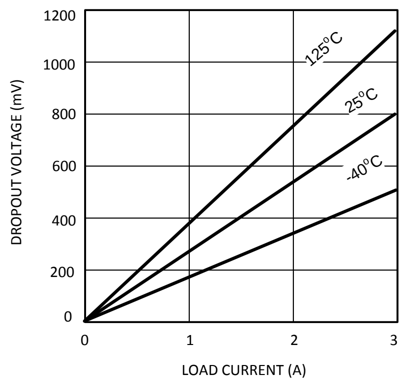


Figure 3.

Ground Current vs Output Load Current V_{OUT} = 5V

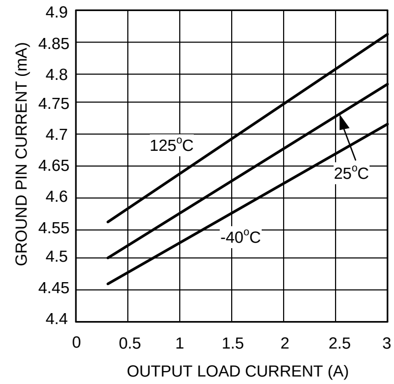


Figure 4.

Ground Current vs Output Voltage I_L = 3A

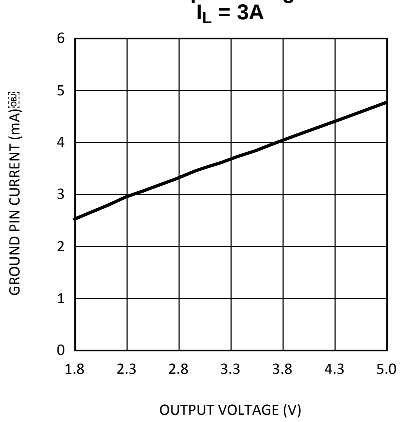


Figure 5.

Shutdown I_Q vs Junction Temperature

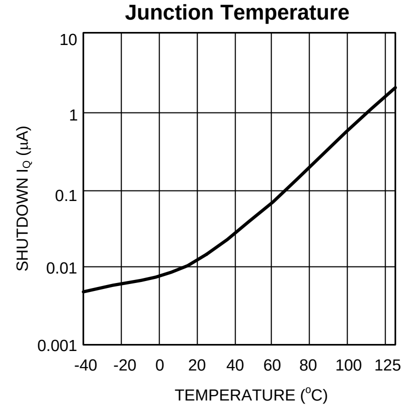


Figure 6.

Error Flag Threshold vs Junction Temperature

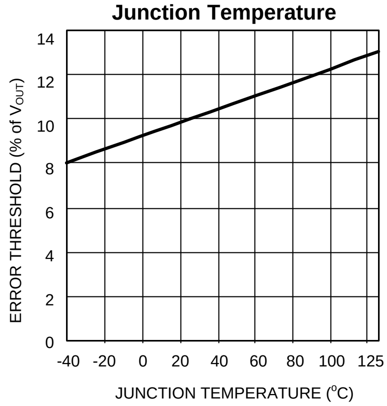


Figure 7.

DC Load Reg. vs Junction Temperature

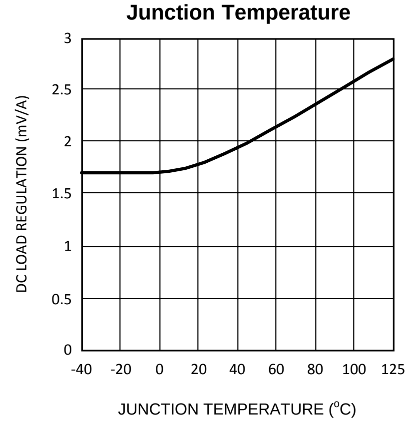


Figure 8.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_J = 25°C, C_{OUT} = 10µF, C_{IN} = 10µF, S/D pin is tied to V_{IN}, V_{OUT} = 2.5V, V_{IN} = $V_{O(NOM)}$ + 1V, I_L = 10mA

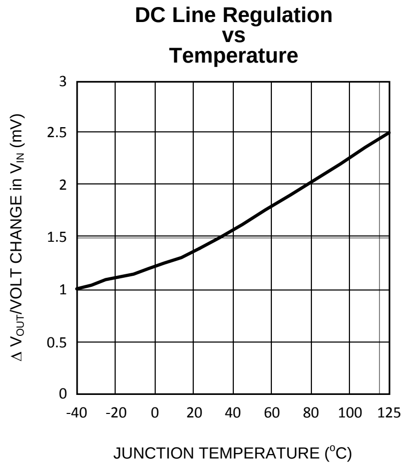


Figure 9.

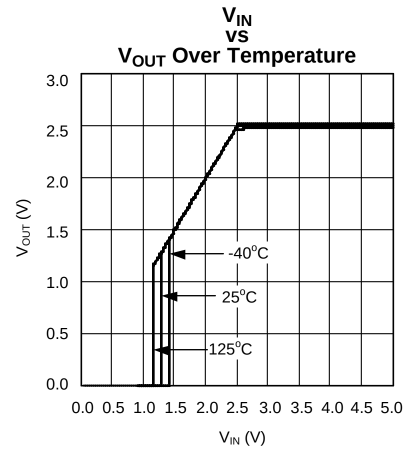


Figure 10.

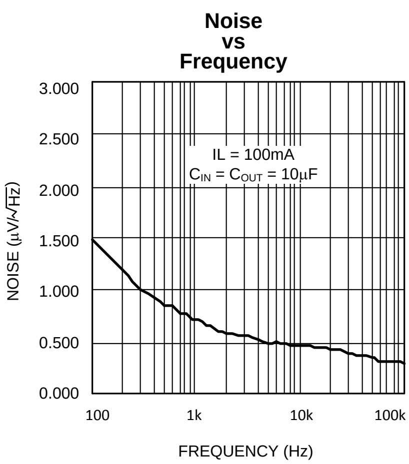


Figure 11.

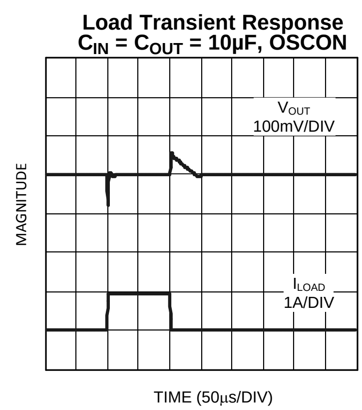


Figure 12.

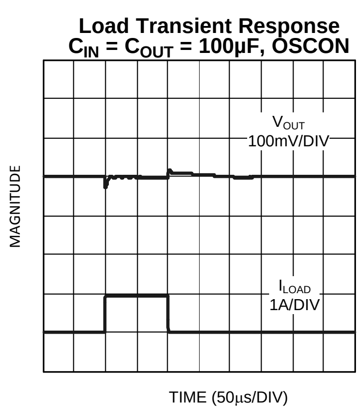


Figure 13.

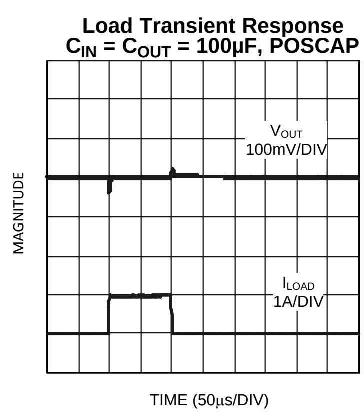


Figure 14.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_J = 25°C, C_{OUT} = 10µF, C_{IN} = 10µF, S/D pin is tied to V_{IN}, V_{OUT} = 2.5V, V_{IN} = $V_{O(NOM)}$ + 1V, I_L = 10mA

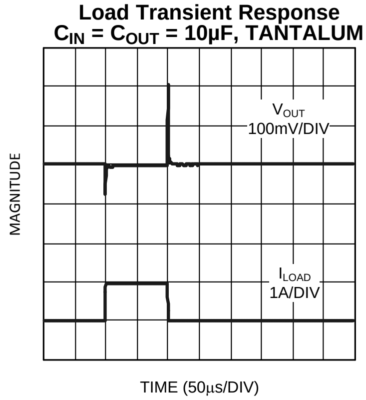


Figure 15.

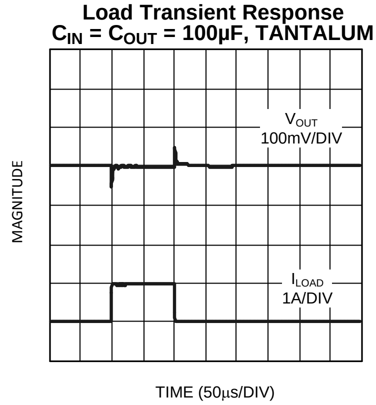


Figure 16.

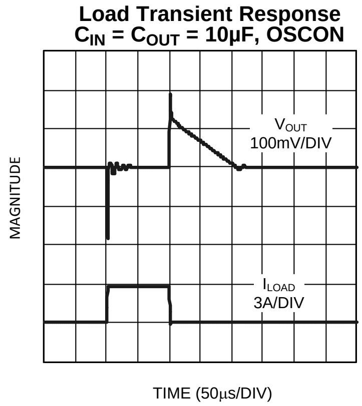


Figure 17.

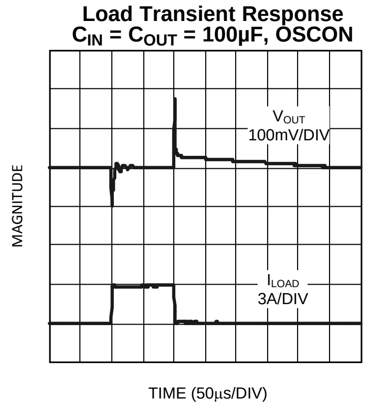


Figure 18.

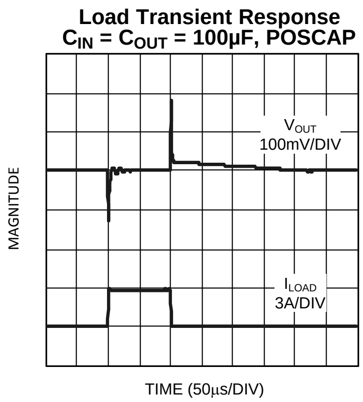


Figure 19.

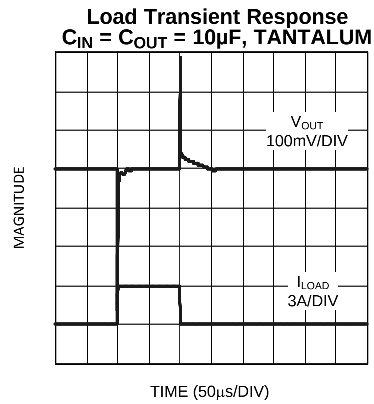


Figure 20.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_J = 25°C, C_{OUT} = 10µF, C_{IN} = 10µF, S/D pin is tied to V_{IN}, V_{OUT} = 2.5V, V_{IN} = $V_{O(NOM)}$ + 1V, I_L = 10mA

Load Transient Response
C_{IN} = C_{OUT} = 100µF, TANTALUM

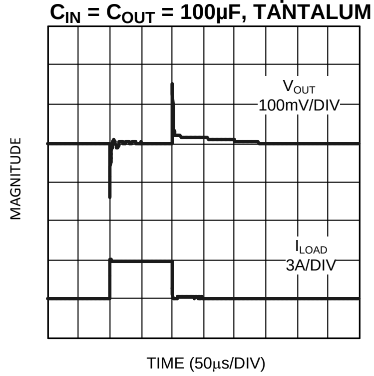


Figure 21.

APPLICATION HINTS

EXTERNAL CAPACITORS

Like any low-dropout regulator, external capacitors are required to assure stability. these capacitors must be correctly selected for proper performance.

INPUT CAPACITOR: An input capacitor of at least 1µF is required. Ceramic or Tantalum may be used, and capacitance may be increased without limit

OUTPUT CAPACITOR: An output capacitor is required for loop stability. It must be located less than 1 cm from the device and connected directly to the output and ground pins using traces which have no other currents flowing through them (see PCB LAYOUT section).

The minimum value of the output capacitance that can be used for stable full-load operation is 10 µF, but it may be increased without limit. The output capacitor must have an ESR value as shown in the stable region of the curve (below).

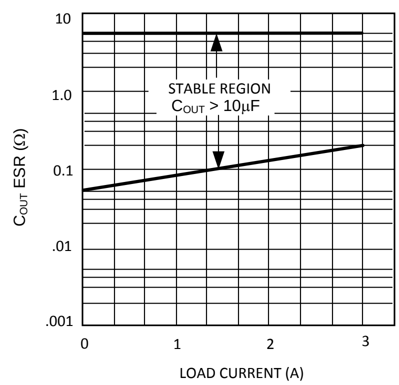


Figure 22. ESR Curve

SELECTING A CAPACITOR

It is important to note that capacitance tolerance and variation with temperature must be taken into consideration when selecting a capacitor so that the minimum required amount of capacitance is provided over the full operating temperature range. In general, a good Tantalum capacitor will show very little capacitance variation with temperature, but a ceramic may not be as good (depending on dielectric type). Aluminum electrolytics also typically have large temperature variation of capacitance value.

Equally important to consider is a capacitor's ESR change with temperature: this is not an issue with ceramics, as their ESR is extremely low. However, it is very important in Tantalum and aluminum electrolytic capacitors. Both show increasing ESR at colder temperatures, but the increase in aluminum electrolytic capacitors is so severe they may not be feasible for some applications (see CAPACITOR CHARACTERISTICS Section).

CAPACITOR CHARACTERISTICS

CERAMIC: For values of capacitance in the 10 to 100 µF range, ceramics are usually larger and more costly than tantalums but give superior AC performance for bypassing high frequency noise because of very low ESR (typically less than 10 mΩ). However, some dielectric types do not have good capacitance characteristics as a function of voltage and temperature.

Z5U and Y5V dielectric ceramics have capacitance that drops severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it. The Z5U and Y5V also exhibit a severe temperature effect, losing more than 50% of nominal capacitance at high and low limits of the temperature range.

X7R and X5R dielectric ceramic capacitors are strongly recommended if ceramics are used, as they typically maintain a capacitance range within ±20% of nominal over full operating ratings of temperature and voltage. Of course, they are typically larger and more costly than Z5U/Y5U types for a given voltage and capacitance.

TANTALUM: Solid Tantalum capacitors are recommended for use on the output because their typical ESR is very close to the ideal value required for loop compensation. They also work well as input capacitors if selected to meet the ESR requirements previously listed.

Tantalums also have good temperature stability: a good quality Tantalum will typically show a capacitance value that varies less than 10-15% across the full temperature range of 125°C to −40°C. ESR will vary only about 2X going from the high to low temperature limits.

The increasing ESR at lower temperatures can cause oscillations when marginal quality capacitors are used (if the ESR of the capacitor is near the upper limit of the stability range at room temperature).

ALUMINUM: This capacitor type offers the most capacitance for the money. The disadvantages are that they are larger in physical size, not widely available in surface mount, and have poor AC performance (especially at higher frequencies) due to higher ESR and ESL.

Compared by size, the ESR of an aluminum electrolytic is higher than either Tantalum or ceramic, and it also varies greatly with temperature. A typical aluminum electrolytic can exhibit an ESR increase of as much as 50X when going from 25°C down to −40°C.

It should also be noted that many aluminum electrolytics only specify impedance at a frequency of 120 Hz, which indicates they have poor high frequency performance. Only aluminum electrolytics that have an impedance specified at a higher frequency (between 20 kHz and 100 kHz) should be used for the LP387X. Derating must be applied to the manufacturer's ESR specification, since it is typically only valid at room temperature.

Any applications using aluminum electrolytics should be thoroughly tested at the lowest ambient operating temperature where ESR is maximum.

TURN-ON CHARACTERISTICS FOR OUTPUT VOLTAGES PROGRAMMED TO 2.0V OR BELOW

As Vin increases during start-up, the regulator output will track the input until Vin reaches the minimum operating voltage (typically about 2.2V). For output voltages programmed to 2.0V or below, the regulator output may momentarily exceed its programmed output voltage during start up. Outputs programmed to voltages above 2.0V are not affected by this behavior.

PCB LAYOUT

Good PC layout practices must be used or instability can be induced because of ground loops and voltage drops. The input and output capacitors must be directly connected to the input, output, and ground pins of the regulator using traces which do not have other currents flowing in them (Kelvin connect).

The best way to do this is to lay out C_{IN} and C_{OUT} near the device with short traces to the V_{IN}, V_{OUT}, and ground pins. The regulator ground pin should be connected to the external circuit ground so that the regulator and its capacitors have a "single point ground".

It should be noted that stability problems have been seen in applications where "vias" to an internal ground plane were used at the ground points of the IC and the input and output capacitors. This was caused by varying ground potentials at these nodes resulting from current flowing through the ground plane. Using a single point ground technique for the regulator and it's capacitors fixed the problem.

Since high current flows through the traces going into V_{IN} and coming from V_{OUT}, Kelvin connect the capacitor leads to these pins so there is no voltage drop in series with the input and output capacitors.

RFI/EMI SUSCEPTIBILITY

RFI (radio frequency interference) and EMI (electromagnetic interference) can degrade any integrated circuit's performance because of the small dimensions of the geometries inside the device. In applications where circuit sources are present which generate signals with significant high frequency energy content (> 1 MHz), care must be taken to ensure that this does not affect the IC regulator.

If RFI/EMI noise is present on the input side of the regulator (such as applications where the input source comes from the output of a switching regulator), good ceramic bypass capacitors must be used at the input pin of the IC.

If a load is connected to the IC output which switches at high speed (such as a clock), the high-frequency current pulses required by the load must be supplied by the capacitors on the IC output. Since the bandwidth of the regulator loop is less than 100 kHz, the control circuitry cannot respond to load changes above that frequency. The means the effective output impedance of the IC at frequencies above 100 kHz is determined only by the output capacitor(s).

In applications where the load is switching at high speed, the output of the IC may need RF isolation from the load. It is recommended that some inductance be placed between the output capacitor and the load, and good RF bypass capacitors be placed directly across the load.

PCB layout is also critical in high noise environments, since RFI/EMI is easily radiated directly into PC traces. Noisy circuitry should be isolated from "clean" circuits where possible, and grounded through a separate path. At MHz frequencies, ground planes begin to look inductive and RFI/EMI can cause ground bounce across the ground plane.

In multi-layer PCB applications, care should be taken in layout so that noisy power and ground planes do not radiate directly into adjacent layers which carry analog power and ground.

OUTPUT NOISE

Noise is specified in two ways-

Spot Noise or **Output noise density** is the RMS sum of all noise sources, measured at the regulator output, at a specific frequency (measured with a 1Hz bandwidth). This type of noise is usually plotted on a curve as a function of frequency.

Total output Noise or **Broad-band noise** is the RMS sum of spot noise over a specified bandwidth, usually several decades of frequencies.

Attention should be paid to the units of measurement. Spot noise is measured in units µV/√Hz or nV/√Hz and total output noise is measured in µV(rms).

The primary source of noise in low-dropout regulators is the internal reference. In CMOS regulators, noise has a low frequency component and a high frequency component, which depend strongly on the silicon area and quiescent current. Noise can be reduced in two ways: by increasing the transistor area or by increasing the current drawn by the internal reference. Increasing the area will decrease the chance of fitting the die into a smaller package. Increasing the current drawn by the internal reference increases the total supply current (ground pin current). Using an optimized trade-off of ground pin current and die size, LP3873/LP3876 achieves low noise performance and low quiescent current operation.

The total output noise specification for LP3873/LP3876 is presented in the Electrical Characteristics table. The Output noise density at different frequencies is represented by a curve under typical performance characteristics.

SHORT-CIRCUIT PROTECTION

The LP3873 and LP3876 are short circuit protected and in the event of a peak over-current condition, the short-circuit control loop will rapidly drive the output PMOS pass element off. Once the power pass element shuts down, the control loop will rapidly cycle the output on and off until the average power dissipation causes the thermal shutdown circuit to respond to servo the on/off cycling to a lower frequency. Please refer to the section on POWER DISSIPATION/HEATSINKING for power dissipation calculations.

$\overline{\text{ERROR}}$ FLAG OPERATION

The LP3873/LP3876 produces a logic low signal at the $\overline{\text{Error}}$ Flag pin when the output drops out of regulation due to low input voltage, current limiting, or thermal limiting. This flag has a built in hysteresis. The timing diagram in Figure 23 shows the relationship between the $\overline{\text{ERROR}}$ flag and the output voltage. In this example, the input voltage is changed to demonstrate the functionality of the Error Flag.

The internal $\overline{\text{Error}}$ flag comparator has an open drain output stage. Hence, the $\overline{\text{ERROR}}$ pin should be pulled high through a pull up resistor. Although the $\overline{\text{ERROR}}$ flag pin can sink current of 1mA, this current is energy drain from the input supply. Hence, the value of the pull up resistor should be in the range of 10kΩ to 1MΩ. **The ERROR pin must be connected to ground if this function is not used.** It should also be noted that when the shutdown pin is pulled low, the $\overline{\text{ERROR}}$ pin is forced to be invalid for reasons of saving power in shutdown mode.

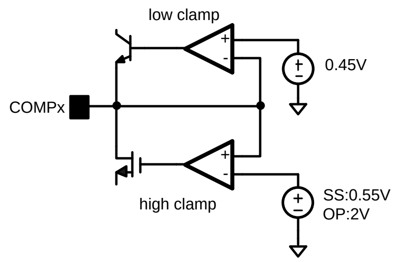


Figure 23. $\overline{\text{Error}}$ Flag Operation

SENSE PIN

In applications where the regulator output is not very close to the load, LP3876 can provide better remote load regulation using the SENSE pin. Figure 24 depicts the advantage of the SENSE option. LP3873 regulates the voltage at the output pin. Hence, the voltage at the remote load will be the regulator output voltage minus the drop across the trace resistance. For example, in the case of a 3.3V output, if the trace resistance is 100mΩ, the voltage at the remote load will be 3V with 3A of load current, I_{LOAD}. The LP3876 regulates the voltage at the sense pin. Connecting the sense pin to the remote load will provide regulation at the remote load, as shown in Figure 24. If the sense option pin is not required, the sense pin must be connected to the V_{OUT} pin.

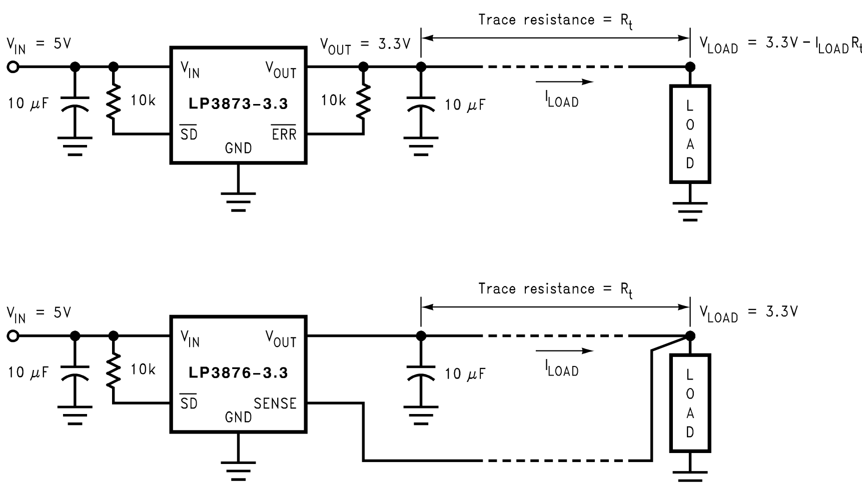


Figure 24. Improving remote load regulation using LP3876

SHUTDOWN OPERATION

A CMOS Logic level signal at the shutdown ($\overline{SD}$) pin will turn-off the regulator. Pin $\overline{SD}$ must be actively terminated through a 10kΩ pull-up resistor for a proper operation. If this pin is driven from a source that actively pulls high and low (such as a CMOS rail to rail comparator), the pull-up resistor is not required. This pin must be tied to Vin if not used.

DROPOUT VOLTAGE

The dropout voltage of a regulator is defined as the minimum input-to-output differential required to stay within 2% of the nominal output voltage. For CMOS LDOs, the dropout voltage is the product of the load current and the Rds(on) of the internal MOSFET.

REVERSE CURRENT PATH

The internal MOSFET in LP3873 and LP3876 has an inherent parasitic diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, if the output is pulled above the input in an application, then current flows from the output to the input as the parasitic diode gets forward biased. The output can be pulled above the input as long as the current in the parasitic diode is limited to 200mA continuous and 1A peak.

POWER DISSIPATION/HEATSINKING

LP3873 and LP3876 can deliver a continuous current of 3A over the full operating temperature range. A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible conditions, the junction temperature must be within the range specified under operating conditions. The total power dissipation of the device is given by:

$P_D = (V_{IN} - V_{OUT})I_{OUT} + (V_{IN})I_{GND}$

where I_{GND} is the operating ground current of the device (specified under Electrical Characteristics).

The maximum allowable temperature rise (T_{Rmax}) depends on the maximum ambient temperature (T_{Amax}) of the application, and the maximum allowable junction temperature (T_{Jmax}):

$T_{Rmax} = T_{Jmax} - T_{Amax}$

The maximum allowable value for junction to ambient Thermal Resistance, θ_{JA}, can be calculated using the formula:

$\theta_{JA} = T_{Rmax} / P_D$

LP3873 and LP3876 are available in TO-220 and DDPAK/TO-263 packages. The thermal resistance depends on amount of copper area or heat sink, and on air flow. If the maximum allowable value of θ_{JA} calculated above is ≥ 60 °C/W for TO-220 package and ≥ 60 °C/W for DDPAK/TO-263 package no heatsink is needed since the package can dissipate enough heat to satisfy these requirements. If the value for allowable θ_{JA} falls below these limits, a heat sink is required.

HEATSINKING TO-220 PACKAGE

The thermal resistance of a TO-220 package can be reduced by attaching it to a heat sink or a copper plane on a PC board. If a copper plane is to be used, the values of θ_{JA} will be same as shown in next section for TO263 package.

The heatsink to be used in the application should have a heatsink to ambient thermal resistance,

$\theta_{HA} \leq \theta_{JA} - \theta_{CH} - \theta_{JC}$.

In this equation, θ_{CH} is the thermal resistance from the case to the surface of the heat sink and θ_{JC} is the thermal resistance from the junction to the surface of the case. θ_{JC} is about 3°C/W for a TO-220 package. The value for θ_{CH} depends on method of attachment, insulator, etc. θ_{CH} varies between 1.5°C/W to 2.5°C/W. If the exact value is unknown, 2°C/W can be assumed.

HEATSINKING DDPAK/TO-263 PACKAGE

The DDPAK/TO-263 package uses the copper plane on the PCB as a heatsink. The tab of these packages are soldered to the copper plane for heat sinking. Figure 25 shows a curve for the θ_{JA} of DDPAK/TO-263 package for different copper area sizes, using a typical PCB with 1 ounce copper and no solder mask over the copper area for heat sinking.

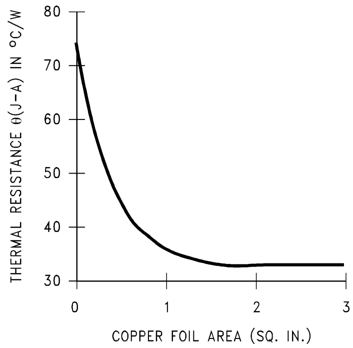


Figure 25. θ_{JA} vs Copper (1 Ounce) Area for DDPAK/TO-263 package

As shown in the figure, increasing the copper area beyond 1 square inch produces very little improvement. The minimum value for θ_{JA} for the DDPAK/TO-263 package mounted to a PCB is 32°C/W.

Figure 26 shows the maximum allowable power dissipation for DDPAK/TO-263 packages for different ambient temperatures, assuming θ_{JA} is 35°C/W and the maximum junction temperature is 125°C.

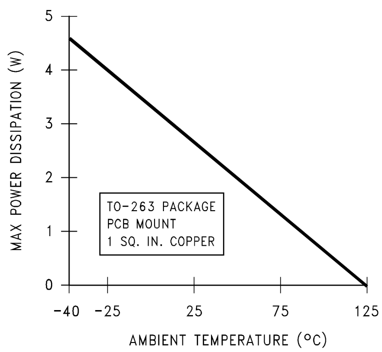


Figure 26. Maximum power dissipation vs ambient temperature for DDPAK/TO-263 package

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3873ES-1.8/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3873ES -1.8	Samples
LP3873ES-2.5	NRND	DDPAK/ TO-263	KTT	5	45	TBD	Call TI	Call TI	-40 to 125	LP3873ES -2.5	
LP3873ES-2.5/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3873ES -2.5	Samples
LP3873ES-3.3	NRND	DDPAK/ TO-263	KTT	5	45	TBD	Call TI	Call TI	-40 to 125	LP3873ES -3.3	
LP3873ES-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3873ES -3.3	Samples
LP3873ES-5.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3873ES -5.0	Samples
LP3873ESX-1.8/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3873ES -1.8	Samples
LP3873ESX-3.3	NRND	DDPAK/ TO-263	KTT	5	500	TBD	Call TI	Call TI	-40 to 125	LP3873ES -3.3	
LP3873ESX-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3873ES -3.3	Samples
LP3873ESX-5.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3873ES -5.0	Samples
LP3876ES-1.8/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3876ES -1.8	Samples
LP3876ES-2.5/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3876ES -2.5	Samples
LP3876ES-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3876ES -3.3	Samples
LP3876ES-5.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3876ES -5.0	Samples
LP3876ESX-1.8/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3876ES -1.8	Samples
LP3876ESX-2.5/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3876ES -2.5	Samples
LP3876ET-1.8/NOPB	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LP3876ET -1.8	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3876ET-2.5/NOPB	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LP3876ET -2.5	Samples
LP3876ET-3.3/NOPB	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LP3876ET -3.3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

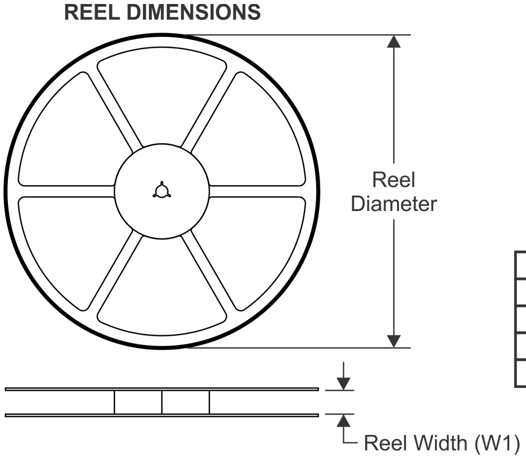
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

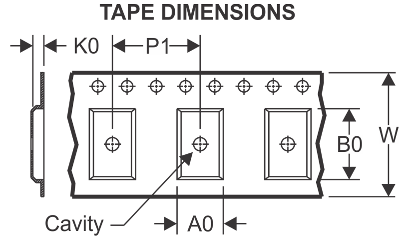
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

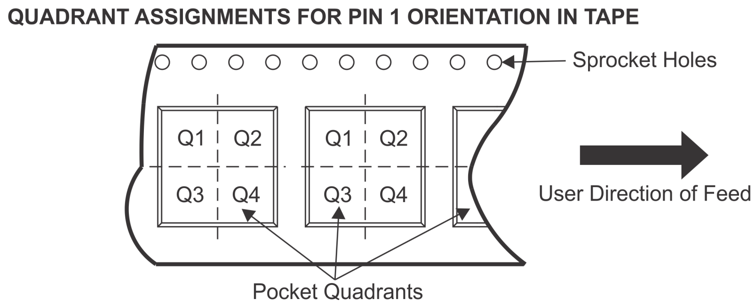
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION





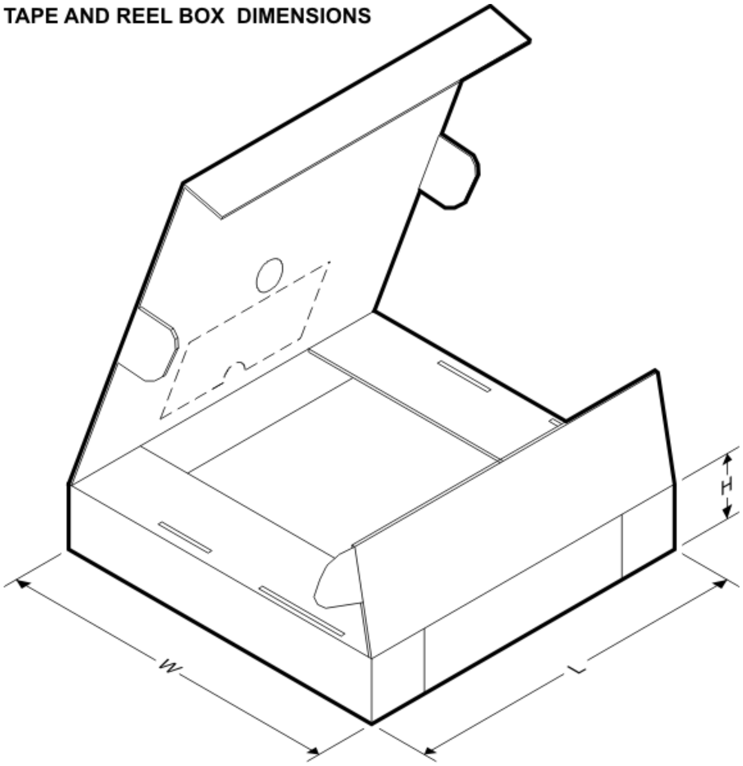
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3873ESX-1.8/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3873ESX-3.3	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3873ESX-3.3/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3873ESX-5.0/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3876ESX-1.8/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3876ESX-2.5/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

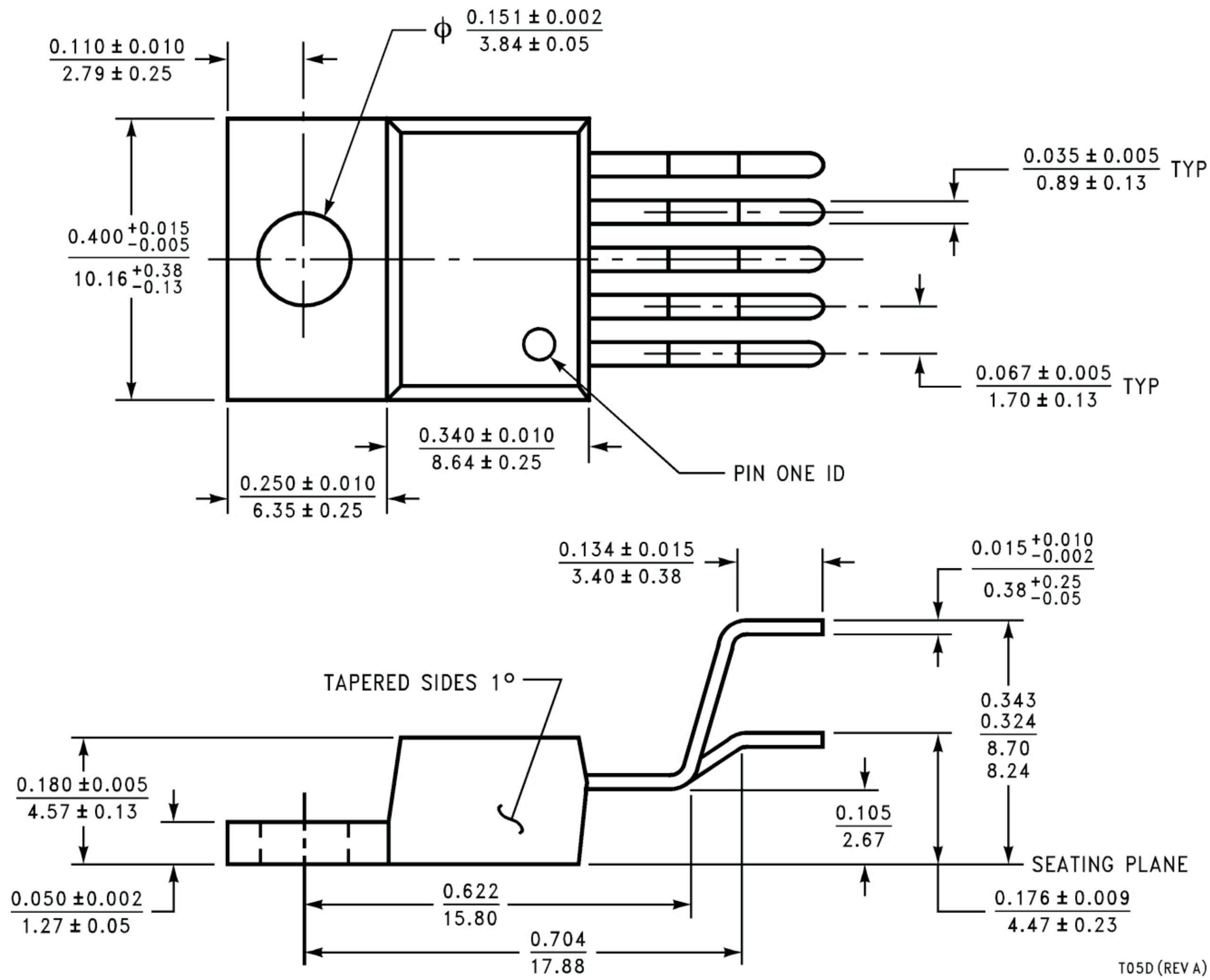
TAPE AND REEL BOX DIMENSIONS



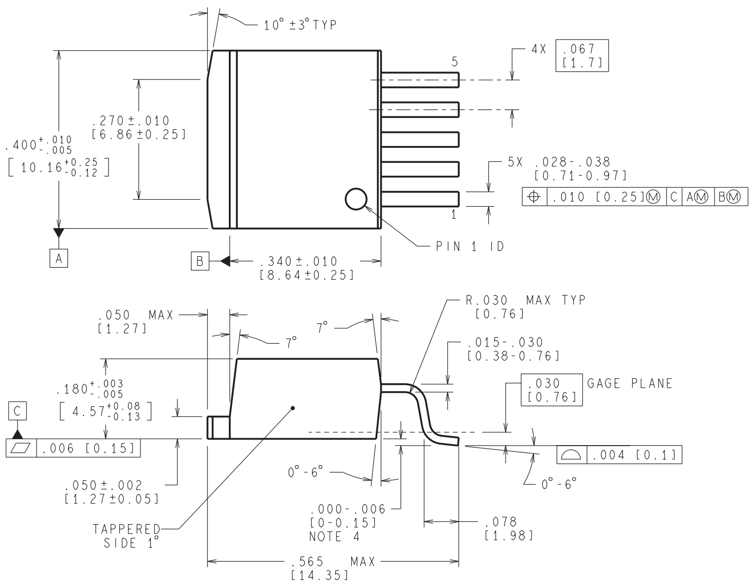
*All dimensions are nominal

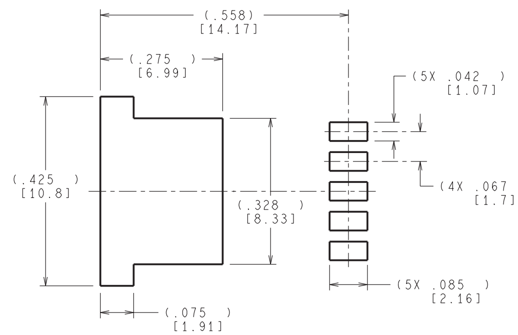
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3873ESX-1.8/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LP3873ESX-3.3	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LP3873ESX-3.3/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LP3873ESX-5.0/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LP3876ESX-1.8/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LP3876ESX-2.5/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0

NDH0005D

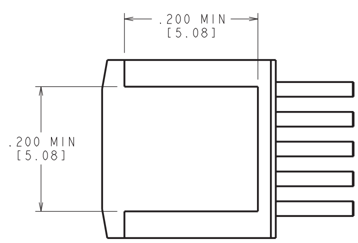

0.110 ± 0.010
2.79 ± 0.25
φ 0.151 ± 0.002
3.84 ± 0.05
0.035 ± 0.005 TYP
0.89 ± 0.13
0.400 +0.015 −0.005
10.16 +0.38 −0.13
0.067 ± 0.005 TYP
1.70 ± 0.13
0.340 ± 0.010
8.64 ± 0.25
PIN ONE ID
0.250 ± 0.010
6.35 ± 0.25
0.134 ± 0.015
3.40 ± 0.38
0.015 +0.010 −0.002
0.38 +0.25 −0.05
TAPERED SIDES 1°
0.343
0.324
8.70
8.24
0.180 ±0.005
4.57 ± 0.13
0.105
2.67
SEATING PLANE
0.050 ±0.002
1.27 ± 0.05
0.622
15.80
0.176 ± 0.009
4.47 ± 0.23
0.704
17.88
T05D (REV A)

KTT0005B





LAND PATTERN RECOMMENDATION



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

TS5B (Rev D)

BOTTOM SIDE OF PACKAGE

IMPORTANT NOTICE AND DISCLAIMER

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265