DIO2125XM10

3Vrms Audio Driver with Adjustable Gain

Features

- Voltage Output at 2.5kΩ Load:
  3Vrms With 5V Supply Voltage
- Ultra Low Distortion:
  SNR>109dB
  Typical Vn<7μVrms
  THD+N<0.001%
- No Pop/Clicks Noise when Power ON/OFF
- No Need for Output DC-Blocking Capacitors
- Optimized Frequency Response between 20Hz–20kHz
- Featuring external under voltage mute
- Output Pin HBM ESD protection 8kV
- Package available in EP-MSOP-10 with exposed Pad

Applications

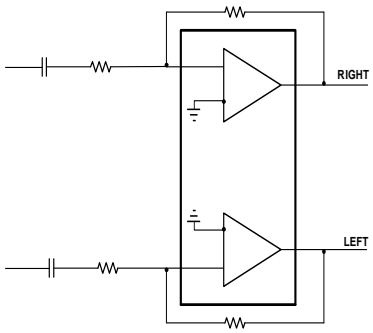
- Set-Top Boxes
- High Definition DVD Players
- Car Entertainment System
- Medical
- Flat Panel TV

Descriptions

The DIO2125 is an integrated solution for Set-top box and high definition player, and designed to optimize the audio driver circuit performance while reducing the BOM cost by eliminating the peripheral discrete components for noise reduction. DIO2125 is able to deliver up to 3Vrms audio output with no need of output AC- coupling capacitors.

The DIO2125 is able to offer 3Vrms output with 2.5kΩ load under 5V supply. Meanwhile, the DIO2125 offers built-in shut-down control circuitry for maximum noise reduction under power-up or power-down conditions.

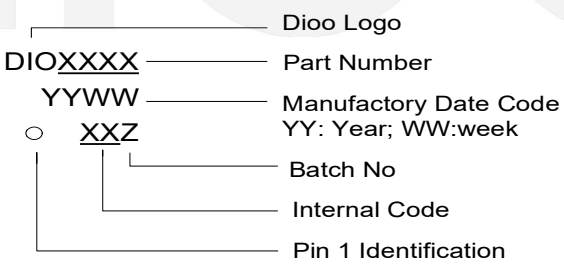
Block Diagram



Ordering Information

Order Part Number	Top Marking		T_A	Package	
DIO2125XM10	DIO2125	Green/RoHS	-40 to +85°C	EP-MSOP-10	Tape & Reel, 3000

Marking Definition



Pin Assignment

MSOP-10(Exposed pad)

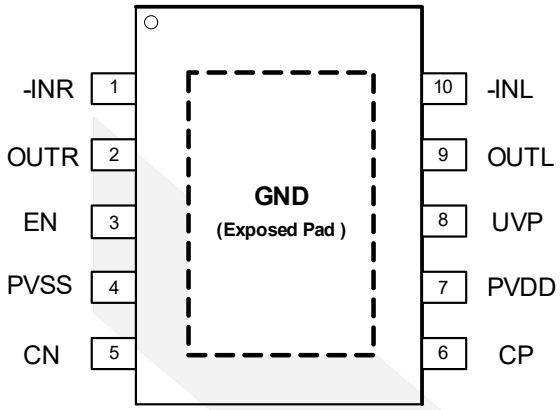


Figure 1 Pin Assignment (Top View)

Pin Descriptions

PIN Name	I/O	Description
-INR	I	Right-channel negative input
OUTR	O	Right-channel output
EN	I	Enable input, active-high
PVSS	P	Supply voltage output
CN	I/O	Charge-pump flying capacitor negative terminal
CP	I/O	Charge-pump flying capacitor positive terminal
PVDD	P	Positive supply
GND	P	Ground (Exposed Pad)
UVP	P	Under voltage protection input
OUTL	O	Left-channel output
-INL	I	Left-channel negative input

Note: For simplicity, all V_{DD} below stands for PVDD

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maxim rating conditions for extended periods may affect device reliability.

Parameter		Rating	Unit
Supply Voltage		-0.3 to 7.5	V
Input Voltage		V_{SS}-0.3 to V_{DD}+0.3	V
Minimum load impedance		>600	Ω
EN to GND		-0.3 to V_{DD}+0.3	V
Storage Temperature Range		-65 to 150	°C
Junction Temperature		150	°C
MSOP-10Θ_{JA}		190	°C/W
HBM ESD, JESD22-A114	Output pins	8	kV
	Other pins	7.5	

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended Operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not Recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.75	5	5.25	V
V_{IH}	EN High level Input Voltage	1.2			V
V_{IL}	EN Low level Input Voltage			0.4	V
T_A	Operating Temperature Range	-40		85	°C

Electrical Characteristics

Typical value: T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OS}	Output Offset Voltage	V_{DD}=5V, Input grounded, Gain=100		2		mV
OVP	V_{DD} Over Voltage Protection	V_{DD}>5.5V, then IC shutdown	5.5			V
PSRR	Power supply rejection ratio	V_{DD}=4.75V to 5.25V		85		dB
V_{OH}	High level output voltage	V_{DD}=5V, R_L=2.5kΩ	3.1			V
V_{OL}	Low level output voltage	V_{DD}=5V, R_L=2.5kΩ			-3.05	V
I_{IH}	EN High level input current	V_{DD}=5V, V_I=V_{DD}			1	μA
I_{IL}	EN Low level input current	V_{DD}=5V, V_I=0V			1	μA
I_{DD}	Supply current	V_{DD}=5V, EN= V_{DD}, No load		14		mA
		V_{DD}=5V, EN= 0, No load		1.5		

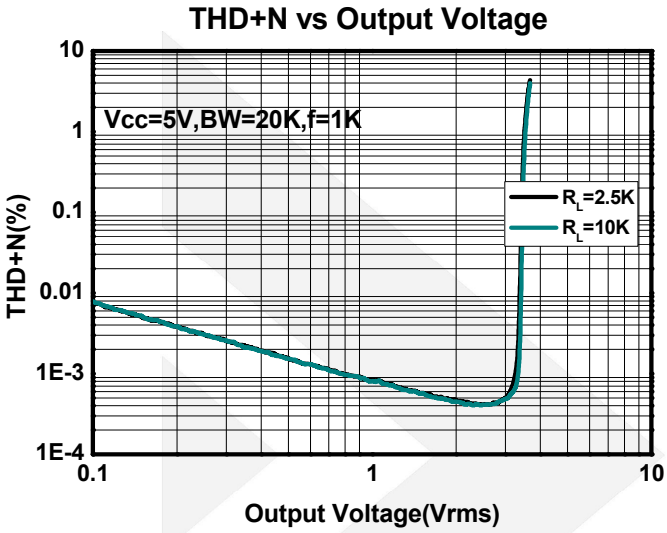
Operating Characteristics

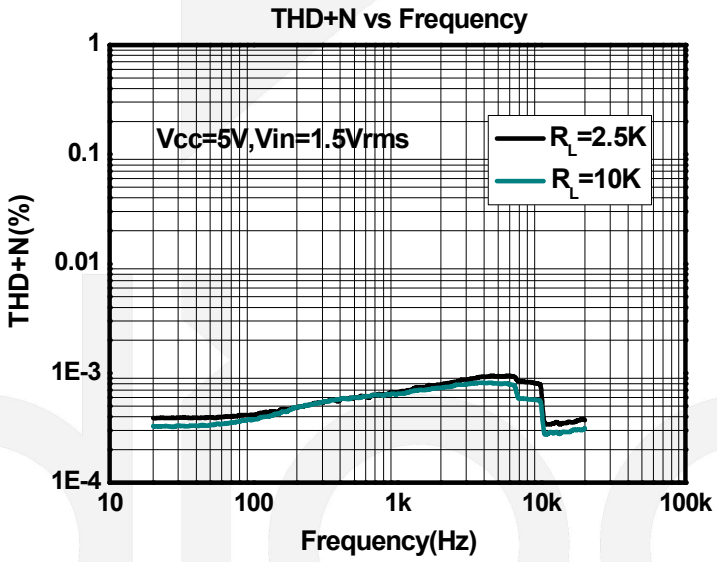
Typical value: V_{DD}=5V, R_L=2.5kΩ, C_{PUMP}=0.33μF, C_{PVSS}=1μF, C_{IN}=10μF, R_{IN}=10kΩ, R_{fb}=20kΩ, T_A=25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_O	Output Voltage	THD=1%, V_{DD}=5V, f=1kHz, R_L=100kΩ	3.1			V_{RMS}
THD+N	Total harmonic distortion + noise	V_O=3V_{RMS}, f=1kHz		0.001		%
X_{TALK}	Channel crosstalk	V_O=3V_{RMS}, f=1kHz		-100		dB
I_O	Maximum output current	V_{DD}=5V		18		mA
SNR	Signal noise ratio	V_O=3V_{RMS}, THD+N=0.1%, BW=22kHz A-weighted		108		dB
SR	Slew rate			11.8		V/μs
C_L	Maximum capacitive load			220		pF
V_N	Noise output voltage	BW=20Hz to 22kHz		6		μV_{RMS}
G_{BW}	Unity gain bandwidth			8		MHz
A_{VO}	Open loop voltage gain			150		dB
V_{UVP}	External under-voltage detection		1.11	1.15	1.205	V
I_{Hys}	External under-voltage detection hysteresis current			5		μA
f_{CP}	Charge pump frequency		265		450	kHz

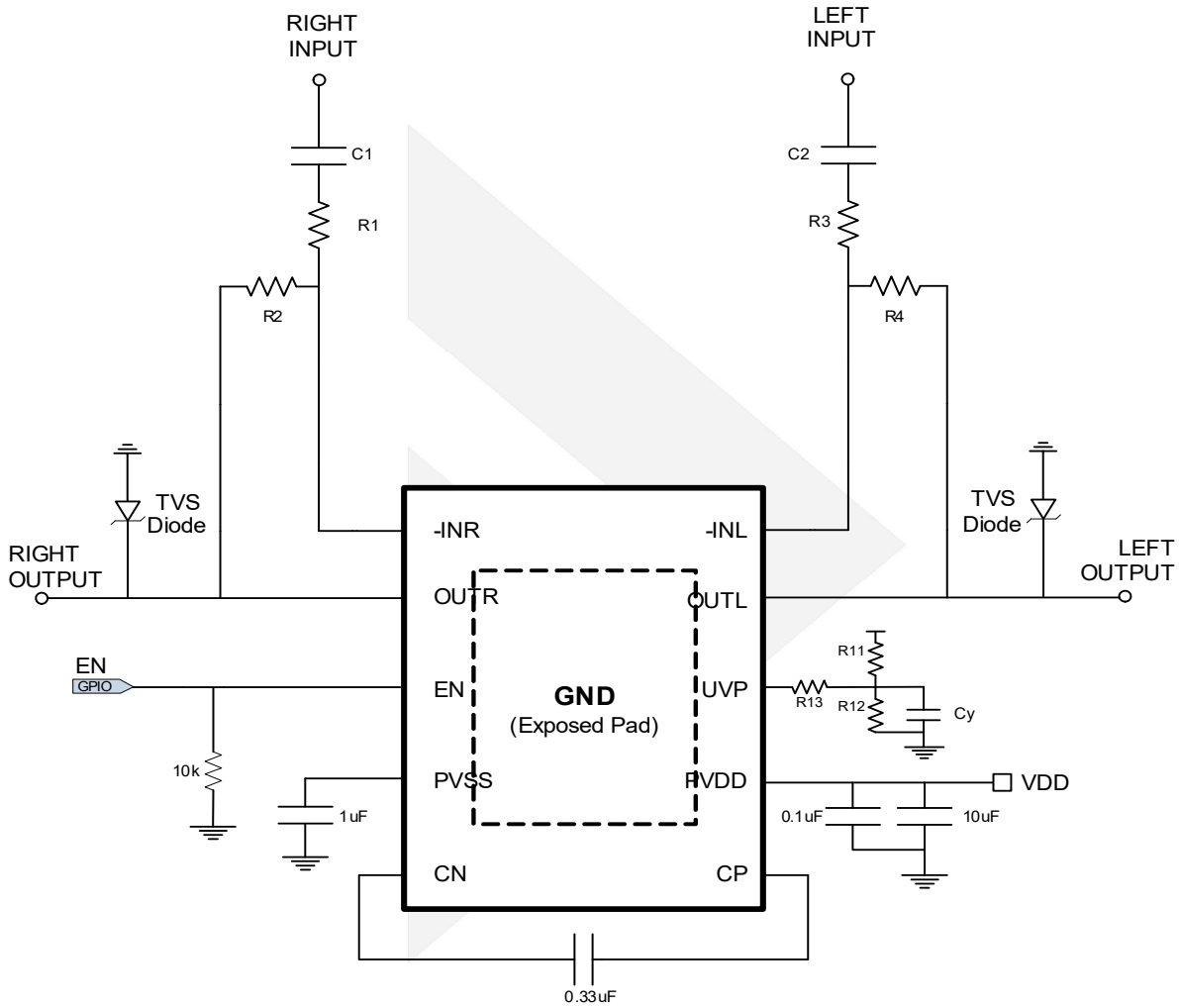
Typical Performance Characteristics

At T_A = +25℃, C_{PUMP}=0.33μF, C_{PVSS}=1μF, unless otherwise noted.





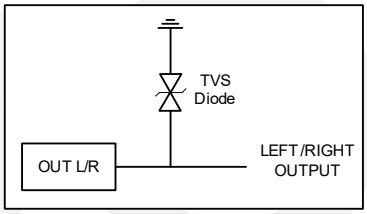
Application Circuit



Important Note:

1. In some applications, if the power supply noise needs to be filtered, the ferrite bead is recommended in a value of 600ohm@100MHz, instead of RC network. RC network normally will lower the power supply resulting in the degraded the audio performance. If the resistor is not chosen properly, which can trigger the internal UVP detection circuit and mute the output. As depicted below.

2. In order to protect the device against the power surge, transient voltage suppressor (TVS) devices are recommended at the output pins OUTL/OUTR



Application Notes

Gain-Setting Resistors Ranges and Input-Blocking Capacitors

The gain-setting resistors, R_{IN} and R_{FB}, must be chosen so that noise, stability, and input capacitor size of the DIO2125 are kept within acceptable limits. Voltage gain is defined as R_{FB} divided by R_{IN}.

Table 1 lists the recommended resistor value for different gain settings. Selecting values that are too low demands a large input ac-coupling capacitor $C_{IN.}$ Selecting values that are too high increases the noise of the amplifier.

The gain-setting resistor must be placed close to the input pins to minimize capacitive loading on these input pins and to ensure maximum stability.

Table 1 Input Capacitor with 2Hz cutoff and Resistor Values Recommended

Input Res., R_{IN}	Feedback Res., R_{fb}	Inverting Gain
22 kΩ	22 kΩ	-1 V/V
15 kΩ	30 kΩ	-2 V/V
10 kΩ	100 kΩ	-10 V/V

$$f_{CIN} = \frac{1}{2\pi R_{IN} C_{IN}}, \quad \text{or}$$

$$C_{IN} = \frac{1}{2\pi R_{IN} f_{CIN}}$$

Equation 1 Cutoff decision Cutoff

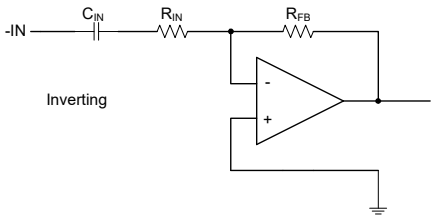


Figure 2 Inverting Gain Configurations

INPUT-BLOCKING CAPACITORS

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of DIO2125. These capacitors block the dc portion of the audio source and allow DIO2125 inputs to be properly biased to provide maximum performance.

These capacitors form a high-pass filter with the input resistor, R_{IN}. The cutoff frequency is calculated using the equation below. For this calculation, the capacitance used is the input-blocking capacitor, and the resistance is the input resistor chosen from Table 1; then the frequency and/or capacitance can be determined when one of the two values is given.

Charge Pump Flying Capacitor and PVSS Capacitor

The charge pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The PVSS capacitor must be at least equal to the charge pump capacitor in order to allow maximum charge

transfer. Low ESR X5 or X7 capacitors are recommended selection, and a value of 0.33μF is typical. Capacitor values that are smaller than 0.33μF can be used, but the maximum output voltage may be reduced and the device may not operate to specifications.

Decoupling Capacitors

The DIO2125 requires adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically a combine of paralleled 0.1μF and 10μF, placed as close as possible to the device VDD lead works best. Placing this decoupling capacitor close to the DIO2125 is important for the performance of the amplifier. For filtering lower-frequency noise signals, a 10μF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

Pop-Free Power-Up

Pop-free power up is ensured by keeping the EN (shutdown pin) low during power-supply ramp up and ramp down. The EN pin should be kept low until the input ac-coupling capacitors are fully charged before asserting the EN pin high to achieve pop-less power up. Figure 4 illustrates the preferred sequence.

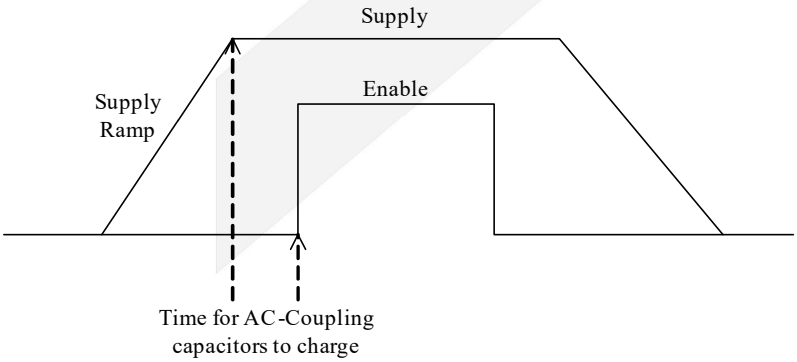


Figure 4 Power-Up Sequences

Capacitive Load

The DIO2125 has the ability to drive a high capacitive load up to 220 pF directly. Higher capacitive loads can be accepted by adding a series resistor of 47Ω or larger.

External Under-voltage Detection

External under-voltage detection can be used to shut down the DIO2125 before an input device can generate a pop. Although the shutdown voltage is 1.15V, customers need to consider the accuracy of system passive components such as resistors and associated temperature variation. Users often select a resistor divider to obtain the power-on and shutdown threshold for the specific application. The typical thresholds can be calculated as follows, respectively for VSUP_MO at 5V and 12V. Usually for best power down noise performance, 12V

supply is recommended for UVP circuitry as below. Typically this 12V is the power supply which generates the 5V supply for DIO2125 VDD pins.

Case 1: VSUP_MO= 12V (**Recommended**)

V_{UVP}=(1.15V-6μA*R13)*(R11+R12)/R12;

$V_{hysteresis}$=5μA*R13*(R11+R12)/R12;

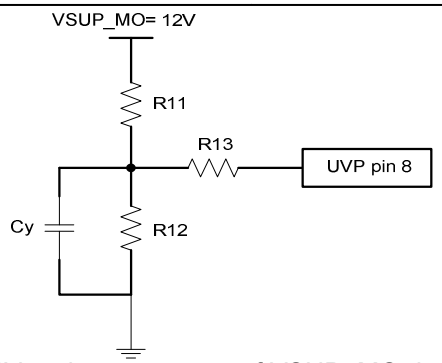
With the condition R13>>R11//R12.

For example, if R11=11k, R12=1.4k and R13=47k,

Then V_{UVP}=7.688V; $V_{hysteresis}$=2.081V

Here, V_{UVP} is the shutdown threshold.

In this case, the voltage at UVP pin 8 is greater than 1.44V under worst case of VSUP_MO ripples.



Case 2: VSUP_MO= 5.0V

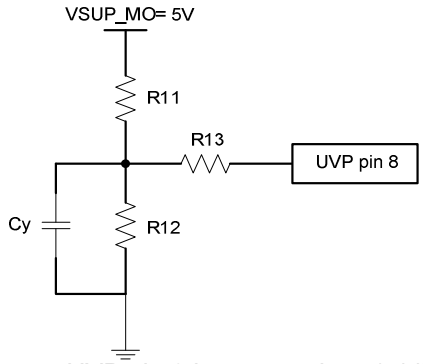
V_{UVP}=(1.15V-6μA*R13)*(R11+R12)/R12;

$V_{hysteresis}$=5μA*R13*(R11+R12)/R12;

With the condition R13>>R11//R12.

For example, if R11=5.6k, R12=2.2k and R13=47k,

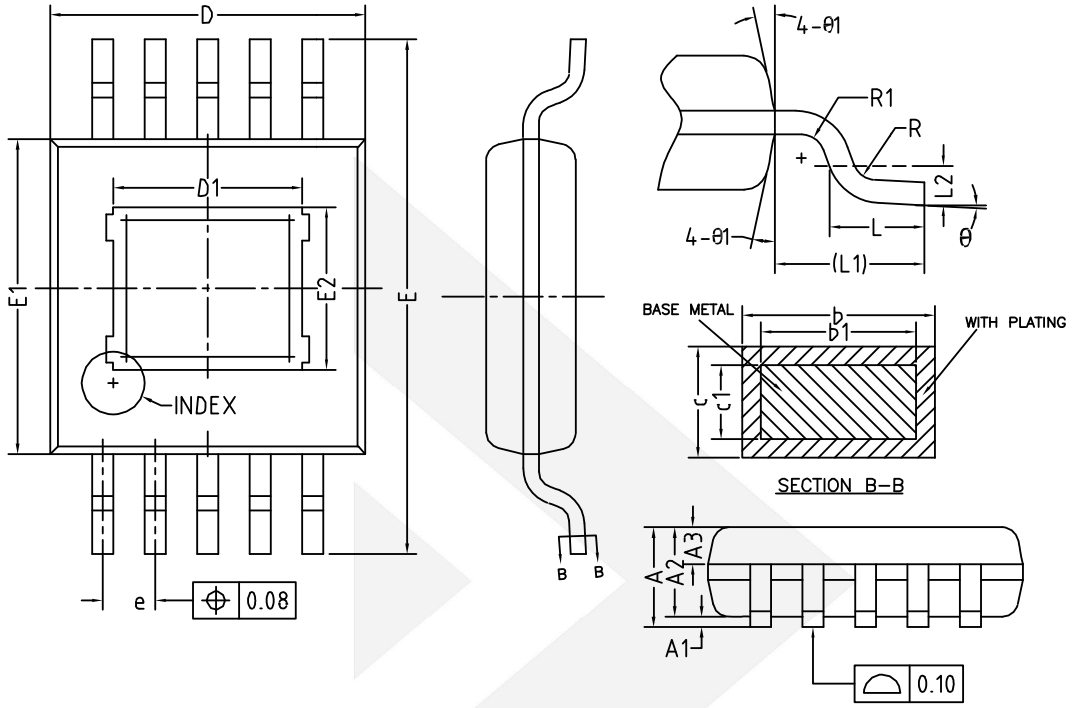
Then V_{UVP}=3.077V; $V_{hysteresis}$=0.833V



Here, V_{UVP} is the shutdown threshold. In this case, the voltage at UVP pin 8 is greater than 1.44V under worst case of VSUP_MO ripples.

For further assistance, please contact DIOO worldwide sales office to seek technical support. You can find DIOO sales office information at www.dioo.com.

Physical Dimensions: EP-MSOP-10(Exposed Pad)



Symbol	Min	Typ	Max
A	-	-	1.10
A1	0	-	0.15
A2	0.75	0.85	0.95
A3	0.25	0.35	0.39
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.15	-	0.20
c1	0.14	0.15	0.16
D	2.90	3.00	3.10
D1	0.75	-	2.50
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
E2	0.75	-	2.50
e	0.40	0.50	0.60
L	0.40	0.60	0.80
L1	0.95REF		
L2	0.25BSC		
R	0.07	-	-
R1	0.07	-	-
Θ	0°	-	8°
Θ1	9°	12°	15°

CONTACT US

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