L99H92

Datasheet

Half-bridge pre-driver for automotive applications

QFN32 5x5
exposed pad

TQFP32 7x7
exposed pad

Product status link
L99H92

Product summary	
Order code	**L99H92Q5-TR**
Package	QFN32
Packing	Tape and reel
Order code	**L99H92QF-TR**
Package	TQFP32 7x7
Packing	Tape and reel

Features

- AEC-Q100 qualified
- RoHs compliant device
- Power supply operating range from 4.51 V to 28 V (gate drivers operative from 5.41 V)
- 3.3 V/5 V compatible I/Os
- All pins linked to the microcontroller, fail-safe input and VDD are made tolerant to battery exposure
- Dual half-bridge driver compatible with standard level threshold NMOSFETs
- Configurable full-bridge or dual independent half-bridges control
  - Programmable recirculation path in case of full-bridge control
- Dual stage charge pump supporting 100% PWM duty cycle down to 5.41 V battery voltage
  - High and low side minimum V_{GS}=6.2 V @ VDH=5.5 V and charge pump load current (I_{CPLOAD}) equal to 5 mA
  - High and low side minimum V_{GS}=8.2 V @ VDH≥8 V and charge pump load current (I_{CPLOAD}) equal to 10 mA
- Charge pump output available for driving an external reverse battery NMOSFET protection
- Programmable gate driving current (up to 170 mA) for output voltage slew rate control
- Programmable drain-source monitoring for overcurrent protection and programmable cross-current protection time (dead-time)
- Open load and output short circuit detection in off-state diagnostic mode
- SPI for control and diagnosis (ST SPI 4.1)
- Programmable diagnostic output
- Two independent current sense amplifiers
  - Low offset with extremely low thermal drift
  - Suitable for high-side, in-line and low–side current sensing
  - Independently programmable gain (10x, 20x, 50x, 100x)
  - Analog output centered at V_{DD}/2 or VDD/22
- Overtemperature prewarning and shutdown
- Analog and digital power supply inputs over/undervoltage protections
- Asynchronous and logic independent fail-safe input to switch off all the MOSFETs
- Low quiescent current
- Support for random HW faults up to ASIL B

Applications

- Sun-roof
- Power trunk lift gate
- Sliding doors
- Window lift, seat-belt pre-tensioners, etc.

- Electric park brake system

Description

The L99H92 is designed to drive 4 external N-channel MOSFET transistors in single H-bridge or dual independent half bridge configuration for DC-motor control in automotive applications. Two free configurable current sense amplifiers are integrated.

The device has a low power mode (standby mode) where the current consumption is less than 5 µA.

Programmable gate driving current allows minimizing EMI. Each gate driver monitors independently its external MOSFET drain-source voltage for fault conditions.

Programmable cross current protection time avoids concurrency of high side and low side activation for each half bridge.

Two off-state diagnostic comparators detect potential short to ground, short to battery or open load conditions.

The integrated standard serial peripheral interface (SPI) controls the device and provides diagnostic information. An additional DIAGN output pin alerts the microcontrollers of a fault occurred into the device faster than the SPI communication.

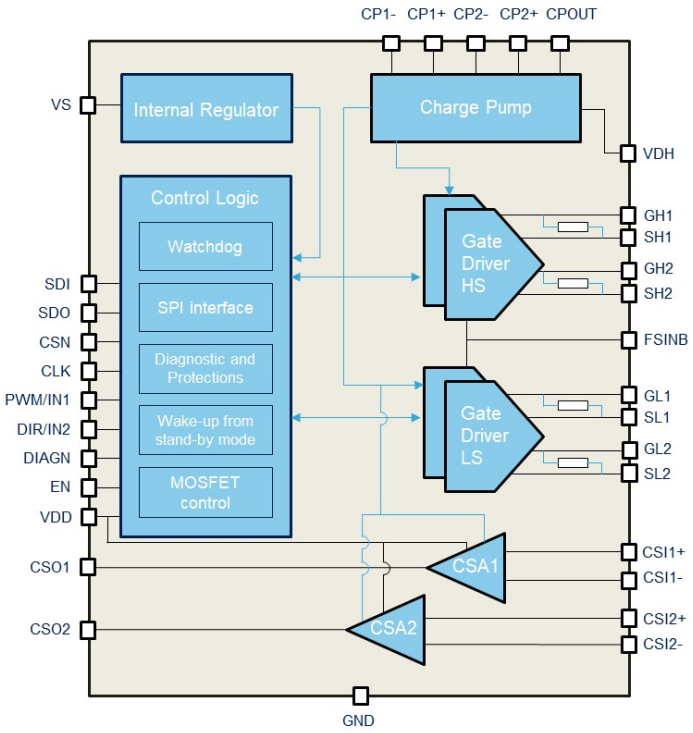
The L99H92 device implements diagnostic and protection features such as supply voltage monitoring, charge pump voltage monitoring, overcurrent protection, temperature warning and overtemperature shutdown.

The devices are hosted in a TQFP32 and a QFN32 package both with exposed pad. QFN32 has wettable flanks for easy visual inspection of the solder joint.

1 Block diagram and pins description

1.1 Block diagram

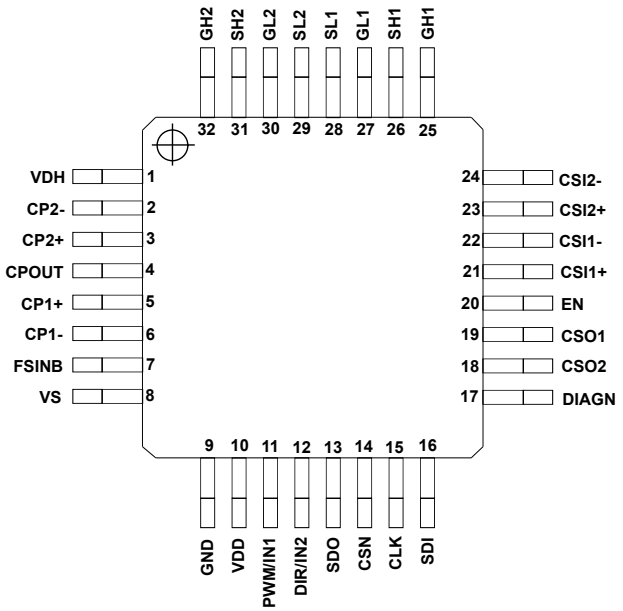
Figure 1. Block diagram



GADG120920220920SA

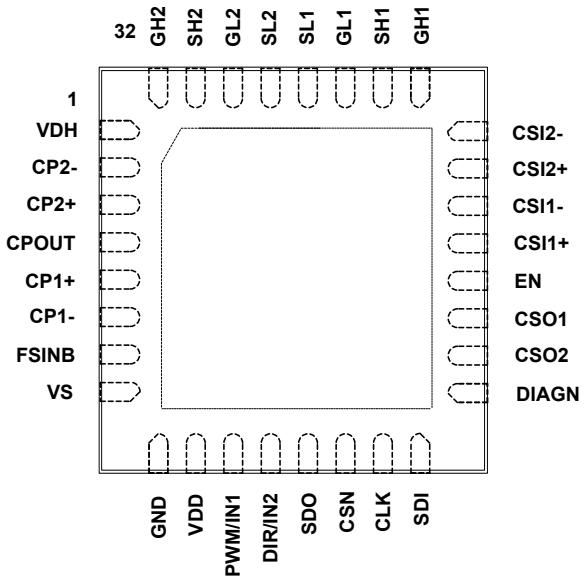
1.2 Pinout

Figure 2. Pinout - TQFP32



GADG120920221234SA

Figure 3. **Pinout - QFN 32**



GADG120920221236SA

1.3 Pins description

Table 1. **Pin definitions and functions**

Pin	Name	Description
1	VDH	High-side drain connection
2	CP2-	Charge pump stage 2 negative connection
3	CP2+	Charge pump stage 2 positive connection
4	CPOUT	Charge pump output
5	CP1+	Charge pump stage 1 positive connection
6	CP1-	Charge pump stage 1 negative connection
7	FSINB	Fail-safe input not
8	VS	Power supply input
9	GND	Ground connection
10	VDD	3.3 V/5 V supply for I/Os and current sense amplifiers output stage
11	PWM/IN1	PWM input or leg 1 input
12	DIR/IN2	Direction input or leg 2 input
13	SDO	SPI serial data output
14	CSN	SPI chip select not
15	CLK	SPI serial clock
16	SDI	SPI serial data input
17	DIAGN	Diagnostic output not
18	CSO2	Current sense amplifier 2 output
19	CSO1	Current sense amplifier 1 output
20	EN	Enable input
21	CSI1+	Current sense amplifier 1 positive input
22	CSI1-	Current sense amplifier 1 negative input

Pin	Name	Description
23	CSI2+	Current sense amplifier 2 positive input
24	CSI2-	Current sense amplifier 2 negative input
25	GH1	High-side gate of leg 1
26	SH1	High-side source of leg 1 and Low-side drain of leg 1
27	GL1	Low-side gate of leg 1
28	SL1	Low-side source of leg 1
29	SL2	Low-side source of leg 2
30	GL2	Low-side gate of leg 2
31	SH2	High-side source of leg 2 and Low-side drain of leg 2
32	GH2	High-side gate of leg 2
Exposed pad		Connection to GND is recommended

2 Device description

2.1 Supply pins

The device has three supply input pins:

- VS is the supply input of the internal regulator that supplies the logic.
- VDH is the supply input of the charge pump that supplies the gate drivers and the current sense amplifiers input stage.
- VDD is the supply input of the I/Os and the current sense amplifiers output stage. This voltage has to be the same as the application microcontroller supply (for example, 3.3 V or 5 V).

None of the supply input pins are internally protected against negative voltage. The VDD supply input can withstand a short to battery up to VDD absolute maximum rating as shown in Table 17.

2.1.1 VS overvoltage warning (VSOVW)

When the VS supply input voltage rises above the programmable overvoltage warning threshold (VSOVWT1 for OVTS=0 or VSOVWT2 for OVTS=1) for a time longer than t_{ovuv_filt}, then the corresponding overvoltage warning flag (VSOVW) is set, and no action is taken.

The overvoltage warning flag VSOVW can be cleared by an SPI “Read & Clear” command only if the VS overvoltage condition is no longer present, namely if VS<VSOVWT1 or VS<VSOVWT2, depending on the OVTS control bit value, for a time longer than the corresponding filtering time t_{ovuv_filt}.

2.1.2 VDH overvoltage (VDHOV)

When the VDH supply input voltage rises above the programmable overvoltage protection threshold (VDHOVT1 for OVTS=0 or VDHOVT2 for OVTS=1) for a time longer than t_{ovuv_filt}, then the corresponding overvoltage flag (VDHOV) is set, and to protect the application the charge pump is disabled and the external MOSFETs are switched off. In particular, the LS MOSFETs gate drivers are forced in sink switch mode to switch off actively the LS MOSFETs with the maximum available current, regardless of the programmed gate discharge current (SLEWDx control bits), whereas the HS MOSFETs gate drivers are forced in sink switch mode for 32 µs (up to 64 µs) and as long as VCP>VDH+3 V to switch off actively the HS MOSFETs with the maximum available current, regardless of the programmed gate discharge current. Once the 32 µs (up to 64 µs) are over or VCP<VDH+3 V the HS MOSFETs gate drivers are disabled leaving just an internal resistive connection (RGSHx) between gate and source of the MOSFETs. The charge pump is automatically enabled once the VDH falls back below the overvoltage protection threshold (VDHOVT1 for OVTS=0 or VDHOVT2 for OVTS=1) for a time longer than the corresponding filtering time t_{ovuv_filt}, while the LS MOSFETs gate drivers remain in sink switch mode and the HS MOSFETs gate drivers remain disabled until the VDHOV flag is cleared.

The overvoltage protection flag VDHOV can be cleared by an SPI “Read & Clear” command only if the VDH overvoltage condition is no longer present, namely if the foresaid condition that automatically enables the charge pump is fulfilled.

2.1.3 VDH undervoltage (VDHUV)

When the VDH supply input voltage falls below the undervoltage protection threshold (VDHUV) for a time longer than t_{ovuv_filt}, then the corresponding undervoltage flag (VDHUV) is set, and to protect the external power stage the external MOSFETs are switched off. In particular, the LS MOSFETs gate drivers are forced in sink switch mode to switch off actively the LS MOSFETs with the maximum available current, regardless of the programmed gate discharge current (SLEWDx control bits). The HS MOSFETs gate drivers are forced in sink switch mode, as long as VCP>VDH+3 V, otherwise the HS MOSFETs gate drivers are disabled and the HS MOSFETs are passively switched off through the internal resistive connection between gate and source (RGSHx). The gate drivers come out of forced sink switch mode/disabled mode once the undervoltage flag VDHUV is cleared. The under-voltage flag VDHUV can be cleared by an SPI “Read & Clear” command only if the VDH undervoltage condition is no longer present, namely if VDH>VDHUV for a time longer than the corresponding filtering time t_{ovuv_filt}.

2.1.4 VDD overvoltage (VDDOV)

When the VDD exceeds the V_{DDOV} threshold for a time longer than t_{ovuv_filt}, then the corresponding overvoltage flag (VDDOV) is set, and to protect the application all the gate drivers are forced in sink switch mode to switch off actively all the MOSFETs with the maximum available current, regardless of the programmed gate discharge current (SLEWDx control bits). The gate drivers come out of forced sink switch mode once the overvoltage flag VDDOV is cleared. The overvoltage flag VDDOV can be cleared by an SPI “Read & Clear” command only if the VDD overvoltage condition is no longer present, namely if VDD<VDDOV for a time longer than the corresponding filtering time t_{ovuv_filt}. The VDD overvoltage protection aims at making the application robust against VDD short to battery.

2.1.5 Digital input/output overvoltage (DIOOV)

When the voltage at any of the digital input/output pins listed below exceeds the V_{DIOOV} threshold for a time longer than t_{ovuv_filt}, then the corresponding overvoltage flag (DIOOV) is set, and to protect the application all the gate drivers are forced in sink switch mode to switch off actively all the MOSFETs with the maximum available current, regardless of the programmed gate discharge current (SLEWDx control bits). The gate drivers come out of forced sink switch mode once the overvoltage flag DIOOV is cleared. The overvoltage flag DIOOV can be cleared by an SPI “Read & Clear” command only if the digital input/output overvoltage condition is no longer present namely if VDIO<VDIOOV for a time longer than the corresponding filtering time t_{ovuv_filt}. The digital input/output overvoltage protection aims to make the application robust against digital input/output pins short to battery. The digital input/output pins monitored for overvoltage events are: PWM/IN1, DIR/IN2, DIAGN, CSO1, CSO2, CSN, SDI, SDO, CLK. Any overvoltage detection affecting the device digital output pins DIAGN and SDO will not affect/propagate internally to VDD. Anyhow, all the digital input/output pins, FSINB pin and EN pin included, can withstand a short to battery up to the related absolute maximum rating (see Table 17).

2.1.6 Power-on reset (POR)

The device gets out of standby mode to get into active mode as soon as the EN pin is high, the VDD is above V_{DDPOR_OFF} and the VS is above V_{SPOR_OFF}.

If either the VDD falls below V_{DDPOR_ON} or the VS falls below V_{SPOR_ON} with the EN pin still high, the device experiences a power-on reset and enter in standby mode. In standby mode the gate drivers and the charge pump are switched off, leaving just the internal resistive link between gate and source at each MOSFET (RGSHx and RGSLx). Besides, the content of all the registers is reset to default value. Once out of standby mode the global status byte RSTB bit will be set indicating that all the device registers have been reset to default value. This bit is automatically cleared by any valid SPI communication frame.

2.2 Standby mode (EN)

The L99H92 is enabled/disabled by pulling the EN input pin high/low. If VDD > V_{DDPOR_OFF}, VS>V_{SPOR_OFF} and EN input pin is high, the device enters in active mode. If any of the above conditions is not met, the device will remain in standby mode. When the EN input pin is left floating, because of the internal pull-down current (IIN), the device enters (if not already) in standby mode minimizing its current consumption. In standby mode the minimum current drawn by VS, less than 5 µA (I_{Sq}) for CSN = high (SDO in tristate), can be achieved by pulling the EN input pin low. Besides, in standby mode, the gate drivers together with the charge pump are switched off. All the MOSFETs are passively switched off by the internal resistive link between gate and source present at each MOSFET (regardless of the control input pins PWM/IN1, DIR/IN2 and FSINB logic levels), and all the registers are reset to default values. Out of standby mode the device diagnostic is available and all the operations on the device registers are available as well.

2.3 Active mode (OUTE)

As soon as the EN pin is high, the VDD is above V_{DDPOR_OFF} and the VS is above V_{SPOR_OFF} the device comes out of standby mode to go in active mode. In active mode the device diagnostic is available.

In active mode with no faults, the charge pump is enabled, and the gate drivers are enabled as long as the OUTE control bit is set. Instead, if the OUTE control bit is reset, then all the gate drivers are disabled and all the MOSFETs are switched off passively through the internal resistive connection between gate and source present at each MOSFET. In active mode with no fault and with OUTE set, the MOSFETs to be turned on are controlled through the combination of the input signals PWM/IN1, DIR/IN2 and the control bits INPMODE, AFWE and FWS.

2.4 Thermal warning and thermal shutdown (TW/TSD)

When the device junction temperature rises above the T_{jTW_ON} threshold for a time longer than $t_{fTjTW/TSD}$, then the temperature warning flag TW is set and no action is taken. The TW flag can be cleared by an SPI “Read & Clear” command only if the thermal warning condition is no longer present, namely if $T_j < T_{jTW\_OFF}$ for a time longer than the corresponding filtering time $t_{fTjTW/TSD}$.

When the junction temperature rises above the T_{jSD_ON} threshold for a time longer than $t_{fTjTW/TSD}$, then the thermal shutdown flag TSD is set and the external MOSFETs, together with the charge pump are switched-off to protect the device. In particular, the LS MOSFETs gate drivers are forced in sink switch mode to switch off actively the LS MOSFETs with the maximum available current, regardless of the programmed gate discharge current (SLEWDx control bits). The HS MOSFETs gate drivers are forced in sink switch mode for 32µs (up to 64 µs) and as long as VCP>VDH+3 V to switch off actively the HS MOSFETs with the maximum available current, regardless of the programmed gate discharge current. Once the 32 µs (up to 64 µs) are over or VCP<VDH+3 V the HS MOSFETs gate drivers are disabled leaving just an internal resistive connection between gate and source of the HS MOSFETs.

The LS gate drivers remain in sink switch mode and the HS gate drivers remain disabled together with the charge pump until the TSD flag is cleared.

The TSD flag can be cleared by an SPI “Read & Clear” command only if the thermal shutdown condition is no longer present, namely if $T_j < T_{jSD\_OFF}$ for a time longer than the corresponding filtering time $t_{fTjTW/TSD}$.

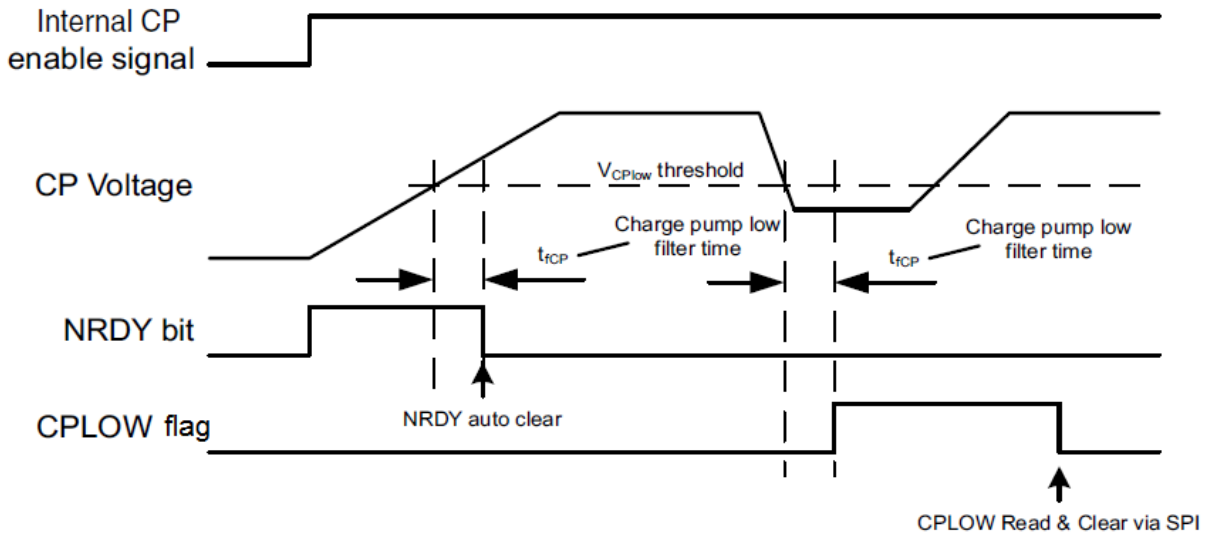
2.5 Charge pump (CPOUT)

The dual stage charge pump uses two external flying capacitors, which are switched at the frequency f_{CP}, and one output capacitor connected between the CPOUT pin and the VDH pin. The output of the charge pump has a current limitation (ICP_lim). The NRDY status bit indicates that the charge pump is still not ready to provide enough driving voltage to the gate drivers. This status bit is set during any charge pump startup event because of the device transition from standby mode to active mode or because of the charge pump being enabled once the fault condition/flag that disabled the charge pump is no longer present/set. While the NRDY status bit is set the gate drivers are disabled. The NRDY status bit is automatically cleared once the charge pump output voltage is no longer below the low voltage threshold (V_{CP_low}) for a time longer than the t_{CP} filtering time. Out of standby mode and without any fault the charge pump is enabled. In standby mode, after a thermal shutdown event detection, or in VDH overvoltage condition the charge pump is disabled. To enable the charge pump disabled by a thermal shut down event detection, the TSD flag has to be cleared. To enable the charge pump disabled by VDH overvoltage condition, it is enough that the VDH falls back below the overvoltage threshold (VDHOVT1 or VDHOVT2) for a time longer than the t_{ovuv_filt} filtering time.

After the charge pump startup, once the NRDY status bit is cleared, if the charge pump output voltage falls below the charge pump output voltage low threshold V_{CP_low} for a time longer than t_{CP}, then the CPLOW flag is set and the external MOSFETs are switched off. In particular, the LS MOSFETs gate drivers are forced in sink switch mode to switch off actively the LS MOSFETs with the maximum available current, regardless of the programmed gate discharge current (SLEWDx control bits). The HS MOSFETs gate drivers are forced in sink switch mode as long as VCP>VDH+3 V, otherwise the HS MOSFETs gate drivers will be disabled and the HS MOSFETs will be switched off passively through the internal resistive connection between gate and source (RGSHx). If the CP_LOW_CONFIG control bit is set to one, the CPLOW status flag becomes a status bit (set and reset automatically) and the gate drivers come out of forced sink switch mode automatically upon recovery from the charge pump low voltage condition. In this case, the status bit is automatically cleared as soon as the charge pump output voltage is no longer below the low voltage threshold for a time longer than t_{CP}. If the CP_LOW_CONFIG control bit is set to zero, the gate drivers come out of forced sink switch mode only once the charge pump low voltage flag CPLOW is cleared via SPI. The charge pump low voltage flag CPLOW can be cleared by an SPI “Read & Clear” command only if the charge pump low voltage condition is no longer present, namely if $VCP > V_{CP\_LOW}$ for a time longer than t_{CP}.

To reduce electromagnetic emissions, the charge pump frequency dithering is enabled by default. However, the dithering can be disabled through the control bit CPFDD.

Figure 4. **NRDY status bit and CPLOW flag**



2.6 Gate drivers

2.6.1 Outputs driving signals (PWM/IN1 and DIR/IN2)

When the OUTE control bit is reset with the FSINB pin high, all the gate drivers are disabled and the turned on MOSFETs are passively shut off through the internal resistance connected between gate and source of each MOSFET (RGSHx and RGSLx). Regardless of the OUTE control bit value, when the FSINB pin is pulled low all the MOSFETs are actively shut off by the gate drivers forced in sink switch mode.

Once the OUTE control bit is set and the FSINB pin is high, the external MOSFETs are driven by the input pins PWM/IN1 and DIR/IN2. Both input pins, PWM/IN1 and DIR/IN2, have an internal pull-down current (IPWM_in and IDIR_in) to put the outputs in a well-known condition in case any of the pins will no longer be driven by the microcontroller. Depending on the value of the INPMODE control bit, the device can work as full-bridge driver or dual half-bridge driver:

- If INPMODE = 0 (default value), the device works in full-bridge mode. In this case the active full-bridge diagonal, fixing the rotational direction of the motor is selected by DIR/IN2 input while the driving PWM signal has to be applied to PWM/IN1 input.

Depending on the active free-wheeling enable control bit value (AFWE) and the freewheeling selection control bit value (FWS), four different freewheeling strategies are available: active or passive and freewheeling on either high-side or low-side MOSFETs. The *DIR input pin sets the active diagonal. The AFWE control bit enables or disables active free-wheeling and the FWS control bit sets the free-wheeling path (HS or LS).*

Table 2. **Truth table**

Device in active mode with INPMODE=0 (FULL-BRIDGE MODE)									
Inputs						Outputs (in case of no faults)			
OUTE bit	AFWE bit	FWS bit	FSINB pin	DIR pin	PWM pin	HS1	LS1	HS2	LS2
x	x	x	0(1)	x	x	OFF	OFF	OFF	OFF
0	x	x	1	x	x	OFF(2)	OFF(2)	OFF(2)	OFF(2)
1	0	0	1	0	0	OFF	OFF	OFF	ON
1	x	x	1	0	1	ON	OFF	OFF	ON
1	0	1	1	0	0	ON	OFF	OFF	OFF

Device in active mode with INPMODE=0 (FULL-BRIDGE MODE)									
Inputs						Outputs (in case of no faults)			
OUTE bit	AFWE bit	FWS bit	FSINB pin	DIR pin	PWM pin	HS1	LS1	HS2	LS2
1	1	0	1	x	0	OFF	ON	OFF	ON
1	1	1	1	x	0	ON	OFF	ON	OFF
1	0	0	1	1	0	OFF	ON	OFF	OFF
1	x	x	1	1	1	OFF	ON	ON	OFF
1	0	1	1	1	0	OFF	OFF	ON	OFF

1. *In this case, when the FSINB input pin goes from high to low, the device moves from active mode to fail-safe mode. In fail-safe mode the OUTE control bit is automatically reset and all the gate drivers are forced in sink switch mode so that all the MOSFETs are actively switched off with the maximum available discharge current.*
2. *In this case, the MOSFET is passively switched off through the internal resistive connection between gate and related source. In all the other cases where the MOSFET is off, it is actively switched off and forced off by the gate driver working in sink switch mode.*

- If INPMODE = 1, the device works in dual half-bridge mode. The two half-bridges can be driven separately by IN1 and IN2 input pins and can be individually disabled through DIS1 and DIS2 control bits.

Table 3. Dual half-bridge mode

Device in active mode with INPMODE=1 (DUAL HALF-BRIDGE MODE)				
Inputs			Outputs (in case of no faults); x=1,2	
FSINB	OUTE bit	DISx bit	HSx	LSx
1	1	0	Inx	$\overline{Inx}$
1	0	x	OFF(1)	OFF(1)
All the other cases			OFF	OFF

1. *In this case, the MOSFET is passively switched off through the internal resistive connection between gate and related source. In all the other cases where the MOSFET is off, it is actively switched off and forced off by the gate driver working in sink switch mode.*

"Inx" means ON if logic level on Inx pin input is high and vice versa." $\overline{Inx}$" means OFF if logic level on Inx pin input is high and vice versa (x=1,2).

2.6.2 Slew rate control (SLEW)

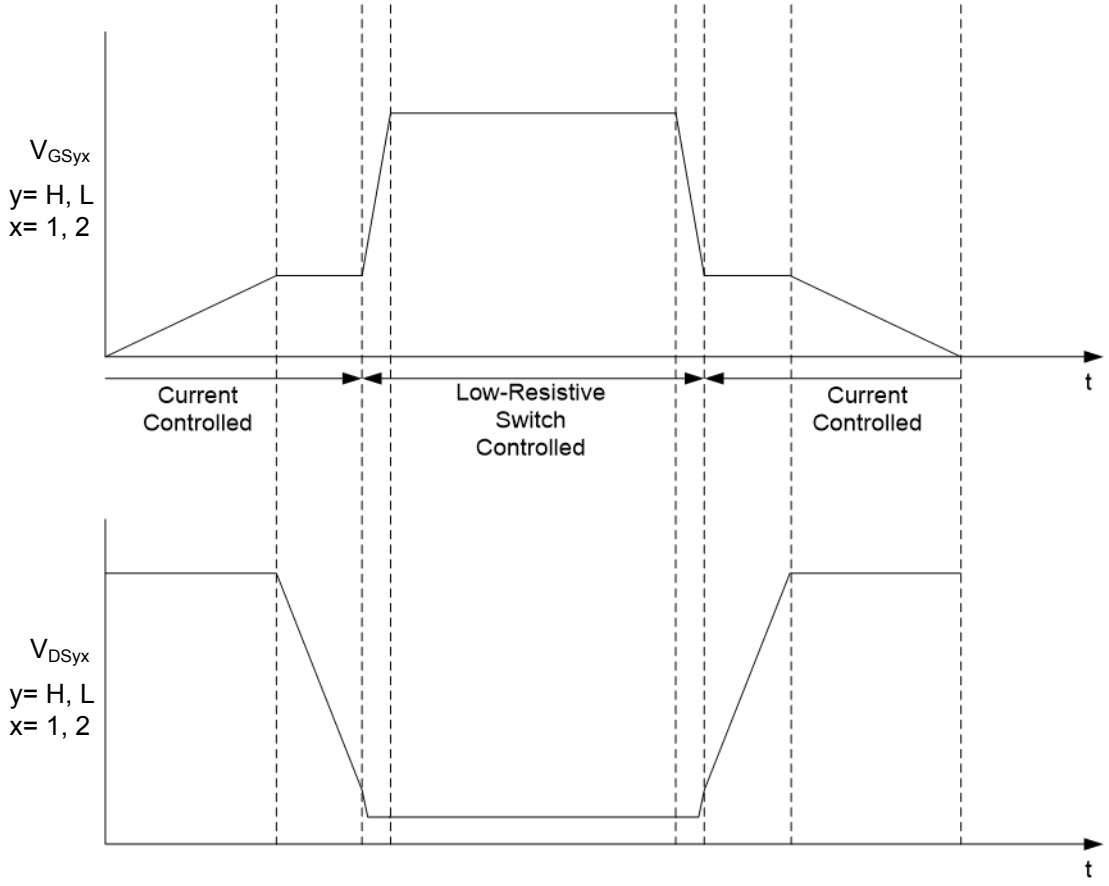
The rising and falling voltage slopes at the outputs can be controlled through slew rate control bits. When the SLEWzx control bits are all set to zero the gate drivers will work in switch mode providing the maximum available current to charge/discharge the MOSFETs input capacitance. The maximum available source/sink current in switch mode is internally limited (IGHx(Ch) and IGLx(Ch)). If any value different from zero is programmed, then the gate drivers will work as current source, instead of low impedance switch, as long as during the MOSFET turning on/off the drain-source voltage over the MOSFETs is above/below the switch threshold (VDSHxfSW and VDSHxrSW). Once the switch threshold is reached, the drivers will work in switch mode. The gate drivers source (charge) and sink (discharge) currents can be independently programmed through dedicated control bits in order to have different output voltage slopes during the turning on and the turning off of the MOSFETs. The MOSFETs gate charging current is programmed using the control bits SLEWCx[4:0], while the MOSFETs gate discharging current is programmed using the control bits SLEWDx[4:0]. The gate current is set depending on the SLEWzx control bits value according to the formula:

$$I_{GATE} = \frac{SLEWzx[4:0]}{31} * I_{GATEMAX} \quad (1)$$

SLEWzx can be either SLEWDx or SLEWCx, while $I_{GATEMAX}$ can be either $I_{GLxymax}$ or $I_{GHxymax}$ (y=r for source current; y=f for sink current).

Programming SLEWzx[4:0] to 0 disables the slew rate control and enables gate driving through the low-impedance switch during the entire turning on/off process.

Figure 5. **Full-bridge GSHx and GSLx slopes**



2.6.3 Short circuit detection / drain-source monitoring (DSHS/DSLS)

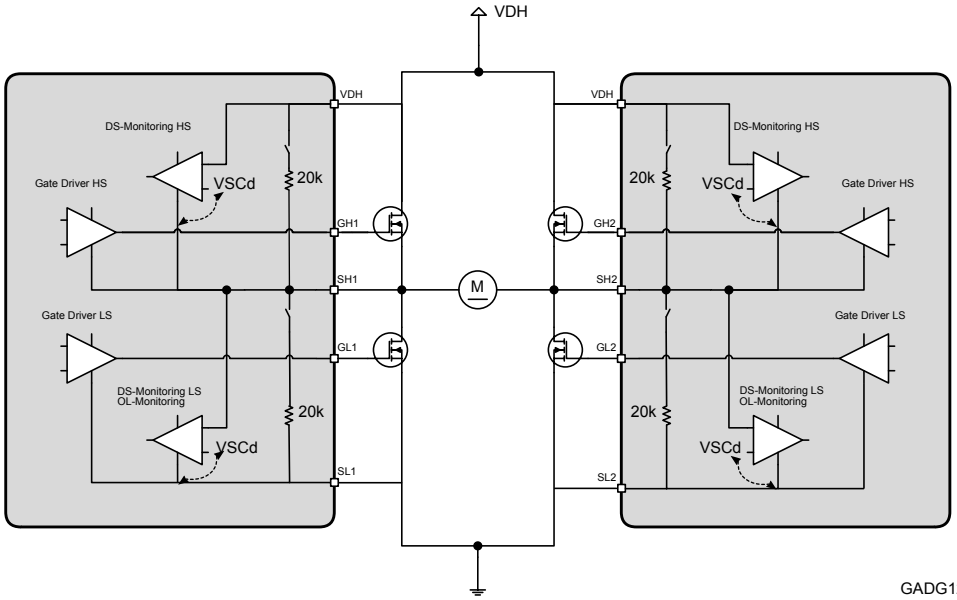
The voltage-drop over each MOSFET is sensed and compared to a programmable threshold to detect an overcurrent condition. This monitoring is active only on the MOSFETs driven to be turned on. In dual half-bridge mode, each half-bridge has its own programmable threshold (DSMONx[2:0]), blanking time (DSBTx[2:0]) and filtering time (FTx[1:0]). As soon as the gate driver starts to turn on a MOSFET, the corresponding drain source monitoring comparator output is masked for the programmed blanking time to give time to the MOSFET to turn on. Besides the blanking time, a filtering time is also present to filter noise. Both values have to be chosen depending on the application.

If the voltage-drop over the driven MOSFET exceeds the programmed threshold voltage V_{SCdx} (DSMON1[2:0] control bits for full-bridge or leg 1 and DSMON2[2:0] control bits for leg 2 in dual half-bridge mode) for a time longer than the programmed filtering time (and the programmed blanking time, where applicable), then:

- with DSMON_CONFIG control bit set to zero the gate drivers belonging to the faulty leg are forced in sink switch mode to switch off actively the half-bridge MOSFETs with the maximum available current, regardless of the programmed gate discharge current (SLEWDx control bits)
- for INPMODE set to zero and DSMON_CONFIG control bit set to one all the gate drivers are forced in sink switch mode to switch off actively all the full-bridge MOSFETs.

In any case, the drain source monitoring flag DSHSx or DSLSx of the MOSFET detecting the fault is set. The drain-source monitoring flags have to be cleared through SPI to reactivate the affected half-bridge/full-bridge gate drivers that are forced in sink switch mode. The drain-source monitoring flag DSHSx/DSLSx can be cleared by an SPI “Read & Clear” command only if the fault condition is no longer present.

Figure 6. Full-bridge drain-source monitoring diagnosis



2.6.4 Programmable cross current protection time (DT)

In any input mode (dual half-bridge mode or full-bridge mode), the device automatically adds a dead-time between the turn-off of a MOSFET and the turn-on of the complementary one (that is, the other MOSFET of the same leg) to avoid cross-conduction in any of the half-bridges.

In dual half-bridge mode, each half-bridge dead-time t_{DT} (from t_{DT0000} to t_{DT1111}) is independently configurable by control bits DT1[3:0] and DT2[3:0]. Instead, in full-bridge mode, the dead time of both half-bridges is set by control bits DT1[3:0].

2.7 Diagnostic in off-mode (O1DS/O2DS)

Two off-state diagnostic comparators compare the drop between each half-bridge output (SHx pin) and related LS MOSFET source (SLx) to a programmable threshold , while all the transistors are switched off. Possible system faulty conditions such as open-load, output shorted to ground or to battery, before even turning on any of the MOSFETs can be so detected.

The outputs of the off-state diagnostic comparators are always available (except in standby mode) and can be read through O1DS and O2DS status bits of the status register DSR2.

When the OUTE control bit set, the O1DS and the O2DS status bits provide the not filtered SH1 and SH2 output logic levels respect to the threshold, selected by the DSMONxy control bits, respectively. In all the other cases (except in standby mode, where everything is disabled) the O1DS and the O2DS status bits provide the not filtered SH1 and SH2 output logic levels respect to the threshold, selected by the OLTHH control bit, respectively. To run off-state diagnostic the device has to be in off-state diagnostic mode.

To enter in off–state diagnostic mode at least the OLH1L2 control bit or the OLH2L1 control bit has to be set to one with the device OUTE control bit set to zero and CSA must be disabled. To exit from off–state diagnostic mode either the OUTE control bit is set to one or both the OLH1L2 and the OLH2L1 are set to zero. In off–state diagnostic mode a pull-up resistor is connected to one of the half-bridge outputs or to both and two pull-down resistors are connected to the two half-bridge outputs.

Considering that the pull-up resistance is the same as the pull-down resistances, the VDS of the two low side transistors (that is, the two half-bridge outputs) is expected to be equal to 1/3 VDH if a low resistive load is connected between the two legs.

On the contrary if the VDS of any of the two low sides is lower than 1/6 VDH (OLTHH=0) or higher than 5/6 VDH (OLTHH=1), then a faulty condition must be present.

Below figures and table summarize the possible faulty conditions and related OxDS status bits values.

Figure 7. **Full-bridge open-load detection (no open-load detected)**

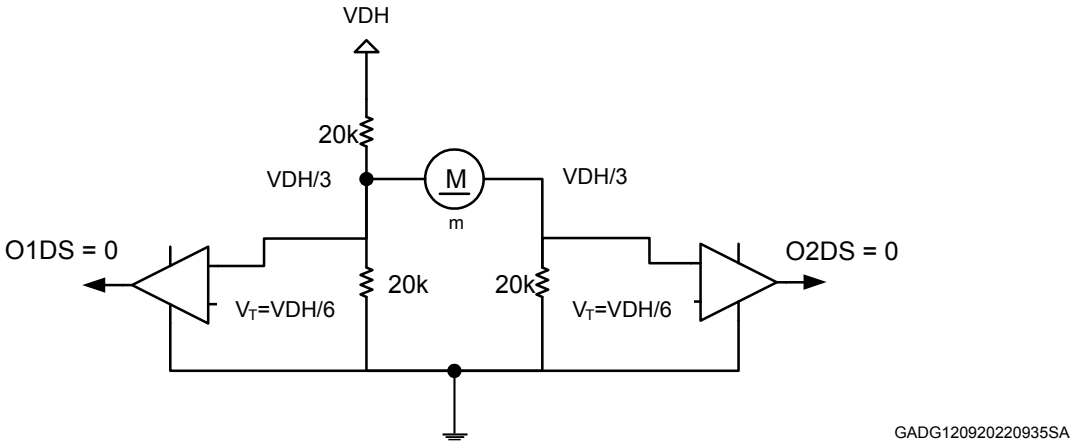


Figure 8. **Full-bridge open-load-detection (open-load detected)**

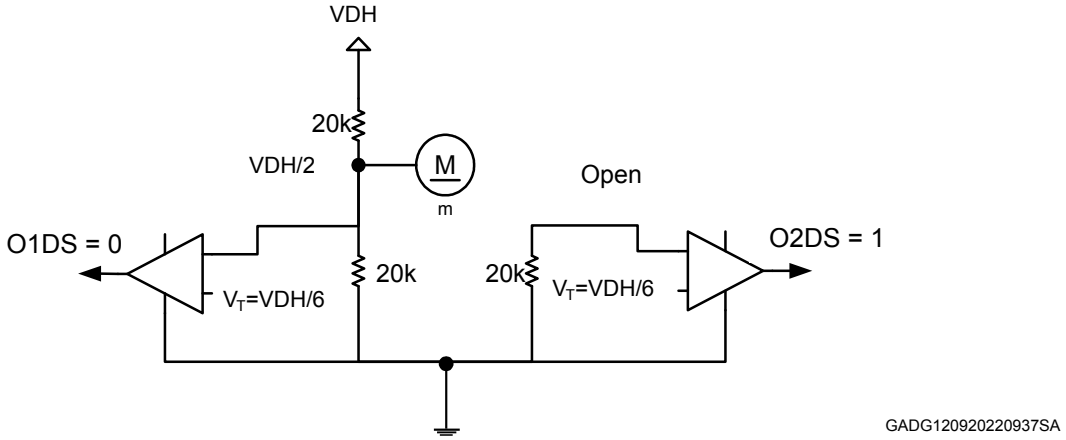


Figure 9. **Full-bridge open-load-detection (short to ground detected)**

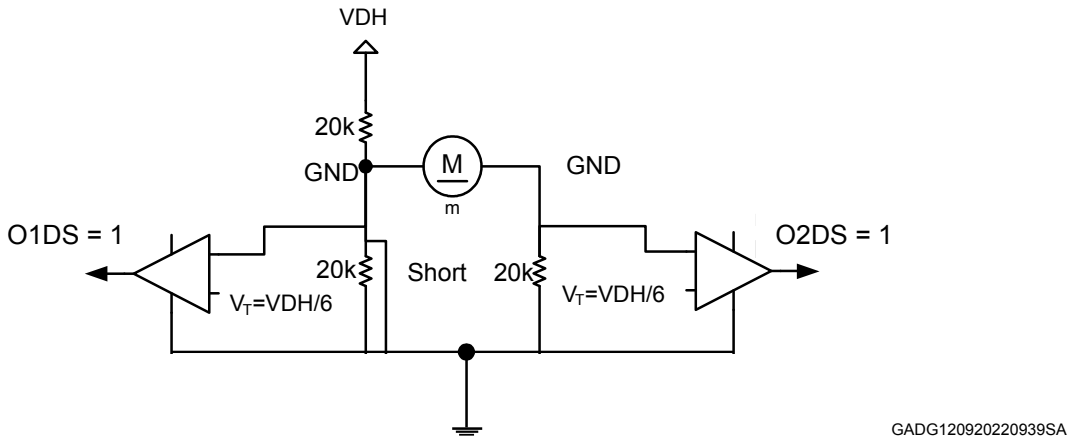
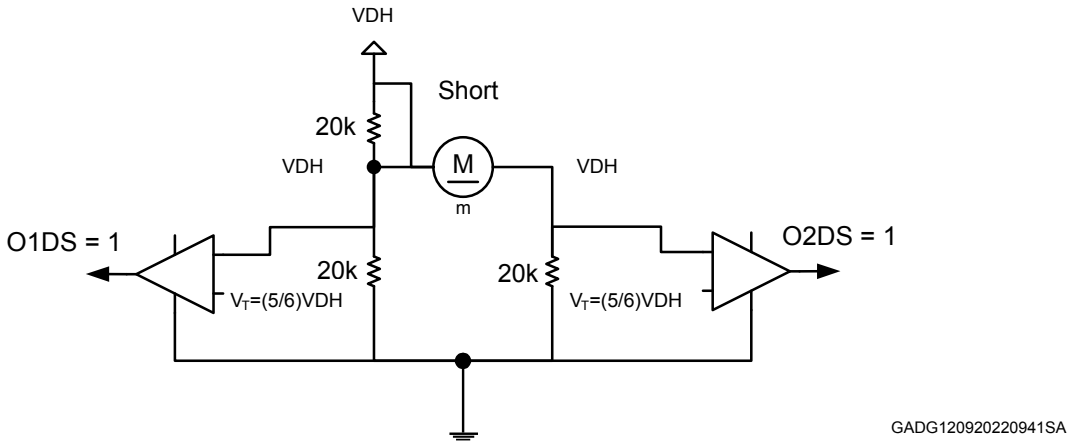


Figure 10. **Full-bridge open-load-detection (short to VDH detected)**



In case of short to VDH detection, achieved for OLTHH=1, the outputs of the two off-state diagnostic comparators are inverted to be compliant to Table 4.

Table 4. **Full-bridge monitoring in off-mode**

Control bits			Failure bits		Comments
OLH1L2	OLH2L1	OLTHH	O1DS	O2DS	
0	0	0	0	0	Off-state diagnostic disabled
1	0	x	0	0	No open-load detected
1	0	0	0	1	Open-load SH2
1	0	0	1	1	Short to GND
1	0	1	1	1	Short to VDH
0	1	x	0	0	No open-load detected
0	1	0	1	0	Open-load SH1
0	1	0	1	1	Short to GND
0	1	1	1	1	Short to VDH

What reported in this chapter applies only to single motor full-bridge configuration; that is, the case where one full-bridge drives only one motor.

In dual half-bridge mode (INPMODE = 1), the device can still detect an open-load condition.

In off-state diagnostic mode, it is recommended to wait at least 2.5 ms, starting from any change of OLH2L1, OLH1L2 or OLTHH control bits, before reading stable O1DS and O2DS status bits values.

2.8 Fail-safe output switch-off input not pin (FSINB)

The L99H92 features an asynchronous, logic independent fail-safe input pin working as a redundant switch-off path for all MOSFETs. The fail-safe input not pin (FSINB), active low, has an internal pull-down resistance RFSINB. As soon as the FSINB pin falls below the VFSINBLTH threshold for a time longer than t_{FSINB_filt}, the FSINLL status bit together with the FSIN status bit are set and the device is put in fail-safe mode. In fail-safe mode the OUTE control bit is reset and the gate drivers are forced in sink switch mode to switch off actively all the MOSFETs with the maximum available current, regardless of the programmed gate discharge current (SLEWDx control bits). As long as the FSINB input pin is low, the gate drivers are forced in sink switch mode and the OUTE control bit is forced to zero. For functional safety reasons, the FSINHS1,2 and the FSINLS1,2, status bits indicate whether the HS1,2 and the LS1,2, gate drivers have been put successfully in sink switch mode or not, because of the FSINB pin pulled low. Once the FSINB pin has been pulled low, in order to reactivate again the gate drivers that are forced in sink switch mode, the FSINB pin has to rise above the VFSINHTH threshold for a time longer than the filtering time. All the FSINHSx and the FSINLSx status bits have to go back to zero (indicating that all the gate drivers came out of forced sink switch mode and making the device come out of fail-safe mode) and then the OUTE control bit has to be set back to one via SPI. In case where at least one of the status bits FSINHSx or FSINLSx remains set, indicating that at least one gate driver did not come out of forced sink switch mode, the device remains in fail-safe mode. With the FSINB pin high and the OUTE control bit reset, the gate drivers are disabled, leaving just a resistive link between gate and source of each MOSFET.

The FSINB input pin status can be read, but not cleared, through FSINLL status bit. The FSIN status bit, linked to the global status byte fail-safe bit (FS), is the logical OR of the following status bits: FSINLL, FSINHS1, FSINLS1, FSINHS2, and FSINLS2. The fail-safe input pin acts just on the gate drivers and on the OUTE control bit.

2.9 Diagnostic not output (DIAGN)

The microcontroller can use the DIAGnostic not (DIAGN) output pin, active low, to detect a device fault, including a device power-on-reset event. The purpose of the DIAGN output pin is to warn immediately the microcontroller that a new fault has been detected by the device, without the need of periodic SPI transfers. The DIAGN output pin has an internal weak pull-up resistance (RDIAGN). The logic level signal at the pin is the logical NOR combination of all the status flags and status bits linked to the pin through the DIAGCR control register, together with the global status byte RSTB bit. Once the device comes out of standby mode, the DIAGN pin is pulled low because of the global status byte RSTB bit. If just the global status byte RSTB bit is set, any valid SPI communication frame clears the RSTB bit pulling up the DIAGN pin. Any read access to the DSR1 register resets this signal to high level, until an error coming from a new source occurs pulling again the pin low. If a fault coming from a new error source occurs during the read access to the DSR1 register, the DIAGN output pin remains low (this avoids any loss of information since the new error source status flag/bit will not be reported by the concomitant read access, but a new read access would be required). Even if a read operation of the status register should always come before a Read & Clear operation, any Read & Clear operation of status register DSR1 will pull the DIAGN pin high. If a new source of fault triggers an error during the Read & Clear access to the DSR1 register, the Read & clear operation will not pull the DIAGN pin high at the CSN rising edge of the DSR1 register Read & Clear operation (this will avoid any loss of information since the new error source status flag/bit will not be reported by the concomitant Read & Clear access, but a new read or Read & Clear access would be required).

2.10 Current monitors

The current sense amplifiers (CSA1 and CSA2) are designed for current sensing in automotive applications. They are independent, bidirectional, single-supply differential amplifiers with a wide input common mode voltage range (VICM). They support high-side current sensing, low side-current sensing and in-line current sensing through two sensing resistors.

A gain of 100, 50, 20 or 10 is independently SPI programmable for each CSA. Since the CSAs have a trans-conductance input stage, input series resistors (for filtering etc.) should not exceed 50 Ω to keep the additional gain error below 1%.

The CSO outputs are compliant to the VDD power supply rail and have a programmable offset set by CSA1OO and CSA2OO control bits. If these bits are reset, the output offset is set to VO0, otherwise it is set to VO1. The current sense amplifiers input stage is supplied by the charge pump. When the charge pump is disabled, the CSAs is disabled as well.

By default, both current sense amplifiers are enabled. To reduce current consumption both of them can be disabled independently through control bits DCSA1 and DCSA2.

2.11 Window watchdog (WDG)

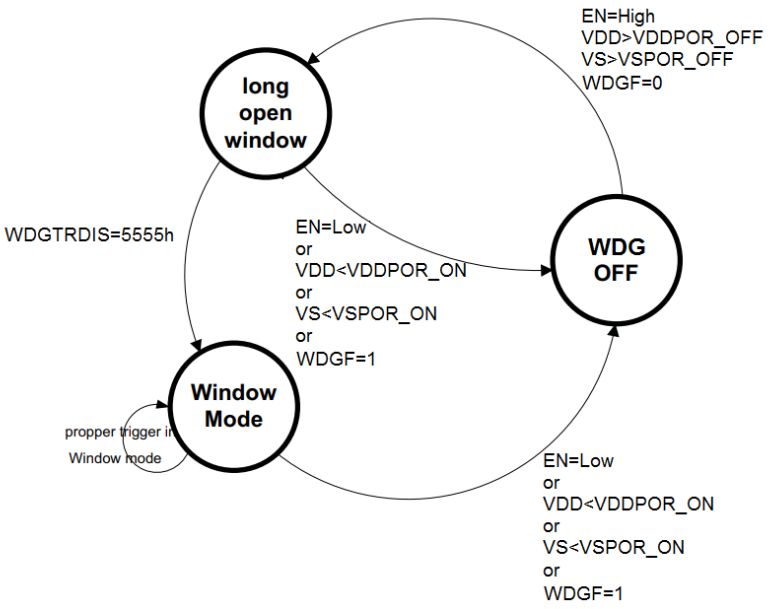
Out of standby mode, the L99H92 watchdog monitors the microcontroller status within a periodic window.

By default, as soon as the device enters in active mode, the watchdog is enabled and starts running with a long open window (t_{LOW}). The long open window provides more time to the microcontroller for the L99H92 initialization and allows the watchdog disabling procedure to be run, when no watchdog is required by the application. To trigger the watchdog for the first time during a Long Open Window (LOW), the microcontroller has to write 5555h to the watchdog trigger/disable register (WDGTRDIS) before the end of the long open window. After the first valid watchdog trigger, the watchdog will enter in window mode. In window mode the microcontroller has to serve the watchdog by alternating the watchdog trigger bits (that is, 2AAAh,5555h,…) of the watchdog trigger/disable register (WDGTRDIS) within the watchdog open window (t_{CW} and t_{WDP}). Any correct watchdog trigger SPI frame will immediately start a new window.

In case of a watchdog failure (root cause can be any watchdog trigger outside the open window; invalid or unexpected watchdog trigger bits value; any watchdog timeout; any disabling procedure out of the LOW; any wrong disabling procedure during the LOW) will set the WDGF flag, stop the watchdog and put the device in fail-safe mode. In fail-safe mode the OUTE control bit is reset and the gate drivers are forced in sink switch mode to switch off actively all the MOSFETs with the maximum available current, regardless of the programmed gate discharge current (SLEWDx control bits). To reactivate the gate drivers that are forced in sink switch mode, the WDGF flag has to be cleared via SPI (clearing the WDGF flag makes the device come out of the fail-safe mode and makes the watchdog start again with a long open window) and then the OUTE control bit has to be set to one via SPI. As long as the device is in fail-safe mode (WDGF=1), the OUTE control bit is reset and cannot be set via SPI. Once the watchdog starts running again with a long open window after coming out of the fail-safe mode, to enter in window mode the microcontroller has to write 5555h to the watchdog trigger/disable register (WDGTRDIS). To disable the watchdog, the microcontroller has to write a specific key, consisting in two consecutive valid SPI frames to be sent in the right order, to control register WDGTRDIS before the end of any long open window. Just one attempt to disable the watchdog is allowed per LOW, if not successful, a watchdog fault is generated, and it will no longer be possible to disable the watchdog until the next LOW. Any other SPI transfer between the two SPI frames carrying the key including an invalid SPI transfer generating an SPIE aborts the disable process and generates a watchdog fault (WDGF). Besides, the keys sent in the wrong order will not disable the watchdog and generate a watchdog fault as well. Once in window mode, it will no longer be possible to disable the watchdog until the next LOW. Any attempt to disable the watchdog outside the LOW will generate a watchdog fault (WDGF).

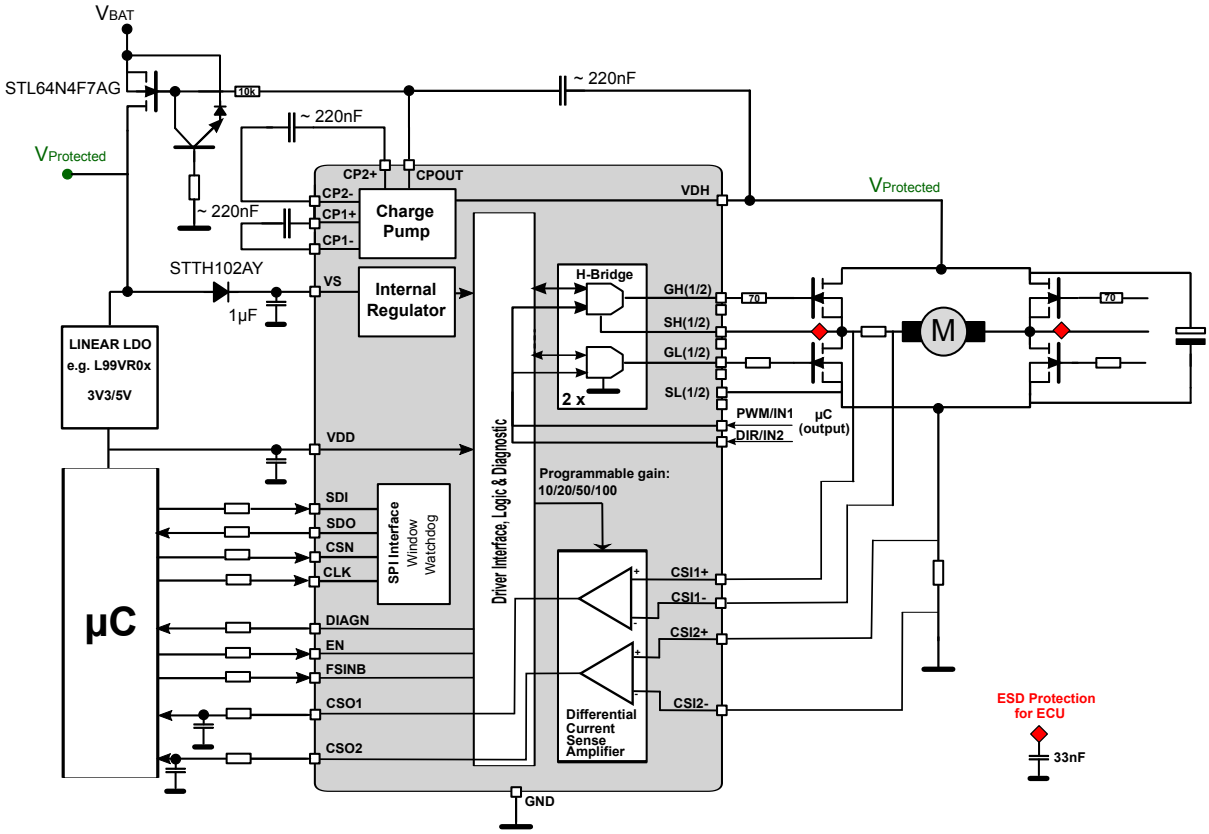
Any read access to the WDGTRDIS register provides information concerning the watchdog disabling procedure result together with the three least significant bits of the latest write operation performed on the same register.

Figure 11. Watchdog state diagram



3 Application

Figure 12. **Application schematic**



GADG120920220948SA

4 Serial peripheral interface (SPI)

A 24-bit SPI is used for bidirectional communication with the microcontroller.

The microcontroller SPI peripheral must run in the following configuration:

CPOL = 0 and CPHA = 0.

In this configuration the input data is sampled by the low to high transition of the serial clock CLK, and the output data is changed by the high to low transition of the serial clock CLK.

Any fault condition can be detected without even providing any serial clock CLK by setting CSN low. In fact, if CSN = 0, the serial data output SDO pin will reflect the global error flag (GSBN bit of the global status byte) of the device.

- Chip select not (CSN)

The CSN input pin is used to address the SPI communication with the device. When CSN is high, the output pin (SDO) is in high impedance. When CSN is low, the output pin (SDO) driver is enabled and a serial communication can start. The information transferred during CSN = 0 is called a communication frame.

If CSN = low for $t > t_{CSNfail}$ the SDO output will be switched into high impedance to allow SPI communications with other SPI nodes.

- Serial data in (SDI)

The SDI input pin is used to transfer data into the device. The data applied to the SDI will be sampled at the rising edge of the serial CLK signal and shifted into an internal 24 bit shift register. At the rising edge of the CSN signal the content of the shift register will be transferred to Data Input Register. The writing to the selected Data Input Register is enabled only if exactly 24 bits are transmitted within one communication frame (that is, CSN low). If more or less than 24 clock pulses are counted within one frame the complete frame will be ignored. This safety function is implemented to avoid an activation of the output stages by any wrong communication frame.

Note: Due to this safety functionality, daisy chaining is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected IC's is recommended.

- Serial data out (SDO)

The SDO output driver is activated by a logical low level at the CSN input and will go from high impedance to low or high level depending on the global error flag value (GSBN bit). The first falling edge of the CLK input after a high to low transition of the CSN pin transfers the next global status byte bit out. Each subsequent falling edge of the CLK shifts the following bits out.

- Serial clock (CLK)

The CLK input pin is used to synchronize the input and output serial bit streams. The data input (SDI) is sampled at the rising edge of the CLK and the data output (SDO) will change with the falling edge of the CLK. The SPI can work with a CLK frequency up to 4 MHz ($1/t_{CLK}$).

4.1 ST SPI 4.1

The ST-SPI is a standard used in ST automotive ASSP devices.

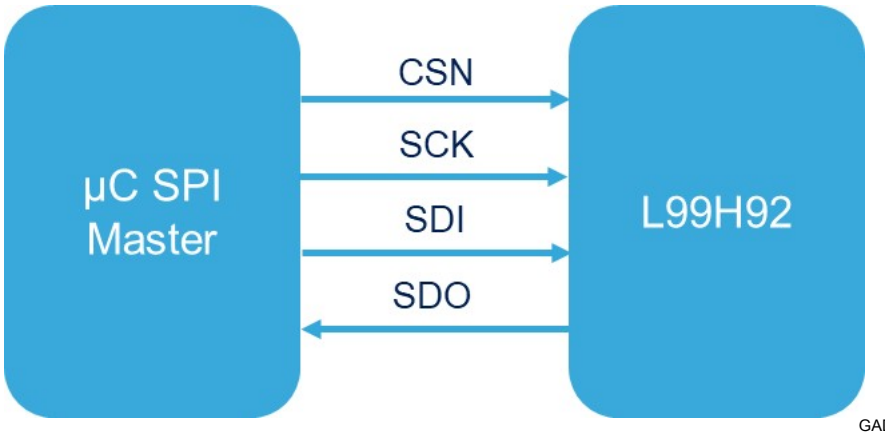
This chapter describes the SPI protocol standardization. It defines a common structure of the communication frames and defines specific addresses for product and status information.

The ST-SPI allows usage of generic software to operate the devices while maintaining the required flexibility to adapt it to the individual functionality of a particular product. In addition, fail-safe mechanisms are implemented to protect the communication from external influences and wrong or unwanted usage.

The device serial peripheral interface is compliant to the ST SPI standard rev. 4.1.

4.1.1 Physical layer

Figure 13. **SPI pins description**



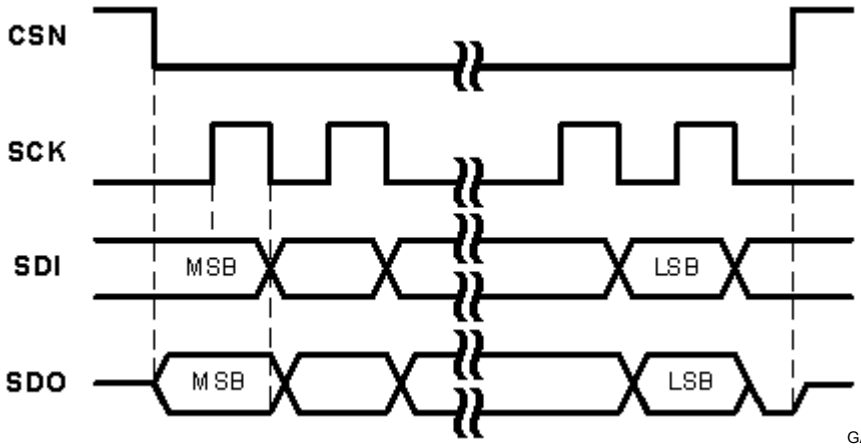
GADG120920220953SA

4.1.2 Clock and data characteristics

The ST-SPI can be driven by a microcontroller with its SPI peripheral running in the configuration:

- CPOL = 0
- CPHA = 0

Figure 14. **SPI signal description**



GADG120920220954SA

Any communication frame starts with the falling edge of the CSN (Communication Start). CLK has to be low.

The SDI data is then latched at the following rising CLK edges into the internal shift registers.

After *Communication Start* the SDO leaves 3-state mode and present the MSB of the data shifted out to SDO. At all following falling CLK edges, data is shifted out through the internal shift registers to SDO.

The communication frame is finished with the rising edge of CSN. If a valid communication took place (for example, correct number of CLK cycles, access to a valid address, no parity error), the requested operation according to the operating code will be performed (write or clear operation).

4.1.3 Communication protocol

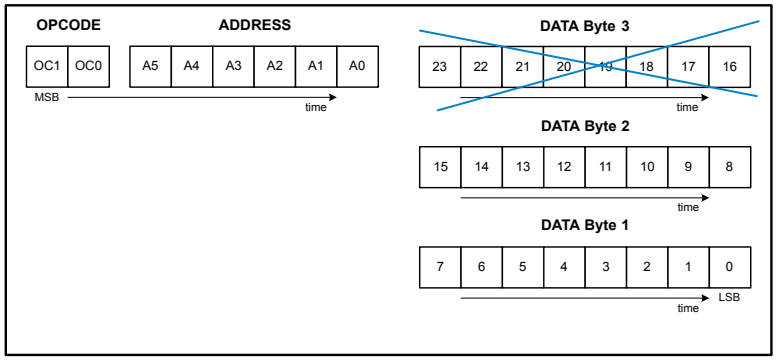
SDI frame

The device data-in frame consists of 24 bits (OpCode (2 bits) + Address (6 bits) + Data Byte 2 (8 bits) + Data Byte 1 (8 bits)).

The first two transmitted bits (MSB, MSB-1) contain the operation code, which represents the command/ instruction that will be performed. The following 6 bits (MSB-2 to MSB-7) represent the address on which the command/operation will be performed.

The subsequent two bytes contain the payload.

Figure 15. SDI frame



GADG120920221006SA

Operating code

The operating code is used to distinguish between different commands/operations on registers of the slave device.

Table 5. Operation codes

OC1	OC0	Description
0	0	Write command
0	1	Read command
1	0	Read & Clear command
1	1	Read device information command

Any ***Write command*** (with no parity error, no wrong address and no CLK count error) will modify the content of the addressed control register with the payload. Besides this, a shift out of the content (data present at *Communication Start*) of the addressed register is performed.

A ***Read command*** shifts out the data present in the addressed register at *Communication Start*. The payload data is ignored, and the data of the addressed register will not be modified. Moreover, a *Burst Read* can be performed.

A ***Read & Clear command*** (with no parity error, no wrong address and no CLK count error) will lead to a clear of addressed status bits. The bits to be cleared are defined first by address, second by payload bits set to '1'. Besides this, a shift out of the content (data present at *Communication Start*) of the register is performed.

Note: to avoid any loss of any reported status, it is recommended to clear just the status register bits, which are already reported in the previous communication frame (Selective Bitwise Clear).

Advanced operation codes

Two *Advanced Operation Codes* can be used to set all control registers to the default value and to clear all status registers by one single SPI frame respectively.

A *'set all control registers to default'* command is launched when an SPI frame with OpCode '11' and address '111111' is sent to the device.

A *'clear all status registers'* command is launched when an SPI frame with OpCode '10' and address'111111' is sent to the device.

Data-in payload

The *Payload* (Data Byte 1 to Data Byte 2) is the data transferred to the device with every SPI communication. The *Payload* always follows the OpCode and the Address bits.

For write access the *Payload* represents the new data written to the addressed register. For *Read & Clear* commands the *Payload* defines which bits of the addressed Status Register will be cleared. In case of a '1' at the corresponding bit position the status flag will be cleared.

For a Read Operation, the *Payload* is not used. For functional safety reasons it is recommended to set unused *Payload* to '0'.

SDO frame

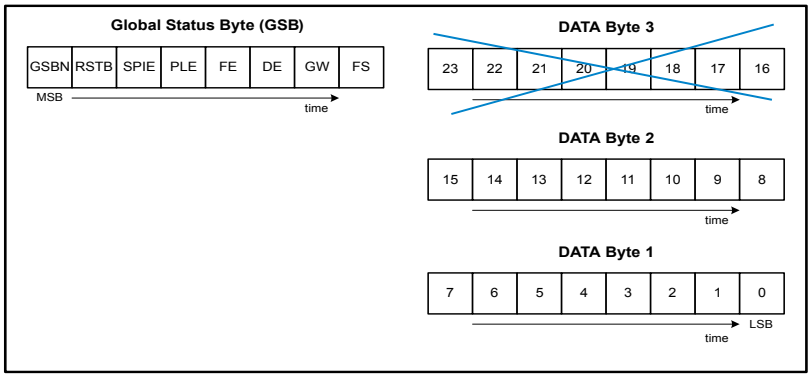
The data-out frame consists of 24 bits (GSB (8 bits) + Data Byte 2 (8 bits) + Data Byte 1 (8 bits)).

The first eight transmitted bits contain the device related status information and are latched into the shift register at the time of the *Communication Start*. These 8 bits are transmitted at every SPI transaction.

The subsequent bytes contain the payload data and are latched into the shift register with the eighth positive CLK edge.

This could lead to an inconsistency of data between the GSB and *Payload* due to different shift register load times. Anyhow, no unwanted status register clear should appear, as status information should just be cleared with a dedicated bit clear after.

Figure 16. SDO frame



GADG120920221019SA

Global status byte (GSB)

The global status byte bits, from Bit16 to Bit19, represent a logical OR combination of status flags and status bits located in the status register DSR1. Therefore, no direct Read & Clear command can be performed on these GSB bits.

Table 6. Global status byte

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
GSBN	RSTB	SPIE	-	FE	DE	GW	FS

Global status bit not (GSBN)

The GSBN is a logically NOR combination of global status byte bits from bit 16 to bit 22. This bit can also be used as *Global Error Flag* without starting a complete communication frame as it is directly present on SDO after pulling CSN low.

GSBN = 1 (No error)

GSBN = 0 (Error)

- **ReSeT bit (RSTB)**

The RSTB bit indicates that all the device registers have been reset to default. By default, it is set to one coming out from standby mode. It is reset automatically after any valid SPI communication frame.

- **SPI error bit (SPIE)**

The SPIE bit is a logical OR combination of all the errors related to a wrong SPI communication.

Besides, the CLK count, the CSN low timeout and the SDI stuck at errors, the parity error and the read/write from/to wrong address are reported here as well.

The SPIE bit is automatically cleared by any valid SPI communication frame.

- **Functional error bit (FE)**

The FE bit is a logical OR combination of errors coming from application specific functional items:

Overcurrent status flags (DSHSx, DSLSx)

Device error bit (DE)

The DE bit is a logical OR combination of errors related to device specific blocks:

- VDH overvoltage status flag (VDHOV)
- VDH undervoltage status flag (VDHUV)
- VDD overvoltage status flag (VDDOV)
- Thermal shutdown status flag (TSD)
- Charge pump not ready status bit (NRDY)
- Charge pump low status flag/bit (CPLOW)
- Digital input/output overvoltage status flag (DIOOV)

Global warning bit (GW). The GW bit is a logical OR combination of all warning flags:

- Thermal warning status flag (TW)
- VS overvoltage warning status flag (VSOVW)

Fail-safe bit (FS). The FS bit indicates that the device was forced into fail-safe mode due to watchdog failure or due to FSINB input pin pulled low.

- Watchdog fault status flag (WDGF)
- Fail-safe input not status bit (FSIN)

Data-out payload

The *Payload* (data Byte1 and 2) is the data transferred from the slave device with every SPI communication to the master device (in-frame-response). The *Payload* always follows the global status byte.

4.1.4 Address definition

Table 7. Address definition - device application access

Device application access	
Operating code	
OC1	OC0
0	0
0	1
1	0

Table 8. Address definition - device information read access

Device information read access	
Operating code	
OC1	OC0
1	1

Table 9. Address definition - RAM access

RAM address	Description	Access
3FH	Advanced Op.	C
3EH	Reserved	None
...	...	
...	...	
...	...	

RAM address	Description	Access
0DH	Reserved	None
0CH	Reserved (RESVDI)	R
0BH	Reserved (RESVDO)	R/W
0AH	Contro register (WDGTRDIS)	R/W
...	...	
02H	Status register (DSR2)	R
01H	Status register (DSR1)	R/C
00H	Reserved	None

Table 10. Address definition - ROM access

ROM Address	Description	Access
3FH	<Advanced op.>	W
3EH	<GSB options>	R
...		
20H	<SPI CPHA test>	R
16H	<WD bit pos. 4>	R
15H	<WD bit pos. 3>	R
14H	<WD bit pos. 2>	R
13H	<WD bit pos. 1>	R
12H	<WD type 2>	R
11H	<WD type 1>	R
10H	<SPI mode>	R
…		
0AH	<Silicon ver.>	R
...		
05H	<Device n.4>	R
04H	<Device n.3>	R
03H	<Device n.2>	R
02H	<Device n.1>	R
01H	<Device family>	R
00H	<Company code>	R

Information registers

The device information registers can be read by using OpCode ‘11’. After shifting out the GSB the 8-bit wide payload will be transmitted. By reading device information registers a communication width which is minimum 16 bits plus a multiple by 8 can be used. After shifting out the GSB followed by the 8bit wide payload a series of ‘0’ is shifted out at the SDO.

Table 11. L99H92 information registers map

ROM Address	Description	Access		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3FH	<Advanced Op.>										
3EH	<GSB Options>	R	→	0	0	0	1	0	0	0	0

ROM Address	Description	Access		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
…											
20H	<SPI CPHA test>	R	→	0	1	0	1	0	1	0	1
16H	<WD bit pos. 4>	R	→	**00H**							
15H	<WD bit pos. 3>	R	→	**00H**							
14H	<WD bit pos. 2>	R	→	**00H**							
13H	<WD bit pos. 1>	R	→	**49H**							
12H	<WD Type 2>	R	→	**A4H**							
11H	<WD Type 1>	R	→	**4AH**							
10H	<SPI mode>	R	→	**A1H**							
…			→								
0AH	<Silicon Ver.>	R	→	major revision				minor revision			
…			→								
05H	<Device No.4>	R	→	**4CH**							
04H	<Device No.3>	R	→	**36H**							
03H	<Device No.2>	R	→	**52H**							
02H	<Device No.1>	R	→	**55H**							
01H	<Device Family>	R	→	**01H**							
00H	<Company Code>	R	→	**00H**							

Device identification registers

These registers represent a unique signature to identify the device and silicon version.

<Company Code>: 00H (STMicroelectronics)

<Device Family>: 01H (BCD Power Management)

<Device No. 1>: 55H (ASCII code for U)

<Device No. 2>: 52H (ASCII code for R)

<Device No. 3>: 36H (ASCII code for 6)

<Device No. 4>: 4CH (ASCII code for L)

SPI modes

By reading out the <SPI Mode> register, general information of the device SPI can be read.

Table 12. SPI mode registers

Bit7	Bit6	Bit5	Bit 4	Bit 3	Bit 2	Bit1	Bit0
BR	DL2	DL1	DL0	0	0	S1	S0
1	0	1	0	0	0	0	1

<SPI Mode>: A1H (Burst Mode read available, 24 bit SPI frame, parity error check)

SPI burst read

Table 13. Burst read bit

Bit 7	Description
0	BR not available
1	BR available

The *SPI Burst Read* bit indicates whether the burst read mode is available or not. The *Burst Read* can be used to perform a device internal memory dump to the SPI Master.

The start of the *Burst Read* is like a normal *Read Operation*. The difference is that after the *SPI Data Length* the CSN is not pulled high and the CLK will be continuously clocked. When the normal CLK max count is reached (SPI data length) the consecutive addressed data is latched into the shift register. This procedure is performed every time the CLK payload length is reached.

In case the automatically incremented address is not used by the device, undefined data is shifted out. An automatic address overflow is implemented when address 3FH is reached.

The *SPI Burst Read* is limited by the CSN low timeout.

SPI data length

The *SPI Data Length* value indicates the length of the CLK count monitor which is running for all accesses to the *Device Registers*. Any communication frame with a CLK count not equal to the reported one will trigger an SPI error and the corresponding command/operation will be ignored.

Table 14. SPI data length

Bit 6	Bit 5	Bit 4	Description
DL2	DL1	DL0	
0	0	0	invalid
0	0	1	16-bit SPI
0	1	0	24-bit SPI
0	1	1	32-bit SPI
			…
1	1	1	64-bit SPI

Data consistency check (parity/CRC)

Table 15. Data consistency check

Bit 1	Bit 0	Description
S1	S0	
0	0	not used
0	1	Parity used
1	0	CRC used
1	1	Invalid

Watchdog identification registers

The <WD Type 1> and <WD Type 2> ROM registers are defined as follows:

Table 16. WD type ROM registers

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	WD1	WD0						
<WD type 1>	0	1	WT5	WT4	WT3	WT2	WT1	WT0
			Watchdog timeout/long open window WT[5:0] * 5 ms					
<WD type 2>	1	0	OW1	OW0	CW3	CW2	CW1	CW0
			Open window OW[1:0] *5 ms		Closed window CW[3:0] * 5 ms			

The binary value of WT[5:0] times 5 ms indicates the maximal safe long open window time. CW[3:0] times 5 ms defines the maximum closed window time and WW[1:0] times 5 ms defines the minimum safe open window time.

The watchdog trigger register address is defined by the <WD bit pos. 1> ROM register.

Device application registers (RAM)

The *Device Application Registers* are all registers accessible using OpCode ‘00’, ‘01’ and ‘10’. The functions of these registers are defined in the device specification.

Protocol failure detection

To achieve a communication protocol that covers certain fail-safe requirements a basic set of SPI communication failure detection mechanisms is implemented.

Clock monitor

During communication (CSN low) a clock monitor counts the valid CLK clock edges. If the CLK edges do not correlate with the *SPI Data Length* an SPIE is reported with the next command and the actual command is rejected.

By accessing the *Device Information Registers* (OpCode = ‘11’) the *Clock Monitor* is set to a minimum of 24 CLK edges plus a multiple by 16 (for example, 16, 32, , …).

Providing no CLK edge during the CSN low phase is not recognized as an SPIE. For an *SPI Burst Read* also the *SPI Data Length* plus multiple numbers of *Payloads* CLK edges are assumed as a valid communication.

CLK polarity (CPOL) check

To detect the wrong polarity access via CLK the internal clock monitor is used. Providing first a negative edge on CLK during communication (CSN low) or a positive edge at last will lead to an *SPI Error* reported in the next communication and the actual command is rejected.

CLK phase (CPHA) check

To verify that the *CLK Phase* of the SPI master is set correctly a special *Device Information Register* is implemented. By reading this register the data must be 55H. In case AAH is read, the CPHA setting of the SPI master is wrong and a proper communication cannot be guaranteed.

CSN timeout

By pulling CSN low the SDO is set active and leaves its tristate condition. To ensure communication between other SPI devices within the same bus even in case of CSN stuck @ low a CSN timeout is implemented. By pulling CSN low an internal timer is started. When the timer reaches its end, the ongoing command is rejected, the SPIE is set (and it will be visible at the next communication) and the SDO is set in tristate condition.

SDI stuck at LOW

As a communication with data all-‘0’ and OpCode ‘00’ on address b’000000 cannot be distinguished between a valid command and a SDI stuck @ LOW, this communication is not allowed. Nevertheless, in case a stuck @ LOW is detected the command will be rejected and the SPIE will be set and it will be visible at the next communication.

SDI stuck at HIGH

As a communication with data all-‘1’ and OpCode ‘11’ on address b’111111 cannot be distinguished between a valid command and a SDI stuck @ HIGH, this communication is not allowed. In case a stuck @ HIGH is detected the command will be rejected and the SPIE will be set and it will be visible at the next communication.

SDO stuck @

The SDO stuck @ GND and stuck @ HIGH have to be detected by the SPI master. As the definition of the GSB guarantees at least one toggle, a GSB with all ‘0’ or all ‘1’ reports a stuck at error.

5 Electrical characteristics

5.1 Absolute maximum ratings

Stressing the device above the rating listed in Table 17 may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 17. Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{DH}, V_S	Power supply voltage		- 0.3 to 28	V
	Single pulse t_{max} < 400 ms		40	
VDD	I/O supply voltage		-0.3 to 18	V
SDI, SDO, CLK, CSN, EN, DIR/IN2, PWM/IN1, DIAGN, FSINB	Digital input/ output voltage		-0.3 to V_{DD} + 0.3	V
CSO1, CSO2	Analog output voltage		-0.3 to V_{DD} + 0.3	V
CSI1+, CSI1-, CSI2+, CSI2-	HV signal pins		-6 to 40	V
CSI1+, CSI1-, CSI2+, CSI2-	Differential input voltage range HV signal pins		-19 to +19	V
GL2, GH2, GL1, GH1 (Gxy)	HV signal pins		Sxy – 0.3 to Sxy + 13; VCPOUT + 0.3	V
SL2, SH2, SL1, SH1	HV signal pins		-6 to 40	V
CP2-, CP1-	HV signal pins		-0.3 to 42	V
CP1+	HV signal pin	VDH ≤ 26 V	VDH-0.3 to VDH+14	V
		VDH > 26 V	VDH-0.3 to +42	
CP2+	HV signal pin	VDH ≤ 26 V	VDH-0.6 to VDH+14	V
		VDH > 26 V	VDH-0.6 to +42	
CPOUT	HV signal pin	VDH ≤ 26 V	VDH-0.3 to VDH+14	V
		VDH > 26 V	VDH-0.3 to +42	

5.2 ESD protection

Table 18. ESD protection

Parameter	Value	Unit
Electrostatic discharge test (AECQ100-002-E) all pins	±2	kV
Electrostatic discharge test (AECQ100-002-E) output pins SHx (X = 1,2), CSI1x (X = +,-) , CSI2x (X = +,-)	±4	kV
Charge device model (CDM-AEC-Q100-011) all pins	±500	V
Charge device model (CDM-AEC-Q100-011) corner pins	±750	V

5.3 Thermal data

Table 19. Thermal operating range

Item	Symbol	Parameter	Value	Unit
5.3.1	T_J	Operating junction temperature	-40 to 150	°C
5.3.2	T_{stg}	Storage temperature	-55 to 150	°C

Table 20. Temperature warning and thermal shutdown

Item	Symbol	Parameter		Min.	Typ.	Max.	Unit
5.3.3	TjTW_ON	Junction temperature thermal warning threshold	T_J increasing	140	150	165	°C
5.3.4	TjTW_OFF		T_J decreasing	135	145	160	°C
5.3.5	TjSD_ON	Junction temperature thermal shutdown threshold	T_J increasing	170	180	190	°C
5.3.6	TjSD_OFF		T_J decreasing	160	170	185	°C
5.3.7	$t_{fTjTW/TSD}$	Temperature warning/ shutdown filtering time	Tested by scan	24		43	µs

Note: Those parameters are guaranteed at hot only

Table 21. Packages thermal resistance

Item	Symbol	Parameter	Value		Unit
			QFN32	TQFP32	
5.3.8	$R_{thj\text{-}amb}$ (1)(2)	Thermal resistance junction ambient	28.5	26	°C/W
5.3.9	$R_{thj\text{-}case}$ (3)	Thermal resistance junction to case	7.5	5.0	°C/W

1. *The parameter is retrieved according to JEDEC 51.2 referring to thermal testing method in still air .*
2. *PCB designed according to JEDEC 51.7 referring to high effective thermal conductivity test board. The values quoted are for PCB 129 mm x 60 mm x 1.6 mm, FR4, 4 layers; Copper thickness 0.070 mm, thermal vias separation 1.2 mm, Thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 0.025 mm. QFN32 footprint dimensions are 3.5 mm x 3.5 mm. TQFP32 footprint dimensions are 5 mm x 5 mm.*
3. *The $R_{thj\text{-}case}$ is retrieved according to MIL-STD-883E referring to thermal testing method.*

5.4 Electrical characteristics

For an efficient and easy tracking, numbering has been added to each electrical parameter.

Device features are split into categories (see Table 22), and each of them is represented by a letter (A, B, C, etc.); all parameters are completely identified by a letter and a three-digit number (for example, B.125, C.096…) for their whole lifetime.

New inserted parameters continue with the numbering of the related category, no matter of where they are placed.

To facilitate insertion, the last number inserted for each category is also reported in the second column of the table.

Table 22. Electrical parameters numbering

Category	Parameters numbering	Last inserted
Analog I/O	A.xxx	-

Category	Parameters numbering	Last inserted
Digital I/O	B.xxx	-
Voltage regulators	C.xxx	-
Outputs	D.xxx	-
Transceivers	E.xxx	-
Others	F.xxx	-

Due to these rules and taking into account that deleted parameter numbers will be no more reassigned, numbering inside each category may be not sequential.

The voltages are referred to the power ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ VS ≤ 28 V; T_J = -40 °C to 150 °C, unless otherwise specified.

5.4.1 Supply, supply monitoring

The voltages are referred to ground and currents are assumed positive when the current flows into the pin. 6 V ≤ VS ≤ 28 V; 6 V ≤ VDH ≤ 28 V; T_J = -40 °C to 150 °C, unless otherwise specified.

Table 23. Operating range

Item	Symbol	Parameter	Min.	Typ.	Max.	Unit
5.4.2	VDH(1)	High-side drain voltage	6(1)	-	28	V
5.4.3	VS	Battery supply voltage	4.51	-	28	V
5.4.4	VDD	I/O supply voltage, CSA supply voltage	3	-	5.5	V
5.4.5	T_J	Operating junction temperature	-40	-	150	°C

1. *Device functionalities are guaranteed down to V_{DH}=5.5V although some electrical parameters may deviate from the limits specified*

Table 24. Supply, supply monitoring

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
5.4.6	V_{DHUV}	VDH undervoltage threshold	VDH increasing / decreasing	4.7		5.4	V
5.4.7	V_{DHUV_hyst}	VDH undervoltage hysteresis		0.04	0.1	0.25	V
5.4.8	V_{SOVWT1}	VS overvoltage warning threshold 1	VS increasing	19.5		22.5	V
5.4.9			VS decreasing	18		22	
5.4.11	V_{SOVWT2}	VS overvoltage warning threshold 2	VS increasing	28.1		32.5	V
5.4.12			VS decreasing	28		32	
5.4.14	V_{DHOVT1}	VDH overvoltage threshold 1	VDH increasing	19.5		22.5	V
5.4.15			VDH decreasing	18		22	
5.4.17	V_{DHOVT2}	VDH overvoltage threshold 2	VDH increasing	28.1		32.5	V
5.4.18			VDH decreasing	28		32	
5.4.20	t_{ovuv_filt}	VS/VDH/VDD/DIO over/undervoltage filtering time	Tested by scan	50		96	µs
5.4.21	V_{DDOV}	Overvoltage threshold on V_{DD}		5.3		5.9	V
5.4.22	V_{Ddhyst_OV}	V_{DD} overvoltage hysteresis		0.04	0.1	0.25	V
5.4.23	V_{DIOOV}	Overvoltage threshold on digital input/output pins		5.45		6.5	V
5.4.24	$V_{DIOhyst\_OV}$	V_{DIO} overvoltage hysteresis		0.05		0.25	V

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
5.4.25	I_{DH}	Current consumption in active mode	VDH = 13 V; VDD = 5 V; Active mode; outputs floating	4.5	7.5	8.7	mA
5.4.26			VDH = 6 V to 28 V; VDD = 5.0 V; active mode; outputs floating	2.5		10	mA
5.4.27	I_{DHq}	VDH quiescent supply current	VDH = 13 V; VDD = 0 V; Standby mode; Ttest = -40°C, 25°C; Outputs floating			5	µA
5.4.28	Is	Current consumption in active mode	VS = 13 V; VDD = 5 V; Active mode; outputs floating			3.5	mA
			VS = 6 V to 28 V; VDD = 5.0 V; active mode; outputs floating			5	
5.4.29	I_{Sq}	VS quiescent supply current	VS = 13 V; VDD = 0 V; Standby mode; Ttest = -40°C, 25°C; Outputs floating			5	µA
5.4.30	I_{DD}	VDD DC supply current	VS = 13 V; VDD = 5 V; active mode		4	4.5	mA
5.4.31	I_{DDq}	VDD quiescent supply current	VDD = 5 V; standby Mode Ttest=125°C		12	18	µA
			VDD = 5 V; standby Mode Ttest= 25°C			14	

5.4.2 Power-on reset

Table 25. Power-on reset

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
5.4.33	V_{DDPOR_OFF}	Power-on reset threshold on VDD	VDD increasing	2.2	2.55	2.85	V
5.4.34	V_{DDPOR_ON}	Power-on reset threshold on VDD	VDD decreasing	2.0	2.25	2.6	V
5.4.35	V_{SPOR_OFF}	Power-on reset threshold on VS	VS increasing		3.45	4.5	V
5.4.36	V_{SPOR_ON}	Power-on reset threshold on VS	VS decreasing	2.3		3.55	V

5.5 Charge pump

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ VDH ≤ 28 V; T_J = -40 °C to 150 °C, unless otherwise specified.

Table 26. Charge pump electrical characteristics

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
5.5.1	V_{CP}	Charge pump output voltage	V_{DH} = 5.5 V, I_{CP} = -5 mA	V_{DH}+6.2	V_{DH}+7		V
5.5.2			V_{DH} ≥ 8 V, I_{CP} = -10 mA	V_{DH}+8.2	V_{DH}+12	V_{DH}+13.5	V
5.5.3	V_{CP_low}	Charge pump low threshold voltage		V_{DH}+4.5	V_{DH}+5	V_{DH}+5.5	V
5.5.4	I_{CP_lim}	Charge pump output current limitation	V_{CP}=V_{DH}, V_{DH}=13.5 V			70	mA
5.5.5	t_{CP}	Charge pump low filter time	Tested by scan	50		96	µs
5.5.6	f_{CP}	Charge pump frequency	Tested by scan	300	400	500	kHz

5.6 Full-bridge driver

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_{DH} ≤ 28 V 6 V ≤ V_S ≤ 28 V; T_J = -40 °C to 150 °C, unless otherwise specified.

Table 27. Full-bridge driver

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
5.6.1	$I_{GHx(Ch)}$	Average charge/ discharge current switch mode	V_{SH}=V_{DH}=13 V average current on 180 nF cap between V_{Ghx}=V_{SHx}+3 V and V_{SHx}+6 V T_J= 25 °C		0.42		A
5.6.2	R_{GHx}	On-resistance (discharge-stage)	V_{SHx} = 0 V; I_{GHx} = 50 mA; T_J = 25 °C	4	10	14	Ω
5.6.3			V_{SHx} = 0 V; I_{GHx} = 50 mA; T_J = 130 °C		14	20	Ω
5.6.4	V_{GSHx}	Gate-on voltage	V_{DH} = V_{SH} = 5.5 V ; I_{CP} = -5 mA	VSHx + 6			V
5.6.5			V_{DH} = V_{SH} ≥ 8 V ; I_{CP} = -10 mA	VSHx + 8	VSHx +10	VSHx +11.5	V
5.6.6	R_{GSHx}	Passive gate-clamp resistance	R_{GH}=(V_{GHx_a}-V_{GHx_b})/($I_{GHx(VGHx\_a)}$-$I_{GHx(VGHx\_b)}$) V_{GHx_a}=8 V, V_{GHx_b}=1 V V_{SHx}=0 V	10.5	15	19.5	kΩ
5.6.7	$I_{GLx(Ch)}$	Average charge/ discharge current switch mode	V_{SL}=0V V_{DH}=13 V average current on 180 nF cap between V_{GLx}=V_{SLx}+3 V and V_{SLx}+6 V T_J = 25 °C		0.42		A
5.6.8	R_{GLx}	On-resistance (discharge-stage)	V_{SLx} = 0 V; I_{GLx} = 50 mA; T_J = 25 °C	4	10	14	Ω
5.6.9			V_{SLx} = 0 V; I_{GLx} = 50 mA; T_J = 130 °C		14	20	Ω
5.6.10	V_{GLx}	Gate-on voltage	V_{SL}=0 V V_{DH} = 5.5 V; I_{CP} = -5 mA	VSLx +6			V
5.6.11			V_{SL}=0 V V_{DH} ≥ 8 V; I_{CP} = -10 mA	VSLx +8	VSLx +10	VSLx +12.5	V
5.6.12	R_{GSLx}	Passive gate-clamp resistance	R_{GH}=(V_{GLx_a}-V_{GLx_b})/($I_{GLx(VGLx\_a)}$-$I_{GLx(VGLx\_b)}$) V_{GLx_a}=8 V, V_{GLx_b}=1 V V_{SLx}=0 V	10.5	15	19.5	kΩ

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
5.6.13	$I_{GLxrmax}$	Maximum source current (current mode)	V_{DH} = 13.5 V; V_{SLx} = 0; V_{GLx} = 5 V; SLEW<4 :0> = 1FH SLEW1=0 SLEW2=0	140	170	200	mA
			V_{DH} = 13.5 V; V_{SLx} = 0; V_{GLx} = 5 V; SLEW<4 :0> = 1FH SLEW1=1 SLEW2=1	70	85	100	
5.6.14	$I_{GLxfmax}$	Maximum sink current (current mode)	V_{DH} = 13.5 V, V_{SLx} = 0; V_{GLx} = 5 V; SLEW<4 :0> = 1FH SLEW1=0 SLEW2=0	140	170	200	mA
			V_{DH} = 13.5 V, V_{SLx} = 0; V_{GLx} = 5 V; SLEW<4 :0> = 1FH SLEW1=1 SLEW2=1	70	85	100	
5.6.15	$T_{G(HL)xHL}$	Propagation delay time high to low (switch mode) (1)	V_{DH} = 13.5 V; V_{SHx} = 0; R_G = 0 Ω; C_G = 4.7 nF	0.01	0.25	2	µs
5.6.16	$T_{G(HL)xLH}$	Propagation delay time low to high (switch mode) (1)	V_{DH} = 13.5 V; V_{SLx} = 0; R_G = 0 Ω; C_G = 4.7 nF	0.01	0.5	2	µs
5.6.17	$I_{GHxrmax}$	Maximum source current (current mode)	V_{DH} = 13.5 V; V_{SHx} = V_{DH}; V_{GHx} = V_{SHx}+5 V; SLEW<4 :0> = 1FH SLEW1=0 SLEW2=0	140	170	200	mA
			V_{DH} = 13.5 V; V_{SHx} = V_{DH}; V_{GHx} = V_{SHx}+5 V; SLEW<4 :0> = 1FH SLEW1=1 SLEW2=1	70	85	100	
5.6.18	$I_{GHxfmax}$	Maximum sink current (current mode)	V_{DH} = 13.5 V, V_{SHx} = 0; V_{GHx} = V_{SHx}+5 V; SLEW<4 :0> = 1FH SLEW1=0 SLEW2=0	140	170	200	mA
			V_{DH} = 13.5 V, V_{SHx} = 0; V_{GHx} = V_{SHx}+5 V; SLEW<4 :0> = 1FH SLEW1=1 SLEW2=1	70	85	100	
5.6.19	dI_{IGHxr}	Source current accuracy	V_{DH} = 13.5 V; V_{SLx} = 0; V_{GLx} = 5 V; SLEW<4 :0> = 1FH	Refer to Figure 18 IGHx, IGLx accuracy			
5.6.20	dI_{IGHxf}	Sink current accuracy	V_{DH} = 13.5 V; V_{SHx} = V_{DH}; V_{GHx} = V_{SHx}+5 V; SLEW<4 :0> = 1FH	Refer to Figure 18 IGHx, IGLx accuracy			
5.6.21	$V_{DSHxrSW}$	Switching voltage (V_{DH}-V_{SH}) between current mode and switch mode (rising)	V_{DH} = 13.5 V	0.85	1.14	1.45	V

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
5.6.22	$V_{DSHxfSW}$	Switching voltage (VDH-VSH) between switch mode and current mode (falling)	V_{DH} = 13.5 V	0.85	1.14	1.45	V
5.6.23	t_{GHxr}	Rise time (switch mode)	V_{DH} = 13.5 V; V_{SHx} = 0; R_G = 0 Ω; C_G = 4.7 nF	20	115	200	ns
5.6.24	t_{GHxf}	Fall time (switch mode)	V_{DH} = 13.5 V; V_{SHx} = 0; R_G = 0 Ω; C_G = 4.7 nF	60	160	200	ns
5.6.25	t_{GLxr}	Rise time	V_{DH} = 13.5 V; V_{SLx} = 0; R_G = 0 Ω; C_G = 4.7 nF	20	115	200	ns
5.6.26	t_{GLxf}	Fall time	V_{DH} = 13.5 V; V_{SLx} = 0; R_G = 0 Ω; C_G = 4.7 nF	60	160	200	ns
5.6.27	t_{DT0000}	Programmable cross-current protection time	Tested by scan		250		ns
5.6.28	t_{DT0001}	Programmable cross-current protection time	Tested by scan		500		ns
5.6.29	t_{DT0010}	Programmable cross-current protection time	Tested by scan		750		ns
5.6.30	t_{DT0011}	Programmable cross-current protection time	Tested by scan		1000		ns
5.6.31	t_{DT0100}	Programmable cross-current protection time	Tested by scan		1250		ns
5.6.32	t_{DT0101}	Programmable cross-current protection time	Tested by scan		1500		ns
5.6.33	t_{DT0110}	Programmable cross-current protection time	Tested by scan		1750		ns
5.6.34	t_{DT0111}	Programmable cross-current protection time	Tested by scan		2000		ns
5.6.35	t_{DT1000}	Programmable cross-current protection time	Tested by scan		2250		ns
5.6.36	t_{DT1001}	Programmable cross-current protection time	Tested by scan		2500		ns
5.6.37	t_{DT1010}	Programmable cross-current protection time	Tested by scan		2750		ns
5.6.38	t_{DT1011}	Programmable cross-current protection time	Tested by scan		3000		ns
5.6.39	t_{DT1100}	Programmable cross-current protection time	Tested by scan		3250		ns
5.6.40	t_{DT1101}	Programmable cross-current protection time	Tested by scan		3500		ns
5.6.41	t_{DT1110}	Programmable cross-current protection time	Tested by scan		3750		ns
5.6.42	t_{DT1111}	Programmable cross-current protection time	Tested by scan		4000		ns
5.6.43	f_{PWMH}	PWMH switching frequency(1)	V_{DH} = 13.5 V; V_{SLx} = 0 V; R_G = 0 Ω; C_G = 2.7 nF; PWMH-Duty-cycle = 50%, tested by scan			50	kHz

1. *Without cross-current protection time t_{DT}.*

Figure 17. **H-driver delay times**

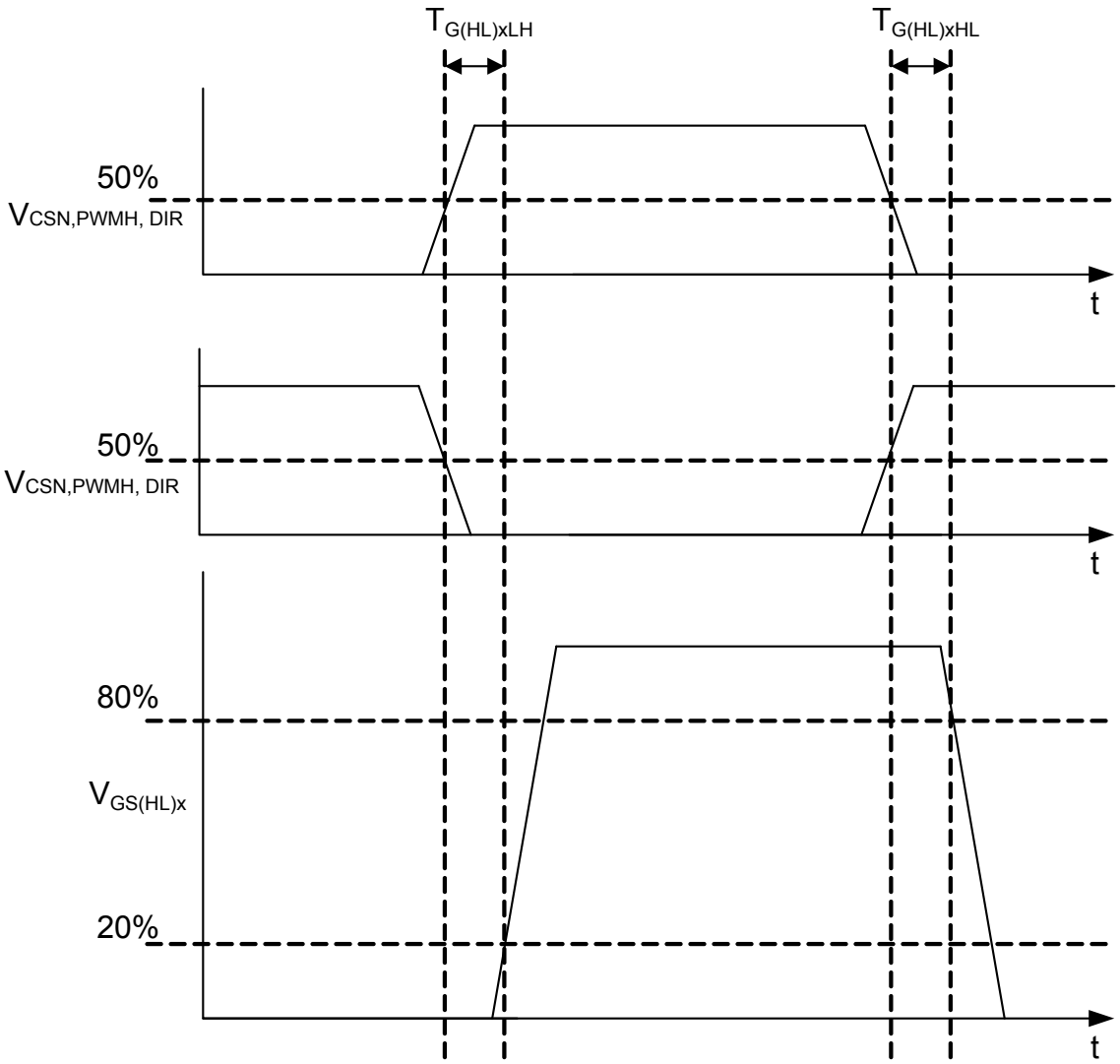
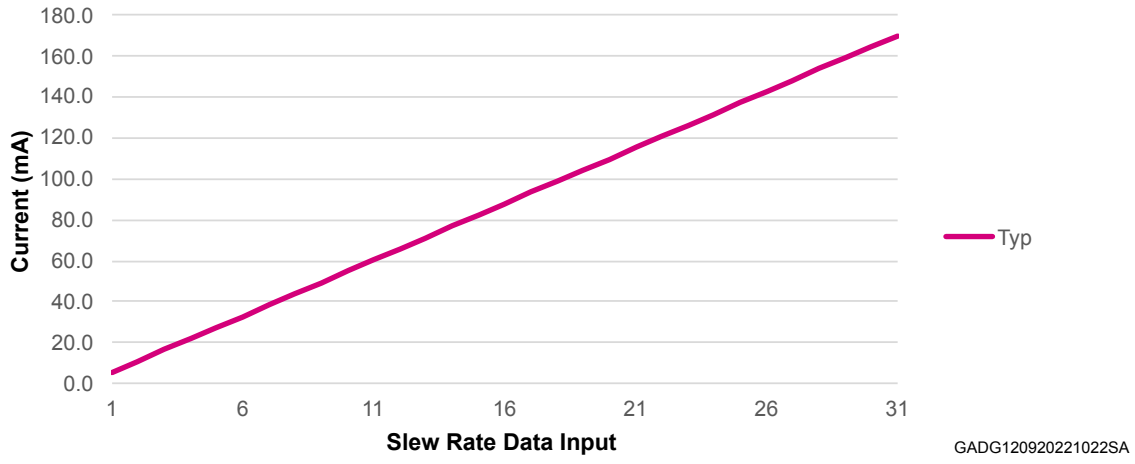


Figure 18. **I_{GHx}, I_{GLx} accuracy**



5.7 VDS monitoring thresholds

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_{DH} ≤ 28 V, V ≤ V_S ≤ 28 V; T_J = -40 °C to 150 °C, unless otherwise specified.

Table 28. Drain-source monitoring external full-bridge

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
5.7.1	V_{SCd0}	Drain-source threshold voltage		-40%	0.075	40%	V
5.7.2	V_{SCd1}	Drain-source threshold voltage		-25%	0.15	25%	V
5.7.3	V_{SCd2}	Drain-source threshold voltage		-25%	0.25	25%	V
5.7.4	V_{SCd3}	Drain-source threshold voltage		-20%	0.4	20%	V
5.7.5	V_{SCd4}	Drain-source threshold voltage		-15%	0.6	15%	V
5.7.6	V_{SCd5}	Drain-source threshold voltage		-15%	0.8	15%	V
5.7.7	V_{SCd6}	Drain-source threshold voltage		-12%	1	12%	V
5.7.8	V_{SCd7}	Drain-source threshold voltage		-12%	1.2	12%	V
5.7.9	t_{FT00}	Drain-source monitor filter time	Tested by scan		1.5		µs
5.7.10	t_{FT01}	Drain-source monitor filter time	Tested by scan		3		µs
5.7.11	t_{FT10}	Drain-source monitor filter time	Tested by scan		4.5		µs
5.7.12	t_{FT11}	Drain-source monitor filter time	Tested by scan		6		µs
5.7.13	t_{B000}	Drain-source monitor blanking time	Tested by scan		1		µs
5.7.14	t_{B001}	Drain-source monitor blanking time	Tested by scan		2		µs
5.7.15	t_{B010}	Drain-source monitor blanking time	Tested by scan		3		µs
5.7.16	t_{B011}	Drain-source monitor blanking time	Tested by scan		4		µs
5.7.17	t_{B100}	Drain-source monitor blanking time	Tested by scan		5		µs
5.7.18	t_{B101}	Drain-source monitor blanking time	Tested by scan		6		µs
5.7.19	t_{B110}	Drain-source monitor blanking time	Tested by scan		7		µs
5.7.20	t_{B111}	Drain-source monitor blanking time	Tested by scan		8		µs
5.7.21	t_{scs}	Drain-source comparator propagation delay	V_S = 13.5 V; V_{DH} = jump from GND to V_S			1	µs

5.7.1 Open-load monitoring external full-bridges

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_{DH} ≤ 28 V; 6 V ≤ V_S ≤ 28 V; T_J = -40 °C to 150 °C, unless otherwise specified.

Table 29. Open-load monitoring external full-bridges

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
5.7.23	V_{ODSL}	Low-side drain-source monitor low off-threshold voltage	V_{SLx} = 0 V; VDH = 13.5 V	0.1 VDH	0.15 VDH	0.2 VDH	V
5.7.24	V_{ODSH}	Low-side drain-source monitor high off-threshold voltage	V_{SLx} = 0 V; VDH = 13.5 V	0.76 VDH	0.81 VDH	0.85 VDH	V
5.7.25	V_{OLSHx}	Output voltage of selected SHx in open-load test mode	V_{SLx} = 0 V; VDH = 13.5 V	0.49 VDH	0.5 VDH	0.51 VDH	V
5.7.26	R_{pdOL}	Pull-down resistance of the non-selected *SHx* pin in open-load mode	V_{SLx} = 0 V; VDH = 13.5 V; V_{SHX} = 4.5 V	15	20	25	kΩ

5.8 Current sense amplifiers (CSA)

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ VDH ≤ 18 V; T_J = -40 °C to 150 °C, unless otherwise specified

Table 30. Current sense amplifiers

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
5.8.1	V_{ICM}	Common mode input voltage		-2		V_{DH}+2	V
5.8.2	G_0	Operational amplifiers gains	GCSAn [1:0]=0 n=1,2; V_{DH}=12.5V	-6%	10	6%	
5.8.3	G_1		GCSAn [1:0]=1 n=1,2; V_{DH}=12.5V	-6%	20	6%	
5.8.4	G_2		GCSAn [1:0]=2 n=1,2; V_{DH}=12.5V	-4%	50	4%	
5.8.5	G_3		GCSAn [1:0]=3 n=1,2; V_{DH}=12.5V	-4%	100	4%	
5.8.6	dG/dT	Gains thermal drifts	V_{DH}=12.5V	-1%(1)		1%(1)	
5.8.7	V_{O0}	Offset on op-amp output	CSAnOO = 0; n=1,2		VDD/22		V
5.8.8	V_{O1}		CSAnOO = 1 n=1,2; V_{DH}=12.5V		VDD/2		V
5.8.9	V_{IO0}	Input offset	GCSAn [1:0]=0 n=1,2; V_{DH}=12.5 V V_{O0}	-10		+10	mV
5.8.10	V_{IO1}		GCSAn [1:0]=1 n=1,2; V_{DH}=12.5V V_{O0}	-8.5		+8.5	mV
5.8.11	V_{IO2}		GCSAn [1:0]=2 n=1,2; V_{DH}=12.5 V V_{O0}	-3		+3	mv

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
5.8.12	V_{IO3}	Input offset	GCSAn [1:0]=3 n=1,2; V_{DH}=12.5 V V_{O0}	-3		+3	mV
5.8.26	$V_{IO0\_VDD\_2}$		GCSAn [1:0]=0 n=1,2; V_{DH}=12.5 V V_{O1}	-9		+9	mV
5.8.27	$V_{IO1\_VDD\_2}$		GCSAn [1:0]=1 n=1,2; V_{DH}=12.5 V V_{O1}	-7		+7	mV
5.8.28	$V_{IO2\_VDD\_2}$		GCSAn [1:0]=2 n=1,2; V_{DH}=12.5V V_{O1}	-2.6		+2.6	mv
5.8.29	$V_{IO3\_VDD\_2}$		GCSAn [1:0]=3 n=1,2; V_{DH}=12.5 V V_{O0}	-2.6		+2.6	mV
5.8.13	dV_{IO}/dT	Thermal drift of input offset	GCSAn [1:0]=0,1 n=1,2; V_{DH}=12.5V	-20	4(1)	20(1)	µV/K
			GCSAn [1:0]=2,3 n=1,2; V_{DH}=12.5 V	-10	2(1)	10(1)	
5.8.14	CMRR	Common mode rejection ratio	V_{DH}=12.5 V (20 kHz)	≥85(1)	≥90(1)		dB
5.8.15	PSRR	Power supply rejection ratio (2)	VDH=12.5 V (20 kHz)	≥85(1)	≥90(1)		dB
5.8.16	VCSOH	High output voltage	I_{OUT} = 2 mA	VDD-0.35			V
5.8.17			I_{OUT}= 200 µA	VDD-0.1	VDD-0.04		V
5.8.18	VCSOL	Low output voltage	I_{OUT} = 2 mA		200	350	mV
5.8.19			I_{OUT}= 200 µA		40	70	mV
5.8.20	t_{SETTLE}(1) (3)	2% settling time	100 mV differential input, GCSAn [1:0]=1, CSAnOO = 0, RC filter: R=1 kΩ; C= 220 pF			2	µs
5.8.21	BW(1)	Bandwidth	GCSAn [1:0]=1; n=1,2 (G=20) RC filter: R=1 kΩ; C= 220 pF	0.8			MHz
5.8.22	trecovery G01	+/-5% recovery time (G=10, 20, 50)	1V down to 0.4xV_{DD}/ G_{CSA} for CSAnOO =1			2(4)	µs
5.8.24		+/-5% recovery time (G=100)	RC filter: R=1 kΩ; C= 220 pF			3(4)	
5.8.23	trecovery G00	+/-5% recovery time (G=10, 20, 50)	1V down to 0.04xV_{DD}/G_{CSA} for CSAnOO =0			2(4)	µs
5.8.25		+/-5% recovery time (G=100)	RC filter: R=1 kΩ; C= 220 pF			3(4)	

1. *Guaranteed by design, not tested in production*
2. $PSRR = 20log\frac{\Delta V_S * G_{DIFF}}{\Delta V_{OUT}} = 20log\frac{\Delta V_S}{\Delta V_{IN}}$
3. t_{SETTLE} *is guaranteed by design for the following gains:*

1. *G=10 with a differential input of 25 mV to 450 mV*
2. *G=20 with a differential input of 12.5 mV to 225 mV*
3. *G=50 with a differential input of 5 mV to 90 mV*
4. *G=100 with a differential input of 2.5 mV to 45 mV*

4. *Guaranteed by design for G=10, 20, 50 100*

5.9 Fail-safe switch-off input FSINB

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 18 V; T_J = -40 °C to 150 °C, unless otherwise specified.

Table 31. Fail-safe switch-off input FSINB

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
5.9.1	VFSINBLTH	Input voltage low threshold				0.8	V
5.9.2	VFSINBHTH	Input voltage high threshold		2.0			V
5.9.4	t_{FSINB_filt}	Fail-safe input filter time	Tested by scan	1		3	µs
5.9.5	RFSINB	Input pull-down resistance at input FSINB		50	100	200	kΩ

5.10 Enable

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 18 V; T_J = -40 °C to 150 °C, unless otherwise specified.

Table 32. Input: ENABLE

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
5.10.1	VINL	Input voltage low threshold on EN				0.8	V
5.10.2	VINH	Input voltage high threshold on EN		2.0			V
5.10.5	IIN	Input pull-down current on EN	VIN = 5 V VDD=0 V VS=VDH=0 V	25	45	100	µA

5.11 DIAGN

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ VS ≤ 18 V; T_J = -40 °C to 150 °C, unless otherwise specified.

Table 33. Outputs: DIAGN

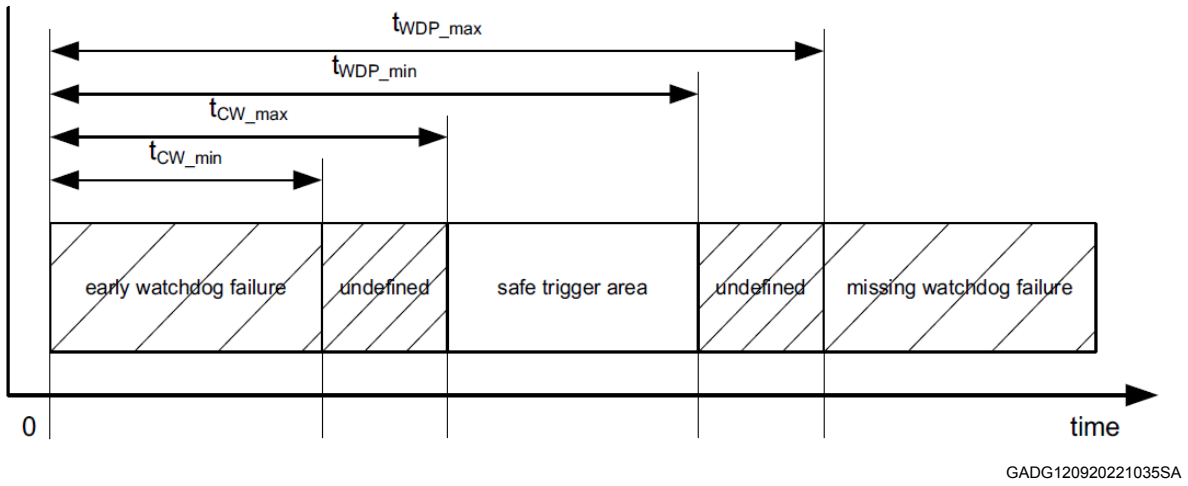
Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
5.11.1	V_{OL}	Low-level output voltage	Iout=4 mA			0.5	V
5.11.2	R_{DIAGN}	Pull-up resistance at output DIAGN	V_{DIAGN} = 0	10	30	60	kΩ

5.12 Watchdog

Table 34. Watchdog

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
5.12.1	t_{LOW}	Long open window	Tested by scan	52	-	87	ms
5.12.2	t_{CW}	Closed window	Tested by scan	11	-	20	ms
5.12.3	t_{WDP}	Watchdog period	Tested by scan	32	-	54	ms

Figure 19. Watchdog early, late, and safe window



GADG120920221035SA

5.13 SPI electrical characteristics

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 18 V; T_J = -40 °C to 150 °C, unless otherwise specified.

Table 35. Inputs: CSN, CLK, PWM, DIR, EN and SDI

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
5.13.1	VIL	Low-level input voltage				1.0	V
5.13.2	VIH	High-level input voltage		2.3			V
5.13.4	ICSN_in	Pull-up resistor CSN	VCSN= 0V	13	29	46	kΩ
5.13.5	ICLK_in	Pull-down current at input CLK	VCLK = 1.5 V	5	30	60	µA
5.13.6	ISDI_in	Pull-down current at input DI	VDI = 1.5 V	5	30	60	µA
5.13.7	IDIR_in	Pull-down current at input DIR	VDIR = 1.5 V	5	30	60	µA
5.13.8	IPWM_in	Pull-down current at input PWM	VPWM = 1.5 V	5	30	60	µA
5.13.10	Cin(1)	Input capacitance at input	0 V < VDD < 5.3 V		10	15	pF

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
		CSN, CLK, DI, DIR, PWM and EN					

1. *Value of input capacity is not measured in production test. Parameter is guaranteed by design.*

Table 36. DI, CLK and CSN timing

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
5.13.11	t_{CLK}	Clock period	Tested by scan	250	-		ns
5.13.12	t_{CLKH}	Clock high time	Tested by scan	100	-		ns
5.13.13	t_{CLKL}	Clock low time	Tested by scan	100	-		ns
5.13.14	t_{set} CSN	CSN setup time, CSN low before rising edge of CLK	Tested by scan	150	-		ns
5.13.15	t_{set} CLK	CLK setup time, CLK high before rising edge of CSN	Tested by scan	150	-		ns
5.13.16	t_{set} SDI	SDI setup time	Tested by scan	25	-		ns
5.13.17	thold SDI	SDI hold time	Tested by scan	25	-		ns
5.13.18	tr in	Rise time of input signal SDI,CLK, CSN	Tested by scan		-	25	ns
5.13.19	t_f in	Fall time of input signal SDI, CLK, CSN	Tested by scan		-	25	ns

Note: *See Figure 21.*

Table 37. SDO

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
5.13.20	VSDOL	Output low level	ID = +4 mA			0.5	V
5.13.21	VSDOH	Output high level	ID = -4 mA	VDD – 0.5			V
5.13.22	ISDOLK	Tristate leakage current	VCSN= VDD; 0 V < VSDO< VDD	-10		10	µA
5.13.23	CSDO	Tristate input capacitance	Guaranteed by design		10	15	pF

Table 38. SDO timing

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
5.13.24	tr SDO	SDO rise time	CL = 50 pF; Iload = -1 mA	-		25(1)	ns
5.13.25	tf SDO	SDO fall time	CL = 50 pF; Iload = +1 mA	-		25(1)	ns
5.13.26	ten DO tri L	SDO enable time from CSN falling edge: 3-state to low level on SDO	CL = 50 pF; Iload = +1mA; pull-up load to VDD	-	50	100	ns
5.13.27	tdis SDO L tri	SDO disable time from CSN rising edge: low level to 3-state on SDO	CL = 50 pF; Iload = +1mA; pull-up load to VDD	-	50	100	ns

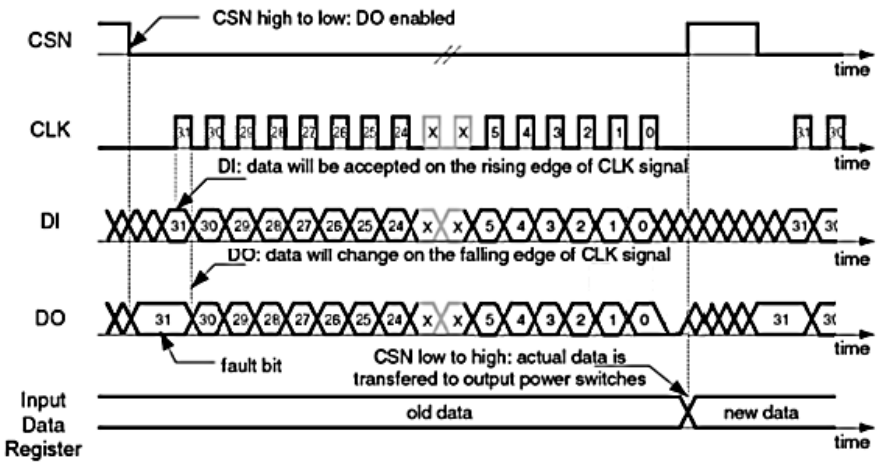
Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
5.13.28	ten SDO tri H	SDO enable time from CSN falling edge: 3-state to high level on SDO	CL = 50 pF; Iload = +1 mA; pull-down load to VDD	-	50	200	ns
5.13.29	tdis SDO H tri	From CSN rising with DO at high level to 3-states measured at 0.3 VDD	CL = 50 pF; Iload = -1 mA; pull-down load to GND	-	50	100	ns
5.13.30	td SDO	SDO delay time	VSDO < 0.3 VDD; VSDO > 0.7 VDD; CL = 50 pF	-	30	60	ns

1. *Guaranteed by design.*

Table 39. CSN timing

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
5.13.31	tCSN_HI, min	Minimum CSN high time, active mode	Transfer of SPI-command to input register	6			µs
5.13.32	tCSNfail	CSN low timeout	Tested by scan	20	35	50	ms

Figure 20. SPI transfer timing diagram



GADG120920221042SA

The SPI can be driven by a microcontroller with its SPI peripheral running in the mode:

CPOL = 0 and CPHA = 0.

For this mode input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

Figure 21. **SPI input timing**

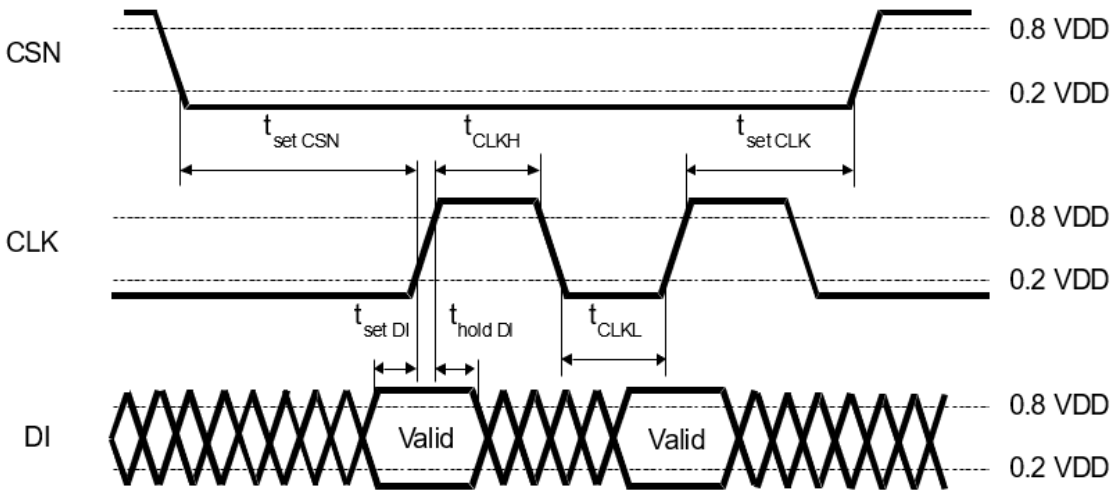


Figure 22. **SPI output timing**

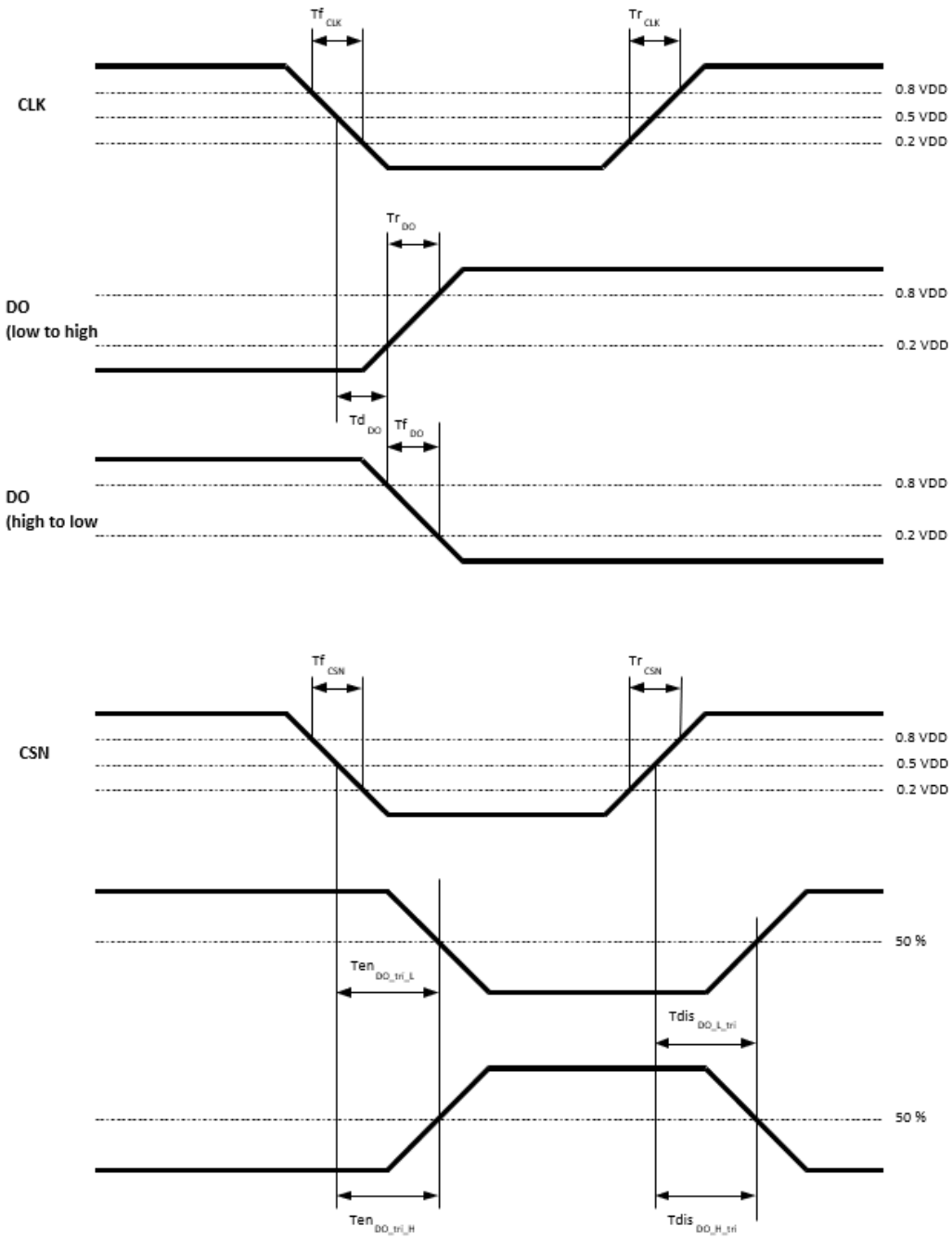
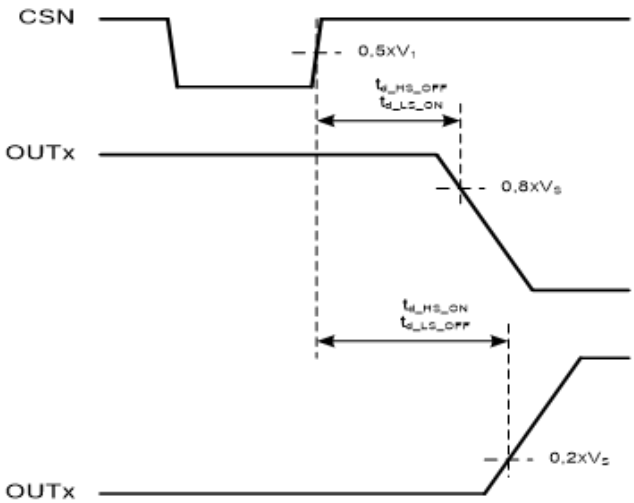
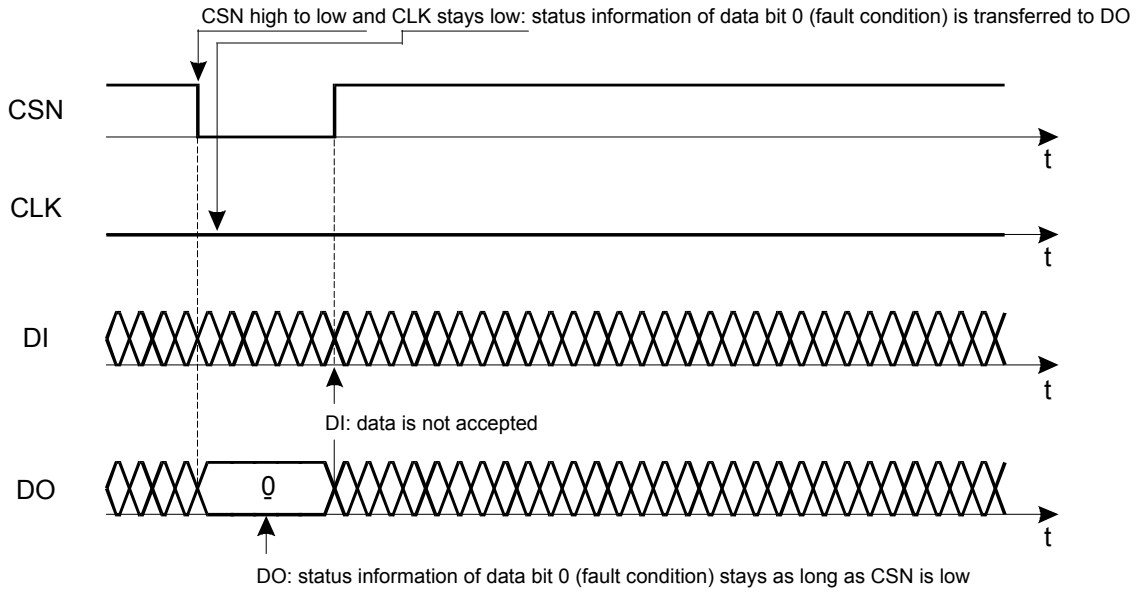


Figure 23. **SPI CSN output timing**



GADG120920221116SA

Figure 24. **SPI CSN low to high transition and global status bit access**



5.14 Oscillator

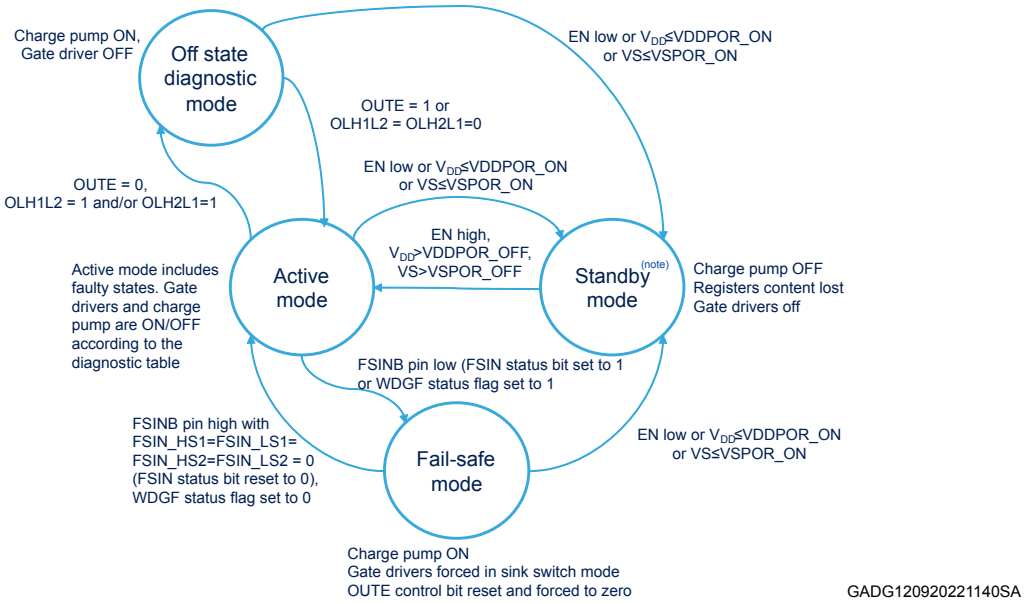
The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V≤ V_S ≤ 28 V; 6 V ≤ V_{DH}≤ 28 V ; T_J = -40 °C... 150 °C, unless otherwise specified.

Table 40. **Oscillator**

Item	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
5.14.1	F_{CLK2}	Oscillation frequency		12.8	16.0	19.2	MHz

5.15 Operating modes

Figure 25. **Operating modes**



Note: To achieve the device minimum current consumption in standby mode, the EN pin has to be pulled low.

Table 41. **Diagnostic table**

Event	Status register flag/bit	Global status byte bit	Device actions	DIAGN pin behavior
VDH overvoltage	VDHOV	DE	Active switch-off of external LS MOSFETs with maximum available gate current (LS gate drivers forced in sink switch mode). Active switch-off of external HS MOSFETs with maximum available gate current for 32 µs up to 64 µs and as long as VCP>VDH+3 V, followed by passive/resistive turn off. Charge-pump switched off	Pulled low if DGVDHOVE is set
VDH undervoltage	VDHUV	DE	Active switch-off of external LS MOSFETs with maximum available gate current (LS gate drivers forced in sink switch mode). Active switch-off of external HS MOSFETs with maximum available gate current as long as VCP>VDH+3V, otherwise passive/resistive turn off.	Pulled low if DGVDHUVE is set
VS overvoltage Warning	VSOVW	GW	None	Pulled low if DGVSOVWE is set
VDD overvoltage	VDDOV	DE	Active switch-off of all external MOSFETs with maximum available gate current (all gate drivers forced in sink switch mode).	Pulled low if DGVDDOVE is set
Thermal warning	TW	GW	None	Pulled low if DGTWE is set
Thermal shutdown	TSD	DE	Active switch-off of external LS MOSFETs with maximum available gate current (LS gate drivers forced in sink switch mode). Active switch-off of external HS MOSFETs with maximum available gate current for 32 µs up to 64µs and as long as VCP>VDH+3 V, followed by passive/resistive turn off. Charge-pump switched off.	Pulled low if DGTSDE is set

Event	Status register flag/bit	Global status byte bit	Device actions	DIAGN pin behavior
FSINB activation	FSIN	FS	Active switch-off of all external MOSFETs with maximum available gate current (all gate drivers forced in sink switch mode). The OUTE control bit is reset.	Pulled low if DGFSINE is set
Charge pump not ready	NRDY	DE	The gate drivers are disabled. A passive resistive connection between gate and source of each MOSFET is present.	Pulled low if DGNRDYE is set
Charge pump low	CPLOW	DE	Active switch-off of external LS MOSFETs with maximum available gate current (LS gate drivers forced in sink switch mode). Active switch-off of external HS MOSFETs with maximum available gate current as long as VCP>VDH+3 V, otherwise passive/resistive turn off.	Pulled low if DGCPLOWE is set
Watchdog fault	WDGF	FS	Active switch-off of all external MOSFETs with maximum available gate current (all gate drivers forced in sink switch mode).The OUTE control bit is reset.	Pulled low if DGWDGFE is set
Digital input/output overvoltage	DIOOV	DE	Active switch-off of all external MOSFETs with maximum available gate current (all gate drivers forced in sink switch mode).	Pulled low if DGDIOOVE is set
VDS monitoring (Leg x, HS or LS)	DSHSx or DSLSx	FE	For DSMON_CONFIG control bit set to one and INPMODE control bit set to zero: active switch-off of all external MOSFETs with maximum available gate current (all gate drivers forced in sink switch mode). In all the other cases: active switch-off of affected leg external MOSFETs with maximum available gate current (affected leg gate drivers forced in sink switch mode).	Pulled low if DGDSxE is set
VS<VSPOR_ON Followed by VS>VSPOR_OFF	NA	RSTB	In standby mode the charge pump is switched off together with the gate drivers, so a passive resistance between gate and source switches off the external MOSFETs as well. Once back in active mode, all the registers are reset to default values, the charge pump is automatically enabled (no need to clear the RSTB bit) and the gate drivers are disabled leaving just a passive resistance between gate and source of each MOSFET.	By default pulled low once out of standby mode and until the global status byte RSTB bit is cleared by any valid SPI communication frame
VDD<VDDPOR_ON Followed by VDD>VDDPOR_OFF				
Enable pin pulled low Followed by Enable pin pulled high				
SPI error (parity bit, write/ read to/from wrong address, CLK count error, SDI stuck at, CSN timeout)	NA	SPIE	The operation linked to the invalid SPI frame is not run.	Pulled low if DGSPIEE is set

6 SPI registers

6.1 Global status byte GSB

Table 42. **Global status byte GSB**

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
1 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)
GSBN	RSTB	SPIE	-	FE	DE	GW	FS
Global status bit not	ReSeT bit	SPI error	Reserved bit	Functional error	Device error	Global warning	Fail-safe

Bit	Name	Description
23	**GSBN**	**Global status bit not** The GSBN bit is a logically NOR combination of GSB bits from bit 16 to bit 22. This bit can also be used as global error flag without starting a complete communication frame as it is present at SDO after pulling CSN low. 0 = error detected (1 or several GSB bits from 16 to 22 are set) 1 = no error detected
22	**RSTB**	**Reset bit** The RSTB bit indicates that all the device registers have been reset to default. By default it is set to one coming out from standby mode. It is cleared automatically after any valid SPI communication frame.
21	**SPIE**	**SPI error bit** The SPIE bit indicates errors related to any wrong SPI communication. • SPI CLK count error • Parity error • Read/Write to wrong address • SDI stuck at • CSN timeout This bit is visible inside the communication frame following the not valid one. This bit is cleared automatically by any valid SPI communication frame. 0 = no error (default) 1 = error detected
20	**RES**	**Reserved**
19	**FE**	**Functional error bit** The FE bit is a logical OR combination of errors coming from application specific functional blocks. • Overcurrent status flags (DSHSx, DSLSx) 0 = no error (default) 1 = error detected The FE bit is cleared by a *Read & Clear* command of the overcurrent status flags.
18	**DE**	**Device error bit** The DE bit is a logical OR combination of errors related to the device specific blocks. • VDH overvoltage status flag (VDHOV) • VDH undervoltage status flag (VDHUV) • VDD overvoltage status flag (VDDOV) • Thermal shutdown status flag (TSD) • Charge pump not ready status bit (NRDY) • Charge pump low status flag/bit (CPLOW) • Digital input/output over-voltage status flag (DIOOV)

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
		0 = no error (default) 1 = error detected The DE bit is cleared by a *Read & Clear* command of all related flags in the *Status Register DSR1*. The NRDY status bit together with the CPLOW status bit (for CP_LOW_CONFIG=1) cannot be cleared by a *Read & clear* command.					
17	**GW**	**Global warning bit** The GW bit is a logical OR combination of warning flags. Warning bits do not lead to any device state change or switch off of functions. • Thermal warning status flag (TW) • VS overvoltage warning status flag (VSOVW) 0 = no warning (default) 1 = warning detected The GW bit is cleared by a *Read & clear* command of all related flags in the *Status Register DSR1*.					
16	**FS**	**Fail-safe bit** The FS bit indicates that the device was forced into fail-safe mode. • Watchdog fault status flag (WDGF) • Fail-safe input not status bit (FSIN) 0 = no error (default) 1 = error detected The FS bit is cleared by a *Read & clear* command of the *Status register* WDGF flag assuming that the FSIN status bit is reset to zero. The FSIN status bit, logical OR of FSINLL, FSINHS1, FSINLS1, FSINHS2 and FSINLS2, cannot be cleared by a *Read & Clear* command.					

6.2 Register map overview

Table 43. **Register map**

Global status			GSBN	RSTB	SPIE	-	FE	DE	GW	FS	Mode
											R
Addr.	Name	Bits	15	14	13	12	11	10	9	8	
			7	6	5	4	3	2	1	0	
0x01	DSR1	MSB	VDHOV	VDHUV	VSOVW	VDDOV	TW	TSD	FSIN	NRDY	R/C
		LSB	CPLOW	WDGF	DIOOV	DSHS1	DSLS1	DSHS2	DSLS2	P	
0x02	DSR2	MSB	RES	RES	RES	RES	FSINLL	FSINHS1	FSINLS1	FSINHS2	R
		LSB	FSINLS2	RES	RES	RES	O1DS	RES	O2DS	P	
0x03	DCR	MSB	INPMODE	OUTE	AFWE	FWS	DIS1	DIS2	DSMON_CONFIG	OLH1L2	R/W
		LSB	OLH2L1	OLTHH	CP_LOW_CONFIG	CPFDD	OVTS	RES	RES	P	
0x04	GD1CR1	MSB	SLEWC1[4]	SLEWC1[3]	SLEWC1[2]	SLEWC1[1]	SLEWC1[0]	DT1[3]	DT1[2]	DT1[1]	R/W
		LSB	DT1[0]	RES	SLEWD1[4]	SLEWD1[3]	SLEWD1[2]	SLEWD1[1]	SLEWD1[0]	P	
0x05	GD1CR2	MSB	RES	RES	RES	RES	DSMON1[2]	DSMON1[1]	DSMON1[0]	RES	R/W
		LSB	DSBT1[2]	DSBT1[1]	DSBT1[0]	RES	FT1[1]	FT1[0]	RES	P	
0x06	GD2CR1	MSB	SLEWC2[4]	SLEWC2[3]	SLEWC2[2]	SLEWC2[1]	SLEWC2[0]	DT2[3]	DT2[2]	DT2[1]	R/W
		LSB	DT2[0]	RES	SLEWD2[4]	SLEWD2[3]	SLEWD2[2]	SLEWD2[1]	SLEWD2[0]	P	
0x07	GD2CR2	MSB	RES	RES	RES	RES	DSMON2[2]	DSMON2[1]	DSMON2[0]	RES	R/W
		LSB	DSBT2[2]	DSBT2[1]	DSBT2[0]	RES	FT2[1]	FT2[0]	RES	P	
0x08	CSCR	MSB	RES	GCSA1[1]	GCSA1[0]	RES	DCSA1	RES	CSA1OO	RES	R/W
		LSB	RES	GCSA2[1]	GCSA2[0]	RES	DCSA2	RES	CSA2OO	P	
0x09	DIAGCR	MSB	DGVDHOVE	DGVDHUVE	DGVSOVWE	DGVDDOVE	DGTWE	DGTSDE	DGFSINE	DGNRDYE	R/W
		LSB	DGCPLOWE	DGWDGFE	DGDIOOVE	DGDS1E	DGSPIEE	DGDS2E	RES	P	
0x0A	WDGTRDIS	MSB	WDGTRDIS[14]	WDGTRDIS[13]	WDGTRDIS[12]	WDGTRDIS[11]	WDGTRDIS[10]	WDGTRDIS[9]	WDGTRDIS[8]	WDGTRDIS[7]	W
		LSB	WDGTRDIS[6]	WDGTRDIS[5]	WDGTRDIS[4]	WDGTRDIS[3]	WDGTRDIS[2]	WDGTRDIS[1]	WDGTRDIS[0]	P	
		MSB	RES	RES	RES	RES	RES	RES	RES	RES	R
		LSB	RES	RES	RES	WDGSTATUS	WDGINF[2]	WDGINF[1]	WDGINF[0]	P	
0x0B	RESVDO	MSB	RES_RW_14	RES_RW_13	RES_RW_12	RES_RW_11	RES_RW_10	RES_RW_9	RES_RW_8	RES_RW_7	R/W
		LSB	RES_RW_6	RES_RW_5	RES_RW_4	RES_RW_3	RES_RW_2	RES_RW_1	RES_RW_0	P	
0x0C	RESVDI	MSB	RES	RES	RES	RES	RES	RES	RES	RES_RO_7	R

Global status			GSBN	RSTB	SPIE	-	FE	DE	GW	FS	Mode
											R
Addr.	Name	Bits	15	14	13	12	11	10	9	8	
			7	6	5	4	3	2	1	0	
0x0C	RESVDI	LSB	RES_RO_6	RES_RO_5	RES_RO_4	RES_RO_3	RES_RO_2	RES_RO_1	RES_RO_0	P	R

6.3 Status registers

Table 44. Status register DSR1 (0x01) MSB

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (R/C)	0 (R/C)	0 (R/C)	0 (R/C)	0 (R/C)	0 (R/C)	0 (R)	0 (R)
VDHOV	VDHUV	VSOVW	VDDOV	TW	TSD	FSIN	NRDY
VDH overvoltage flag	VDH undervoltage flag	VS overvoltage warning flag	VDD overvoltage flag	Thermal warning flag	Thermal shutdown flag	Fail-safe input not bit	Charge pump not ready bit

Bit	Name	Description
15	VDHOV	VDH overvoltage flag. This flag is set and latched as soon as an overvoltage is detected on VDH supply. It can be cleared by SPI, only if the source of the fault is no longer present.
14	VDHUV	VDH undervoltage flag. This flag is set and latched as soon as an undervoltage is detected on VDH supply. It can be cleared by SPI, only if the source of the fault is no longer present.
13	VSOVW	VS overvoltage warning flag. This flag is set and latched as soon as an overvoltage is detected on VS supply. It can be cleared by SPI, only if the source of the fault is no longer present.
12	VDDOV	VDD overvoltage flag. This flag is set and latched as soon as an overvoltage is detected on VDD supply. It can be cleared by SPI, only if the source of the fault is no longer present.
11	TW	Thermal warning flag. This flag is set and latched as soon as device junction temperature exceeds TW threshold for a time longer than the corresponding filtering time. It can be cleared by SPI, only if the source of the fault is no longer present.
10	TSD	Thermal shutdown flag. This flag is set and latched as soon as device junction temperature exceeds TSD threshold for a time longer than the corresponding filtering time. It can be cleared by SPI, only if the source of the fault is no longer present.
9	FSIN	Fail-safe input not bit. This bit is the logic OR of DSR2 bits from BIT7 to BIT11. It is automatically set anytime the FSINB pin is pulled low for a time longer than the corresponding analog filtering time (t_{FSINB_filt}) and automatically reset anytime the FSINB pin is pulled high for a time longer than the analog filtering time and FSINHS1=FSINHS2=FSINLS1=FSINLS2=0. It is a read only bit, so it cannot be cleared by SPI. In case the FSINB pin is left floating, because of the internal pull-down at the FSINB pin, the value of this bit will be automatically set to one.
8	NRDY	Charge pump not ready bit. This bit is automatically set anytime the charge-pump is enabled and automatically reset a filtering time (t_{CP}) after its output voltage reaches CPLOW threshold (VCP_low). It is a read only bit, so it cannot be cleared by SPI.

Table 45. Status register DSR1 (0x01) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (R/C) (1)	0 (R/C)	0 (R/C)	0 (R/C)	0 (R/C)	0 (R/C)	0 (R/C)	
CPLOW	WDGF	DIOOV	DSHS1	DSLS1	DSHS2	DSLS2	P
Charge pump low flag/bit	Watchdog fault flag	Digital IO overvoltage flag	VDS monitoring flags				Parity bit

Bit	Name	Description
7	CPLOW	Charge pump low flag/bit. If CP_LOW_CONFIG control bit is set to one, the CPLOW is a read only status bit automatically set as soon as the charge pump output voltage falls below CPLOW threshold (VCP_low) for a time longer than the corresponding filtering time (t_{CP}) and automatically reset as soon as the charge pump output voltage rises back above CPLOW threshold for a time longer than the filtering time. If CP_LOW_CONFIG control bit is set to zero, the CPLOW is a read & clear status flag set and latched as soon as the charge pump output voltage falls below CPLOW threshold (VCP_low) for a time longer than the corresponding filtering time. The CLOW flag can be cleared by SPI, only if the source of the fault is no longer present.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
6	WDGF	Watchdog fault flag. This flag is set and latched as soon as a watchdog fault is detected. The flag can be cleared by proper SPI Read & Clear command.					
5	DIOOV	Digital IO overvoltage flag. This flag is set and latched as soon as an overvoltage is detected on any of the following digital input/output pins: PWM/IN1, DIR/IN2, DIAGN, CSO1, CSO2, CSN, SDI, SDO, CLK. It can be cleared by SPI, only if the source of the fault is no longer present.					
4	DSHS1	VDS monitoring flags. Flag DSxSn (x=L,S / n=1,2) is set and latched as soon as the VDS of the corresponding MOSFET exceeds the relative threshold (set by DSMON[3:0] bits) for a time longer than the corresponding filtering time or blanking plus filtering time, where the blanking time is applicable. It can be cleared by SPI, only if the source of the fault is no longer present.					
3	DSLS1						
2	DSHS2						
1	DSLS2						

1. *The CPLOW is a Read & Clear status flag or a read only status bit depending on the value of the control bit CP_LOW_CONFIG.*

Table 46. Status register DSR2 (0x02) MSB

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)
RES	RES	RES	RES	FSINLL	FSINHS1	FSINLS1	FSINHS2
Reserved bit	Reserved bit	Reserved bit	Reserved bit	Fail-safe input not logic level bit	Fail-safe input not effect on HS1 bit	Fail-safe input not effect on LS1 bit	Fail-safe input not effect on HS2 bit

Bit	Name	Description
15	RES	Reserved
14	RES	Reserved
13	RES	Reserved
12	RES	Reserved
11	FSINLL	Fail-safe input not logic level bit. This bit reflects the inverted logic level of the FSINB pin taking into account the corresponding analog filtering time (tFSINB_filt). This bit is automatically set anytime the FSINB pin is pulled low for a time longer than the corresponding filtering time and automatically reset anytime the FSINB pin is pulled high for a time longer than the filtering time. It is a read only bit, so it cannot be cleared by SPI. In case the FSINB pin is left floating, because of the internal pull-down at the FSINB pin, the bit is automatically set to one.
10	FSINHS1	Fail-safe input not effect on HS1 bit. This bit indicates whether the HS1 gate driver is configured in sink switch mode (FSINHS1=1) because of the FSINLL set to one or not (FSINHS1=0). In case of no faults the FSINHS1 bit should be automatically set once the FSINLL is set and automatically reset once the FSINLL is reset. It is a read only bit, so it cannot be cleared by SPI.
9	FSINLS1	Fail-safe input not effect on LS1 bit. This bit indicates whether the LS1 gate driver is configured in sink switch mode (FSINLS1=1) because of the FSINLL set to one or not (FSINLS1=0). In case of no faults the FSINLS1 bit should be automatically set once the FSINLL is set and automatically reset once the FSINLL is reset. It is a read only bit, so it cannot be cleared by SPI.
8	FSINHS2	Fail-safe input not effect on HS2 bit. This bit indicates whether the HS2 gate driver is configured in sink switch mode (FSINHS2=1) because of the FSINLL set to one or not (FSINHS2=0). In case of no faults the FSINHS2 bit should be automatically set once the FSINLL is set and automatically reset once the FSINLL is reset. It is a read only bit, so it cannot be cleared by SPI.

Table 47. **Status register DSR2 (0x02) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	
FSINLS2	RES	RES	RES	O1DS	RES	O2DS	P
Fail-safe input not effect on LS2 bit	Reserved bit	Reserved bit	Reserved bit	Output 1 digital status bit	Reserved bit	Output 2 digital status bit	Parity bit

Bit	Name	Description
7	FSINLS2	Fail-safe input not effect on LS2 bit. This bit indicates whether the LS2 gate driver is configured in sink switch mode (FSINLS2=1) because of the FSINLL set to one or not (FSINLS2=0). In case of no faults the FSINLS2 bit should be automatically set once the FSINLL is set and automatically reset once the FSINLL is reset. It is a read only bit, so it cannot be cleared by SPI.
6	RES	Reserved
5	RES	Reserved
4	RES	Reserved
3	O1DS	Output 1 digital status bit. This bit provides the SH1 output logic level respect to the programmed threshold in any operating conditions, no matter what the OUTE value is. When OUTE=0, this bit reflects the not filtered output of the LS1 off-state diagnostic comparator having the programmed OLTHH threshold. When OUTE=1, this bit reflects the not filtered output of the LS1 DSMonitoring comparator having the programmed VSCdx threshold.
2	RES	Reserved
1	O2DS	Output 2 digital status bit. This bit provides the SH2 output logic level respect to the programmed threshold in any operating conditions, no matter what the OUTE value is. When OUTE=0, this bit reflects the not filtered output of the LS2 off-state diagnostic comparator having the programmed OLTHH threshold. When OUTE=1, this bit reflects the not filtered output of the LS2 DSMonitoring comparator having the programmed VSCdx threshold.
0	P	Parity bit

6.4 Control registers

Table 48. **Control register DCR (0x03) MSB**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (R/W)(1)	0 (R/W)(2)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)
INPMODE	OUTE	AFWE	FWS	DIS1	DIS2	DSMON_CONFIG	OLH1L2
Input mode selection bit	Outputs enable bit	Active free-wheeling enable bit	Free-wheeling selection bit	Disable leg1 bit	Disable leg2 bit	DSMonitoring configuration bit	Open load in off-state bit

Bit	Name	Description
15	INPMODE	Input mode selection control bit: full-bridge mode (reset) or dual half-bridge mode (set). This bit can be modified only when OUTE is reset, otherwise its value is frozen and it cannot be changed.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
14	OUTE	Outputs enable control bit. Assuming that the FSINB pin is high, if this bit is reset, all the gate drivers are disabled and the MOSFTEs are passively shut down through the internal resistance connected between gate and source. Assuming that the FSINB pin is high, if this bit is set, all the gate drivers are enabled and the MOSFETs are turned on/off according to Table 2 or Table 3 depending on the INPMODE control bit value. Assuming the device in active mode, when the FSINB pin goes low, the MOSFETs gate drivers are forced in sink switch mode and the OUTE control bit is reset. While the FSINB pin is low, the OUTE control bit value is frozen and cannot be changed via SPI. When a watchdog fault occurs, setting the WDGF flag, the OUTE control bit is reset. While the WDGF flag is set, the OUTE control bit value is frozen and cannot be changed via SPI.						
13	AFWE	Active free-wheeling enable control bit. In case INPMODE is reset, this bit enables/disables active free-wheeling. When set it enables the active free-wheeling. When reset it disables the active free-wheeling. In case INPMODE is set, this bit has no effect.					
12	FWS	Free-wheeling selection control bit. In case INPMODE is reset and active free-wheeling is enabled (AFWE=1), this bit sets whether the active free-wheeling is performed on high side (FWS=1) or on low-side (FWS=0). In case INPMODE is reset and active free-wheeling is disabled (AFWE=0), this bit sets whether the passive free-wheeling is performed on high side (FWS=1) or on low-side (FWS=0).In case INPMODE is set, this bit has no effect.					
11	DIS1	Disable leg1,2 control bits. In case INPMODE is set, these bits switch-off both the external MOSFETs of leg 1 (DIS1=1) and/or leg 2 (DIS2=1). In case INPMODE is reset, these bits have no effect.					
10	DIS2						
9	DSMON_CONFIG	DSMonitoring configuration control bit. In case this bit is set and INPMODE is reset, any VDS monitoring fault will actively switch off all the full-bridge MOSFETs by configuring all the gate drivers in sink switch mode. In all the other cases INPMODE=1 or INPMODE=0 with DSMON_CONFIG=0 just the affected/offended half-bridge MOSFETs are actively switched off configuring the corresponding gate drivers in sink switch mode.					
8	OLH1L2	Open load in off-state control bit. This bit is really taken into account only when OUTE is reset, otherwise it is discarded (and related circuitry is disconnected from device power outputs). See Table 4. Full-bridge monitoring in off-mode.					

1. *The INPMODE will be a read only or a read and write control bit depending on the value of the control bit OUTE.*
2. *The OUTE is a read only or a read and write control bit depending on the logic level at the input pin FSINB and on the status flag WDGF value.*

Table 49. Control register DCR (0x03) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R)	0 (R)	
OLH2L1	OLTHH	CP_LOW_CONFIG	CPFDD	OVTS	RES	RES	P
Open load in off-state bit	Off-state diagnostic comparator threshold selection bit	Charge pump low configuration bit	Charge pump frequency dithering disable bit	Overvoltage threshold selection bit	Reserved bit	Reserved bit	Parity

Bit	Name	Description
7	OLH2L1	Open load in off-state control bit. This bit is really taken into account only when OUTE is reset, otherwise it is discarded (and related circuitry is disconnected from device power outputs). See Table 4. Full-bridge monitoring in off-modering in off-mode
6	OLTHH	Off-state diagnostic comparator threshold selection bit. The off-state diagnostic comparator threshold is set to 1/6VDH for OLTHH reset and to 5/6VDH for OLTHH set. See Table 4. Full-bridge monitoring in off-mode
5	CP_LOW_CONFIG	Charge pump low configuration control bit. Setting this bit, CPLOW status flag/bit behaves as a read only status bit and the outputs are re-activated automatically upon recovery of the charge pump output voltage. If this bit is reset, CPLOW status flag/bit behaves as a read & clear status flag so that the outputs are disabled until the CPLOW status flag is cleared. In this latter case, the charge pump output voltage has to rise above VCP_low for a time longer than the corresponding filtering time and CPLOW status flag has to be reset to re-enable device outputs.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
4	CPFDD	Charge pump frequency dithering disable control bit. If this bit is set the charge pump frequency dithering is disabled, otherwise it is enabled.					
3	OVTS	Overvoltage threshold selection control bit. In case this bit is reset, the VS/VDH overvoltage threshold is set to V_{SOVWT1}/ V_{DHOVT1}, otherwise it is set to V_{SOVWT2}/ V_{DHOVT2}.					
2	RES	Reserved					
1	RES	Reserved					
0	P	Parity					

Table 50. Control register GD1CR1 (0x04) MSB

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)
SLEWC1[4]	SLEWC1[3]	SLEWC1[2]	SLEWC1[1]	SLEWC1[0]	DT1[3]	DT1[2]	DT1[1]
Gate charge current configuration bits					Dead-time configuration bits		

Bit	Name	Description
15	SLEWC1[4]	Gate charge current configuration bits for the full-bridge (INPMODE=0) or for leg 1 (INPMODE=1). SLEWC1[4:0]=n sets gate charge current to n x IGMAX/31. Setting SLEWC1[4:0]=0 disables gate charge current control and enables gate charging through low impedance switches.
14	SLEWC1[3]	
13	SLEWC1[2]	
12	SLEWC1[1]	
11	SLEWC1[0]	
10	DT1[3]	Dead-time configuration control bits for the full-bridge (INPMODE=0) or for leg 1 (INPMODE=1). 0000=250ns 0001=500ns 0010=750ns 0011=1000ns 0100=1250ns … 1110=3750ns 1111=4000ns
9	DT1[2]	
8	DT1[1]	

Table 51. Control register GD1CR1 (0x04) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (R/W)	0 (R)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	
DT1[0]	RES	SLEWD1[4]	SLEWD1[3]	SLEWD1[2]	SLEWD1[1]	SLEWD1[0]	P
Dead-time configuration bit	Reserved bit	Gate discharge current configuration bits					Parity bit

Bit	Name	Description
7	DT1[0]	Dead-time current configuration control bit for the full-bridge (INPMODE=0) or for leg 1 (INPMODE=1).
6	RES	Reserved
5	SLEWD1[4]	Gate discharge current configuration bits for the full-bridge (INPMODE=0) or for leg 1 (INPMODE=1). SLEWD1[4:0]=n sets gate discharge current to n x IGMAX/31. Setting SLEWD1[4:0]=0 disables gate discharge current control and enables gate discharging through low impedance switches.
4	SLEWD1[3]	
3	SLEWD1[2]	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2	SLEWD1[1]	Gate discharge current configuration bits for the full-bridge (INPMODE=0) or for leg 1 (INPMODE=1). SLEWD1[4:0]=n sets gate discharge current to n x IGMAX/31. Setting SLEWD1[4:0]=0 disables gate discharge current control and enables gate discharging through low impedance switches.						
1	SLEWD1[0]						
0	P	Parity bit					

Table 52. Control register GD1CR2 (0x05) MSB

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (R)	0 (R)	0 (R)	0 (R)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R)
RES	RES	RES	RES	DSMON1[2]	DSMON1[1]	DSMON1[0]	RES
Reserved bit	Reserved bit	Reserved bit	Reserved bit	VDS monitoring threshold configuration bits			Reserved bit

Bit	Name	Description
15	RES	Reserved
14	RES	
13	RES	
12	RES	
11	DSMON1[2]	VDS monitoring threshold configuration control bits for the full-bridge (INPMODE=0) or for leg 1 (INPMODE=1). 000=0.075V 001=0.15V 010=0.25V 011=0.4V 100=0.6V 101=0.8V 110=1V 111=1.2V
10	DSMON1[1]	
9	DSMON1[0]	
8	RES	Reserved

Table 53. Control register GD1CR2 (0x05) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (R/W)	0 (R/W)	0 (R/W)	0 (R)	0 (R/W)	0 (R/W)	0 (R)	
DSBT1[2]	DSBT1[1]	DSBT1[0]	RES	FT1[1]	FT1[0]	RES	P
VDS monitoring blanking time configuration bits			Reserved bit	VDS monitoring filtering time configuration bits		Reserved bit	Parity bit

Bit	Name	Description
7	DSBT1[2]	VDS monitoring blanking time configuration control bits for the full-bridge (INPMODE=0) or for leg 1 (INPMODE=1). Blanking time in µs = DSBT1[2:0] + 1 (min= 1us, max= 8us)
6	DSBT1[1]	
5	DSBT1[0]	
4	RES	Reserved
3	FT1[1]	VDS monitoring filtering time configuration control bits for the full-bridge (INPMODE=0) or for leg 1 (INPMODE=1). Filter time in µs = (FT1[1:0] + 1)*1.5 (min= 1.5us, max= 6us)
2	FT1[0]	
1	RES	Reserved

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	P	Parity bit					

Table 54. Control register GD2CR1 (0x06) MSB

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)
SLEWC2[4]	SLEWC2[3]	SLEWC2[2]	SLEWC2[1]	SLEWC2[0]	DT2[3]	DT2[2]	DT2[1]
Gate charge current configuration bits					Dead-time configuration bits		

Bit	Name	Description
15	SLEWC2[4]	Gate charge current configuration bits for the leg 2 in case INPMODE are set. These bits have no effect if INPMODE is reset. SLEWC2[4:0]=n sets gate charge current to n x IGMAX/31. Setting SLEWC2[4:0]=0 disables gate charge current control and enables gate charging through low impedance switches.
14	SLEWC2[3]	
13	SLEWC2[2]	
12	SLEWC2[1]	
11	SLEWC2[0]	
10	DT2[3]	Dead-time configuration bits for the leg 2 in case INPMODE is set. These bits have no effect if INPMODE is reset. 0000=250ns 0001=500ns 0010=750ns 0011=1000ns 0100=1250ns … 1110=3750ns 1111=4000ns
9	DT2[2]	
8	DT2[1]	

Table 55. Control register GD2CR1 (0x06) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (R/W)	0 (R)	0 (R)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	
DT2[0]	RES	SLEWD2[4]	SLEWD2[3]	SLEWD2[2]	SLEWD2[1]	SLEWD2[0]	P
Dead-time configuration bit	Reserved bit	Gate discharge current configuration bits					Parity bit

Bit	Name	Description
7	DT2[0]	Dead-time configuration control bit for the leg 2 in case INPMODE is set. This bit has no effect if INPMODE is reset.
6	RES	Reserved
5	SLEWD2[4]	Gate discharge current configuration bits for the leg 2 in case INPMODE is set. These bits have no effect if INPMODE is reset. SLEWD2[4:0]=n sets gate discharge current to n x IGMAX/31. Setting SLEWD2[4:0]=0 disables gate discharge current control and enables gate discharging through low impedance switches.
4	SLEWD2[3]	
3	SLEWD2[2]	
2	SLEWD2[1]	
1	SLEWD2[0]	
0	P	Parity bit

Table 56. **Control register GD2CR2 (0x07) MSB**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (R)	0 (R)	0 (R)	0 (R)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R)
RES	RES	RES	RES	DSMON2[2]	DSMON2[1]	DSMON2[0]	RES
Reserved bit	Reserved bit	Reserved bit	Reserved bit	VDS monitoring threshold configuration bits			Reserved bit

Bit	Name	Description
15	RES	Reserved
14	RES	
13	RES	
12	RES	
11	DSMON2[2]	VDS monitoring threshold configuration control bits for the leg 2 in case INPMODE are set. These bits have no effect if INPMODE is reset. 000=0.075V 001=0.15V 010=0.25V 011=0.4V 100=0.6V 101=0.8V 110=1V 111=1.2V
10	DSMON2[1]	
9	DSMON2[0]	
8	RES	

Table 57. **Control register GD2CR2 (0x07) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (R/W)	0 (R/W)	0 (R/W)	0 (R)	0 (R/W)	0 (R/W)	0 (R)	
DSBT2[2]	DSBT2[1]	DSBT2[0]	RES	FT2[1]	FT2[0]	RES	P
VDS monitoring blanking time configuration bits			Reserved bit	VDS monitoring filter time configuration bits		Reserved bit	Parity bit

Bit	Name	Description
7	DSBT2[2]	VDS monitoring blanking time configuration control bits for the leg 2 in case INPMODE are set. These bits have no effect if INPMODE is reset. Blanking time in µs = DSBT2[2:0] + 1 (min= 1 µs, max= 8 µs)
6	DSBT2[1]	
5	DSBT2[0]	
4	RES	Reserved
3	FT2[1]	VDS monitoring filtering time configuration control bits for the leg 2 in case INPMODE are set. These bits have no effect if INPMODE is reset. Filter time in µs = (FT2[1:0] + 1)*1.5 (min= 1.5 µs, max= 6 µs)
2	FT2[0]	
1	RES	Reserved
0	P	Parity bit

Table 58. **Control register CSCR (0x08) MSB**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (R)	0 (R/W)	0 (R/W)	0 (R)	0 (R/W)	0 (R)	0 (R/W)	0 (R)
RES	GCSA1[1]	GCSA1[0]	RES	DCSA1	RES	CSA1OO	RES

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reserved bit	CSA1 gain selection bits		Reserved bit	CSA1 disable bit	Reserved bit	CSA1 output offset bit	Reserved bit

Bit	Name	Description
15	RES	Reserved
14	GCSA1[1]	CSA1 gain selection control bits.
13	GCSA1[0]	00=10 01=20 10=50 11=100
12	RES	Reserved
11	DCSA1	CSA1 disable control bit. If this control bit is set the CSA1 is disabled, otherwise it is enabled.
10	RES	Reserved
9	CSA1OO	CSA1 output offset control bit. If this bit is reset, the output offset is set to VO0, otherwise it is set to VO1.
8	RES	Reserved

Table 59. Control register CSCR (0x08) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (R)	0 (R/W)	0 (R/W)	0 (R)	0 (R/W)	0 (R)	0 (R/W)	
RES	GCSA2[1]	GCSA2[0]	RES	DCSA2	RES	CSA2OO	P
Reserved bit	CSA2 gain selection bits		Reserved bit	CSA2 disable bit	Reserved bit	CSA2 output offset bit	Parity bit

Bit	Name	Description
7	RES	Reserved
6	GCSA2[1]	CSA2 gain selection control bits.
5	GCSA2[0]	00=10 01=20 10=50 11=100
4	RES	Reserved
3	DCSA2	CSA2 disable control bit. If this control bit is set the CSA2 is disabled, otherwise it is enabled.
2	RES	Reserved
1	CSA2OO	CSA2 output offset control bit. If this bit is reset, the output offset is set to VO0, otherwise it is set to VO1.
0	P	Parity bit

Table 60. Diagnostic control register DIAGCR (0x09) MSB

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)
DGVDHOVE	DGVDHUVE	DGVSOVWE	DGVDDOVE	DGTWE	DGTSDE	DGFSINE	DGNRDYE
Diagnostic output VDHOV enable bit	Diagnostic output VDHUV enable bit	Diagnostic output VSOVW enable bit	Diagnostic output VDDOV enable bit	Diagnostic output TW enable bit	Diagnostic output TSD enable bit	Diagnostic output FSIN enable bit	Diagnostic output NRDY enable bit

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Bit	**Name**	**Description**					
15	DGVDHOVE	Diagnostic output VDHOV enable control bit. Setting this bit enables VDHOV status flag to be mapped on diagnostic output pin (DIAGN).					
14	DGVDHUVE	Diagnostic output VDHUV enable control bit. Setting this bit enables VDHUV status flag to be mapped on diagnostic output pin (DIAGN).					
13	DGVSOVWE	Diagnostic output VSOVW enable control bit. Setting this bit enables VSOVW status flag to be mapped on diagnostic output pin (DIAGN).					
12	DGVDDOVE	Diagnostic output VDDOV enable control bit. Setting this bit enables VDDOV status flag to be mapped on diagnostic output pin (DIAGN).					
11	DGTWE	Diagnostic output TW enable control bit. Setting this bit enables TW status flag to be mapped on diagnostic output pin (DIAGN).					
10	DGTSDE	Diagnostic output TSD enable control bit. Setting this bit enables TSD status flag to be mapped on diagnostic output pin (DIAGN).					
9	DGFSINE	Diagnostic output FSIN enable control bit. Setting this bit enables FSIN status bit to be mapped on diagnostic output pin (DIAGN).					
8	DGNRDYE	Diagnostic output NRDY enable control bit. Setting this bit enables NRDY status bit to be mapped on diagnostic output pin (DIAGN).					

Table 61. Diagnostic control register DIAGCR (0x09) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R)	
DGCPLOWE	DGWDGFE	DGDIOOVE	DGDS1E	DGSPIEE	DGDS2E	RES	P
Diagnostic output CPLOW enable bit	Diagnostic output WDGF enable bit	Diagnostic output DIOOV enable bit	Diagnostic output leg 1 drain-source monitoring enable bit	Diagnostic output SPIE enable bit	Diagnostic output leg 2 drain-source monitoring enable bit	Reserved bit	Parity bit
Bit	**Name**	**Description**					
7	DGCPLOWE	Diagnostic output CPLOW enable control bit. Setting this bit enables CPLOW status flag/bit to be mapped on diagnostic output pin (DIAGN).					
6	DGWDGFE	Diagnostic output WDGF enable control bit. Setting this bit enables WDGF status flag to be mapped on diagnostic output pin (DIAGN).					
5	DGDIOOVE	Diagnostic output DIOOV enable control bit. Setting this bit enables DIOOV status flag to be mapped on diagnostic output pin (DIAGN).					
4	DGDS1E	Diagnostic output DS1 enable control bit. Setting this bit enables DSHS1 and DSLS1 status flags to be mapped on diagnostic output pin (DIAGN).					
3	DGSPIEE	Diagnostic output SPIE enable control bit. Setting this bit enables SPIE global status byte bit to be mapped on diagnostic output pin (DIAGN).					
2	DGDS2E	Diagnostic output DS2 enable control bit. Setting this bit enables DSHS2 and DSLS2 status flags to be mapped on diagnostic output pin (DIAGN).					
1	RES	Reserved					
0	P	Parity bit					

Table 62. Watchdog trigger/disable register WDGTRDIS (0x0A) MSB

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Register write access							
WDGTRDIS[14]	WDGTRDIS[13]	WDGTRDIS[12]	WDGTRDIS[11]	WDGTRDIS[10]	WDGTRDIS[9]	WDGTRDIS[8]	WDGTRDIS[7]
Watchdog trigger/disable bits							

Bit	Name	Description
15	WDGTRDIS[14]	The register can be used either to disable the watchdog or to trigger the watchdog Watchdog trigger/disable bits. In order to trigger the watchdog all the register bits must toggle within the watchdog open window. The first trigger word must be 5555h, this value puts an end to the watchdog long open window and turn the watchdog in window mode. The following trigger values must be 2AAAh, 5555h, 2AAAh and so on. To disable the watchdog, the microcontroller has to send a specific key, consisting in two consecutive words, corresponding to two consecutive valid SPI transfers (without any other SPI transfer between the two of them), during any watchdog long open window. The keys to disable the watchdog are 2F6Bh (first key word) and 1097h (second key word). The two words key has to be sent in the right order, otherwise the watchdog will not be disabled, and a watchdog fault will be generated. **First trigger bits value (5555h): 101010101010101b** **Second trigger bits value (2AAAh): 010101010101010b** **First part of the disable key (2F6Bh): 010111101101011b** **Second part of the disable key (1097h): 001000010010111b**
14	WDGTRDIS[13]	
13	WDGTRDIS[12]	
12	WDGTRDIS[11]	
11	WDGTRDIS[10]	
10	WDGTRDIS[9]	
9	WDGTRDIS[8]	
8	WDGTRDIS[7]	

Table 63. Watchdog trigger/disable register WDGTRDIS (0x0A) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Register write access							
WDGTRDIS[6]	WDGTRDIS[5]	WDGTRDIS[4]	WDGTRDIS[3]	WDGTRDIS[2]	WDGTRDIS[1]	WDGTRDIS[0]	P
Watchdog trigger/disable bits							Parity bit

Bit	Name	Description
7	WDGTRDIS[6]	The register can be used either to disable the watchdog or to trigger the watchdog Watchdog trigger/disable bits. In order to trigger the watchdog all the register bits must toggle within the watchdog open window. The first trigger word must be 5555h, this value puts an end to the watchdog turn open window and turn the watchdog in window mode. The following trigger values must be 2AAAh, 5555h, 2AAAh and so on. In order to disable the watchdog, the microcontroller has to send a specific key, consisting in two consecutive words, corresponding to two consecutive valid SPI transfers (without any other SPI transfer between the two of them), during any watchdog long open window. The keys to disable the watchdog are 2F6Bh (first key word) and 1097h (second key word). The two words key has to be sent in the right order, otherwise the watchdog will not be disabled and a watchdog fault will be generated. **First trigger bits value (5555h): 101010101010101b** **Second trigger bits value (2AAAh): 010101010101010b** **First part of the disable key (2F6Bh): 010111101101011b** **Second part of the disable key (1097h): 001000010010111b**
6	WDGTRDIS[5]	
5	WDGTRDIS[4]	
4	WDGTRDIS[3]	
3	WDGTRDIS[2]	
2	WDGTRDIS[1]	
1	WDGTRDIS[0]	
0	P	Parity bit

Table 64. Watchdog trigger/disable register WDGTRDIS (0x0A) MSB

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Register Read Access							
0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)
RES	RES	RES	RES	RES	RES	RES	RES

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reserved bit	Reserved bit	Reserved bit	Reserved bit	Reserved bit	Reserved bit	Reserved bit	Reserved bit

Bit	Name	Description
15	RES	Reserved
14	RES	
13	RES	
12	RES	
11	RES	
10	RES	
9	RES	
8	RES	

Table 65. Watchdog trigger/disable register WDGTRDIS (0x0A) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Register read access							
0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	
RES	RES	RES	WDGSTATUS	WDGINF2]	WDGINF[1]	WDGINF[0]	P
Reserved bit	Reserved bit	Reserved bit	Watchdog status bit	Watchdog information bits			Parity bit

Bit	Name	Description
7	RES	Reserved
6	RES	
5	RES	
4	WDGSTATUS	Watchdog status bit. This bit is set if the watchdog has been successfully disabled. This bit is reset if the watchdog is enabled.
3	WDGINF[2]	Watchdog information bits. These bits represent the three least significant bits of the latest write command performed on the same register. For example, they will return ”101" after first trigger WDGTRDIS[15:1]=5555h, then ”010" after second trigger WDGR[15:1]=2AAAh. It will return ""111" after writing the second key WDGR[15:1]=1097h. Since no other SPI transfer should fall between the two words that form the key during the procedure to disable the watchdog, ”011" shall not be read after first part of the key write command WDGR[15:1]=2F6Bh, otherwise the disabling procedure will be aborted generating a watchdog fault.
2	WDGINF[1]	
1	WDGINF[0]	
0	P	Parity bit

Table 66. Reserved bits RESVDO (0x0B) MSB

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)
RES_RW_14	RES_RW_13	RES_RW_12	RES_RW_11	RES_RW_10	RES_RW_9	RES_RW_8	RES_RW_7
Reserved bit	Reserved bit	Reserved bit	Reserved bit	Reserved bit	Reserved bit	Reserved bit	Reserved bit

Bit	Name	Description
15	RES_RW_14	Reserved
14	RES_RW_13	
13	RES_RW_12	
12	RES_RW_11	
11	RES_RW_10	

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
10	RES_RW_9	Reserved					
9	RES_RW_8						
8	RES_RW_7						

Table 67. Reserved bits RESVDO (0x0B) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	
RES_RW_6	RES_RW_5	RES_RW_4	RES_RW_3	RES_RW_2	SLEW2	SLEW1	P
Reserved bit	Reserved bit	Reserved bit	Reserved bit	Reserved bit	Source and sink gate current threshold	Source and sink gate current threshold	Parity bit

Bit	Name	Description
7	RES_RW_6	Reserved
6	RES_RW_5	
5	RES_RW_4	
4	RES_RW_3	
3	RES_RW_2	
2	SLEW2	Source and sink gate current threshold configuration for HS and LS in current mode
1	SLEW1	00 => Higher threshold for source and sink current (typ 170 mA) 11 => Lower threshold for source and sink current (typ 85 mA)
0	P	Parity bit

Table 68. Reserved bits RESVDI (0x0C) MSB

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)
RES	RES	RES	RES	RES	RES	RES	RES_RO_7
Reserved bit	Reserved bit	Reserved bit	Reserved bit	Reserved bit	Reserved bit	Reserved bit	Reserved bit

Bit	Name	Description
15	RES	Reserved
14	RES	
13	RES	
12	RES	
11	RES	
10	RES	
9	RES	
8	RES_RO_7	

Table 69. Reserved bits RESVDI (0x0C) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	
RES_RO_6	RES_RO_5	RES_RO_4	RES_RO_3	RES_RO_2	RES_RO_1	RES_RO_0	P
Reserved bit	Reserved bit	Reserved bit	Reserved bit	Reserved bit	Reserved bit	Reserved bit	Parity bit

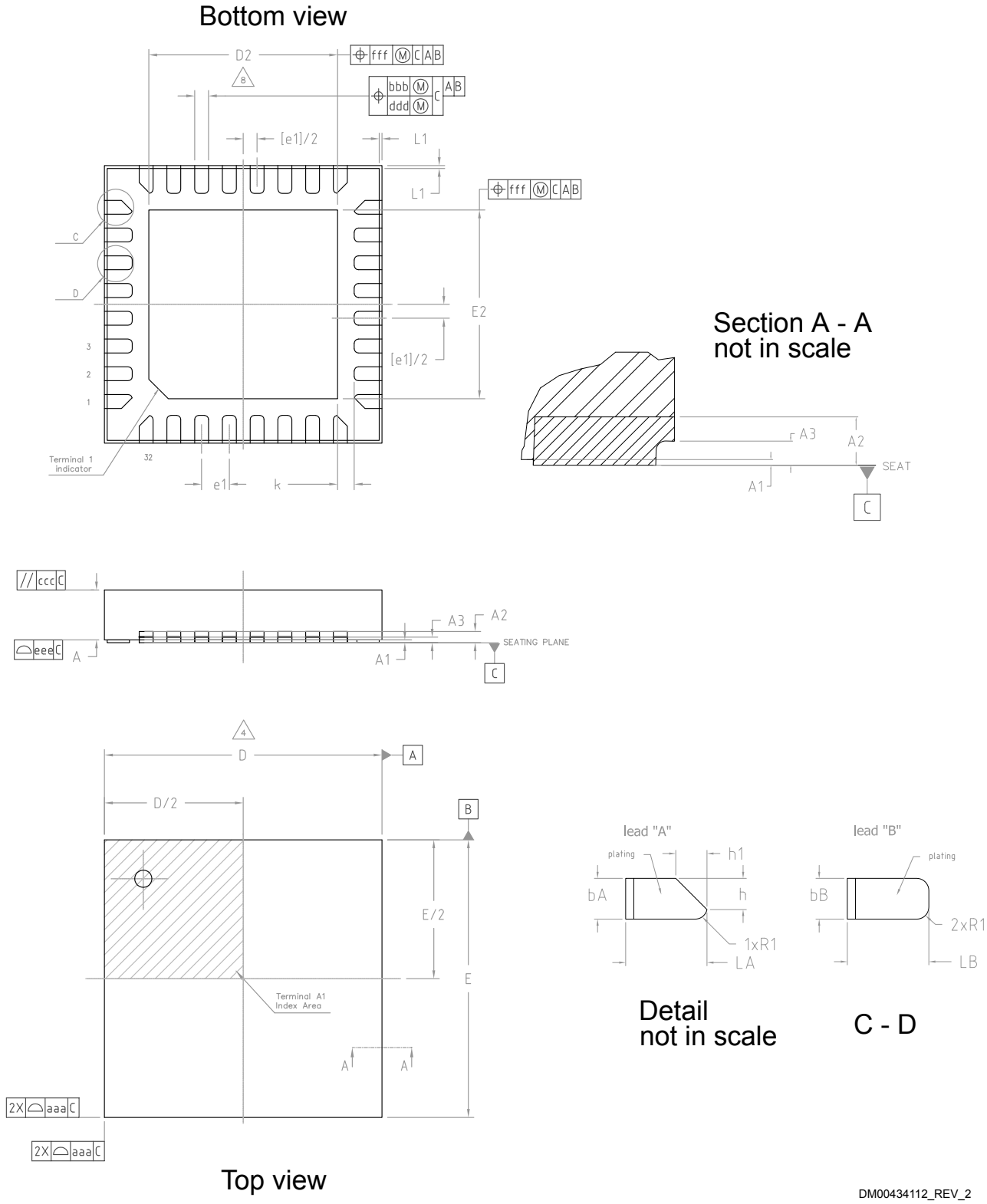
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit	**Name**	**Description**					
7	RES_RO_6	Reserved					
6	RES_RO_5						
5	RES_RO_4						
4	RES_RO_3						
3	RES_RO_2						
2	RES_RO_1						
1	RES_RO_0						
0	P	Parity bit					

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 QFN32L 5x5 mm package information

Figure 26. **QFN32L 5x5 mm package outline**



DM00434112_REV_2

Table 70. **QFN32L 5x5 mechanical data**

Ref.	Dimension		
	Millimeters		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0		0.05
A2		0.2 REF	
A3	0.1		
D		5.00 BSC	
D2		VARIATIONS	
E		5.00 BSC	
E2		VARIATIONS	
e1		0.5 BSC	
k	0.20		
L1			0.05
La	0.40	0.50	0.60
bA	0.20	0.25	0.30
h		0.19 REF	
h1		0.19 REF	
LB	0.45	0.5	0.55
bB	0.20	0.25	0.30
N		32	
R1			0.1

Table 71. **Tolerance of form and position**

Symbol	Tolerance
aaa	0.15
bbb	0.10
ccc	0.10
ddd	0.05
eee	0.08
fff	0.10

Table 72. **Variations of form and position**

Symbol	Variations			
	Min.	Nom.	Max.	Pad opt.
D2	3.40	3.50	3.60	
E2	3.40	3.50	3.60	

7.2 TQFP32L 7x7 mm package information

Figure 27. **TQFP32L 7x7 mm package outline**

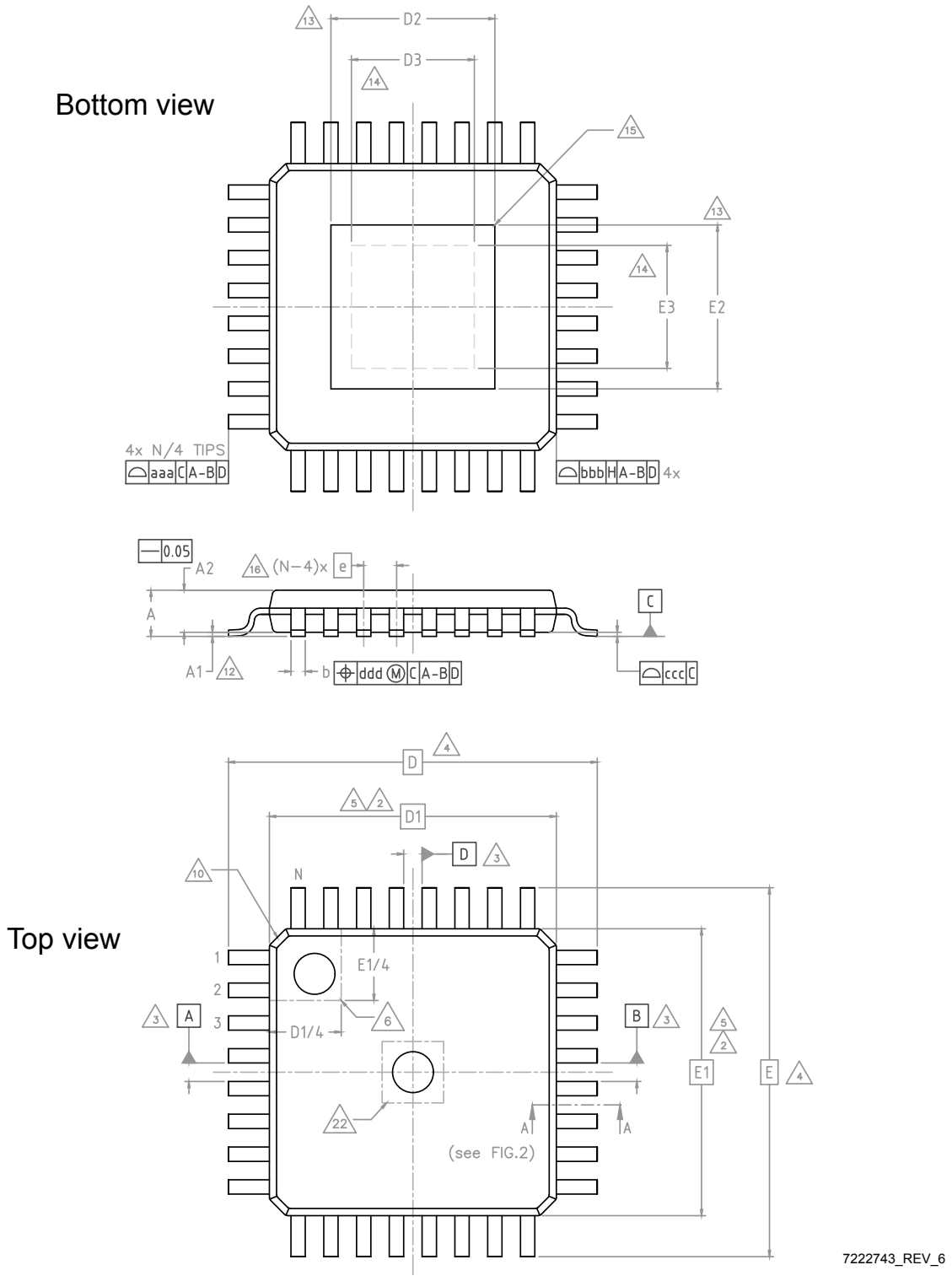


Table 73. **TQFP32L 7x7 mm mechanical data**

Ref.	Dimension		
	Millimeters		
	Min.	Typ.	Max.
ϕ	0°	3.5°	7°
ϕ1	0°		
ϕ2	10°	12°	14°
ϕ3	10°	12°	14°
A			1.20
A1	0.05		0.15
A2	0.95	1.00	1.05
b	0.30	0.37	0.45
b1	0.30	0.35	0.40
c	0.09		0.20
c1	0.09		0.16
D	9.00 BSC		
D1	7.00 BSC		
D2	VARIATIONS		
D3	VARIATIONS		
e	0.80 BSC		
E	9.00 BSC		
E1	7.00 BSC		
E2	VARIATIONS		
E3	VARIATIONS		
L	0.45	0.60	0.75
L1	1.00 REF		
N	32		
R1	0.08		
R2	0.08		0.20
S	0.20		

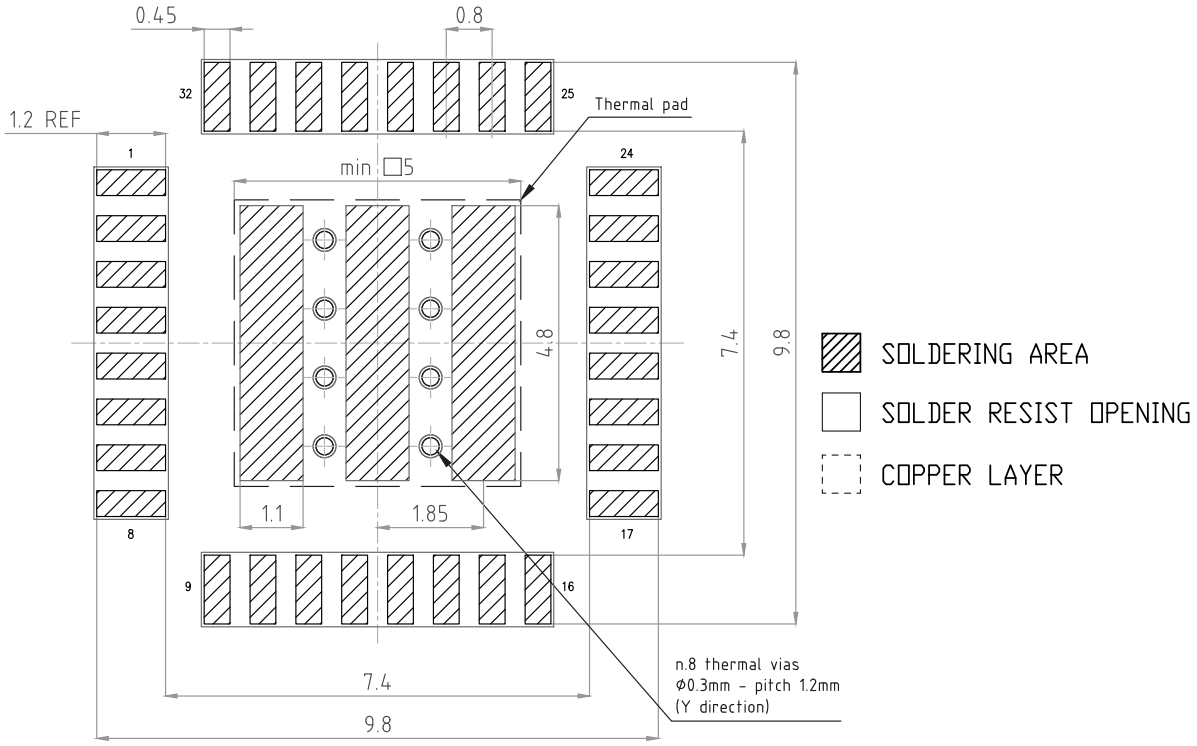
Table 74. **Tolerance of form and position**

Symbol	Tolerance
aaa	0.20
bbb	0.20
ccc	0.10
ddd	0.10

Table 75. **Variations of form and position**

Symbol	Variations			
	Min.	Nom.	Max.	Pad opt.
D2			5.37	5.0x5.0 (T1)
E2			5.37	
D3	3.40			
E3	3.40			

Figure 28. **TQFP32L 7x7 mm footprint**



Revision history

Table 76. **Document revision history**

Date	Revision	Changes
04-Oct-2022	1	Initial release.
24-Feb-2023	2	Updated *Table 24. Supply, supply monitoring*, *Table 27. Full-bridge driver*, *Table 32. Input: ENABLE* and *Table 34. Watchdog*. Updated *Figure 20. SPI input timing* and *Figure 21. SPI output timing*. Minor text changes.
04-May-2023	3	Updated *Section Features* and *Table 27. Full-bridge driver*. Package changed to TQFP32 7x7. The document has been updated accordingly. Minor text changes.
03-Jul-2023	4	Added device in QFN32L. Document updated accordingly.

Contents

List of tables

List of figures

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.