# ft2810D

## 3.2W *Dual-Pump*™ Class-G Audio Power Amplifier

## GENERAL DESCRIPTION

The ft2810D is a highly efficient 3.2W Class-G audio power amplifier for use in battery-based portable device applications. It integrates a filterless Class-D audio power amplifier with a Class-G charge pump regulator based upon proprietary ***Dual-Pump***™ topology. It operates from 3.2V to 4.6V supply. With a 3.6V supply voltage, the ft2810D is capable of delivering into 4Ω load with maximum output power of 3.2W at 10% THD+N in Non-ALC mode, or constant output power of 2.8W at 0.3% THD+N in ALC mode. Its high efficiency, up to 85%, helps extend battery life.

In ft2810D, the power supply rail for the amplifier's output stage is internally boosted and regulated at 6V by an on-chip adaptive charge pump regulator based upon the ***Dual-Pump***™ topology, thus allowing for a much louder audio output than a stand-alone one directly connected to the battery. It makes ft2810D an ideal audio solution for portable devices that are powered by a single-cell lithium battery while requiring higher audio loudness.

The ft2810D features ALC on the audio output signals, which detects the output clipping caused by the over-level input signal and automatically adjusts the voltage gain of the amplifier to eliminate the clipping while maintaining a maximally-allowed dynamic range of the audio output signals. The ALC also eliminates the output clipping due to low battery supply voltage.

## FEATURES

- Proprietary ***Dual-Pump***™ topology
- Filterless Class-D audio amplifier integrated with an adaptive Class-G charge pump regulator
- Automatic level control to eliminate output clipping
- Maximum output power (Non-ALC Mode)
  - 3.2W ($V_{DD}$=3.6V, THD+N=10%, $R_L$=4Ω+33μF)
  - 2.2W ($V_{DD}$=3.6V, THD+N=10%, $R_L$=8Ω+33μF)
- Constant output power (ALC Mode)
  - 2.8W ($V_{DD}$=3.6V, THD+N=0.3%, $R_L$=4Ω+33μF)
  - 1.8W ($V_{DD}$=3.6V, THD+N=0.3%, $R_L$=8Ω+33μF)
- High power efficiency up to 85% ($R_L$=8Ω+33μF)
- Low THD+N: 0.05%
  ($V_{DD}$=3.6V, f=1kHz, $R_L$=8Ω+33μF, Po=1W)
- Low quiescent current: 2.6mA @ $V_{DD}$=3.6V
- High PSRR: 76dB @ 217Hz with $R_L$=8Ω+33μF
- Two gain settings: 28dB/24dB
- One-wire pulse control for the selection of operating mode and voltage gain
- Auto-recovering short-circuit protection
- Available in TQFN-3×3-20AL package

## APPLICATIONS

- Blue-Tooth Speakers
- Mobile Phones
- Tablets
- Portable Multimedia Devices

## APPLICATION CIRCUITS

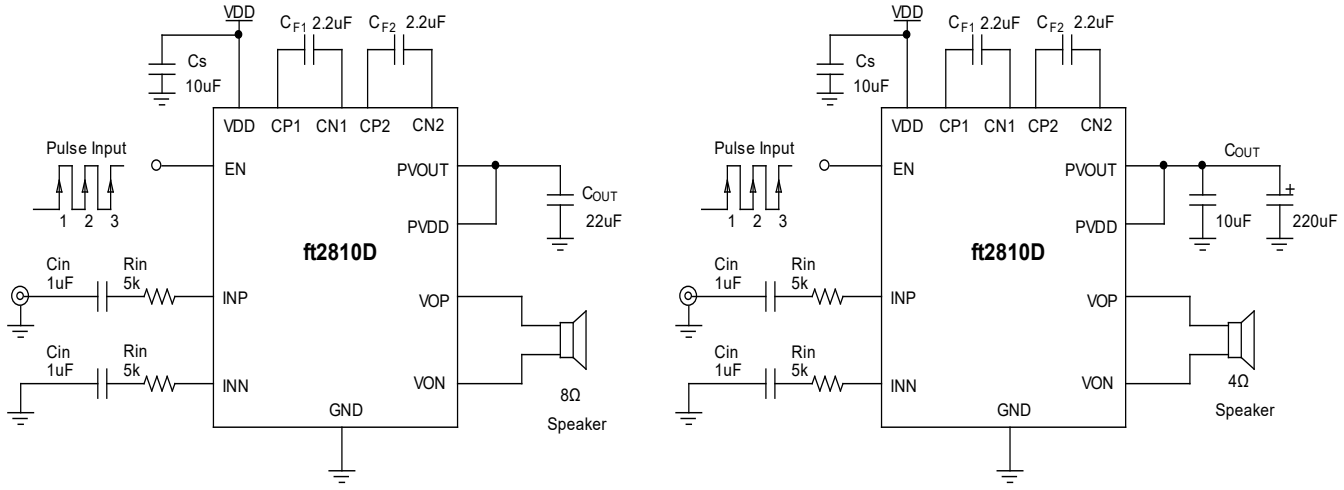
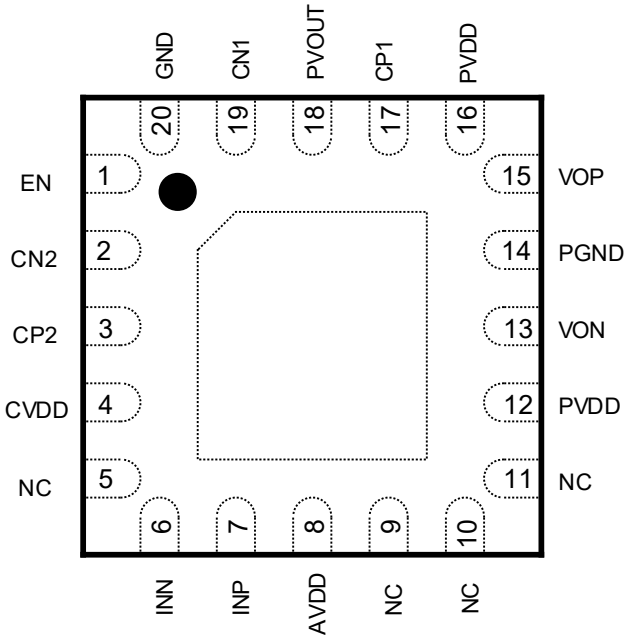



**Figure 1: Typical Application Circuit Diagram of ft2810D**

## PIN CONFIGURATION AND DESCRIPTION




**TOP VIEW**

| SYMBOL | PIN # | I/O | DESCRIPTION |
|---|---|---|---|
| EN | 1 | I | Chip enable & one-wire pulse control. |
| CN2 | 2 | O | Flying capacitor $C_{F2}$ negative terminal. |
| CP2 | 3 | O | Flying capacitor $C_{F2}$ positive terminal. |
| CVDD | 4 | P | Power supply for the charge pump regulator. |
| INN | 6 | I | Negative audio input terminal. |
| INP | 7 | I | Positive audio input terminal. |
| AVDD | 8 | P | Analog power supply. |
| PVDD | 12, 16 | P | Power supply rail for the amplifier output stage. It must be externally shorted to PVOUT. |
| VON | 13 | O | Negative BTL audio output. |
| PGND | 14 | G | Ground. |
| VOP | 15 | O | Positive BTL audio output. |
| CP1 | 17 | O | Flying capacitor $C_{F1}$ positive terminal. |
| PVOUT | 18 | O | Boosted voltage output generated by the charge pump regulator. It must be externally shorted to PVDD on the system board. |
| CN1 | 19 | O | Flying capacitor $C_{F1}$ negative terminal. |
| GND | 20 | G | Ground. |
| NC | 5, 9, 10, 11 | - | No internal connection. |

## ORDERING INFORMATION

| PART NUMBER | TEMPERATURE RANGE | PACKING OPTION | PACKAGE |
|---|---|---|---|
| Ft2810DQ | -40°C to +85°C | Tape and Reel, 5000 | TQFN-3×3-20AL |

## ABSOLUTE MAXIMUM RATINGS (Note 1)

| PARAMETER | VALUE |
|---|---|
| Supply Voltage, $V_{DD}$ (AVDD, CVDD) | -0.3V to 5.5V |
| PVOUT, PVDD, CP1, CP2 | -0.3V to 6.5V |
| All Other Pins | -0.3V to $V_{DD}$+0.3V |
| Continuous Total Power Dissipation | Internally Limited |
| ESD Ratings - Human Body Model (HBM) | 1500V |
| Operating Junction Temperature | -40℃ to +150℃ |
| Maximum Soldering Temperature (@10 sec duration) | 260℃ |
| Storage Temperature | -65℃ to +150℃ |

Note 1: Stresses beyond those listed under absolute maximun ratings may cause permanent damage to the device. These are stress ratings only,and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied.Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## POWER DISSIPATION RATINGS (Note 2)

| PACKAGE | $T_A \leq$ +25℃ | $T_A$ = +70℃ | $T_A$ = +85℃ | $\Theta_{JA}$ |
|---|---|---|---|---|
| TQFN-3×3-20AL | 2.60W | 1.67W | 1.35W | 48℃/W |

Note 2: The thermal pad of the package mus be directly soldered onto a grounded metal island (as a thermal sink) on the system board.

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Supply Voltage, $V_{DD}$ | AVDD, CVDD | 3.2 | | 4.6 | V |
| Operating Free-Air Temperature, $T_A$ | | -40 | | 85 | ℃ |
| Minimum Load Resistance, $R_{LOAD}$ | | 3.6 | | | Ω |

## IMPORTANT APPLICATION NOTES

1. The ft2810D is a high performance Class-G audio amplifier with an exposed thermal pad underneath the device. The thermal pad must be directly soldered onto a grounded metal island as a thermal sink for proper power dissipation. Failure to do so may result in the device entering into thermal overload protection.
2. The ft2810D requires adequate power supply decoupling to ensure its optimum performance in output power, efficiency, THD, and EMI emissions. Place respective decoupling capacitors as individually close to the device's AVDD, CVDD, and PVDD pins as possible.
3. It is strongly recommended to employ a ground plane for ft2810D on the system board. Also, place a small decoupling resistor between AVDD and CVDD to prevent high frequency Class-D transient spikes from interfering with the on-chip linear amplifiers.
4. Use a simple ferrite bead filter for further EMI suppression. Choose a ferrite bead with a rated current no less than 2A or greater for applications with a load resistance less than 6Ω. Also, place the respective ferrite beard filters as close to VOP and VON pins as possible.
5. To avoid excessive load current flowing back into the boosted voltage PVOUT via the Class-D high-side output stage, use speakers with limited phase shift (between voltage and phase) or add a 6.3V Zener diode between PVOUT and ground to ensure the PVOUT voltage does not exceed its absolute maximum rating.
6. Although the Class-D audio amplifier's output stage can withstand a short between VOP and VON, do not connect either output directly to GND, PGND, PVDD, CVDD, or AVDD as this might damage the device.

## FUNCTIONAL BLOCK DIAGRAM

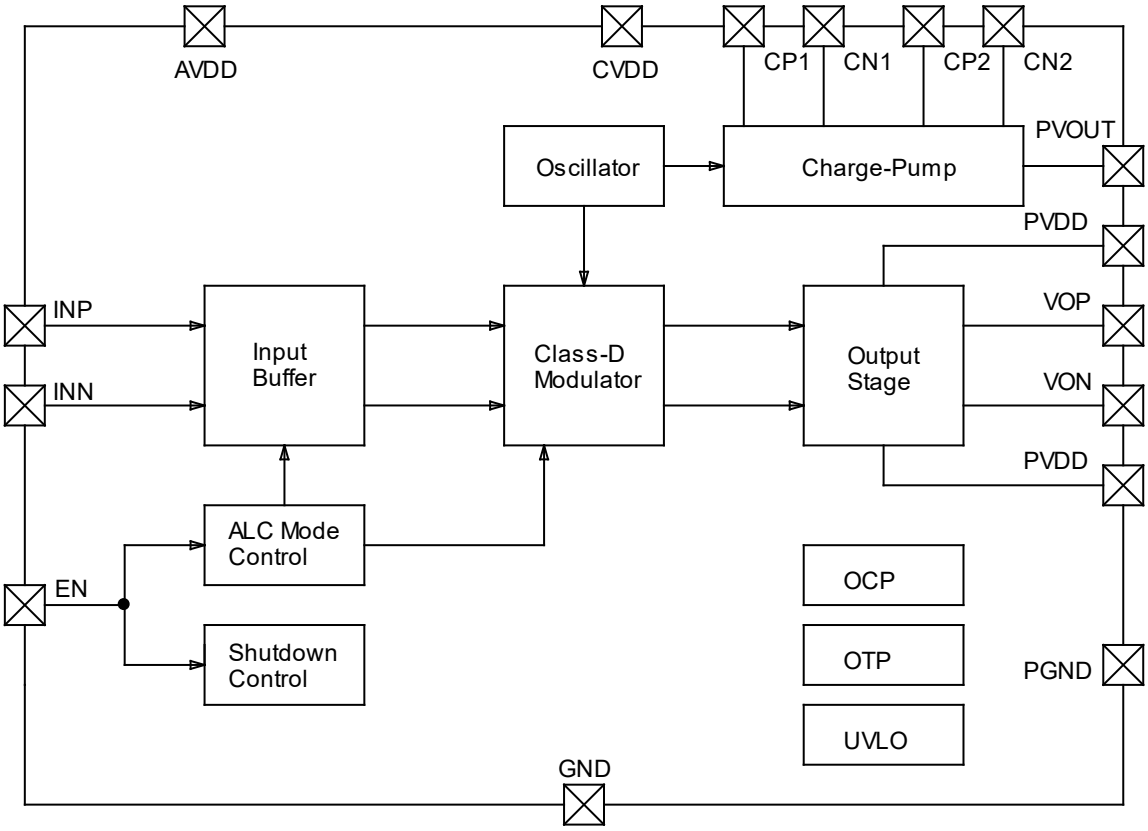



**Figure 2: Simplified Functional Block Diagram of ft2810D**

## ELECTRICAL CHARACTERISTICS

**$V_{DD}$=3.6V, $R_L$=4Ω+33μH, $C_{OUT}$=10μF//220μF, Mode 1, AVDD=1μF, CVDD=10μF, $C_{F1}$=$C_{F2}$=2.2μF, $C_{IN}$=0.33μF, $R_{IN}$=5.1kΩ ($A_V$=25dB), f=1kHz, $T_A$=+25℃, unless otherwise specified.**

| SYMBOL | PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | AVDD, CVDD | | 3.2 | | 4.6 | V |
| $V_{UVLOUP}$ | Power-Up Threshold Voltage | $V_{DD}$ from Low to High | | | 2.2 | | V |
| $V_{UVLODN}$ | Power-Off Threshold Voltage | $V_{DD}$ from High to Low | | | 2.0 | | V |
| $I_{DD}$ | Supply Quiescent Current Inputs AC-Grounded, No Load | $V_{DD}$=3.6V | | 1.5 | 2.5 | 3.5 | mA |
| | | $V_{DD}$=5V | | 1.6 | 2.7 | 3.8 | mA |
| $I_{SD}$ | Shutdown Current | EN=Low | | | 0.1 | 1 | μA |
| $V_{IN}$ | EN High Input Voltage | | | 1.2 | | | V |
| $V_{IL}$ | EN Low Input Voltage | | | | | 0.4 | V |
| $T_{OTSD}$ | Over-Temperature Threshold | | | | 160 | | ℃ |
| $T_{HYS}$ | Over-Temperature Hysteresis | | | | 20 | | ℃ |
| η | Power Efficiency | $P_O$=1.0W, $R_L$=4Ω+33μH | | | 75 | | % |
| **CLASS-G CHARGE PUMP REGULATOR** | | | | | | | |
| PVOUT | Charge Pump Output Voltage | $I_{PVDD}$=100mA | | 5.8 | 6.0 | 6.2 | V |
| $I_{OUT}$ | Max. Output Current | PVDD=5.5V | | | 0.7 | | A |
| $T_{PRECH}$ | Pre-charge time | $C_{OUT}$=10μF//220μF | | | 6 | | ms |
| $T_{SS}$ | Soft-start Time | $V_{in}$ from 0.02VRMS to 0.12VRMS | | | 0.6 | | ms |
| $f_{PUMP}$ | Charge Pump Frequency | | | | 900 | | kHz |
| **CLASS-D AUDIO AMPLIFIER** | | | | | | | |
| $P_{O, MAX}$ | Maximum Output Power $R_L$=4Ω+33μH, $C_{OUT}$=10μF//220μF (Mode 3, ALC Off) | $V_{DD}$=4.2V | THD+N=10% | | 4.0 | | W |
| | | | THD+N=1% | | 3.4 | | |
| | | $V_{DD}$=3.6V | THD+N=10% | | 3.0 | | |
| | | | THD+N=1% | | 2.8 | | |
| $P_{O, ALC}$ | Constant Output Power $R_L$=4Ω+33μH, $C_{OUT}$=10μF//220μF (Mode 1 & 2, ALC On) | $V_{in}$=300mVRMS | $V_{DD}$=4.2V | | 3.2 | | W |
| | | | $V_{DD}$=3.6V | | 2.8 | | |
| $A_V$ | Maximum Voltage Gain | $R_{IN}$=0Ω | Mode 1 (ALC On) | | 28 | | dB |
| | | | Mode 2 (ALC On) | | 24 | | |
| | | | Mode 3 (ALC Off) | | 24 | | |
| $Z_{IN}$ | Input Impedance @ INP, INN | | | | 15 | | kΩ |
| $Z_O$ | Output Impedance in Shutdown | EN Low | | | 3 | | kΩ |
| $V_{OS}$ | Output Offset Voltage | Inputs AC-Grounded, No Load | | | ±10 | | mV |
| THD+N | Total Harmonic Distortion + Noise | $P_O$=0.5W | | | 0.06 | | % |
| | | $P_O$=1.0W | | | 0.08 | | % |
| | | $V_{in}$=300mVRMS, Mode 1 & 2 (ALC On) | | | 0.3 | | % |
| VN | Output Voltage Noise | Inputs AC-Grounded, Mode 2 $R_L$=4Ω+33μH, A-weighted | | | 140 | | $μV_{RMS}$ |
| SNR | Signal-to-Noise Ratio | Maximum Output ($Vo=3.2V_{RMS}$) $R_L$=4Ω+33μH, A-weighted | | | 89 | | dB |
| PSRR | Power Supply Rejection Ratio | 200mVPP Ripple, f=217Hz | | | 72 | | dB |
| | | 200mVPP Ripple, f=1kHz | | | 70 | | dB |
| CMRR | Common Mode Rejection Ratio | | | | 70 | | dB |

## ELECTRICAL CHARACTERISTICS (Cont'd)

**$V_{DD}$=3.6V, $R_L$=4Ω+33μH, $C_{OUT}$=10μF//220μF, Mode 1, AVDD=1μF, CVDD=10μF, $C_{F1}$=$C_{F2}$=2.2μF, $C_{IN}$=0.33μF, $R_{IN}$=5.1kΩ ($A_V$=25dB), f=1kHz, $T_A$=+25℃, unless otherwise specified.**

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **CLASS-D AUDIO AMPLIFIER (Cont'd)** | | | | | | |
| $f_{PWM}$ | PWM Carrier Frequency | | | 450 | | kHz |
| $T_{STUP}$ | Startup Time | | | 20 | | ms |
| $I_{LIMIT}$ | Over-Current Limit | | | 2.0 | | A |
| $T_{HICCUP}$ | Over-Current Recovery Time | | | 250 | | ms |
| **AUTOMATIC LEVEL CONTROL (ALC)** | | | | | | |
| AMAX | Maximum ALC Attenuation | | | 6 | | dB |
| $T_{ATT}$ | ALC Attack Time | | | 30 | | ms |
| $T_{REL}$ | ALC Release Time | | | 1.8 | | s |
| **EN CONTROL** | | | | | | |
| $T_{LO}$ | Time of EN Low | | 0.5 | | 10 | μs |
| $T_{HI}$ | Time of EN High | | 0.5 | | | μs |
| $T_{RST}$ | Time for Mode Reset, Active Low | | 50 | | 500 | μs |
| $T_{SHDN}$ | Time for Shutdown, Active Low | | 5 | | | ms |

Notes:
(1) A 33μH inductor was placed in series with the load resistor to emulate a small speaker for efficiency measurements.
(2) The 33kHz lowpass filter is required even if the analyzer has an internal lowpass filter. An RC lowpass filter (100Ω, 47nF) is used on each output for the data sheet graphs.

## ELECTRICAL CHARACTERISTICS (Cont'd)

**$V_{DD}$=3.6V, $R_L$=8Ω+33μH, $C_{OUT}$=22μF, Mode 1, AVDD=1μF, CVDD=10 μF, $C_{F1}$=$C_{F2}$=2.2μF, $C_{IN}$=0.33μF, $R_{IN}$=5.1kΩ ($A_V$=25dB), f=1kHz, $T_A$=+25℃, unless otherwise specified.**

| SYMBOL | PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| PO, MAX | Maximum Output Power<br>$R_L$=8Ω+33μH, $C_{OUT}$=22μF<br>(Mode 3, ALC Off) | $V_{DD}$=4.2V | THD+N=10% | | 2.5 | | W |
| | | | THD+N=1% | | 2.0 | | |
| | | $V_{DD}$=3.6V | THD+N=10% | | 2.2 | | |
| | | | THD+N=1% | | 1.8 | | |
| PO, ALC | Constant Output Power<br>$R_L$=8Ω+33μH, $C_{OUT}$=22μF<br>(Mode 1 & 2, ALC On) | $V_{in}$=300mVRMS | $V_{DD}$=4.2V | | 2.0 | | W |
| | | | $V_{DD}$=3.6V | | 1.8 | | |
| THD+N | Total Harmonic Distortion + Noise | $P_O$=0.5W, $V_{DD}$=3.6V | | | 0.05 | | % |
| | | $P_O$=1.0W, $V_{DD}$=3.6V | | | 0.06 | | |
| | | $V_{in}$=300mVRMS, Mode 1 & 2 (ALC On) | | | 0.3 | | |
| VN | Output Voltage Noise | Inputs AC-Grounded<br>$R_L$=8Ω+33μH, A-weighted | | | 140 | | $\mu V_{RMS}$ |
| SNR | Signal-to-Noise Ratio | Maximum Output (Vo=3.6$V_{RMS}$)<br>$R_L$=8Ω+33μH, A-weighted | | | 89 | | dB |
| PSRR | Power Supply Rejection Ratio | 200mVPP Ripple, f=217Hz | | | 76 | | dB |
| | | 200mVPP Ripple, f=1kHz | | | 72 | | |
| CMRR | Common Mode Rejection Ratio | | | | 70 | | dB |
| η | Power Efficiency | $P_O$=0.5W, $R_L$=8Ω+33μH | | | 85 | | % |

Notes:

(1) A 33μH inductor was placed in series with the load resistor to emulate a small speaker for efficiency measurements.

(2) The 33kHz lowpass filter is required even if the analyzer has an internal lowpass filter. An RC lowpass filter (100Ω, 47nF) is used on each output for the data sheet graphs.

# TYPICAL PERFORMANCE CHARACTERISTICS

## List of Performance Characteristics

**$V_{DD}$=3.6V, $R_L$=8Ω+33μH, $C_{OUT}$=22μF, Mode 1, AVDD=1μF, $C_{VDD}$=10 μF, $C_{F1}$=$C_{F2}$=2.2μF, $C_{IN}$=0.33μF, $R_{IN}$=5.1kΩ ($A_V$=25dB), f=1kHz, $T_A$=+25℃, unless otherwise specified.**

| DESCRIPTION | CONDITIONS | FIGURE |
|---|---|---|
| Constant Output Power vs. Supply Voltage | $R_L$=8Ω+33μH/4Ω+33μH, Mode 1 (ALC On) | 3 |
| | $R_L$=8Ω+33μH/4Ω+33μH, Mode 2 (ALC On) | 4 |
| Maximum Output Power vs. Supply Voltage | $R_L$=8Ω+33μH, THD+N=1%, 10%, Mode 3 (ALC Off) | 5 |
| | $R_L$=4Ω+33μH, THD+N=1%, 10%, Mode 3 (ALC Off) | 6 |
| Output Power vs. Input Voltage | $V_{DD}$=3.6V, $R_L$=8Ω+33μH, Mode 1 & 2 | 7 |
| | $V_{DD}$=3.6V, $R_L$=8Ω+33μH, Mode 2 & 3 | 8 |
| | $V_{DD}$=4.2V, $R_L$=8Ω+33μH, Mode 1 & 2 | 9 |
| | $V_{DD}$=4.2V, $R_L$=8Ω+33μH, Mode 2 & 3 | 10 |
| | $V_{DD}$=3.6V, $R_L$=4Ω+33μH, Mode 1 & 2 | 11 |
| | $V_{DD}$=.6V, $R_L$=4Ω+33μH, Mode 2 & 3 | 12 |
| | $V_{DD}$=4.2V, $R_L$=4Ω+33μH, Mode 1 & 2 | 13 |
| | $V_{DD}$=4.2V, $R_L$=4Ω+33μH, Mode 2 & 3 | 14 |
| Output Power (on Activation of Charge Pump) vs. Supply Voltage | $R_L$=8Ω+33μH & 4Ω+33μH, Mode 1 (ALC On) | 15 |
| | $R_L$=8Ω+33μH & 4Ω+33μH, Mode 3 (ALC Off) | 16 |
| Power Dissipation vs. Output Power | $R_L$=8Ω+33μH, Mode 1, $V_{DD}$=3.6V, 4.2V | 17 |
| | $R_L$=4Ω+33μH, Mode 1, $V_{DD}$=3.6V, 4.2V | 18 |
| Efficiency vs. Output Power | $R_L$=8Ω+33μH, Mode 1, $V_{DD}$=3.6V, 4.2V | 19 |
| | $R_L$=4Ω+33μH, Mode 1, $V_{DD}$=3.6V, 4.2V | 20 |
| THD+N vs. Output Power | $R_L$=8Ω+33μH, Mode 3, $V_{DD}$=3.6V, 4.2V | 21 |
| | $R_L$=4Ω+33μH, Mode 3, $V_{DD}$=3.6V, 4.2V | 22 |
| THD+N vs. Input Voltage | $R_L$=8Ω+33μH, Mode 1, $V_{DD}$=3.6V, 4.2V | 23 |
| | $R_L$=4Ω+33μH, Mode 1, $V_{DD}$=3.6V, 4.2V | 24 |
| | $R_L$=8Ω+33μH, Mode 2, $V_{DD}$=3.6V, 4.2V | 25 |
| | $R_L$=4Ω+33μH, Mode 2, $V_{DD}$=3.6V, 4.2V | 26 |
| THD+N vs. Input Frequency | $V_{DD}$=3.6V, $R_L$=8Ω+33μH, Mode 1, $P_O$=0.25W, 0.5W | 27 |
| | $V_{DD}$=4.2V, $R_L$=8Ω+33μH, Mode 1, $P_O$=0.25W, 0.5W | 28 |
| | $V_{DD}$=3.6V, $R_L$=4Ω+33μH, Mode 1, $P_O$=0.5W, 1.0W | 29 |
| | $V_{DD}$=4.2V, $R_L$=4Ω+33μH, Mode 1, $P_O$=0.5W, 1.0W | 30 |
| PSRR vs. Input Frequency | $R_L$=8Ω+33μH, Input AC-Grounded, Mode 1, $V_{DD}$=3.6V, 4.2V | 31 |
| | $R_L$=4Ω+33μH, Input AC-Grounded, Mode 1, $V_{DD}$=3.6V, 4.2V | 32 |
| Quiescent Current vs. Supply Voltage | Input AC-Grounded, No Load, Mode 1 | 33 |
| ALC Attack Time | $V_{DD}$=3.6V, Vin=0.15VRMS to 0.30VRMS, $R_L$=8Ω+33μH, Mode 1 | 34 |
| ALC Release Time | $V_{DD}$=3.6V, Vin=0.30VRMS to 0.15VRMS, $R_L$=8Ω+33μH, Mode 1 | 35 |
| Charge Pump Mode Transition Waveforms | $V_{DD}$=3.6V, Vin=0.08VRMS ~ 0.10VRMS, $R_L$=8Ω+33μH, Mode 1 | 36 |
| (VOP-VON) Startup Waveforms | $V_{DD}$=3.6V, $R_L$=8Ω+33μH, Mode 1 | 37 |
| (VOP-VON) Shutdown Waveforms | $V_{DD}$=3.6V, $R_L$=8Ω+33μH, Mode 1 | 38 |

## TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

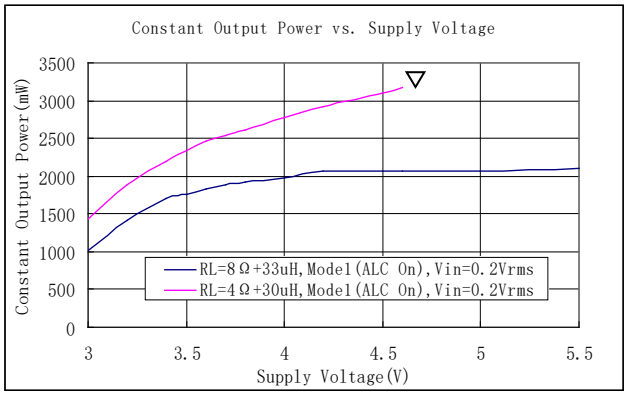



**Figure 3: Constant Output Power vs. Supply Voltage**

**▽: shows where OTSD occurs**

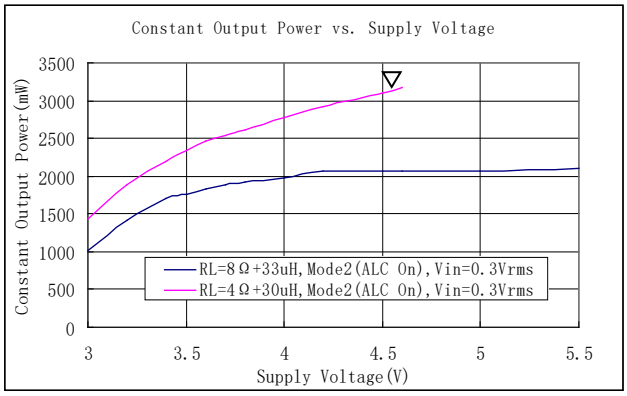



**Figure 4: Constant Output Power vs. Supply Voltage**

**▽: shows where OTSD occurs**

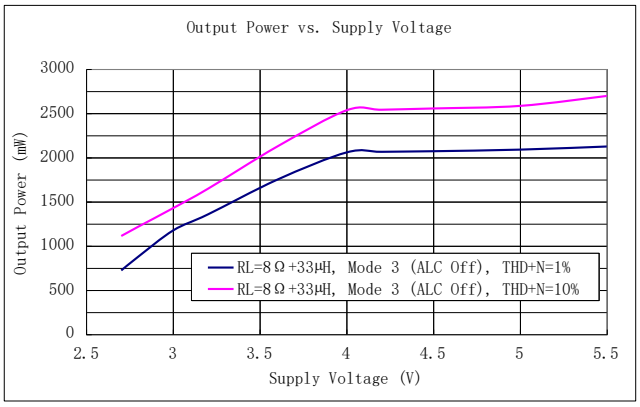



**Figure 5: Output Power vs. Supply Voltage**

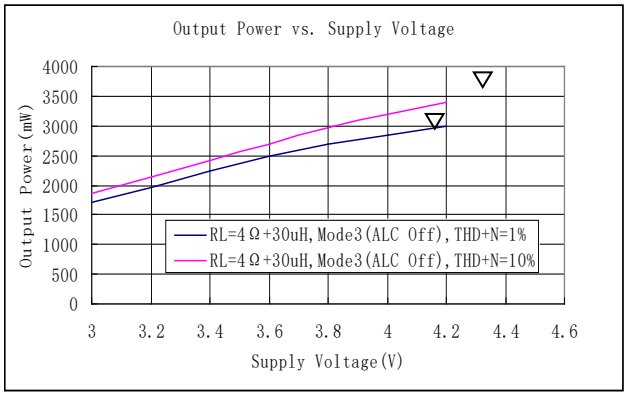



**Figure 6: Output Power vs. Supply Voltage**

**▽: shows where OTSD occurs**

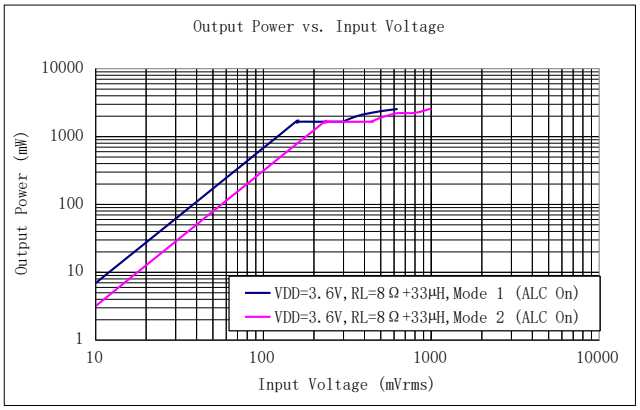



**Figure 7: Output Power vs. Input Voltage**

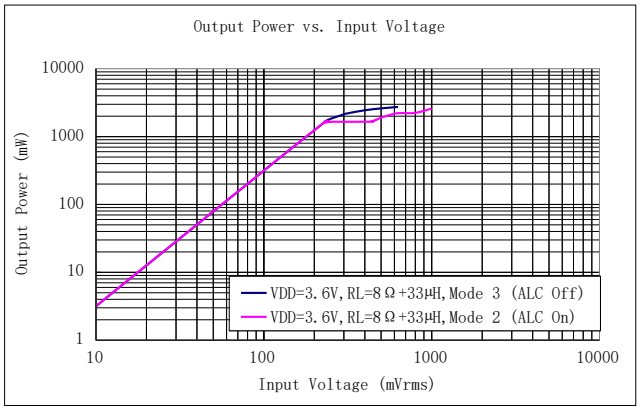



**Figure 8: Output Power vs. Input Voltage**

## TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

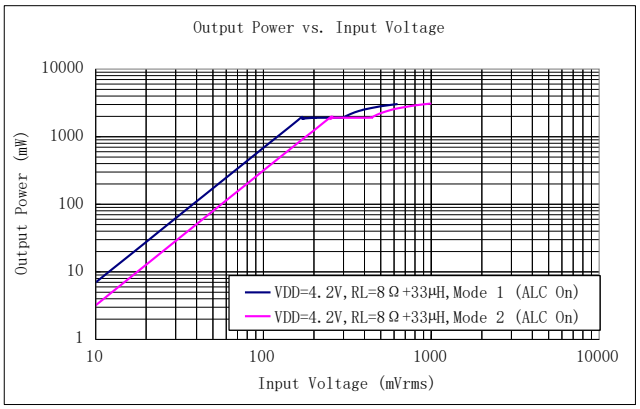



**Figure 9: Output Power vs. Input Voltage**

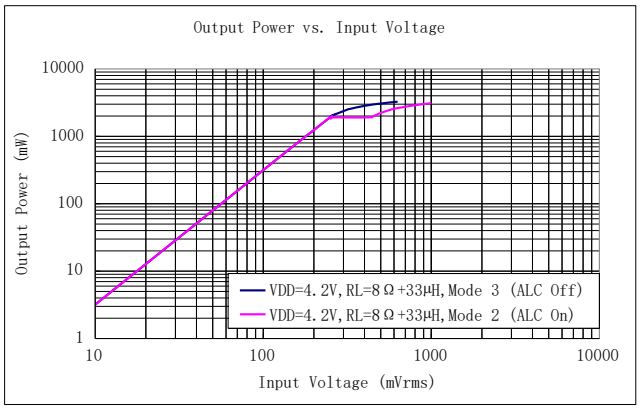



**Figure 10: Output Power vs. Input Voltage**

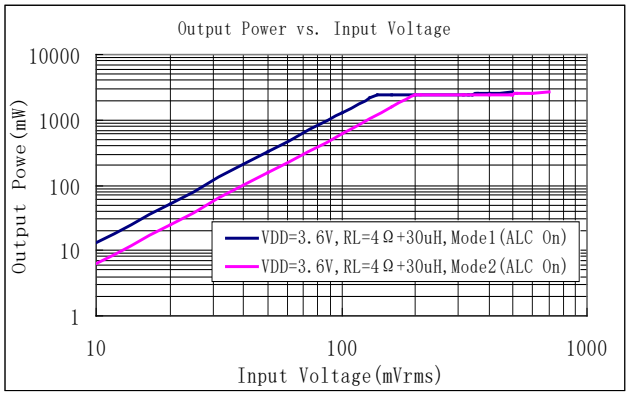



**Figure 11: Output Power vs. Input Voltage**

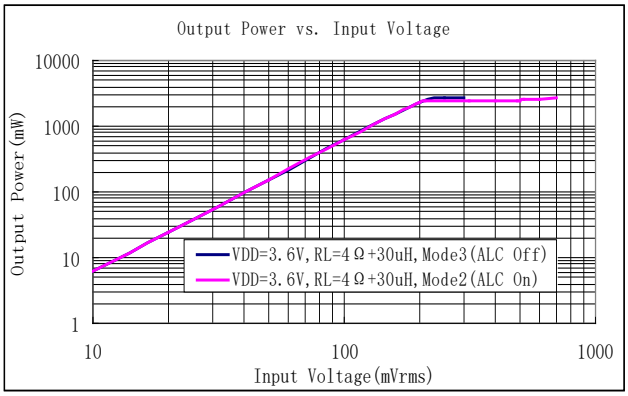



**Figure 12: Output Power vs. Input Voltage**

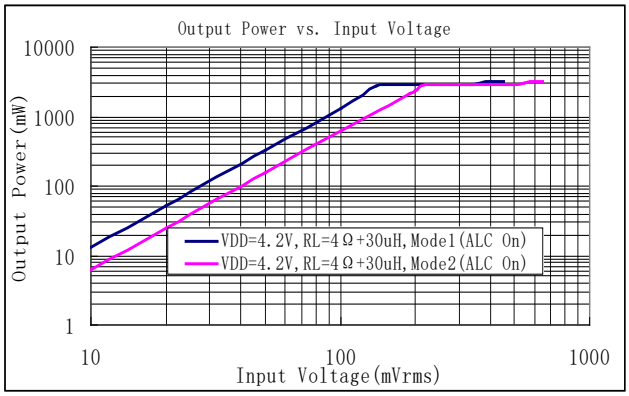



**Figure 13: Output Power vs. Input Voltage**

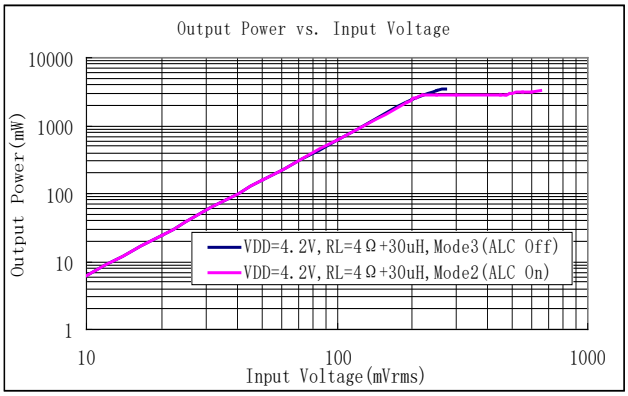



**Figure 14: Output Power vs. Input Voltage**

## TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

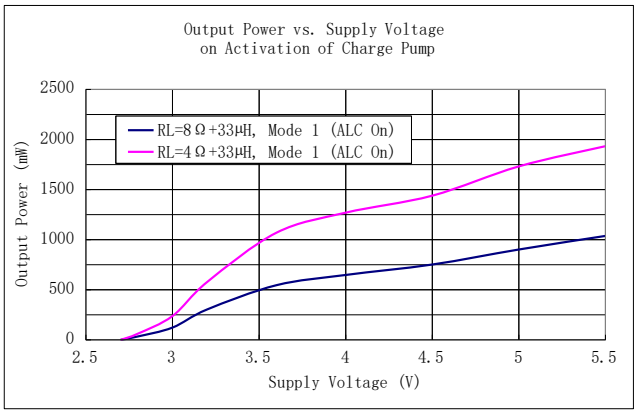



**Figure 15: Output Power (on Activation of Charge Pump) vs. Supply Voltage**

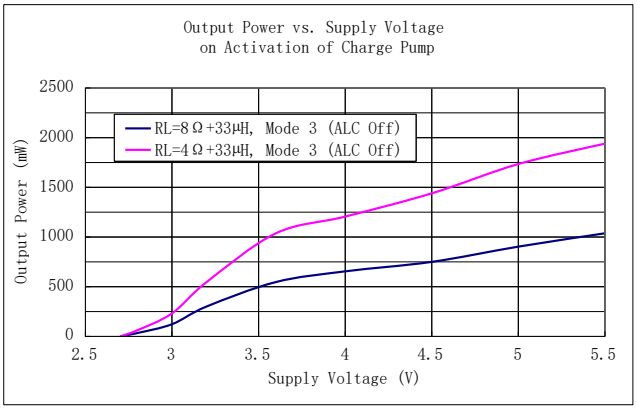



**Figure 16: Output Power (on Activation of Charge Pump) vs. Supply Voltage**

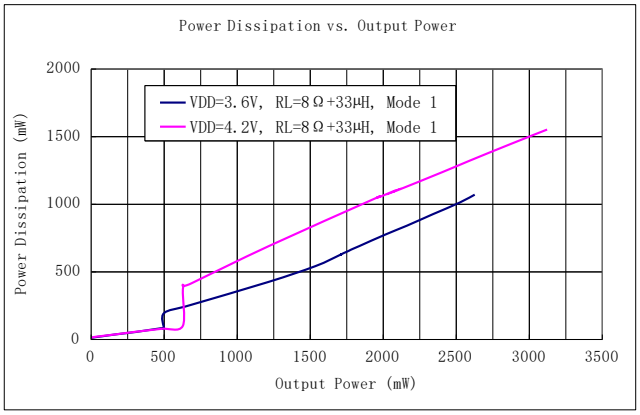



**Figure 17: Power Dissipation vs. Output Power**

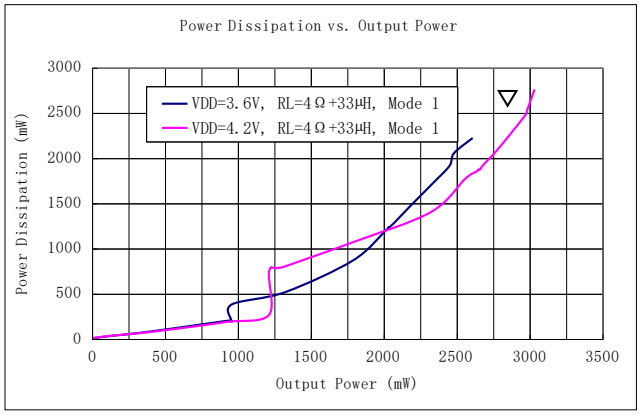



**Figure 18: Power Dissipation vs. Output Power**
**▽: shows where OTSD occurs**

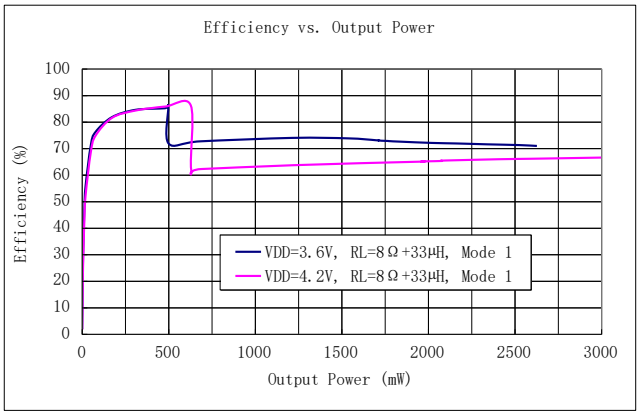



**Figure 19: Efficiency vs. Output Power**

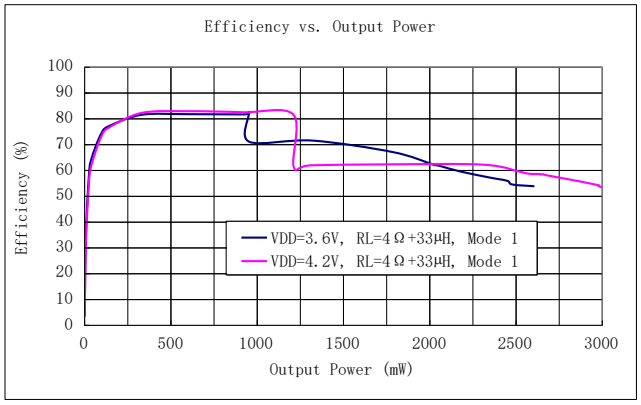



**Figure 20: Efficiency vs. Output Power**

## TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

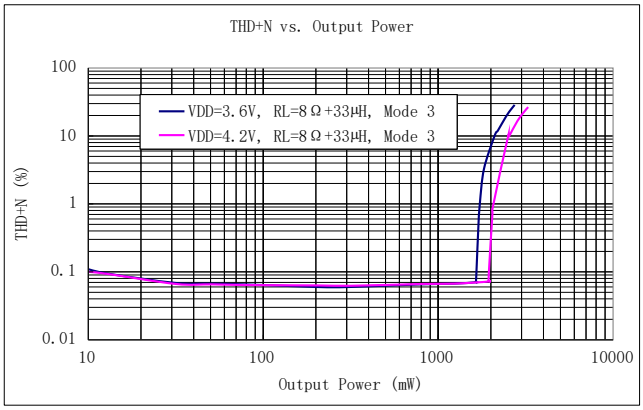



Figure 21: THD+N vs. Output Power

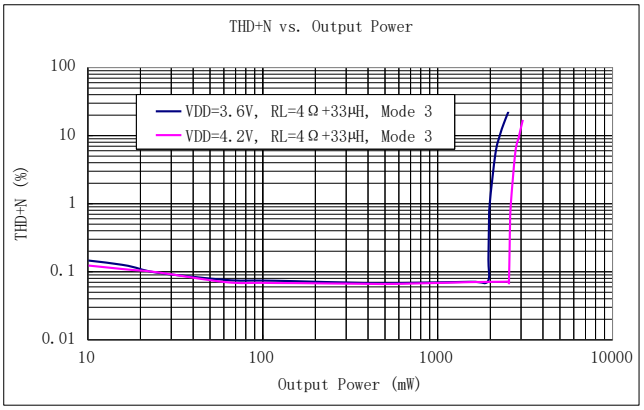



Figure 22: THD+N vs. Output Power

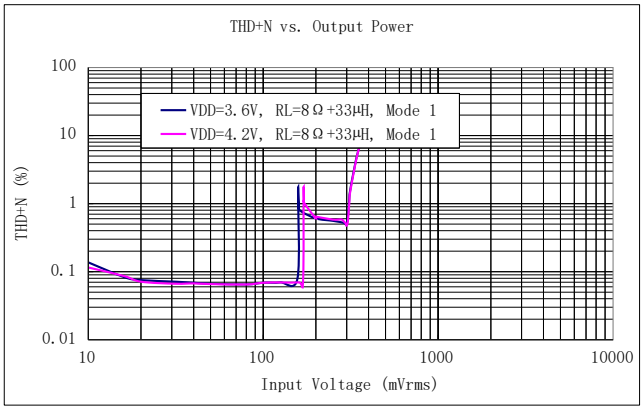



Figure 23: THD+N vs. Input Voltage

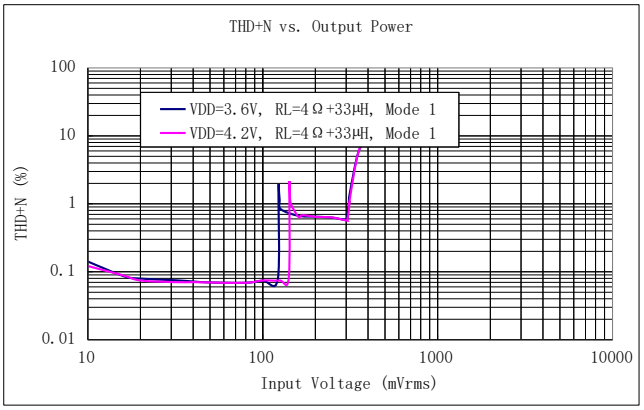



Figure 24: THD+N vs. Input Voltage

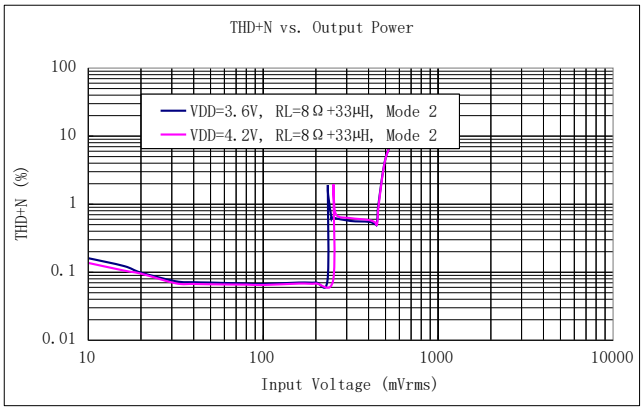



Figure 25: THD+N vs. Input Voltage

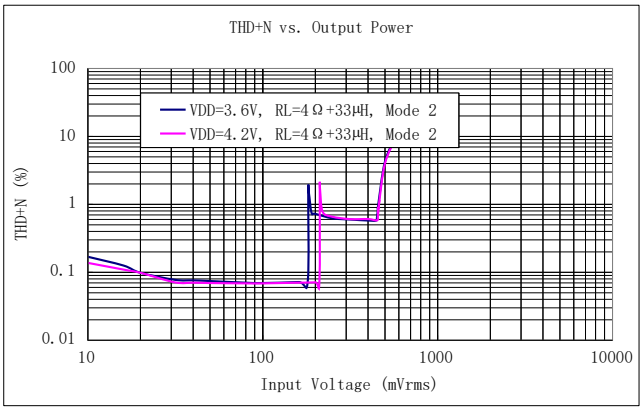



Figure 26: THD+N vs. Input Voltage

## TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

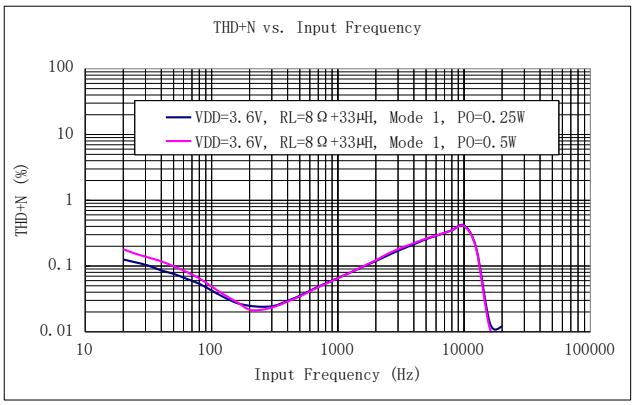



Figure 27: THD+N vs. Input Frequency

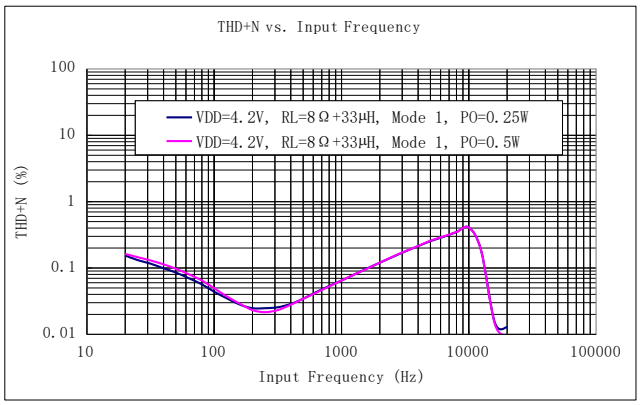



Figure 28: THD+N vs. Input Frequency

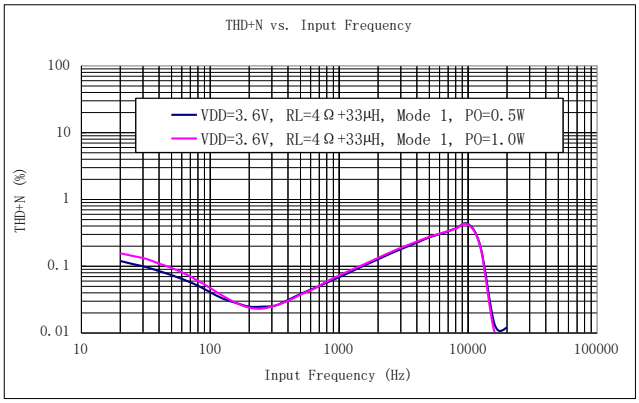



Figure 29: THD+N vs. Input Frequency

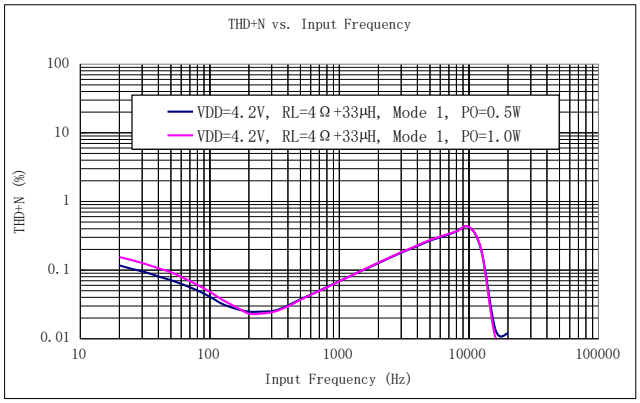



Figure 30: THD+N vs. Input Frequency

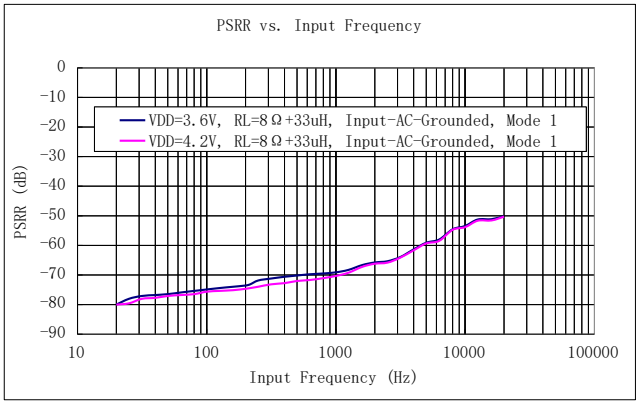



Figure 31: PSRR vs. Input Frequency

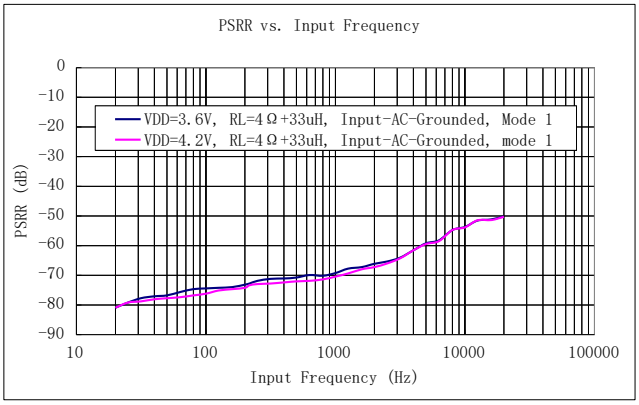



Figure 32: PSRR vs. Input Frequency

## TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

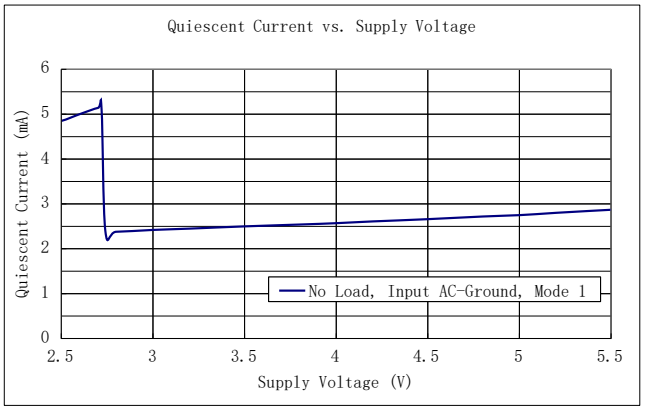



Figure 33: Quiescent Current vs. Supply Voltage

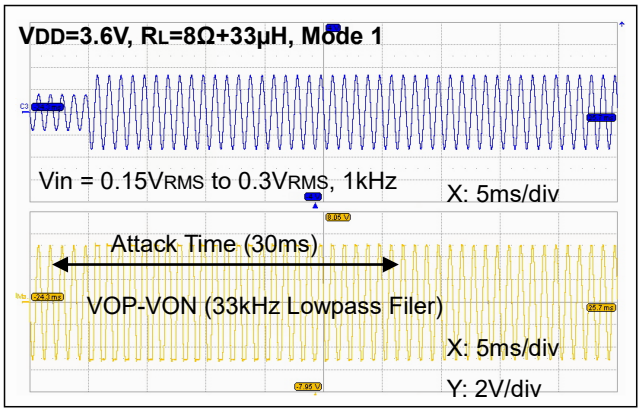



Figure 34: ALC Attack Time

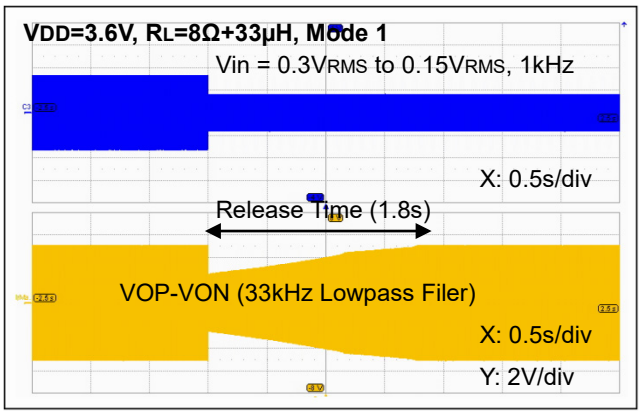



Figure 35: ALC Release Time

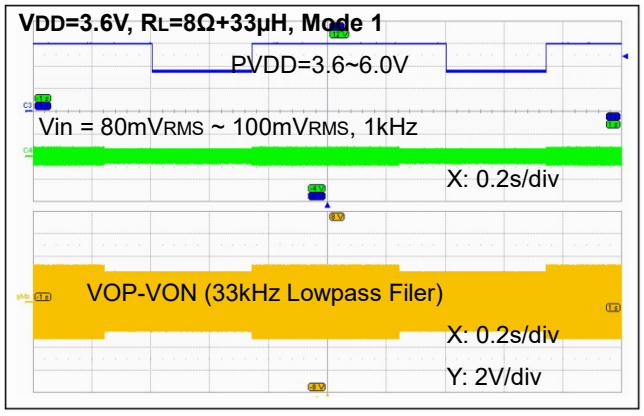



Figure 36: Charge Pump Mode Transition Waveforms

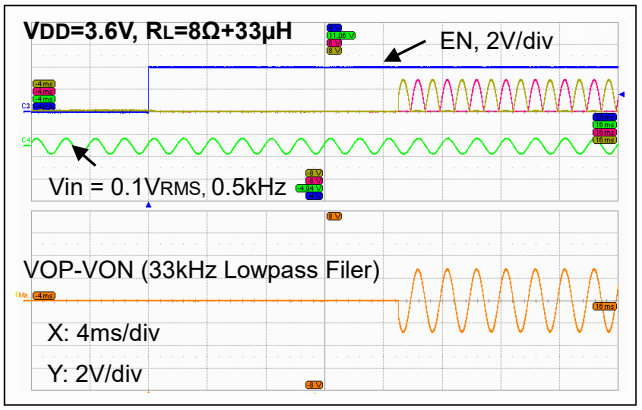



Figure 37: (VOP-VON) Startup Waveforms

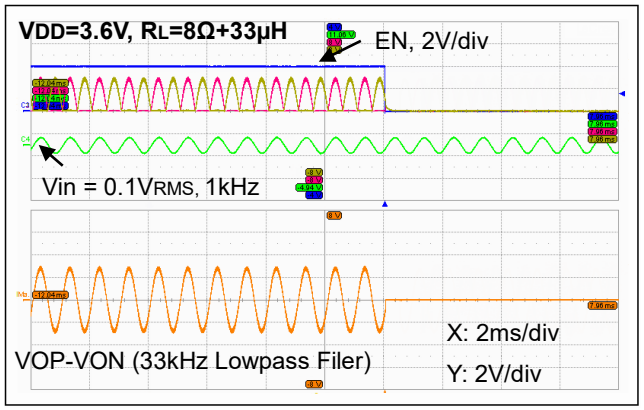



Figure 38: (VOP-VON) Shutdown Waveforms

## APPLICATION INFORMATION

The ft2810D is a highly efficient 3.2W Class-G audio power amplifier for use in battery-based portable device applications. It integrates a filterless Class-D audio power amplifier with a Class-G charge pump regulator based upon proprietary ***Dual-Pump***$^{TM}$ topology. It operates from 3.2V to 4.6V supply. With a 3.6V supply voltage, the ft2810D is capable of delivering into 4Ω load with maximum output power of 3.2W at 10% THD+N in Non-ALC mode, or constant output power of 2.8W at 0.3% THD+N in ALC mode. Its high efficiency, up to 85%, helps extend battery life.

In ft2810D, the power supply rail for the amplifier output stage is internally boosted and regulated at 6V by an on-chip adaptive charge pump regulator based upon the ***Dual-Pump***$^{TM}$ topology, thus allowing for a much louder audio output than a stand-alone one directly connected to the battery. It makes ft2810D an ideal audio solution for portable devices, which are powered by a single-cell lithium battery while requiring higher audio loudness.

The ft2810D also features ALC on the output signals, which detects the output clipping caused by the over-level input signal and automatically adjusts the dynamic range of the output signals to prevent the distortion of the audio signal. The ALC also eliminates the output clipping due to low battery supply voltage.

As specifically designed for portable device applications, the ft2810D incorporates a shutdown mode to minimize the power consumption by holding the EN pin to ground for an extended period more than 5ms. It also includes comprehensive protection features against various operating faults such as over-current, short-circuit, over-temperature, and under-voltage for a safe and reliable operation.

### ADAPTIVE CHARGE PUMP REGULATOR

To allow for a much louder audio output, a charge pump regulator is employed to boost PVDD, the power rail for the amplifier output stage. Whenever the audio inputs are larger than a prescribed level for an extended period of time, the charge pump regulator will be activated to boost and regulate PVOUT at 6V. In this case, the charge pump regulator operates in the regulation mode. For a proper operation, the boosted voltage PVOUT generated by the charge pump regulator must be externally shorted to PVDD via a sufficiently wide metal trace on the system board.

On the other hand, when the audio inputs are less than a prescribed level for an extended period of time, the charge pump regulator will be de-biased and forced into the standby mode. In the standby mode, the amplifier output stage is powered directly by VDD, the battery voltage, through an internal power switch. This adaptive nature of the charge pump regulator can greatly improve the power efficiency of ft2810D when playing audio and thus extends battery life.

### *DUAL-PUMP*$^{TM}$ TECHNOLOGY

In order to maximize the output power, the ft2810D employs a proprietary ***Dual-Pump***$^{TM}$ topology for the internal charge pump regulator using two flying capacitors to boost the supply voltage to a higher value at 6V. To limit the inrush current to an acceptable value when the supply voltage is first applied to the device, the charge pump regulator incorporates soft-start function. Furthermore, when a short-circuit condition at the boosted voltage is detected, the ft2810D limits the charging current to about 100mA for a safe operation.

Compared with a conventional charge pump topology using a single flying capacitor, the output current capability of the ***Dual-Pump***$^{TM}$ can be largely enhanced and the output voltage ripples minimized. In this manner, the performance of the Class-D audio amplifier can be significantly improved, particularly for the speakers whose impedances are less than 6Ω. With the ***Dual-Pump***$^{TM}$ topology, the ft2810D can deliver up to 3.2W into a 4Ω speaker load with THD+N less than 10% when powered by a single-cell lithium battery.

### Selection of Charge Pump Regulator's Flying Regulator's Capacitors ($C_{F1}$ & $C_{F2}$)

A nominal value of 2.2μF is recommended for the flying capacitors ($C_{F1}$ and $C_{F2}$) of the charge pump regulator, but other values can be used. A low equivalent-series-resistance (ESR) ceramic capacitor, such as X7R or X5R, is recommended.

### Selection of Charge Pump Output Regulator's Capacitor ($C_{OUT}$)

The low-frequency RMS output power of the audio amplifier will be affected, to some extent, by the charge pump regulator's output capacitor, particularly for the speakers whose impedances are less than 6Ω. Thus, for best frequency response of the audio amplifier over a wide range of audio frequencies, a 10μF low-ESR ceramic capacitor in parallel with a tantalum or electrolytic capacitor is recommended for the output capacitor ($C_{OUT}$) of the charge pump regulator. The value of the tantalum or electrolytic capacitor shall be between 220μF and 470μF, as much as the system board space allows.

For applications where the speaker impedance is 6Ω or more, a 22μF low-ESR ceramic capacitor is sufficient. Do not use any capacitances higher than 44μF as it can slow the charge pump regulator's response time to output load transients without much further improvement on the output power.

## OPERATING MODE CONTROL AND GAIN SETTING

To support for a wide range of applications, the ft2810D incorporates one-wire pulse control to configure the operating mode and the voltage gain. By applying a string of pulses to the EN pin, users can enable (Constant Output Power mode) or disable (Maximum Output Power mode) the ALC function as well as set the voltage gain. The operating mode is advanced and updated on each low-to-high transition of the pulses applied onto the EN pin. The detailed timing diagram of the one-wire pulse control to select the operating mode is shown in Figure 39.

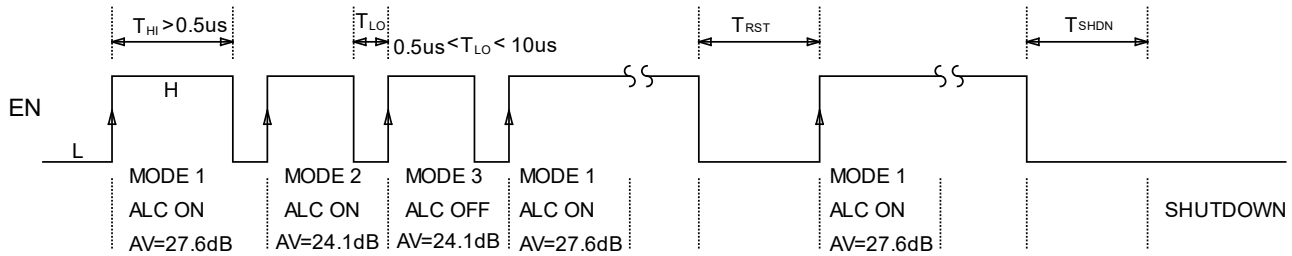



**Figure 39: Operating Mode Control Diagram**

Three operating modes are configured by the application of a string of pulses onto the EN pin. After an initial application of the power supply, the first low-to-high transition at the EN pin will set the device into Mode 1, where the voltage gain is set at 28dB and the ALC function enabled. On the next low-to-high transition, the device advances into Mode 2, where the voltage gain is set at 24dB and the ALC function remains enabled. Finally, on the third low-to-high transition, the device advances into Mode 3, where the ALC function is disabled and the voltage gain remains at 24dB. The operating modes will be cycled and repeated in the same manner as described above for consecutive pulses applied.

Note that each individual pulse must be longer than a minimum of 0.5μs to be recognized. Any pulses shorter than 0.5μs may be ignored. The state of the mode operation can be reset back to Mode 1 by holding the EN pin low more than 50μs but less than 500μs, regardless of the state it is currently operating. Whenever the EN pin held low for more than 5ms, the device enters into the shutdown mode, where all the internal circuitry is de-biased. Once the device is forced into shutdown mode, one or multiple pulses are required for the ft2810D to return to the desired mode of operation.

| Mode | # of Pulses | Voltage Gain | ALC |
|---|---|---|---|
| Mode 1 | 1 | 28dB (24X) | Enable |
| Mode 2 | 2 | 24dB (16X) | Enable |
| Mode 3 | 3 | 24dB (16X) | Disable |

**Table 1: Mode of Operation**

### Operating Mode Reset

The state of the mode operation can be reset back to the default mode, Mode 1 ($A_V$=28dB, ALC On) by holding the EN pin low for more than 50μs but less than 500μs, regardless of the state it is currently operating.

### Shutdown Mode

When the EN pin is held low for 5ms (typical) or longer, the ft2810D will be forced into the shutdown mode. During the shutdown mode, the supply current will be significantly reduced to less than 1μA.

## AUTOMATIC LEVEL CONTROL (ALC)

The automatic level control is to maintain the output signal level for a maximum output swing without distortion when an excessive input that may cause output clipping is applied. With the ALC function, the ft2810D lowers the gain of the amplifier to an appropriate value such that the clipping at the output is avoided. It also eliminates the clipping of the output signal due to the decrease of the power-supply voltage.

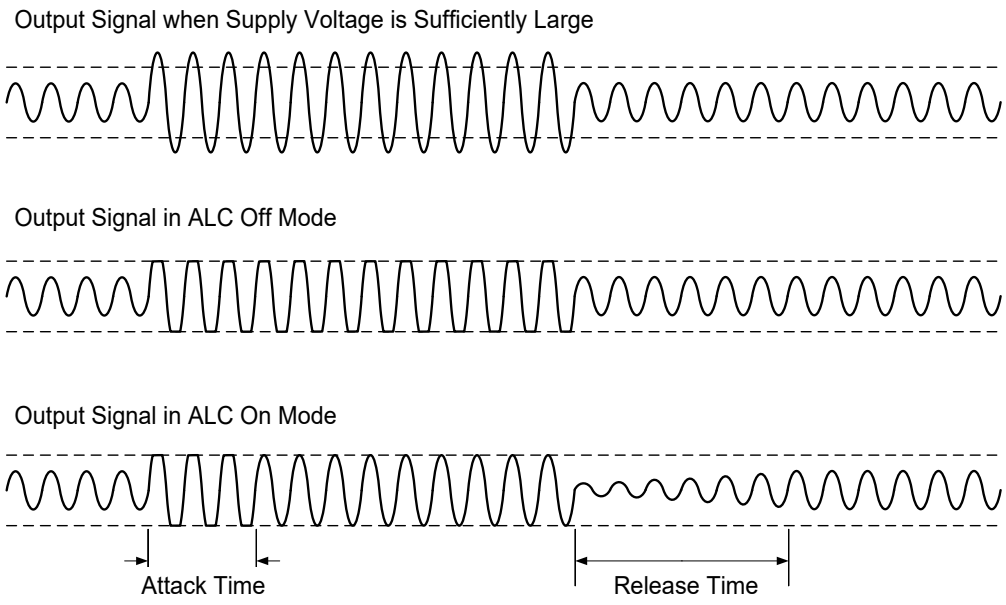



**Figure 40: Automatic Level Control Function Diagram**

The attack time is defined as the time interval required for the gain to fall to its steady-state gain less 3dB approximately, presumed that a sufficiently large input signal is applied. The release time is the time interval required for the amplifier to exit out of the present mode of operation. See Table 2.

| Mode | Attack Time (ms) | Release Time (s) |
|---|---|---|
| Mode 1 & 2 (ALC On) | 30 | 1.8 |

**Table 2: Attack Time & Release Time**

## VOLTAGE GAIN SETTING

The overall voltage gain of the audio amplifier can be externally adjusted by inserting additional input resistors, $R_{IN}$, in series with the input capacitors. The value of $R_{IN}$ for a given voltage gain can be calculated by Equation 1.

$$A_V = 360 / (R_{IN} + 15), \text{ for Mode 1} \quad (1)$$
$$A_V = 240 / (R_{IN} + 15), \text{ for Mode 2 and 3}$$

In Equation 1, $A_V$ is the desired voltage gain of the amplifier and $R_{IN}$ is expressed in kΩ. Table 3 shows suitable resistor values of $R_{IN}$ that can be used for various voltage gains.

| $R_{IN}$, kΩ | 0 | 5 | 8 | 13.6 | 21 | 30 | 42 |
|---|---|---|---|---|---|---|---|
| $A_V$, dB (Mode 1) | 28 | 25 | 24 | 22 | 20 | 18 | 16 |
| $A_V$, dB (Mode 2 & 3) | 24 | 21.6 | 20.4 | 18.5 | 16.5 | 14.5 | 12.5 |

**Table 3: External Input Resistors Required for Various Voltage Gains**

### Click-and-Pop Suppression

The ft2810D audio power amplifier features comprehensive click-and-pop suppression. During startup, the click-and-pop suppression circuitry reduces any audible transients internal to the device. When entering into shutdown, the differential audio outputs are pulled to ground through their individual internal resistors (3kΩ) simultaneously.

### PSRR Enhancement

Without a dedicated pin for the common-mode voltage bias and an external holding capacitor onto the pin, the ft2810D achieves a high PSRR, 80dB at 217Hz, thanks to a proprietary design technique.

## PROTECTION MODES

The ft2810D incorporates various protection functions against possible operating faults for a safe operation. It includes Under-voltage Lockout (UVLO), Over-Current Protection (OCP), and Over-Temperature Shutdown (OTSD).

### Under-Voltage Lockout (UVLO)

The ft2810D incorporates a circuitry to detect a low supply voltage for a safe and reliable operation. When the supply voltage is first applied, the ft2810D will remain inactive until the supply voltage exceeds 2.2V ($V_{UVLU}$). When the supply voltage is removed and drops below 2.0V ($V_{UVLD}$), the ft2810D enters into shutdown mode immediately.

### Over-Current Protection (OCP)

During operation, the output of Class-D amplifier constantly monitors for any over-current and/or short-circuit conditions. When a short-circuit condition between two differential outputs, differential output to VDD, PVDD or ground is detected, the output stage of the amplifier is immediately forced into high impedance state. Once the fault condition persists over a prescribed period, the ft2810D then enters into the shutdown mode and remains in this mode for about 200ms. During the shutdown, the power switches of the charge pump regulator are also turned off, and the PVDD is discharged through a resistor to ground.

When the shutdown mode times out, the ft2810D will initiate another startup sequence and then check if the short-circuit condition has been removed. Meanwhile, the charge pump regulator tries to bring PVDD up to the preset voltage again. If the fault condition is still present, the ft2810D will repeat itself for the process of a startup followed by detection, qualification, and shutdown. It is so-called the hiccup mode of operation. Once the fault condition is removed, the ft2810D automatically restores to its normal mode of operation.

Although the output stage of the Class-D audio amplifier can withstand a short between VOP and $V_{ON}$, do not connect either output directly to GND, PGND, PVOUT, PVDD, CVDD, or AVDD as this might damage the

device permanently, particularly when AVDD is higher than 4.6V.

### Over-Temperature Shutdown (OTSD)

When the die temperature exceeds a preset threshold (160℃), the device enters into the over-temperature shutdown mode, where two differential outputs are pulled to ground through an internal resistor (2kΩ) individually. The device will resume normal operation once the die temperature returns to a lower temperature, which is about 20°C lower than the threshold.

## CLASS-D AUDIO AMPLIFIER

The Class-D audio amplifier in the ft2810D operates in much the same way as a traditional Class-D amplifier and similarly offers much higher power efficiency than Class-AB amplifiers. The high efficiency of a Class-D operation is achieved by the switching operation of the output stage of the amplifier. The power loss associated with the output stage is limited to the conduction and switching loss of the power MOSFETs, which are much less than the power loss associated with a linear output stage in Class-AB amplifiers.

### Fully Differential Amplifier

The ft2810D includes a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common-mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage on the output that is equal to the differential input times the amplifier gain. The common-mode feedback ensures that the common-mode voltage at the output is biased substantially close to an internally-generated voltage reference regardless of the common-mode voltage of the inputs. Although the ft2810D supports for a single-ended input, differential inputs are recommended for the applications, where the environment can be noisy like a wireless handset, in order to ensure maximum SNR.

### Low-EMI Filterless Output Stage

Traditional Class-D amplifiers require for the use of external LC filters, or shielding, to meet EN55022B electromagnetic-interference (EMI) regulation standards. The ft2810D applies an edge-rate control circuitry to reduce EMI emission, while maintaining high power efficiency. Above 10MHz, the wideband spectrum looks like noise for EMI purposes.

### Filterless Design

Traditional Class D amplifiers require an output filter to recover the audio signal from the amplifier's output. The filter adds cost, increases the solution size of the amplifier, and can decrease efficiency and THD+N performance. The traditional PWM scheme uses large differential output swings (twice of supply voltage peak-to-peak) and causes large ripple currents. Any parasitic resistance in the filter components results in loss of power and lowers the efficiency.

The ft2810D does not require an output filter. The device relies on the inherent inductance of the speaker coil and the natural filtering of both the speaker and the human ear to recover the audio component of the square-wave output. By eliminating the output filter, a smaller, less costly, and more efficient solution can be accomplished.

Because the frequency of the ft2810D output is well beyond the bandwidth of most speakers, voice coil movement due to the square-wave frequency is very small. Although this movement is small, a speaker not designed to handle the additional power can be damaged. For optimum results, use a speaker with a series inductance greater than 10μH. Typical 8Ω speakers exhibit series inductances in the range from 20μH to 100μH.

### EMI Reduction

The ft2810D does not require an LC output filter for short connections from the amplifier to the speaker. However, additional EMI suppressions can be made by use of a ferrite bead in conjunction with a capacitor, as shown in Figure 41. Choose a ferrite bead with low DC resistance (DCR) and high impedance (100Ω ~ 330Ω)

at high frequencies (>100MHz). The current flowing through the ferrite bead must be also taken into consideration. The effectiveness of ferrites can be greatly aggravated at much lower than the rated current values. Choose a ferrite bead with a rated current value no less than 2A. The capacitor value varies based on the ferrite bead chosen and the actual speaker lead length. Choose a capacitor less than 1nF based on EMI performance

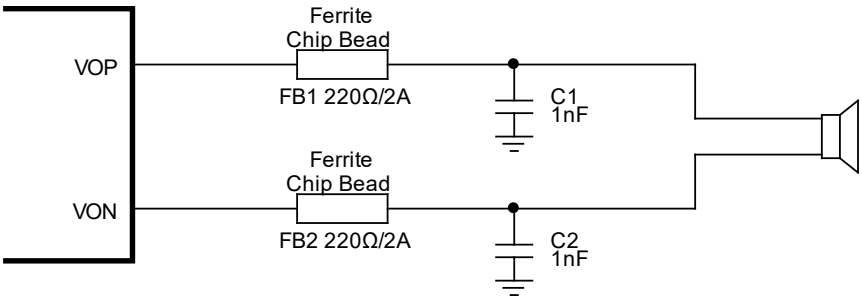



**Figure 41: Ferrite Bead Filter to Reduce EMI**

### Decoupling Capacitor ($C_S$)

The ft2810D is a high-performance Class-D audio power amplifier, which requires adequate power supply decoupling to ensure its high efficiency operation with low total harmonic distortion. Sufficient power supply coupling also prevents oscillations for long lead lengths between the amplifier and the speaker.

Place a low equivalent-series-resistance (ESR) ceramic capacitor (X7R or X5R), typically 1μF, as close as possible to the AVDD lead. This choice of capacitor and placement help reject high frequency transients, spikes, or digital hash on the line. Furthermore, placing the decoupling capacitors close to the ft2810D is important for power efficiency, as any parasitic resistance or inductance between the amplifier and the capacitor causes efficiency loss. For best power supply coupling, place an additional 10μF or greater low ESR capacitor close to the CVDD lead. This larger capacitor serves as a charge reservoir for the flying capacitors $C_{F1}$ or $C_{F2}$ of the charge pump regulator each time one of the flying capacitors is charged, thus reducing the amount of voltage ripple seen at CVDD. This will help reduce the amount of EMI passed back along the power trace to other circuitry on the system board.

### Input Resistors ($R_{IN}$)

To minimize the number of external components required for the application of ft2810D, a set of 15kΩ input resistors are integrated internally at INP and INN pins respectively. The internal input resistors also bring other benefits such as fewer variations on PSRR and turn-on pop noise performances since on-chip resistors can match well. Thus, for typical portable device applications, there is no need for additional input resistors connected to INP or INN pin. However, for applications where additional gain adjustment becomes necessary, a set of external input resistors can be added onto INP and INN pins respectively, as shown in Figure 43. The value of the external input resistors must be included for the calculation of the overall voltage gain (as described by Equation 2) as well as the selection of proper input capacitors (as described by Equation 3). As shown in Equation 2, the external input resistors will attenuate the original overall voltage gain by the ratio of $R_{INTERNAL}$ / ($R_{IN}$+$R_{INTERNAL}$).

$$A_V = A_{V0} \times [R_{INTERNAL} / (RIN + R_{INTERNAL})] \quad (2)$$

where $A_{V0}$ = 24 (28dB) for Mode 1
$A_{V0}$ = 16 (24dB) for Mode 2 and 3
$R_{INTERNAL}$ = 15kΩ

**Input Capacitors ($C_{IN}$)**

DC decoupling capacitors for audio inputs are recommended. The audio input DC decoupling capacitors will remove the DC bias from an incoming analog signal. The input capacitors ($C_{IN}$) and input resistors ($R_{IN}$ plus $R_{INTERNAL}$) form a highpass filter with the corner frequency, $f_C$, as shown in Equation 3.

$$f_C = 1 / [2 \times \pi \times (R_{IN} + R_{INTERNAL}) \times CIN] \quad (3)$$

where $R_{INTERNAL} = 15k\Omega$

$R_{IN}$ is the external input resistance value for a specific voltage gain. Note that the variation of the actual input resistance will affect the voltage gain proportionally.

Choose $C_{IN}$ such that $f_C$ is well below the lowest frequency of interest. Setting it too high affects the amplifiers' low-frequency response. Consider an example where the specification calls for $A_V$=25dB (operating in Mode 1) and a flat frequency response down to 20Hz. In this example, $R_{IN}$=5.1kΩ and $C_{IN}$ is calculated to be about 0.40μF; thus a capacitance of 0.33μF or 0.47μF can be chosen for CIN.

Note that any mismatch in resistance and capacitance between two differential audio inputs will cause a mismatch in the corner frequencies. Severe mismatch may also cause turn-on pop noise, PSRR, CMRR performance. Choose both resistors and capacitors with a tolerance of ±5% or better.

Furthermore, the type of the input capacitors is crucial to audio quality. For best audio quality, use capacitors whose dielectrics have low voltage coefficients, such as tantalum or aluminum electrolytic, for less distortion at low frequencies. Other factors for consideration when designing the input filter include the constraints of the overall system. For example, the physical size of the speakers used in most portable devices limits the low frequency response. In this case, the frequency components below 80Hz may be filtered out.

## PRINTED CIRCUIT BOARD (PCB) LAYOUT

Supply Decoupling Capacitors – The supply decoupling capacitors, Cs, should be individually placed as close to the AVDD and CVDD pins as possible. Place a 10μF capacitor close to the CVDD (Pin 4) pin and a 1μF capacitor close to the AVDD (Pin 8) pin. Also, it is strongly recommended to place the ft2810D as close to the large (220μF or greater) bulk power supply decoupling capacitors on the system board as possible.

Flying Capacitors – Place the $C_{F1}$ flying capacitor as close to the $C_{P1}$ and $C_{N1}$ pins as possible and the $C_{F2}$ flying capacitor as close to the $C_{P2}$ and $C_{N2}$ pins as possible.

Boosted Voltage Holding Capacitor – The boosted voltage holding capacitor, $C_{OUT}$, should be placed as close to the PVDD (Pin 12 and 16) pins as possible. Also, it is required to short the PVOUT (Pin 18) pin to the PVDD pins by a wide and short metal trace on the system board. For high power (greater than 2.8W) applications, it is strongly recommended to place a 220μF tantalum or electrolytic capacitor in parallel with a 10μF ceramic capacitor.

EMI – The ferrite EMI filter should be placed as close to the output terminals as possible for the best EMI performance. Keep the current loop from each of the outputs (VOP and VON) through the ferrite bead, the small filter capacitor, and back to PGND short and in close proximity.

Grounding – For best operation, it is required to employ a solid copper plane as the star ground for ft2810D. The GND (Pin 20) and PGND (Pin 14) pins should be individually connected to the star ground plane with sufficiently wide traces.

Thermal Pad – The thermal pad must be directly soldered onto a grounded metal island for proper power dissipation to ensure optimal performance and long-term reliability. Place five solid VIAs (whose diameter is 0.3mm or less) equally spaced underneath the thermal pad. The VIAs should be connected to a solid copper plane, either on an internal layer or on the bottom layer of the system board. Note that the VIAs must be solid ones, not thermal relief or webbed VIAs.

## TYPICAL APPLICATION CIRCUITS

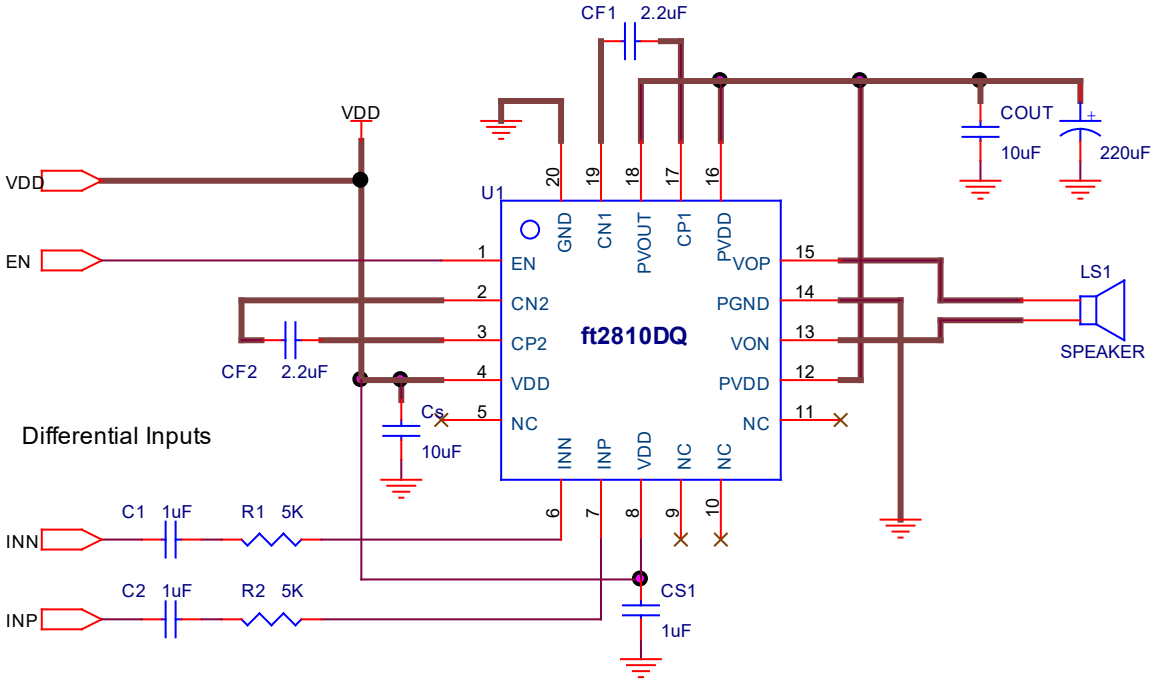



**Figure 42: Differential Audio Inputs**

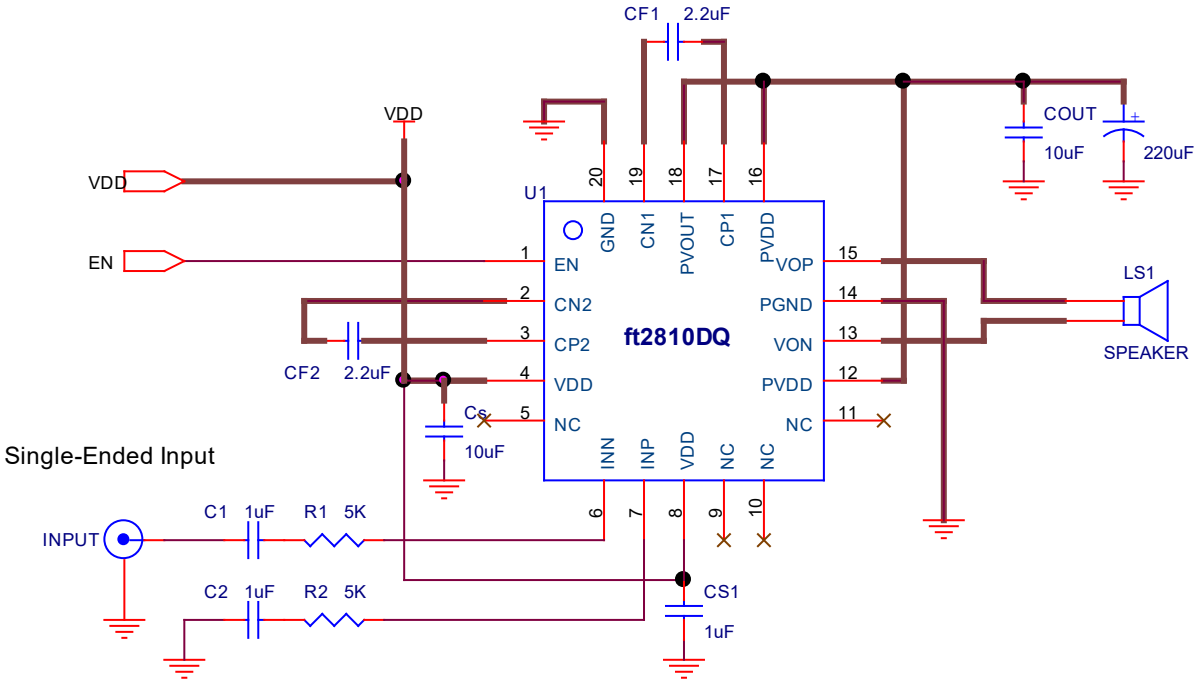



**Figure 43: Single-Ended Audio Input**

Note: The bold lines indicate high current paths and their respective traces are required to be as wide and short as possible on the system board for high power applications.

## TYPICAL APPLICATION CIRCUITS (Cont'd)

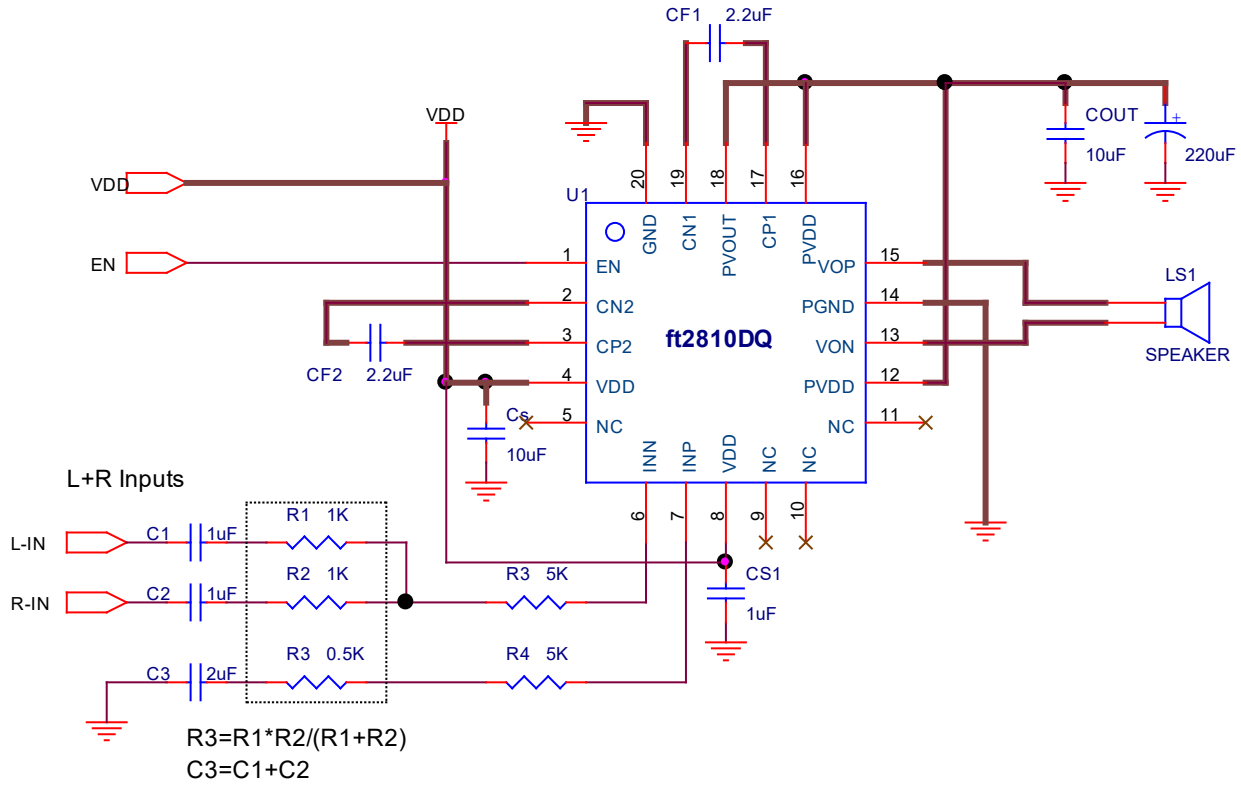



**Figure 44: Dual Channel Audio Inputs**

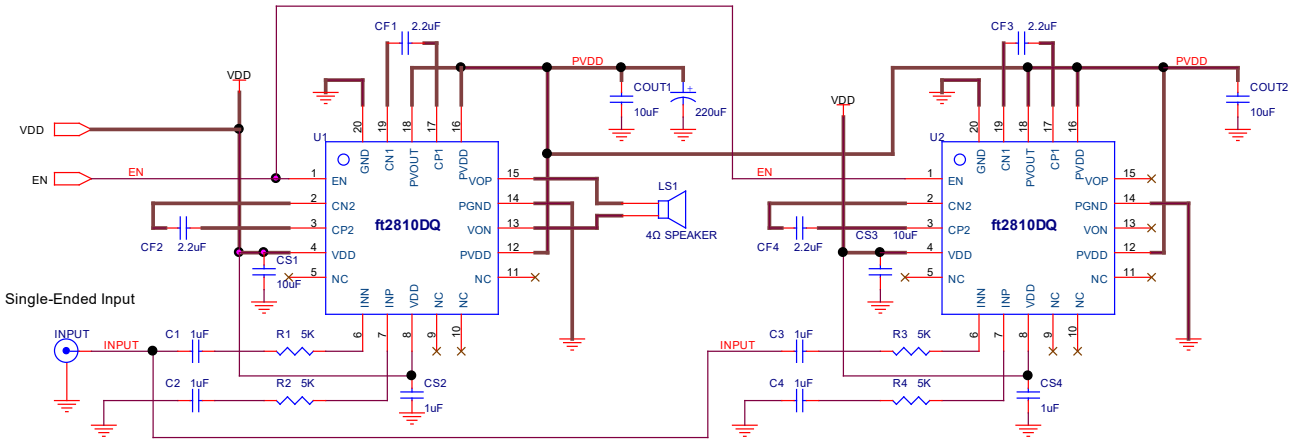
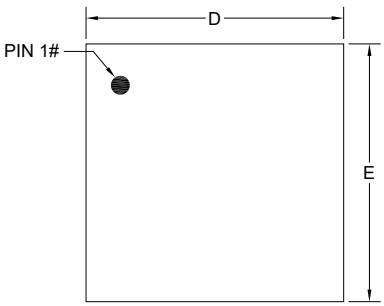



**Figure 45: Dual ft2810Ds in Tandem for Higher Output Power Applications**

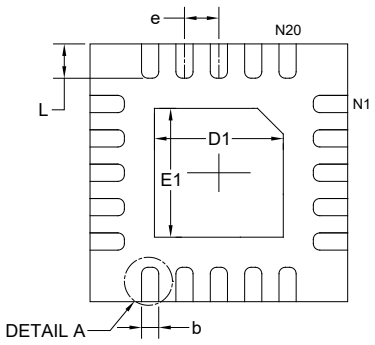
Note: The bold lines indicate high current paths and their respective traces are required to be as wide and short as possible on the system board for high power applications.

# PHYSICAL DIMENSIONS

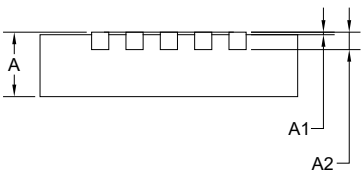
## TQFN-3×3-20AL



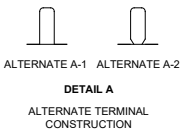

TOP VIEW

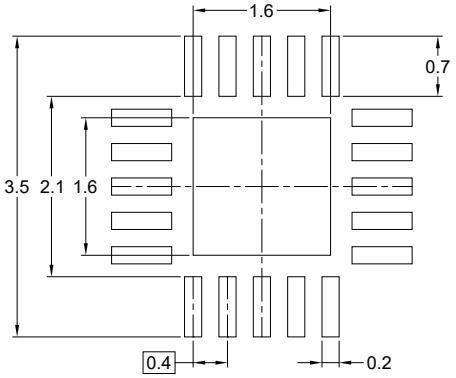



BOTTOM VIEW




SIDE VIEW




**RECOMMENDED LAND PATTERN** (Unit: mm)

| Symbol | Dimensions In Millimeters | | |
|---|---|---|---|
| | MIN | MOD | MAX |
| A | 0.700 | - | 0.900 |
| A1 | 0.000 | - | 0.050 |
| A2 | 0.203 REF | | |
| b | 0.150 | 0.200 | 0.250 |
| D | 2.900 | 3.000 | 3.100 |
| D1 | 1.400 | - | 1.650 |
| E | 2.900 | 3.000 | 3.100 |
| E1 | 1.400 | - | 1.650 |
| e | 0.400 BSC | | |
| L | 0.350 | 0.400 | 0.450 |

NOTE: This drawing is subject to change without notice.

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