

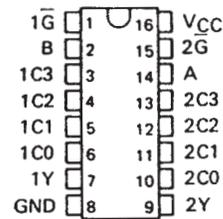
SN54LS253, SN54S253, SN74LS253, SN74S253 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

SDLS147 – SEPTEMBER 1972 – REVISED MARCH 1988

- Three-State Version of SN54/74LS153, SN54/74S153
- Schottky-Diode-Clamped Transistors
- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Fully Compatible with Most TTL Circuits
- Low Power Dissipation
 - 'LS253 . . . 35 mW Typical
 - 'S253 . . . 225 mW Typical

SN54LS253, SN54S253 . . . J OR W PACKAGE
SN74LS253, SN74S253 . . . D OR N PACKAGE

(TOP VIEW)



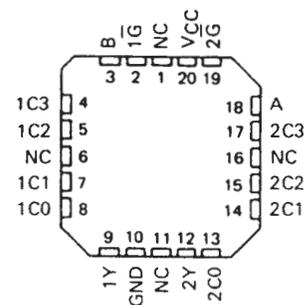
description

Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level.

SN54LS253, SN54S253 . . . FK PACKAGE

(TOP VIEW)



NC-No internal connection

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.

H = high level, L = low level, X = irrelevant, Z = high impedance (off)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage: 'LS253	7 V
'S253	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS253, SN54S253	– 55°C to 125°C
SN74LS253, SN74S253	0°C to 70°C
Storage temperature range	– 65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



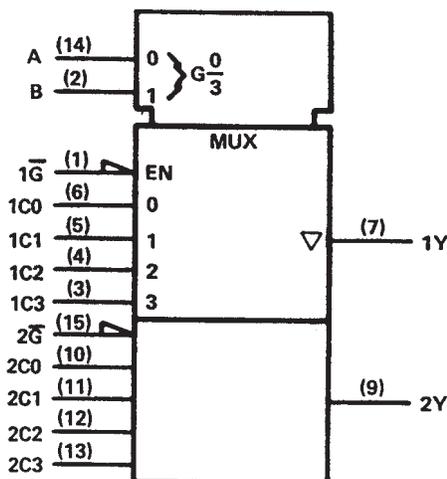
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SN54LS253, SN54S253, SN74LS253, SN74S253 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

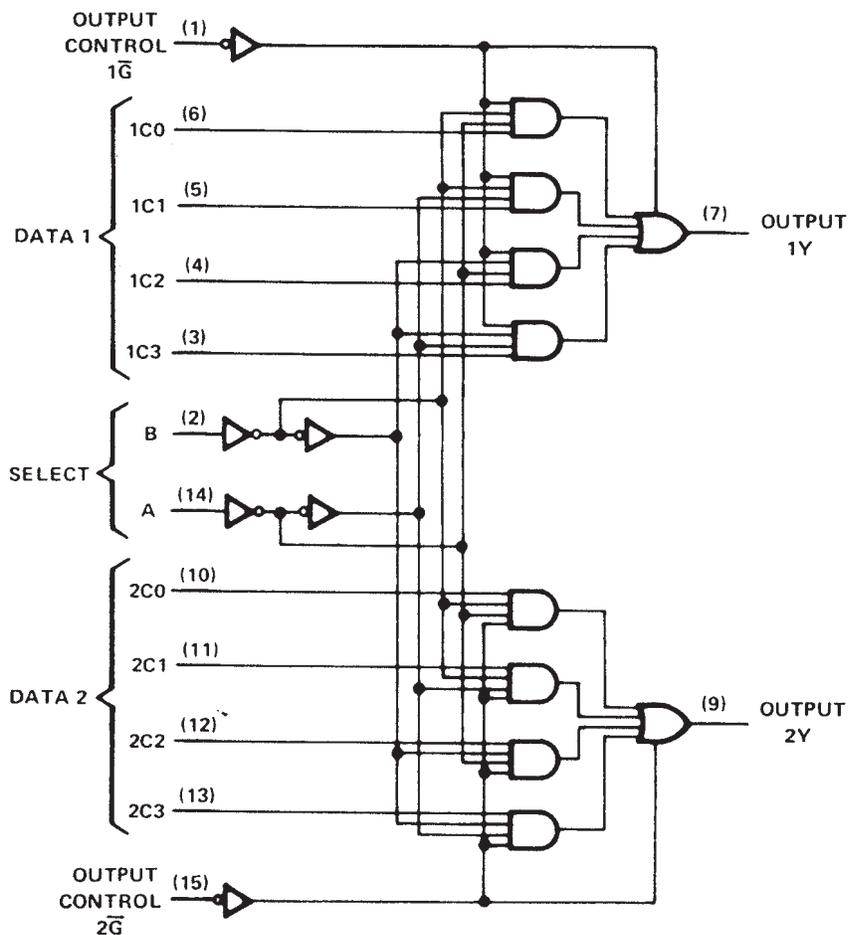
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

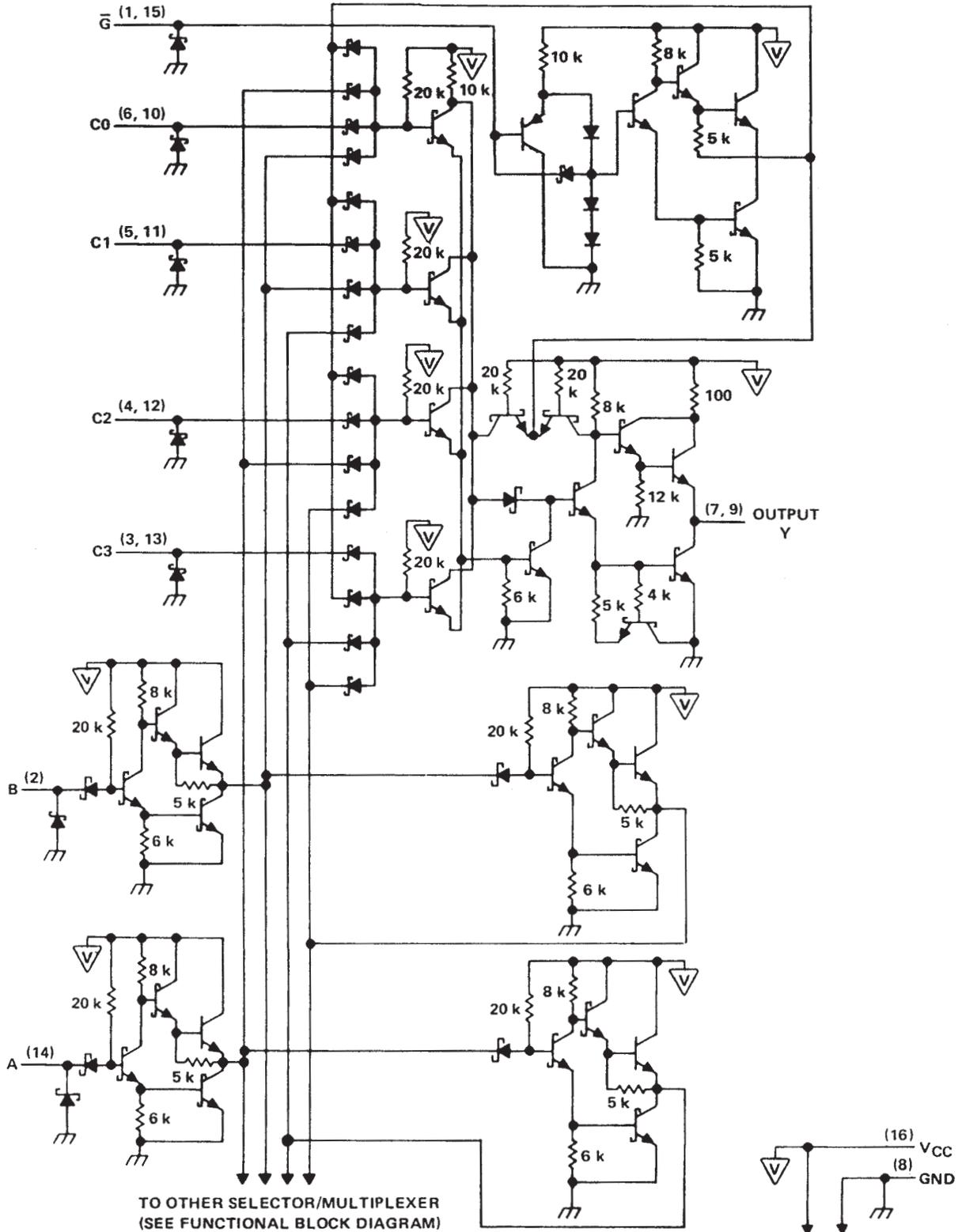


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SN54LS253, SN54S253, SN74LS253, SN74S253 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

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schematic (each selector/multiplexer, and the common select section)



Pin numbers shown are for D, J, N, and W packages.



SN54LS253, SN54S253, SN74LS253, SN74S253 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

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recommended operating conditions

	SN54LS253			SN74LS253			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage	0.7			0.8			V
I _{OH} High-level output current	-1			-2.6			mA
I _{OL} Low-level output current	4			8			mA
T _A Operating free-air temperature	-55 125			0 70			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS253		SN74LS253		UNIT
		MIN	TYP ‡	MAX	MIN	
V _{IK}	V _{CC} = MIN, I _I = -18 mA	-1.5		-1.5		V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4	2.4	3.1	V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OL} = 4 mA		0.25	0.4	V
		I _{OL} = 8 mA		0.25 0.5		
I _{OZ}	V _{CC} = MAX, V _{IH} = 2 V	V _O = 2.7 V		20		μA
		V _O = 0.4 V		-20		
I _I	V _{CC} = MAX, V _I = 7 V	0.1		0.1		mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V	20		20		μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V	G̅		-0.2		mA
		All other		-0.4		
I _{OS} §	V _{CC} = MAX	-30	-130	-30	-130	mA
I _{CC}	V _{CC} = MAX, See Note 2	Condition A		7	12	mA
		Condition B		8.5	14	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration for the short-circuit should exceed one second.

NOTE 2: I_{CC} is measured with the outputs open under the following conditions:

- A. All inputs grounded.
- B. Output control at 4.5 V, all inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Data	Y	C _L = 15 pF, R _L = 2 kΩ, See Note 3	17	25	ns	
t _{PHL}				13	20		
t _{PLH}	Select	Y		30	45	ns	
t _{PHL}				21	32		
t _{PZH}	Output Control	Y		15	28	ns	
t _{PZL}				15	23		
t _{PHZ}	Output Control	Y	C _L = 5 pF, R _L = 2 kΩ, See Note 3	27	41	ns	
t _{PLZ}				18	27		

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



SN54LS253, SN54S253, SN74LS253, SN74S253 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

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recommended operating conditions

	SN54S253			SN74S253			UNIT	
	MIN	NOM	MAX	MIN	NOM	MAX		
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V	
V _{IH} High-level input voltage	2			2			V	
V _{IL} Low-level input voltage	0.8			0.8			V	
I _{OH} High-level output current	-2			-6.5			mA	
I _{OL} Low-level output current	20			20			mA	
T _A Operating free-air temperature	-55			0			70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V _{IK}	V _{CC} = MIN, I _I = -18 mA	-1.2			V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = MAX	Series 54S	2.5	3.4	V
		Series 74S	2.7	3.4	
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA	0.5			V
I _{OZ}	V _{CC} = MAX, V _{IH} = 2 V	V _O = 2.4 V	50		μA
		V _O = 0.5 V	-50		
I _I	V _{CC} = MAX, V _I = 5.5 V	1			mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V	50			μA
I _{IL}	V _{CC} = MAX, V _I = 0.5 V	\bar{G} = 0.8 V	-2		mA
		\bar{G} = 2 V	-0.25		
I _{OS§}	V _{CC} = MAX	-40	-100		mA
I _{CC}	V _{CC} = MAX, See Note 2	Condition A	45	70	mA
		Condition B	65	85	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

Not more than one output should be shorted at a time and duration of short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with the outputs open under the following conditions:

- A. All inputs grounded.
- B. Output control at 4.5 V, all inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Data	Y	R _L = 280 Ω, See Note 3	C _L = 15 pF	6	9	ns
t _{PHL}					6	9	
t _{PLH}	Select	Y			11.5	18	ns
t _{PHL}					12	18	
t _{PZH}	Output	Y			11	16.5	ns
t _{PZL}	Control				12	18	
t _{PHZ}	Output	Y	R _L = 280 Ω, See Note 3	C _L = 5 pF	6.5	9.5	ns
t _{PLZ}					Control	10	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
76017012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	76017012A SNJ54LS 253FK	Samples
7601701EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7601701EA SNJ54LS253J	Samples
7601701EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7601701EA SNJ54LS253J	Samples
7601701FA	NRND	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7601701FA SNJ54LS253W	
7601701FA	NRND	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7601701FA SNJ54LS253W	
JM38510/30908B2A	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 30908B2A	
JM38510/30908B2A	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 30908B2A	
JM38510/30908BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30908BEA	Samples
JM38510/30908BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30908BEA	Samples
JM38510/30908BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30908BFA	Samples
JM38510/30908BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30908BFA	Samples
M38510/30908B2A	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 30908B2A	
M38510/30908B2A	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 30908B2A	
M38510/30908BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30908BEA	Samples
M38510/30908BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30908BEA	Samples
M38510/30908BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30908BFA	Samples
M38510/30908BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30908BFA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										30908BFA	
SN54LS253J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS253J	Samples
SN54LS253J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS253J	Samples
SN74LS253DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS253	Samples
SN74LS253DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS253	Samples
SN74LS253J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	0 to 70		
SN74LS253J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	0 to 70		
SN74LS253N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS253N	Samples
SN74LS253N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS253N	Samples
SN74LS253N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74LS253N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74S253N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74S253N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SNJ54LS253FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	76017012A SNJ54LS 253FK	Samples
SNJ54LS253FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	76017012A SNJ54LS 253FK	Samples
SNJ54LS253J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7601701EA SNJ54LS253J	Samples
SNJ54LS253J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7601701EA SNJ54LS253J	Samples
SNJ54LS253W	NRND	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7601701FA SNJ54LS253W	
SNJ54LS253W	NRND	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7601701FA SNJ54LS253W	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54LS253, SN74LS253 :

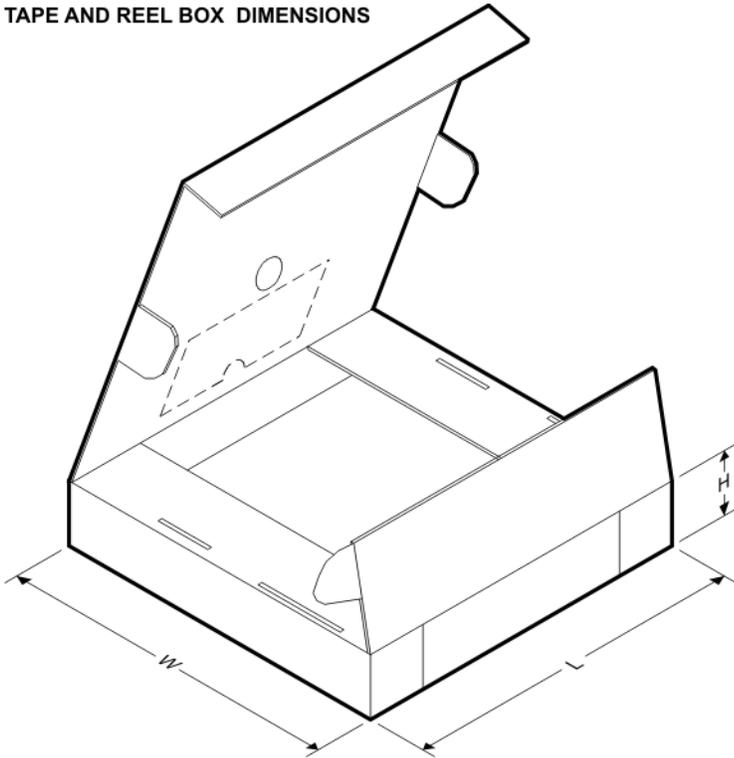
● Catalog: [SN74LS253](#)

● Military: [SN54LS253](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL BOX DIMENSIONS



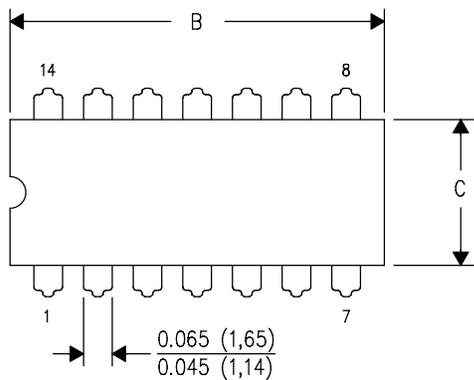
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS253DR	SOIC	D	16	2500	333.2	345.9	28.6

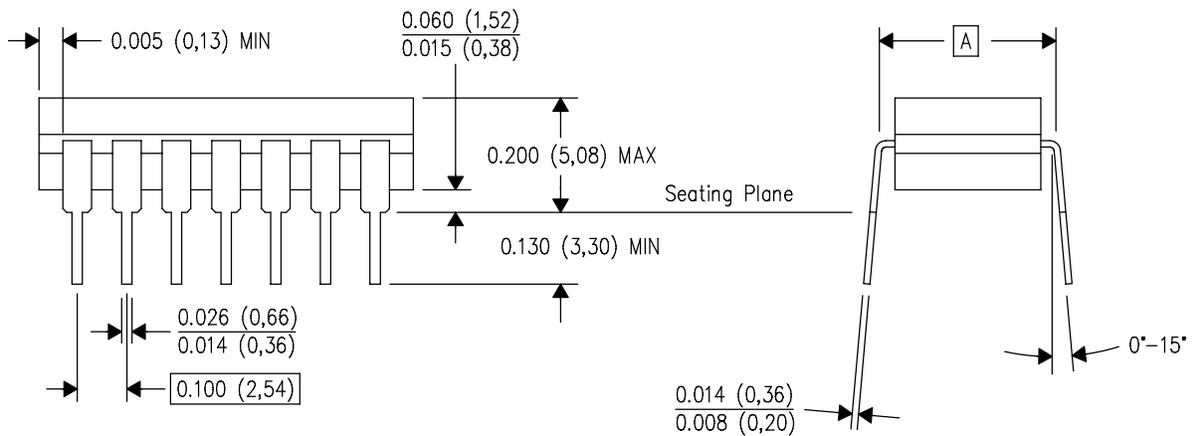
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

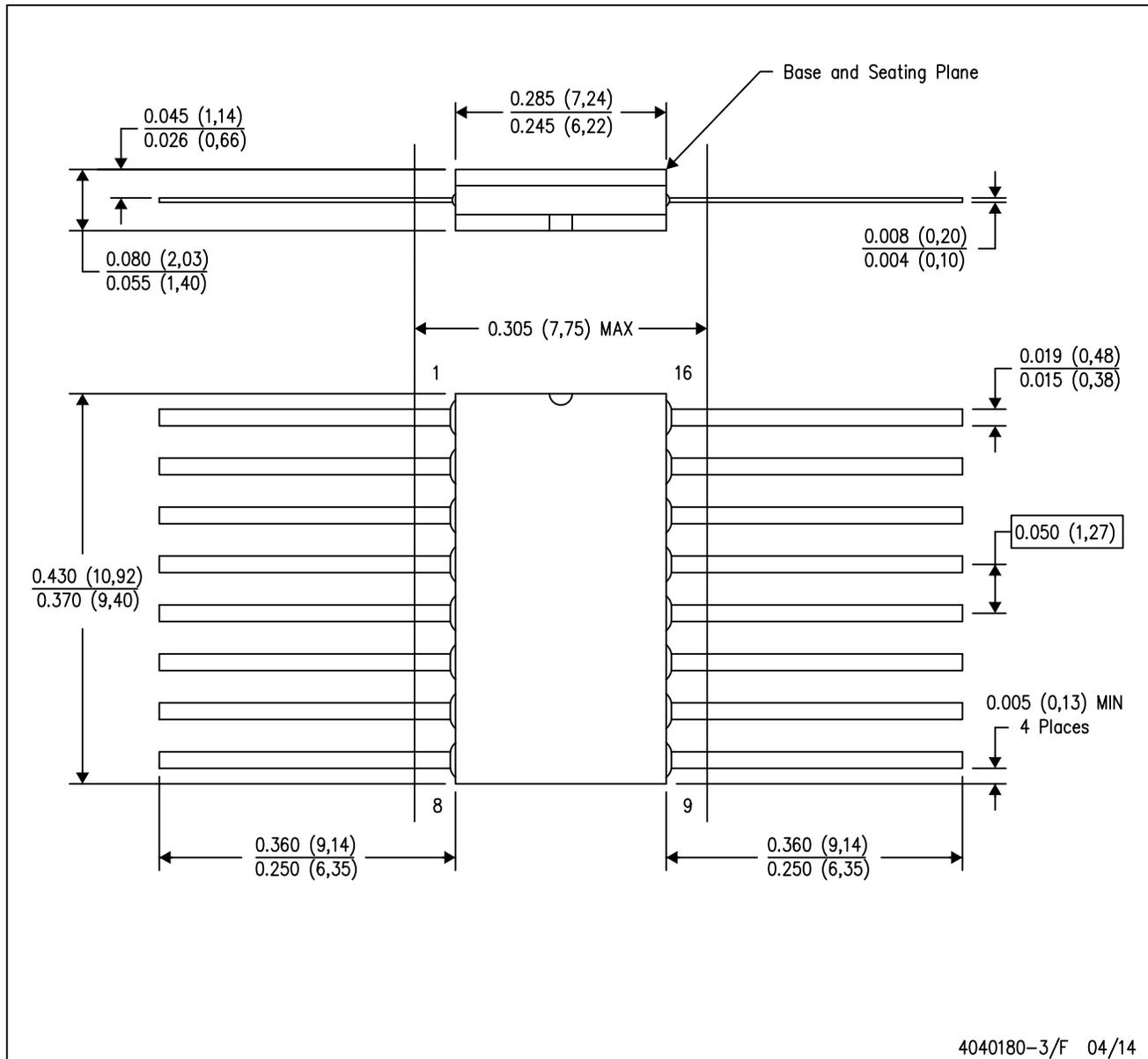


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK

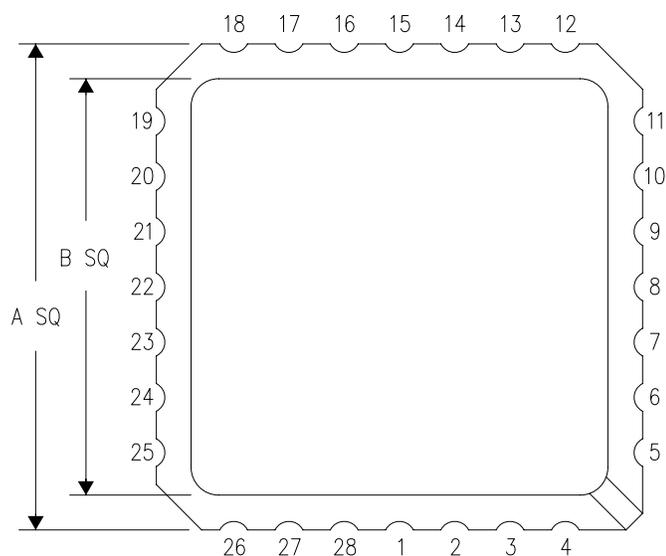


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP2-F16

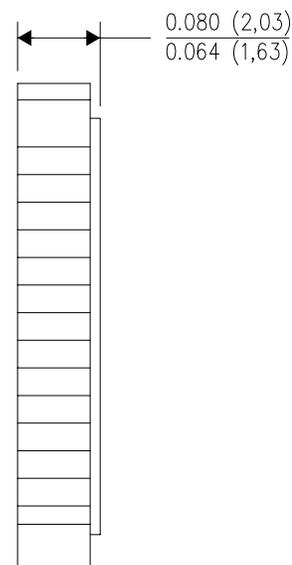
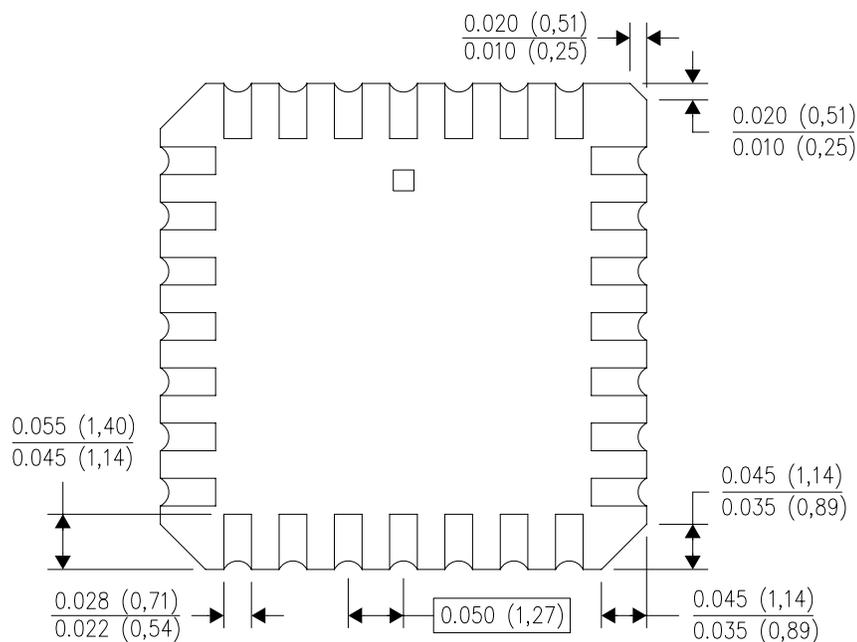
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



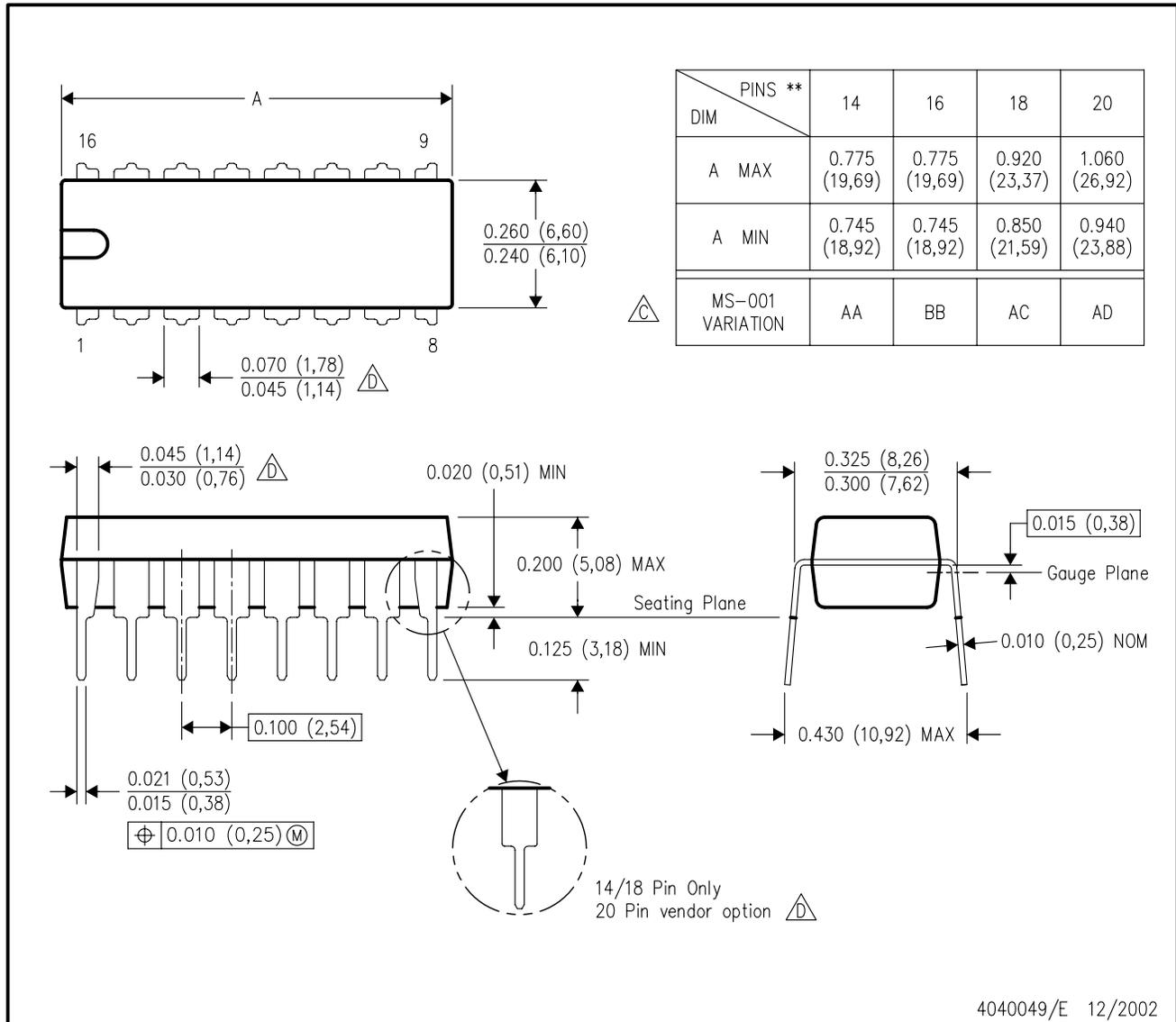
4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

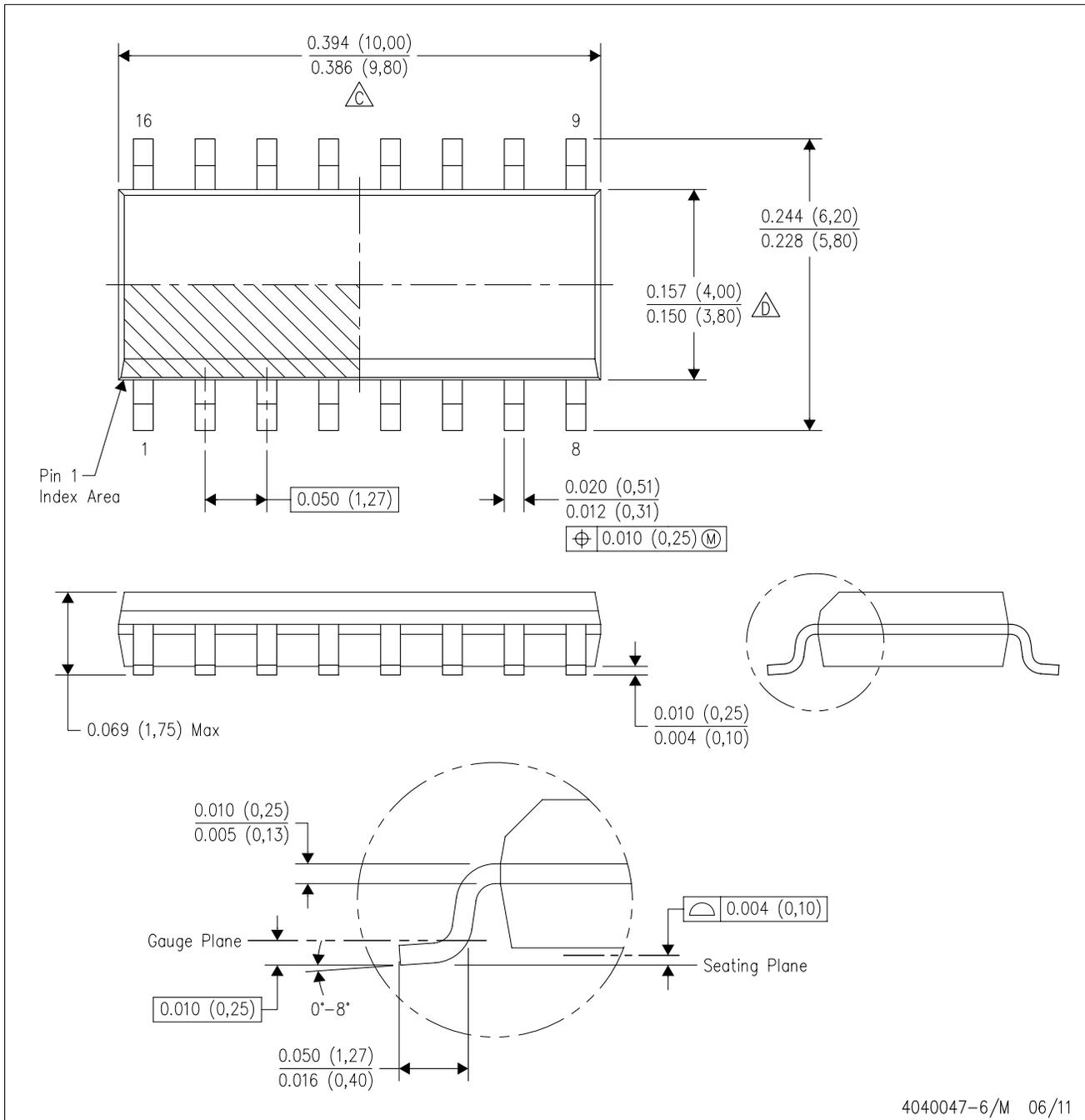
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

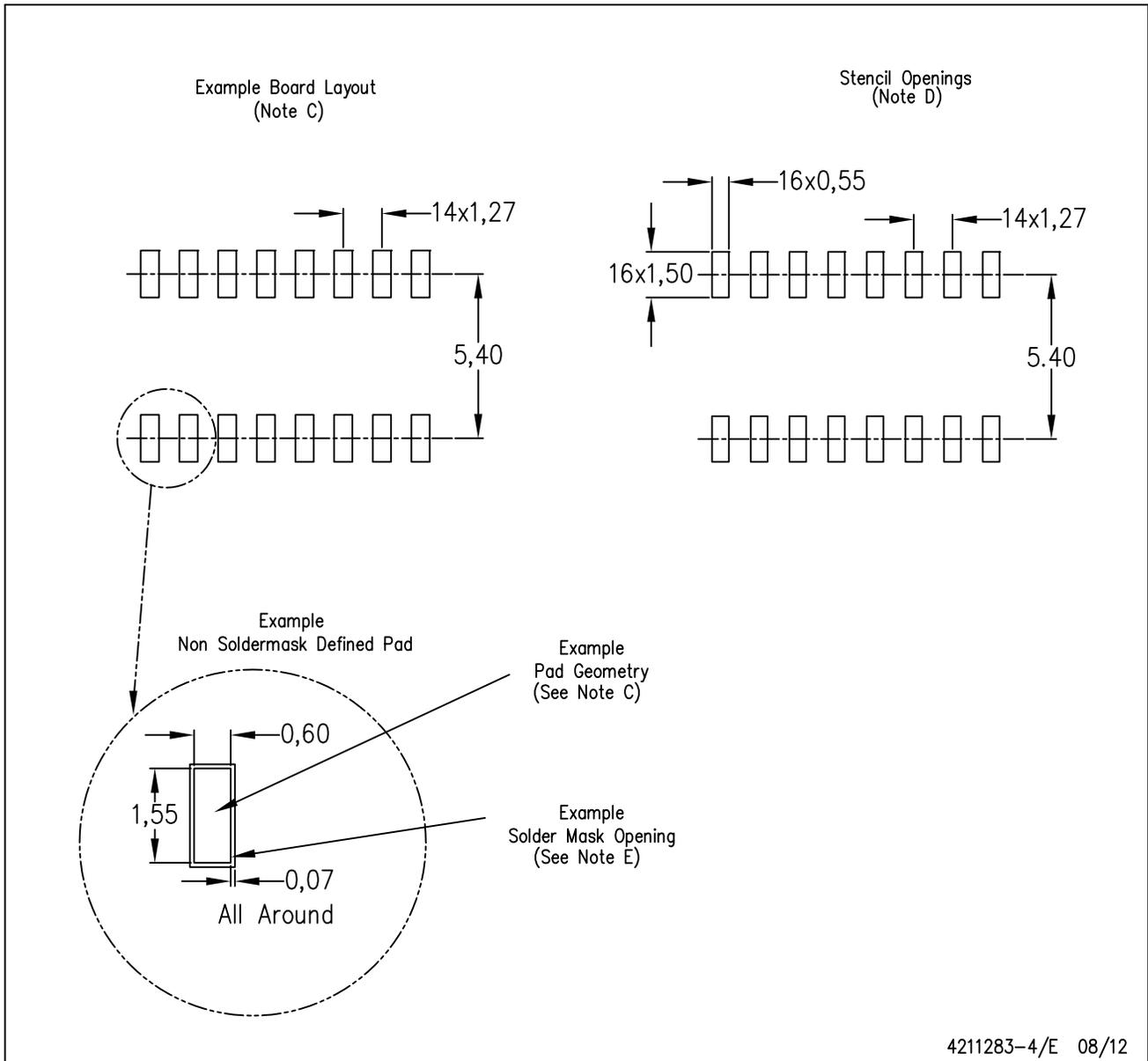
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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