

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

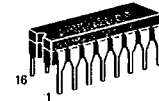
**Hex Buffers/Logic-Level
Down Converters**
High-Performance Silicon-Gate CMOS

The MC54/74HC4049 consists of six inverting buffers, and the MC54/74HC4050 consists of six noninverting buffers. They are identical in pinout to the MC14049UB and MC14050B metal-gate CMOS buffers. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The input protection circuitry on these devices has been modified by eliminating the V_{CC} diodes to allow the use of input voltages up to 15 volts. Thus, the devices may be used as logic-level translators that convert from a high voltage to a low voltage while operating at the low-voltage power supply. They allow MC14000-series CMOS operating up to 15 volts to be interfaced with High-Speed CMOS at 2 to 6 volts. The protection diodes to GND are Zener diodes, which protect the inputs from both positive and negative voltage transients.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 5 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 36 FETs or 9 Equivalent Gates (4049)
24 FETs or 6 Equivalent Gates (4050)

MC54/74HC4049
MC54/74HC4050



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-06



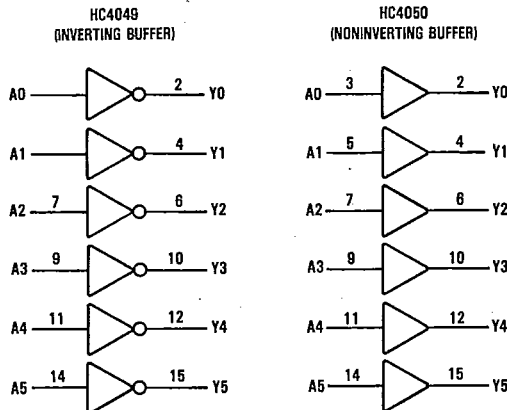
D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXD	SOIC

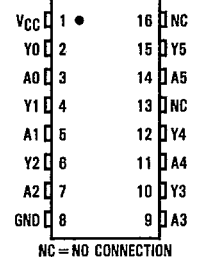
T_A = -55° to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAMS



PIN 1 = V_{CC}
PIN 8 = GND
PINS 13, 16 = NO CONNECTION

***PIN ASSIGNMENT**



FUNCTION TABLE

A Inputs	Y Outputs	
	HC4049	HC4050
L	H	L
H	L	H

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MC54/74HC4049•MC54/74HC4050

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-1.5 to +18	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields referenced to the GND pin, only. Extra precautions must be taken to avoid applications of any voltage higher than the maximum rated voltages to this high-impedance circuit. For proper operation, the ranges $GND \leq V_{in} \leq 15$ V and $GND \leq V_{out} \leq V_{CC}$ are recommended. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{in}	DC Input Voltage (Referenced to GND)	0	V _{CC} to 15	V
V _{out}	DC Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} =2.0 V V _{CC} =4.5 V V _{CC} =6.0 V	0 1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} =0.1 V or V _{CC} -0.1 V I _{out} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} =0.1 V or V _{CC} -0.1 V I _{out} ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V _{OH}	Minimum High-Level Output Voltage	V _{in} =V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} =V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I _{in}	Maximum Input Leakage Current	V _{in} =V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5	3.98	3.84	3.70	μA
			6.0	5.48	5.34	5.20	
			6.0	0.26	0.33	0.40	
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} =15 V or GND I _{out} =0 μA	6.0	±0.1	±1.0	±1.0	μA
			6.0	0.5	5.0	5.0	
			6.0	2	20	40	

NOTE: Information on typical parametric values can be found in Chapter 4.



MC54/74HC4049•MC54/74HC4050

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2.0	85	105	130	ns
		4.5	17	21	26	
		6.0	14	18	22	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: P _D = CPD V _{CC} ² f + I _{CC} V _{CC} For load considerations, see Chapter 4.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		27	

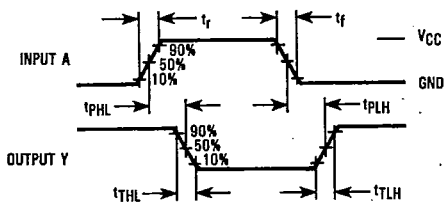


Figure 1a. Switching Waveforms (HC4049)

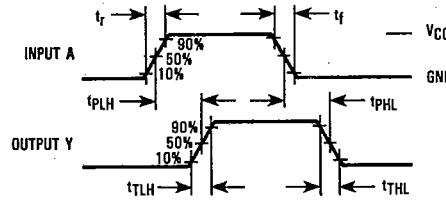
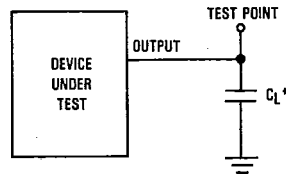


Figure 1b. Switching Waveforms (HC4050)

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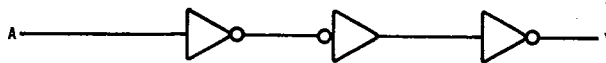
*Includes all probe and jig capacitance.

Figure 2. Test Circuit

MC54/74HC4049•MC54/74HC4050

LOGIC DETAIL

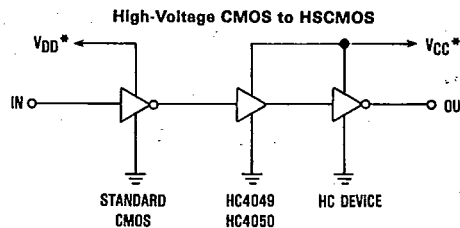
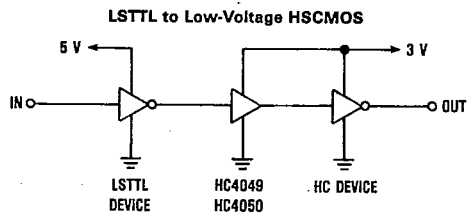
HC4049
(1/6 of the Device)



HC4050
(1/6 of the Device)



TYPICAL APPLICATIONS



NOTE: To determine the noise immunity for the LSTTL to low-voltage configuration, use Eq. 1 and Eq. 2:
 (TTL) $V_{OH} - (CMOS) V_{IH}$ Eq. 1
 (TTL) $V_{OL} - (CMOS) V_{IL}$ Eq. 2

For the supply levels shown:
 $2.4 - 3 (75\%) = 2.4 - 2.25 = 0.15 V$
 $0.4 - 3 (15\%) = 0.4 - 0.45 = -0.05 V$

Therefore, worst case noise immunity is 50 mV.
 For supply levels greater than 4.5 volts use the 74HCT04 for direct interface to TTL outputs.

***Table 1. Supply Examples**

V _{DD}	V _{CC}
15 V	2 V
12 V	5 V
12 V	3 V