

General Description

The SY82806 high efficiency 500kHz synchronous buck converter operates over a wide input voltage range of 4.5V to 30V, and can deliver an output current up to 6A. It integrates a top MOSFET and a bottom MOSFET with very low $R_{DS(ON)}$ to minimize conduction loss. The 500kHz pseudo-constant switching frequency enables using small external inductor and capacitor values.

Silergy's constant on-time and ripple-based control strategy supports high input/output voltage ratios (low duty cycles), and fast transient response while maintaining a near constant operating frequency over line, load and output voltage ranges. This control method provides stable operation without complex compensation, including when using low ESR output ceramic capacitors.

The SY82806 provides cycle-by-cycle current limit, input under voltage lockout, internal soft-start, output under voltage protection and over temperature protection to guarantee safe operation in all operating conditions.

Features

- Low $R_{DS(ON)}$ for Internal MOSFETs: 40mΩ Top, 20mΩ Bottom
- Wide Input Voltage Range: 4.5V ~ 30V
- Adjustable Output Voltage: 0.6V ~ 24V
- 6A Continuous Output Current Capability
- 500kHz Pseudo-Constant Frequency
- $\pm 1.5\%$ 0.6V Reference under $-40^{\circ}\text{C} \sim 125^{\circ}\text{C}$
- Precise EN Threshold
- Internal 1ms Soft-Start Limits the Inrush Current
- Support Smooth Startup with Pre-Biased Output
- Constant On-time and Ripple-Based Control to Achieve Fast Transient Responses
- PFM Light Load Operation for High Efficiency
- Power Good Indicator
- Output Auto-Discharge Function
- Cycle-by-Cycle Valley and Peak Current Limit Protection
- Hic-Cup Mode Output Under Voltage Protection
- Auto-Recovery Mode Over Temperature Protection
- Input Under Voltage Lockout (UVLO)
- RoHS Compliant and Halogen Free
- Compact Package: QFN2x3-14
- Moisture Sensitivity Level (MSL): 1

Applications

- LCD-TV/Net-TV/3DTV
- Set Top Box
- Monitor
- High Power AP

Typical Application

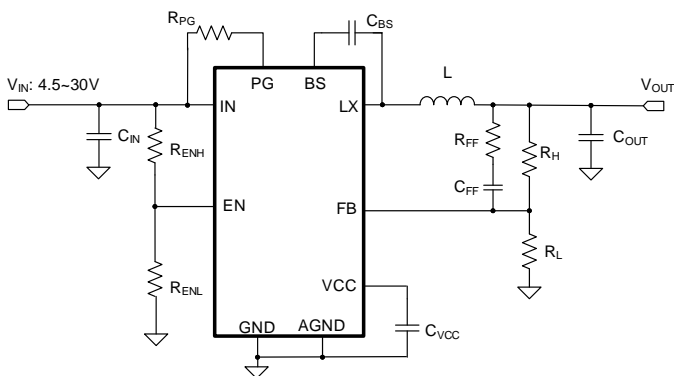


Figure 1. Schematic Diagram

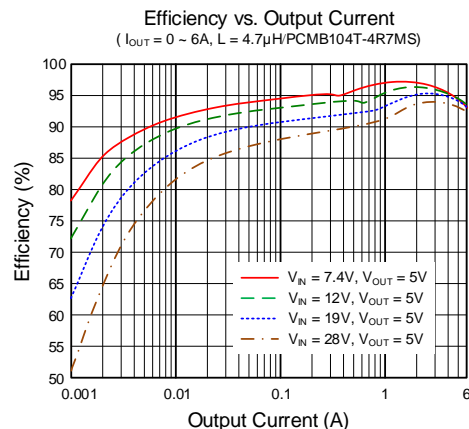


Figure 2. Efficiency vs. Output Current

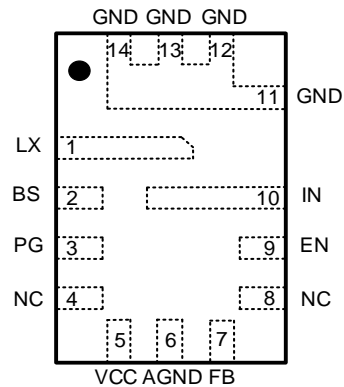


Ordering Information

Ordering Part Number	Package type	Top Mark
SY82806WYQ	QFN2x3-14 RoHS Compliant and Halogen Free	FNExyz

x=year code, y=week code, z=lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	LX	Inductor pin. Connect this pin to the switching node of the inductor.
2	BS	Bootstrap Pin. Supply top MOSFET gate driver. Connect a 0.1μF ceramic capacitor between the BS pin and the LX pin.
3	PG	Power good indicator pin. PG pin should be connected to V _{IN} or another voltage source through a resistor (e.g., 10kΩ ~ 100kΩ). This pin becomes high when the output voltage is within 90% to 120% of regulated value under normal operation.
4, 8	NC	Not connected.
5	VCC	Internal 3.3V LDO output pin. Power supply for internal analog circuits. Decouple this pin to ground with at least a 2.2μF ceramic capacitor.
6	AGND	Analog ground pin.
7	FB	Output feedback pin. Connect this pin to the center point of the output resistor divider as shown in Figure 1. $V_{OUT} = 0.6 \times (1 + R_H/R_L)$.
9	EN	Enable pin. Pull this pin higher than EN rising threshold to turn on the device and pull this pin lower than EN falling threshold to turn off the device. Do not leave this pin floating.
10	IN	Input pin. Decouple this pin to the GND pin with at least a 10μF ceramic capacitor. A 0.1μF ceramic capacitor placed in parallel is recommended to reduce high frequency noise.
11, 12, 13, 14	GND	Power ground pin.

Block Diagram

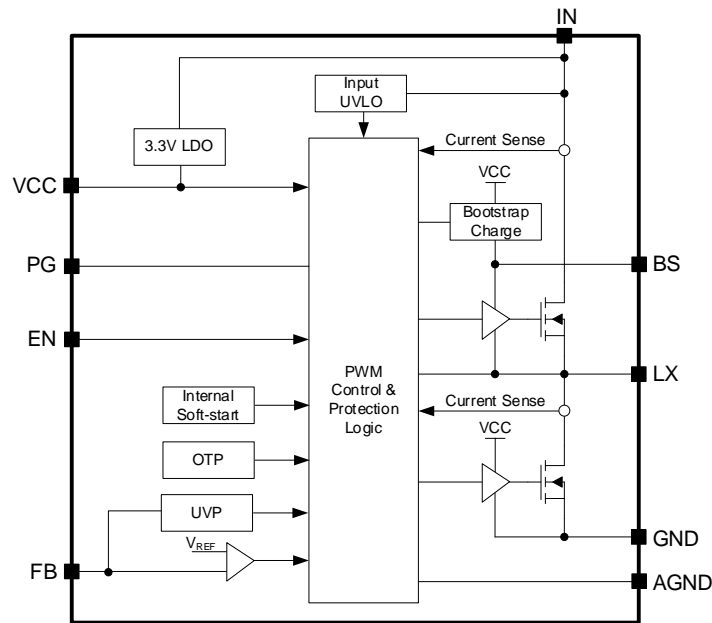


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
IN	-0.3	31	V
LX, PG, EN	-0.3	IN + 0.3	
BS-LX, VCC	-0.3	4	
FB	-0.3	6	
LX, 10ns Duration	GND - 5	IN + 3	
LX, 20ns Duration	GND - 1	IN + 2	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10sec.)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	22	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	3	
P_D Power Dissipation $T_A=25^\circ\text{C}$	4.5	W

Recommended Operating Conditions

Parameter (Note3)	Min	Max	Unit
Input Voltage	4.5	30	V
Output Voltage	0.6	24	
Continuous Output Current		6	A
Ambient Temperature	-40	85	°C
Junction Temperature	-40	125	

Electrical Characteristics

($T_J = 25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $V_{OUT} = 5\text{V}$, $L = 4.7\mu\text{H}$, $C_{OUT} = 66\mu\text{F}$, $I_{OUT} = 1\text{A}$, unless otherwise specified(Note4))

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input	Voltage Range	V_{IN}	4.5		30	V	
	UVLO Rising Threshold	$V_{IN,UVLO}$	V_{IN} rising		4.4		
	UVLO Hysteresis	$V_{IN,HYS}$		0.3			
	Quiescent Current	I_Q	$I_{OUT} = 0\text{A}$, $EN = \text{High}$, $V_{FB} = V_{REF} \times 105\%$		120	μA	
	Shutdown Current	I_{SHDN}	$EN = \text{Low}$		5		10
Output	Voltage Range	V_{SET}	0.6		24	V	
	Feedback Reference Voltage	V_{REF}	$T_J = -40^\circ\text{C} \sim 125^\circ\text{C}$	0.591	0.6		0.609
	Discharge Current	I_{DIS}	$V_{OUT} = 5\text{V}$		80	mA	
	Soft-Start Time	t_{SS}	V_{OUT} from 0% to 100% V_{SET} (Note5)	0.7	1	1.3	ms
	Maximum Duty Cycle	D_{MAX}	Without inductor	98			%
	FB Input Current	I_{FB}	$V_{FB} = 1\text{V}$	-50		50	nA
	UVP Threshold	V_{UVP}		45	50	55	$\%V_{REF}$
	UVP Delay Time	$t_{UVP,DLY}$	(Note5)		40		μs
	UVP Hic-Cup On-Time	$t_{HICCUP,ON}$	(Note5)		2		ms
	UVP Hic-Cup Off-Time	$t_{HICCUP,OFF}$	(Note5)		6		
MOSFETs	Top MOSFET $R_{DS(ON)}$	$R_{DS(ON),TOP}$		40		$\text{m}\Omega$	
	Bottom MOSFET $R_{DS(ON)}$	$R_{DS(ON),BOT}$		20			
	Top MOSFET Current Limit Threshold	$I_{LMT,TOP}$		9		A	
	Bottom MOSFET Current Limit Threshold	$I_{LMT,BOT}$		6			
Enable (EN)	Rising Threshold	$V_{EN,R}$	1.08	1.2	1.32	V	
	Falling Threshold	$V_{EN,F}$	0.9	1.0	1.1		
Frequency	Switching Frequency	f_{SW}	$V_{OUT} = 5\text{V}$, CCM	425	500	575	kHz
	Minimum On-Time	$t_{ON,MIN}$		50		ns	
	Minimum Off-Time	$t_{OFF,MIN}$		100			
Power Good (PG)	Thresholds	$V_{PG,R}$	V_{FB} rising, PG from low to high	86	90	94	$\%V_{REF}$
		$V_{PG,F}$	V_{FB} falling, PG from high to low	81	85	89	
		$V_{PG,OVP}$	V_{FB} rising, PG from high to low	115	120	125	
		$V_{PG,RCY}$	V_{FB} falling, PG recovers high		115		
	Delay Time	$t_{PG,R}$	Low to high (Note5)		200		μs
		$t_{PG,F}$	High to low (Note5)		40		
	Low Voltage	$V_{PG,LOW}$	$V_{FB} = 0\text{V}$, $I_{PG} = 5\text{mA}$			0.4	V
VCC	Output Voltage	V_{CC}	VCC adds 1mA load	3.15	3.3	3.45	

OTP	Temperature	T _{OTP}	(Note5)		150		°C
	Temperature Hysteresis	T _{OTP,HYS}	(Note5)		15		

Note 1: Stresses beyond “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: Package thermal resistance is measured in the natural convection at T_A = 25°C on a 8.5cmx8.5cm size, four-layer Silergy Evaluation Board with 2-oz copper.

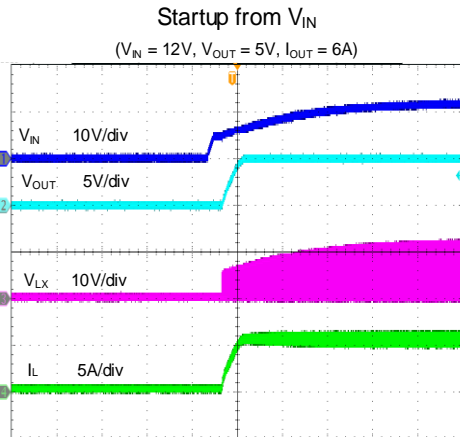
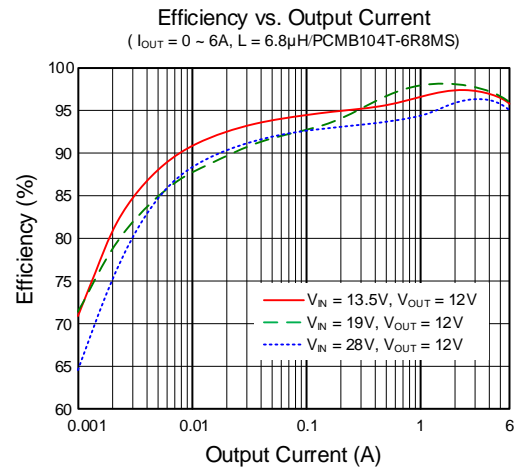
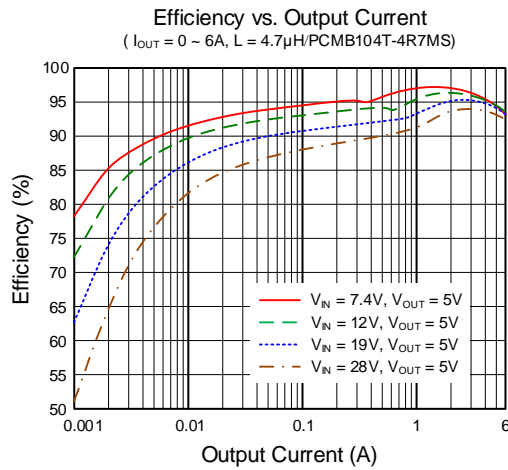
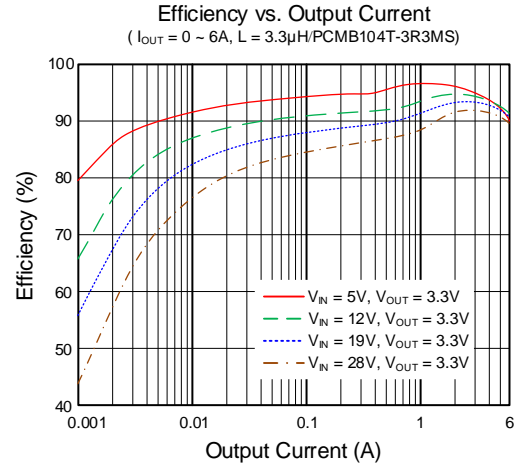
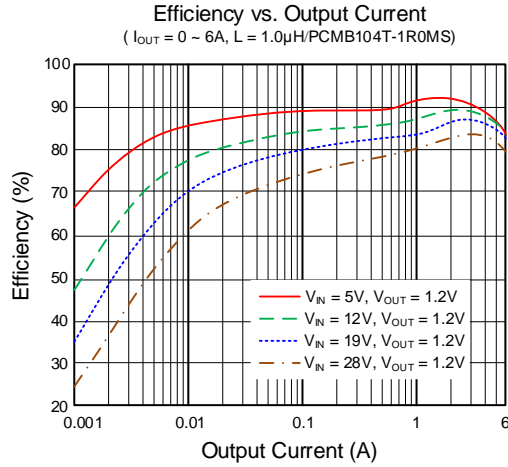
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that T_A ≅ T_J = 25°C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

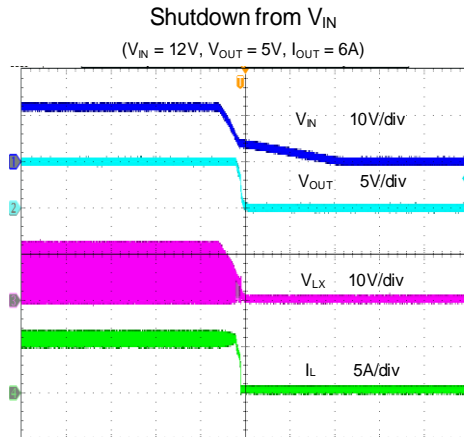
Note 5: Guaranteed by design.

Typical Performance Characteristics

($T_A = 25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $V_{OUT} = 5\text{V}$, $L = 4.7\mu\text{H}$, $C_{OUT} = 66\mu\text{F}$, $C_{FF} = 220\text{pF}$, $R_{FF} = 1\text{k}\Omega$, unless otherwise specified)



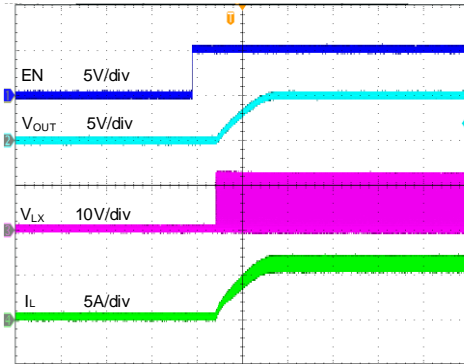
Time (2ms/div)



Time (2ms/div)

Startup from Enable

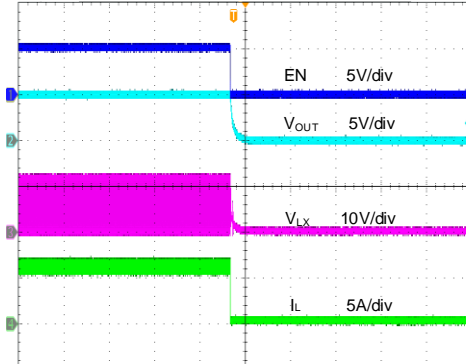
($V_{IN} = 12V$, $V_{OUT} = 5V$, $I_{OUT} = 6A$)



Time (800µs/div)

Shutdown from Enable

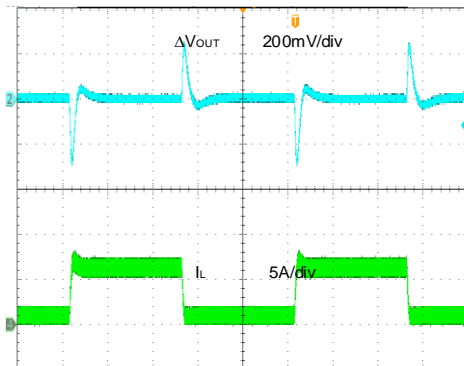
($V_{IN} = 12V$, $V_{OUT} = 5V$, $I_{OUT} = 6A$)



Time (800µs/div)

Load Transient

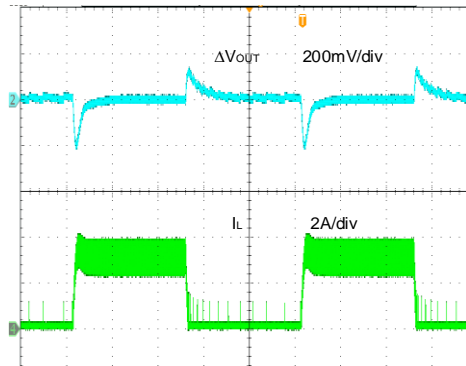
($V_{IN} = 12V$, $V_{OUT} = 5V$, $I_{OUT} = 0.6A \sim 6A$)



Time (200µs/div)

Load Transient

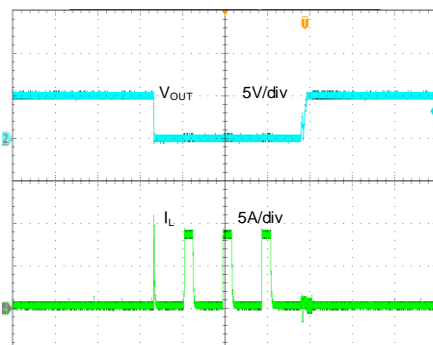
($V_{IN} = 12V$, $V_{OUT} = 5V$, $I_{OUT} = 0A \sim 3A$)



Time (200µs/div)

Output Short Circuit Protection

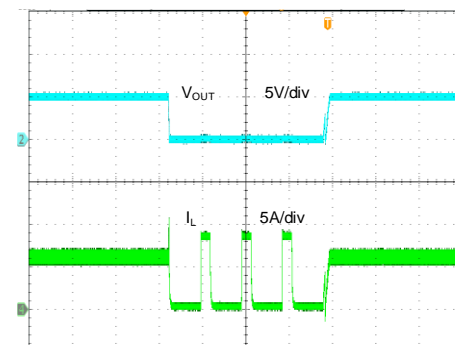
($V_{IN} = 12V$, $V_{OUT} = 5V$, $I_{OUT} = 0A \sim \text{Short}$)



Time (10ms/div)

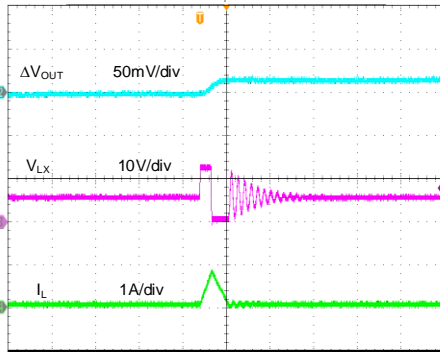
Output Short Circuit Protection

($V_{IN} = 12V$, $V_{OUT} = 5V$, $I_{OUT} = 6A \sim \text{Short}$)



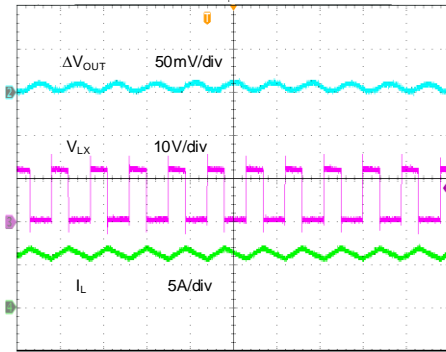
Time (10ms/div)

Output Ripple
($V_{IN} = 12V$, $V_{OUT} = 5V$, $I_{OUT} = 0A$)

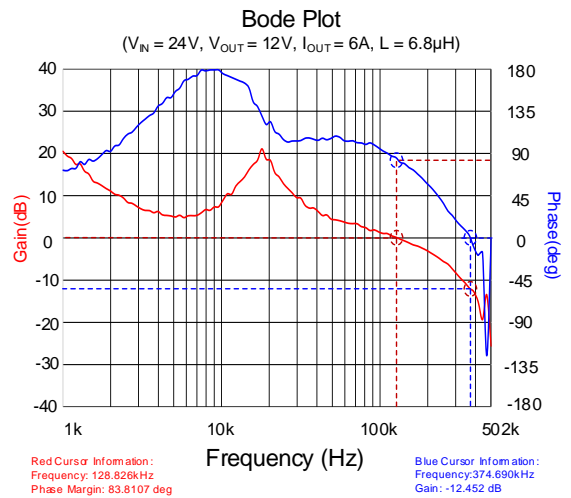
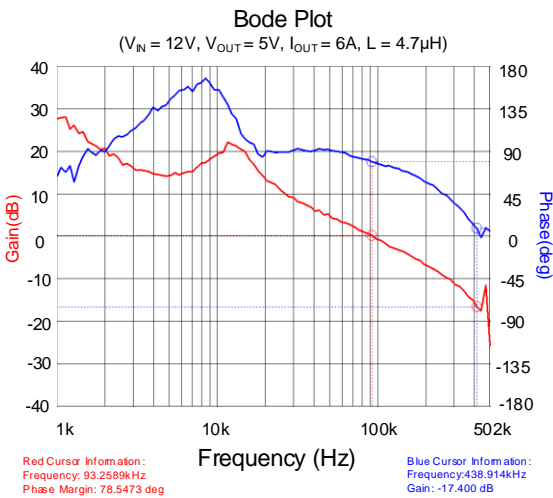
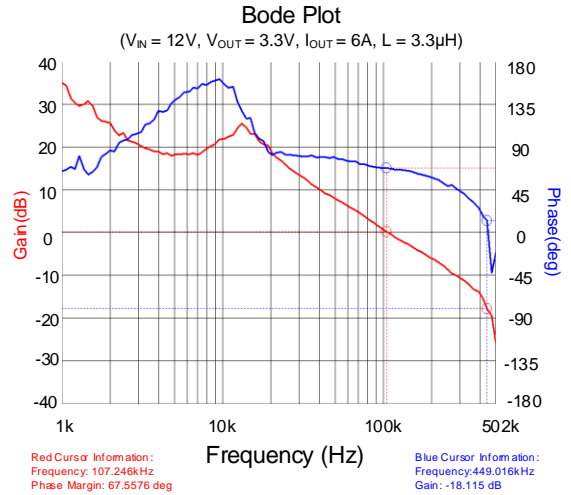
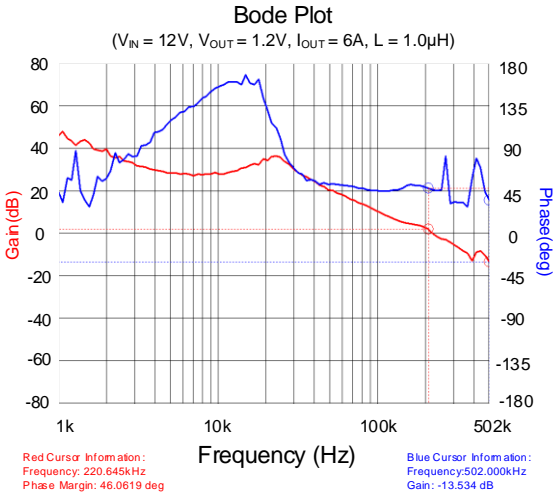


Time (2μs/div)

Output Ripple
($V_{IN} = 12V$, $V_{OUT} = 5V$, $I_{OUT} = 6A$)



Time (2μs/div)



Detailed Description

Constant On-Time Architecture

Fundamental to any constant on-time (COT) architecture is the one-shot circuit or on-time generator, which determines how long to turn on the top MOSFET. Each on-time (t_{ON}) is a “fixed” voltage ratio,

$$t_{ON} = \left(\frac{V_{OUT}}{V_{IN}} \right) \times \left(\frac{1}{f_{SW}} \right)$$

For example, considering that a hypothetical converter targets 5V output from a 28V input at 500kHz, the target on-time is

$$\frac{5V}{28V} \times \frac{1}{500kHz} = 357.14ns$$

Each t_{ON} pulse is triggered by the feedback comparator when the output voltage as measured at FB node drops below the regulated value. After one t_{ON} period, a minimum off-time ($t_{OFF,MIN}$) is imposed before any further switching is initiated, even if the output voltage is lower than the regulated value. This approach avoids making any switching decisions during the noisy periods just after switching events and while the switching node (LX) is rapidly rising or falling.

In a COT architecture, there is no fixed clock, so the top MOSFET can turn on almost immediately after a load transient and subsequent switching pulses can be quickly initiated, ramping the inductor current up to meet load requirements with minimal delays.

Minimum Duty Cycle and Maximum Duty Cycle

In the COT architecture, there is no limitation for operating the part at low duty cycle, since in this case, when the on-time is close to the minimum on-time, the switching frequency is reduced as needed to always ensure a proper operation.

In order to convert output voltage under low input voltage operation, the t_{ON} can be stretched to extend the duty cycle as much as it needs. When the device detects feedback voltage is lower than the reference voltage under normal on-time operation and the duty cycle > 27%, the t_{ON} will be stretched. The maximum on-time can be limited when the peak current limit actions or high side power switch drive voltage (BS-LX voltage) is below its UVLO voltage (~1.8V). The on-time stretch function is disabled when the duty cycle < 17% or the feedback voltage is less than the under voltage protection (UVP) threshold. The device can support 98% open loop duty cycle if not consider duty loss caused by MOSFET $R_{DS(ON)}$ and inductor DCR. The device can also support 100% duty cycle operation if BS-LX voltage adds external > 2.2V voltage source.

Instant-PWM Operation

Silergy’s COT ripple-based control strategy adds several proprietary improvements to the traditional COT architecture. Whereas most legacy based on COT implementations require a dedicated connection to the output voltage terminal to calculate the t_{ON} duration, instant-PWM control method derives this signal internally. Another improvement optimizes operation with low ESR ceramic output capacitors. In many applications it is desirable to utilize very low ESR ceramic output capacitors, but legacy COT converters may become unstable in these cases because the beneficial ramp signal that results from the inductor current flowing into the output capacitor may become too small to maintain stable operation. For this reason, instant-PWM synthesizes a virtual replica of this signal internally. This internal virtual ramp and the feedback voltage are combined and compared to the reference voltage. When the sum is lower than the reference voltage, the t_{ON} pulse is triggered as long as the minimum off-time has been satisfied and the inductor current as measured in the bottom MOSFET is lower than its current limit threshold. As the t_{ON} pulse is triggered, the bottom MOSFET turns off and the top MOSFET turns on. The inductor current ramps up linearly during the t_{ON} period. At the end of the t_{ON} period, the top MOSFET turns off, the bottom MOSFET turns on, and the inductor current ramps down linearly. This action also initiates the minimum off-time timer to ensure sufficient time for stabilizing any transient conditions and settling the feedback comparator before the next cycle is initiated. This minimum off-time is relatively short so that during fast speed load transients, t_{ON} can be retriggered with minimal delay, allowing the inductor current to ramp quickly and provide sufficient energy to the load side.

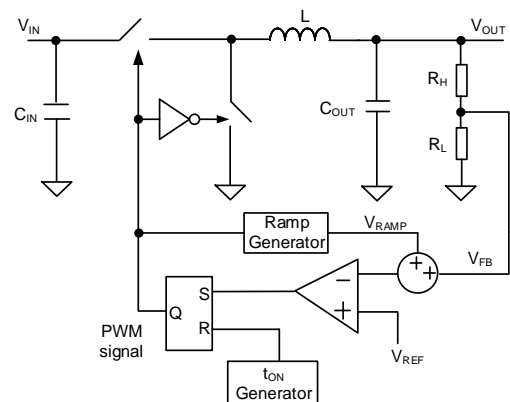


Figure4. Silergy’s COT Ripple-based Control Strategy

In order to avoid shoot-through, a dead time (t_{DEAD}) is generated internally between turning the top MOSFET off and the bottom MOSFET on, as well as between turning the bottom MOSFET off and the top MOSFET on.

Light Load Operation

The device uses pulse-frequency modulation (PFM) operation mode under light load condition for high efficiency. Under light load conditions, typically when the load satisfies the following equation,

$$I_{OUT_CTL} = \frac{\Delta I_L}{2} = \frac{V_{OUT} \times (1 - D)}{2 \times f_{SW} \times L} \quad (1)$$

The current through the bottom MOSFET will ramp to near zero before the next t_{ON} time. When this occurs, the bottom MOSFET turns off, preventing recirculation current that can seriously reduce efficiency under these light load conditions. As load current is further reduced, the combined feedback and ramp signals remain much higher than the reference voltage, the instant-PWM control loop will not trigger another t_{ON} until needed, and the apparent operating switching frequency will correspondingly drop, improving efficiency. The switching frequency can be lower than audible frequency area under deep light load or null load conditions. Continuous conduction mode (CCM) resumes smoothly as soon as the load current increases sufficiently for the inductor current to remain above zero at the time of the next t_{ON} cycle. The buck converter enters CCM once the load current exceeds the threshold shown in (1). Above the threshold, the switching frequency stays fairly constant over the output current range.

While in PFM mode, the output of the device doesn't require over voltage protection because the device stops switching as soon as the voltage at the FB node increases above V_{REF} , preventing the output voltage from increasing further.

Input Under Voltage Lockout (UVLO)

To prevent operation before the internal circuitry is ready and to ensure that the top and bottom MOSFETs can be properly driven, the device incorporates an input undervoltage lockout protection.

The device remains in a low current state and LX node switching actions are inhibited until V_{IN} exceeds the UVLO rising threshold. At that time, if EN is high, the device is enabled and soft-start ramp is initiated. If V_{IN} falls below $V_{IN,UVLO}$ less than the input UVLO hysteresis, LX node switching actions will again be suppressed.

Precise EN Threshold

The EN pin uses precise rising and falling thresholds to provide programmable ON/OFF control. The device will be turned on when the EN pin voltage exceeds the rising threshold. The device will be turned off while the EN pin voltage falls below the falling threshold. Increasing the UVLO startup voltage threshold is possible using an external resistor divider as shown below:

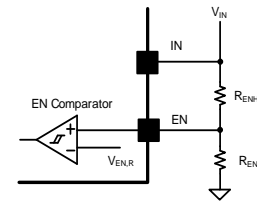


Figure5. Enable Control

It is not recommended to connect EN pin to the V_{IN} directly. A resistor with a value between 1k Ω and 1M Ω is recommended if the EN pin is pulled high to the V_{IN} .

Soft-Start and Startup with Pre-Biased Output

The device incorporates an internal soft-start circuit to ramp the output to the desired voltage whenever the device is enabled. Internally, the soft-start circuit clamps the output at a low voltage and then allows the output to rise to the desired voltage over approximately 1ms, which avoids high current flow and transients during startup.

The device supports startup with pre-biased output. If the output is pre-biased to a certain voltage before startup, the buck converter disables the switching of both the top MOSFET and the bottom MOSFET until the internal soft-start voltage V_{SS} exceeds the sensed output voltage at the FB node. The first pulse on-time is internally calculated based the input voltage and pre-biased output voltage.

PG Power Good Indicator

PG is an open drain output controlled by a window comparator connected to the feedback signal. If the voltage is higher than $V_{PG,R}$ and less than $V_{PG,OVP}$ for at least the power good delay time (low to high), PG will be set to high-impedance state.

PG should be connected to V_{IN} or another voltage source through a resistor (e.g., 100k Ω). After V_{IN} rises until the internal initial power is ready, the PG internal MOSFET is turned on so that PG is actively driven low before output voltage is ready. After the feedback voltage V_{FB} reaches $V_{PG,R}$ or drops from $V_{PG,RCY}$, PG is set to high-impedance state after a delay time of 200 μ s (typ.). When V_{FB} drops to $V_{PG,F}$, or rises above $V_{PG,OVP}$, PG is driven low after a delay time of 40 μ s (typ.).

Output Auto-Discharge Function

The device discharges the output voltage when the buck converter shuts down due to low V_{IN} or EN, or caused by a protection function being triggered, so that the output voltage can be discharged in a minimal time, even if the buck output load current is zero. The discharge MOSFET in parallel with the bottom MOSFET turns on after the bottom MOSFET turns off when the shutdown logic is enabled. The output discharge current is typically 80mA for $V_{OUT} = 5V$. The discharge MOSFET is not active outside of these shutdown conditions.

External Bootstrap Capacitor

This device integrates a floating power supply for the gate driver of the top MOSFET. Proper operation requires a 0.1μF low ESR ceramic capacitor to be connected between BS and LX. This bootstrap capacitor provides the gate driver supply voltage for the N-channel top MOSFET.

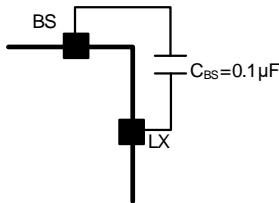


Figure6. Bootstrap Capacitor Connection

VCC Linear Regulator

The device integrates a high performance, low drop-out linear regulator 3.3V VCC, which can power the internal gate drivers, PWM logic, analog circuitry and other blocks. Connect a 2.2μF low ESR ceramic capacitor from VCC to GND.

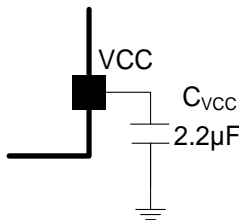


Figure7. VCC Capacitor Connection

Fault Protection Modes

Output Current Limit

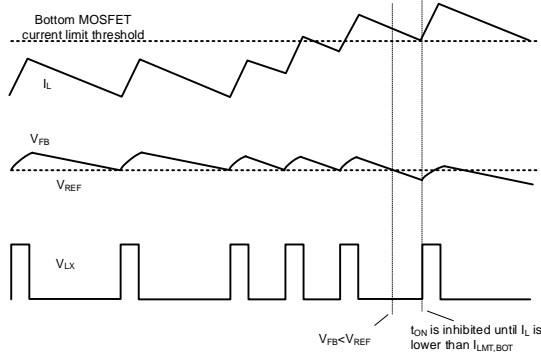


Figure8. Bottom Current Limit Protection

The buck converter features cycle-by-cycle “valley” current limit (bottom MOSFET current limit). The Inductor current is monitored in the bottom MOSFET when it turns on and as the inductor current ramps down. If the monitored current is higher than current limit threshold, t_{ON} is inhibited until the current returns back to below the threshold.

When the valley current limit occurs, the output current limit value is

$$I_{LMT,OUT} = I_{LMT,BOT} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

The buck converter also features cycle-by-cycle peak current limit (top MOSFET current limit). During the t_{ON} time, the top MOSFET current is monitored. If it exceeds the current limit threshold, the MOSFET will be turned off, and the bottom MOSFET will be turned on. t_{ON} can be not inhibited when the bottom MOSFET current is lower than the bottom MOSFET current limit threshold.

Output Under Voltage Protection (UVP)

If $V_{OUT} < \sim 50\%$ of the set point for approximately 40μs occurring when the output short circuit or the load current is much heavier than the maximum current capacity, the output under voltage protection (UVP) will be triggered, and the device will enter into hic-cup protection mode. The hic-cup on time is 2ms, and the hic-cup off time is 6ms. If the output fault conditions are removed, the device will go back to normal operation in the nearest hic-cup on time.

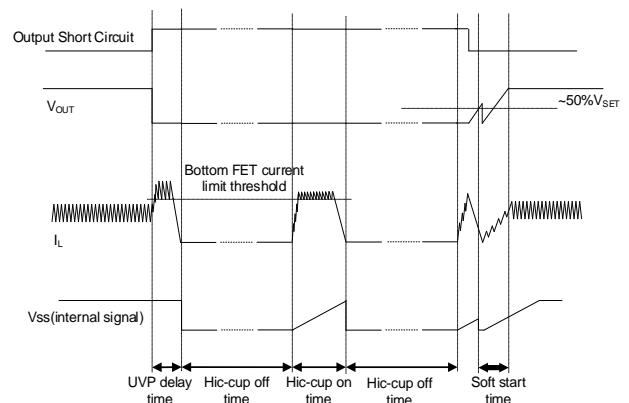


Figure9. Output Under Voltage Protection

To avoid output overshoot, the internal soft-start circuit voltage V_{SS} should be pull low for a while when V_{FB} exceeds UVP threshold if the output fault conditions are removed during hic-cup on time, then the V_{SS} rises smoothly to ramp the output to the desired voltage during a new soft-start cycle.

Over Temperature Protection (OTP)

The device includes over temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 150°C. When the junction temperature is reduced by approximately 15°C, the device will resume normal operation after a complete soft-

start cycle. For continuous operation, provide adequate thermal dissipation so that the junction temperature does not exceed the OTP threshold.

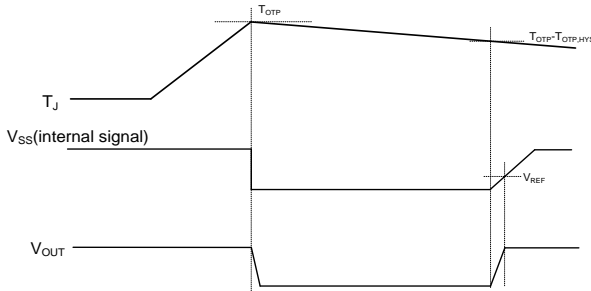


Figure 10. Over Temperature Protection

Design Procedure

The following paragraphs provide information on the selection of the external components needed to meet the targeted application specifications.

Feedback Resistor Divider R_H and R_L

Choose R_H and R_L to program the proper output voltage. A value between 1kΩ and 1MΩ is recommended for both resistors to minimize power consumption under light loads. As an example, if V_{OUT} = 5V and R_H selected value is 100kΩ, R_L can be calculated as follows:

$$R_L = \frac{0.6}{V_{OUT} - 0.6V} \times R_H$$

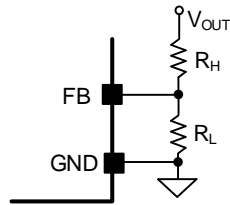


Figure 11. Feedback Resistor Divider

With a calculated value of 13.7kΩ for R_L, a standard 1% 13.7kΩ resistor is selected.

Input Capacitor C_{IN}

For the best performance, select a typical X5R or better grade ceramic capacitor with a 50V rating, and at least 10μF capacitance. The capacitor should be placed as close as possible to the device, while also minimizing the loop area formed by C_{IN} and the IN/GND pins.

When selecting an input capacitor, ensure that its voltage rating is at least 20% greater than the maximum voltage of the input supply. X5R or X7R dielectric types are the most often selected due to their small size, low cost, surge current capability, and high RMS current rating over a wide temperature and voltage range.

In situations where the input rail is supplied through long wires, it is recommended to add some bulk capacitance

like electrolytic, tantalum or polymer type capacitors to reduce the overshoot and ringing caused by the added parasitic inductance.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN_RMS_MAX} = \frac{I_{OUT}}{2}$$

For simplicity, use an input capacitor with an RMS current rating greater than 50% of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN_RIPPLE_CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1 - D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN_RIPPLE_CAP_MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. A single 10μF X5R capacitor is sufficient for most applications.

Output Inductor L

Consider the following when choosing this inductor:

- 1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT} / V_{IN_MAX})}{f_{SW} \times I_{OUT_MAX} \times 0.4}$$

where f_{sw} is the switching frequency and I_{OUT,MAX} is the maximum load current.

The SY82806 has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

- 2) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

- 3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Use an inductor with DCR less than 50mΩ to achieve good overall efficiency.

Output Capacitor C_{OUT}

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting C_{OUT}. For the best performance, use a X5R or better grade ceramic capacitor with a 16V rating, and capacitance of at least 10μF.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed.

The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, consider both.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

The measured capacitive ripple might be higher than the theoretical value because the effective capacitance for ceramic capacitors decreases with the voltage across its terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

Load Transient Considerations

The device integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding an RC network R_{FF} and C_{FF} in parallel with R_H may further speed up the load transient response. R_{FF} = 1kΩ and C_{FF} = 220pF is recommended for most applications. Note that when the output LC parameter is large, the feedforward capacitor can be increased for provide sufficient ripple to FB for small output ripple and good transient behavior.

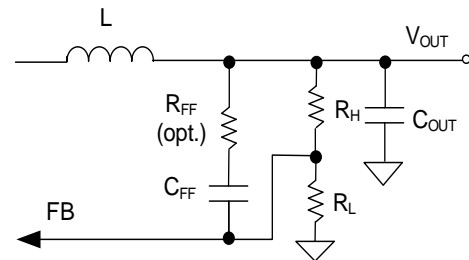


Figure 12. Feedforward Network

Note: For C_{OUT} > 500μF, use feedforward values of R_{FF} = 1kΩ and C_{FF} = 2.2nF to provide sufficient ripple to FB node for low output ripple and good transient behavior.

Thermal Design Considerations

Maximum power dissipation depends on the thermal resistance of the device package, the PCB layout, the surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation may be calculated by:

$$P_{D,MAX} = \frac{T_{J,MAX} - T_A}{\theta_{JA}}$$

Where, T_{J,MAX} is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

To comply with the recommended operating conditions, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For the QFN2x3-14 package the thermal resistance θ_{JA} is 22°C/W when measured on a standard Silergy 8.5cmx8.5cm size four-layer thermal test board. These standard thermal test layouts have a very large area with long 2-oz copper traces connected to each device pin and very large, unbroken 1-oz internal power and ground planes.

Meeting the performance of the standard thermal test board in a typical tiny evaluation board area requires wide copper traces well-connected to the device backside pads leading to exposed copper areas on the component side of the board as well as good thermal via from the exposed pad connecting to a wide middle-layer ground plane and, perhaps, to an exposed copper area on the board's solder side.

The maximum power dissipation at T_A = 25°C may be calculated by the following formula:

$$P_{D,MAX} = \frac{125^\circ\text{C} - 25^\circ\text{C}}{22^\circ\text{C}/\text{W}} = 4.55\text{W}$$

The maximum power dissipation depends on operating ambient temperature for fixed T_{J,MAX} and thermal resistance θ_{JA}. Use the derating curve in figure below to

calculate the effect of rising ambient temperature on the maximum power dissipation.

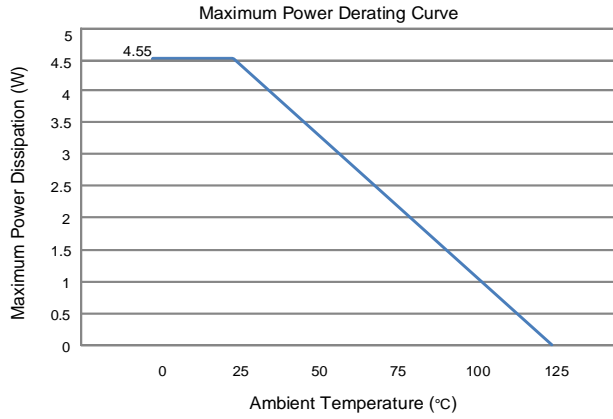
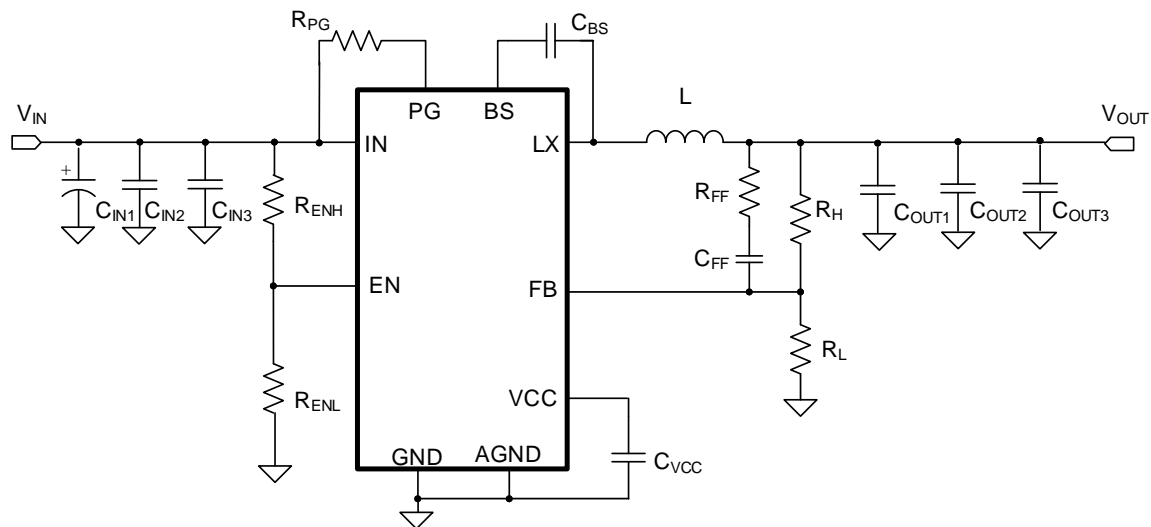


Figure 13. Maximum Power Derating

Application Schematic (V_{OUT}=5V)



BOM List

Reference Designator	Description	Part Number	Manufacturer
C _{IN1}	47μF/50V, Electrolytic Capacitor		
C _{IN2}	10μF/50V/X5R, 1206	GRM31CR61H106KA12L	mμRata
C _{IN3} , C _{BS}	0.1μF/50V/X5R, 0603	GRM188R61H104KA93D	mμRata
C _{OUT1} , C _{OUT2} , C _{OUT3}	22μF/16V/X5R, 1206	GRM31CR61C226ME15L	mμRata
C _{VCC}	2.2μF/16V/X5R, 0603	GRM188R61C225KE15D	mμRata
C _{FF}	220pF/50V/C0G, 0603	GRM1885C1H221JA01D	mμRata
L	4.7μH/8.5A, inductor	PCMB104T-4R7MS	CYNTEC
R _{ENH}	10kΩ, 1%, 0603		
R _{ENL}	1MΩ, 1%, 0603		
R _H , R _{PG}	100kΩ, 1%, 0603		
R _L	13.7kΩ, 1%, 0603		
R _{FF}	1kΩ, 1%, 0603		

Recommend Components Values for Typical Applications

V _{OUT} (V)	R _H (kΩ)	R _L (kΩ)	C _{FF} (pF)	L/Part Number
1.2	100	100	220	1.0μH/PCMB104T-1R0MT
3.3	100	22.1	220	3.3μH/PCMB104T-3R3MS
5	100	13.7	220	4.7μH/PCMB104T-4R7MS
12	100	5.26	220	6.8μH/PCMB104T-6R8MS



Recommend Components Values

V _{OUT} (V)	L(μH)	C _{OUT} (Range)(μF)	R _{FF} (kΩ)	C _{FF} (pF)
1.2	0.68	66-500	1	220
1.2	1.0	66-500	1	220
1.2	1.5	66-500	1	220
3.3	2.2	66-500	1	220
3.3	3.3	66-500	1	220
3.3	4.7	66-100	1	220
3.3	4.7	100-500	1	470
5	3.3	66-500	1	220
5	4.7	66-120	1	220
5	4.7	120-500	1	470
5	5.6	66-500	1	470
12	4.7	66-120	1	220
12	4.7	120-500	1	470
12	5.6	66-120	1	220
12	5.6	120-500	1	680
12	6.8	66-220	1	470
12	6.8	220-500	1	1000

Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation.

Input Capacitors: Place the input capacitor close to IN and GND pins, minimizing the loop formed by these connections. The capacitor should be connected to the IN and GND using a wide copper pour. A 0.1 μ F input ceramic capacitor is recommended to reduce the high-frequency noise.

Output Capacitors: Ensure that the C_{OUT} negative sides are connected to GND using wide copper traces instead of vias, in order to achieve better accuracy and stability of output voltage.

VCC Capacitor: Place the VCC capacitor close to VCC pin using a short, direct copper trace to the nearest AGND pin. Make one Kelvin connection between AGND and GND at the C_{VCC} negative side by multiple vias.

Feedback Network and Output Line: Place the feedback components (R_H, R_L, R_{FF} and C_{FF}) as close to FB pin as possible. Avoid routing the feedback line near LX, BS or other high frequency signal as it is noise sensitive. Use a Kelvin connection for the feedback sampling point at C_{OUT} rather than the inductor output terminal.

LX Connection: Keep LX area small to prevent excessive EMI, while using a wide copper trace to minimize parasitic resistance and inductance.

BS Capacitor: Place the BS capacitor on the same layer as the device, keep the BS voltage path (BS, LX and C_{BS}) as short as possible.

EN Signal: It is not recommended to connect EN signal to V_{IN} or another voltage source directly. A resistor in a range of 1k Ω to 1M Ω should be used if it is pulled high.

GND Vias: Place adequate number of vias on the GND layer around the device for better thermal performance. Place several GND vias near GND pin for heat dissipation.

PCB Board: A four-layer layout with 2-oz copper is strongly recommended to achieve better thermal performance. The top layer and bottom layer should place power IN and GND copper area as wide as possible. Middle1 layer should be used as a GND layer for conducting heat and shielding the middle2 layer signal lines from top layer crosstalk. Place signal lines on middle2 layer instead of the other layers, so that the other layers' GND plane is not cut by signal lines.

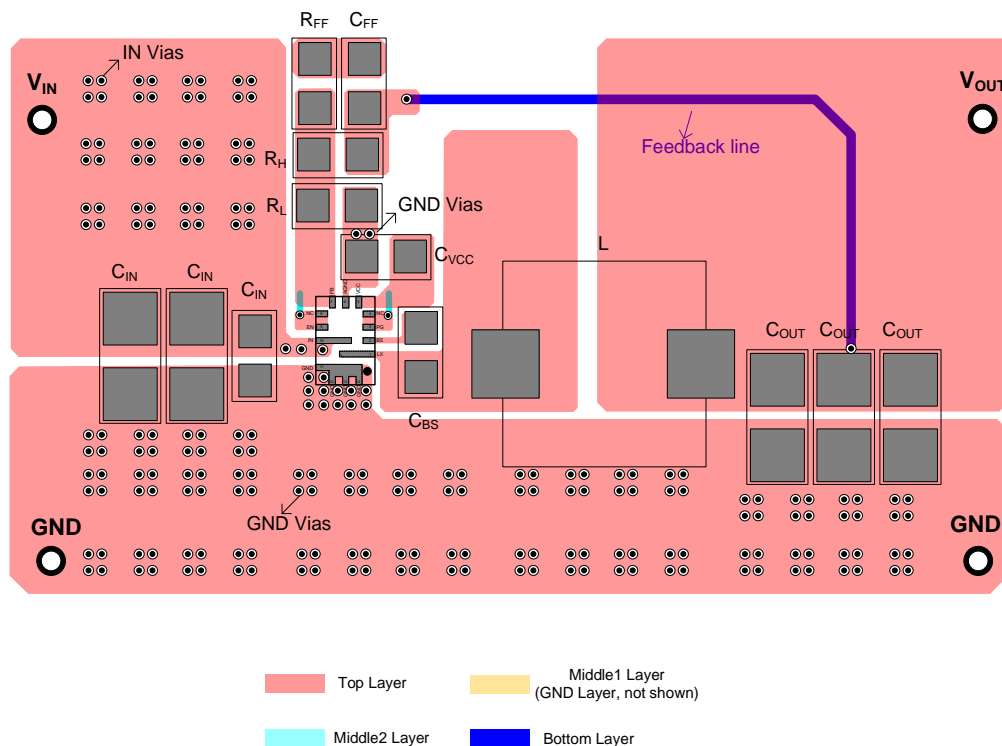
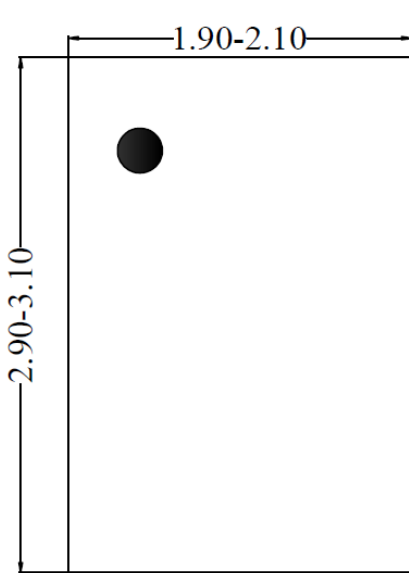
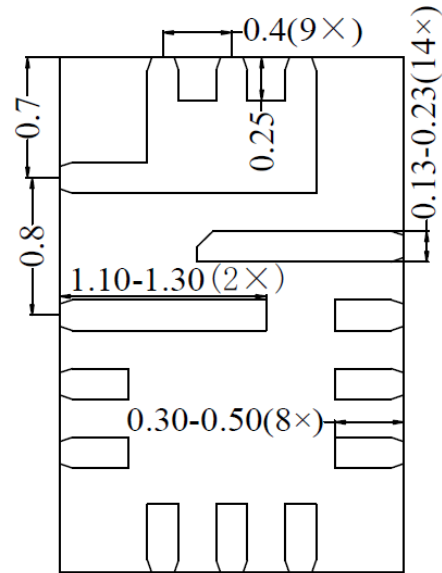


Figure 14. PCB Layout Suggestion

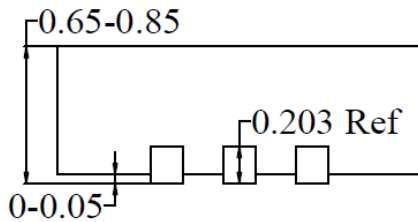
QFN2x3-14 Package Outline Drawing



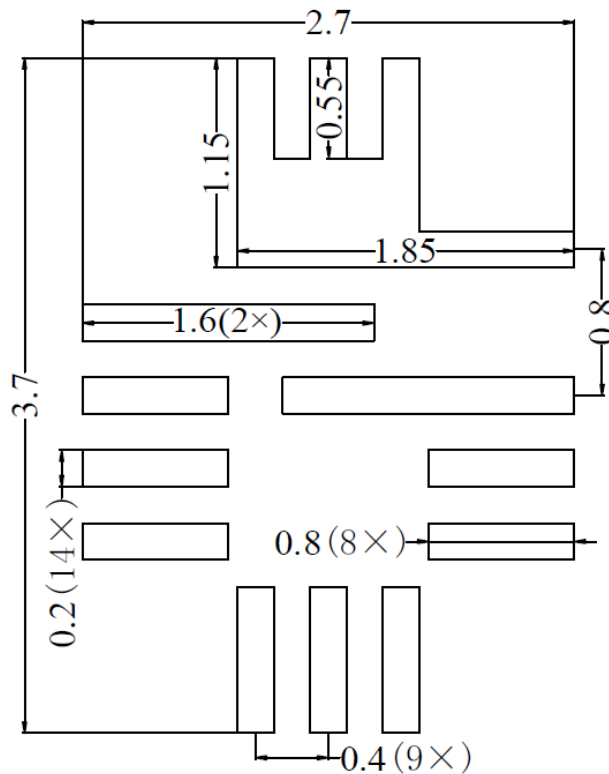
Top View



Bottom view



Front View



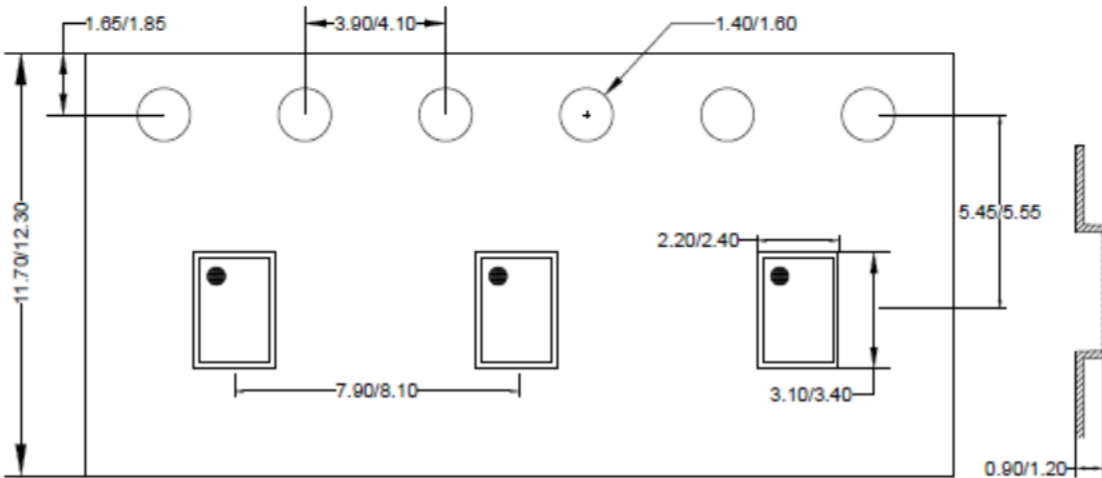
**Recommended PCB layout
(Reference only)**

Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

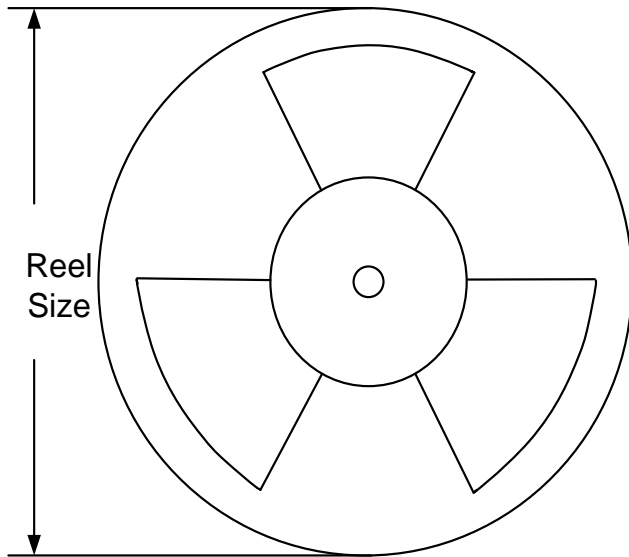
1. Taping Orientation

QFN2x3-14



Feeding Direction →

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel
						(pcs)
QFN2x3-14	12	8	13	400	400	5000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change	Pages changed
Jun 26, 2025	1.0	Initial Release	-

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