

Product Specification

XBLW AOD409

P-Channel Enhancement Mode MOSFET

WEB | www.xinboleic.com



Description

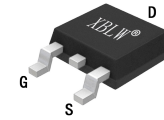
The AOD409 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and Doperation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

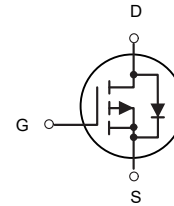
- $V_{DS} = -60V$ $I_D = -50A$
- $R_{DS(ON)} < 24\ m\Omega$ @ $V_{GS} = 10V$

Application

- Battery protection
- Load switch
- Uninterruptible power supply



TO-252-2L



P-Channel MOSFET

Package Marking and Ordering Information

| Product Model | Package Type | Marking | Packing | Packing Qty |
|---------------|--------------|---------|---------|--------------|
| XBLW AOD409 | TO-252-2L | AOD409 | Tape | 2500Pcs/Reel |
| | | | | |
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Absolute Maximum Ratings (TC=25°C unless otherwise noted)

| Symbol | Parameter | Rating | Units |
|---------------------------|--|------------|--------------|
| V_{DS} | Drain-Source Voltage | -60 | V |
| V_{GS} | Gate-Source Voltage | ± 20 | V |
| $I_D @ T_C = 25^\circ C$ | Continuous Drain Current, $V_{GS} @ 10V^1$ | -50 | A |
| $I_D @ T_C = 100^\circ C$ | Continuous Drain Current, $V_{GS} @ 10V^1$ | -27 | A |
| I_{DM} | Pulsed Drain Current ² | -70 | A |
| $P_D @ T_C = 25^\circ C$ | Total Power Dissipation ⁴ | 52.1 | W |
| TSTG | Storage Temperature Range | -55 to 150 | $^\circ C$ |
| T_J | Operating Junction Temperature Range | -55 to 150 | $^\circ C$ |
| $R_{\theta JA}$ | Thermal Resistance Junction-ambient ¹ | 62 | $^\circ C/W$ |
| $R_{\theta JC}$ | Thermal Resistance Junction-Case ¹ | 2.4 | $^\circ C/W$ |

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-------------------------------------|--|--|------|--------|------|-------|
| BV _{DSS} | Drain-Source Breakdown Voltage | V _{GS} =0V, I _D =-250uA | -60 | --- | --- | V |
| ΔBV _{DSS} /ΔT _J | BV _{DSS} Temperature Coefficient | Reference to 25°C, I _D =-1mA | --- | -0.035 | --- | V/°C |
| R _{DS(on)} | Static Drain-Source On-Resistance ² | V _{GS} =-10V, I _D =-18A | --- | 20 | 24 | mΩ |
| | | V _{GS} =-4.5V, I _D =-12A | --- | 25 | 30 | |
| V _{GS(th)} | Gate Threshold Voltage | V _{GS} =V _{DS} , I _D =-250uA | -1.0 | --- | -2.5 | V |
| ΔV _{GS(th)} | V _{GS(th)} Temperature Coefficient | | --- | 4.28 | --- | mV/°C |
| I _{DSS} | Drain-Source Leakage Current | V _{DS} =-48V, V _{GS} =0V, T _J =25°C | --- | --- | 1 | uA |
| | | V _{DS} =-48V, V _{GS} =0V, T _J =55°C | --- | --- | 5 | |
| I _{GSS} | Gate-Source Leakage Current | V _{GS} =±20V, V _{DS} =0V | --- | --- | ±100 | nA |
| g _{fs} | Forward Transconductance | V _{DS} =-10V, I _D =-18A | --- | 23 | --- | S |
| R _g | Gate Resistance | V _{DS} =0V, V _{GS} =0V, f=1MHz | --- | 7 | --- | Ω |
| Q _g | Total Gate Charge (-4.5V) | V _{DS} =-20V, V _{GS} =-4.5V, I _D =-12A | --- | 25 | --- | nC |
| Q _{gs} | Gate-Source Charge | | --- | 6.7 | --- | |
| Q _{gd} | Gate-Drain Charge | | --- | 5.5 | --- | |
| T _{d(on)} | Turn-On Delay Time | V _{DD} =-15V, V _{GS} =-10V, R _G =3.3Ω, I _D =-1A | --- | 38 | --- | ns |
| T _r | Rise Time | | --- | 23.6 | --- | |
| T _{d(off)} | Turn-Off Delay Time | | --- | 100 | --- | |
| T _f | Fall Time | | --- | 6.8 | --- | |
| C _{iss} | Input Capacitance | V _{DS} =-15V, V _{GS} =0V, f=1MHz | --- | 3635 | --- | pF |
| C _{oss} | Output Capacitance | | --- | 224 | --- | |
| C _{rss} | Reverse Transfer Capacitance | | --- | 141 | --- | |

Diode Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-----------------|--|--|------|------|------|------|
| I _S | Continuous Source Current ^{1,5} | V _G =V _D =0V, Force Current | --- | --- | -45 | A |
| I _{SM} | Pulsed Source Current ^{2,5} | | --- | --- | -70 | A |
| V _{SD} | Diode Forward Voltage ² | V _{GS} =0V, I _S =-1A, T _J =25°C | --- | --- | -1 | V |

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- 3.The EAS data shows Max. rating. The test condition is V_{DD}=-25V, V_{GS}=-10V, L=0.1mH, I_{AS}=-47.6A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Typical Characteristics

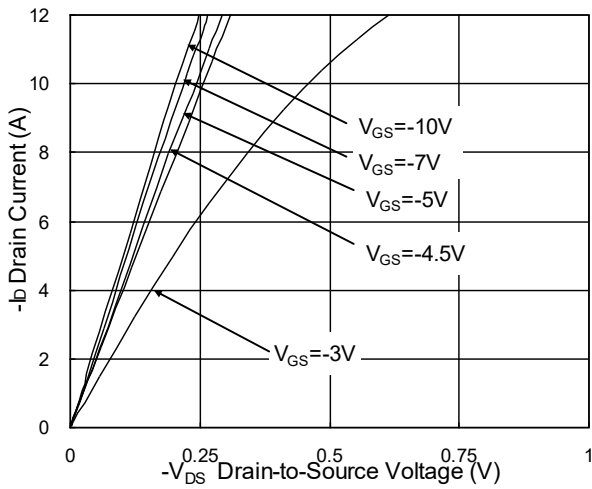


Fig.1 Typical Output Characteristics

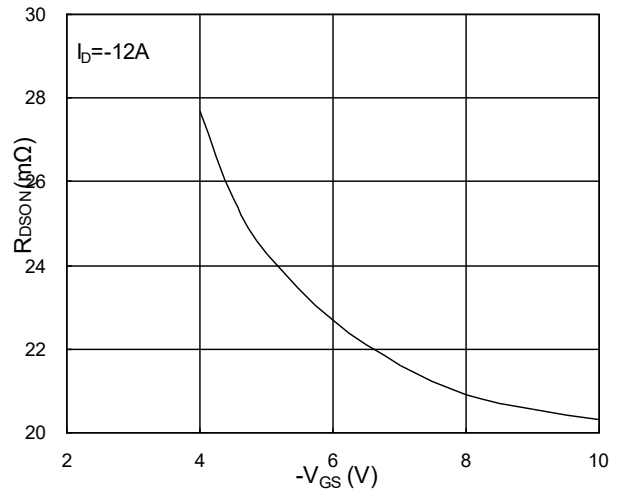


Fig.2 On-Resistance v.s Gate-Source

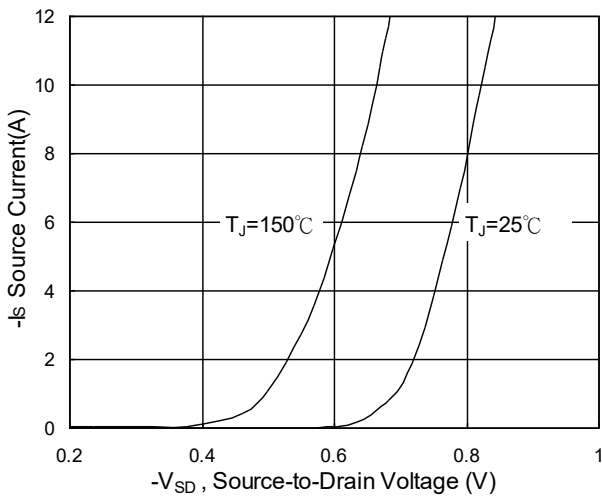


Fig.3 Forward Characteristics Of Reverse

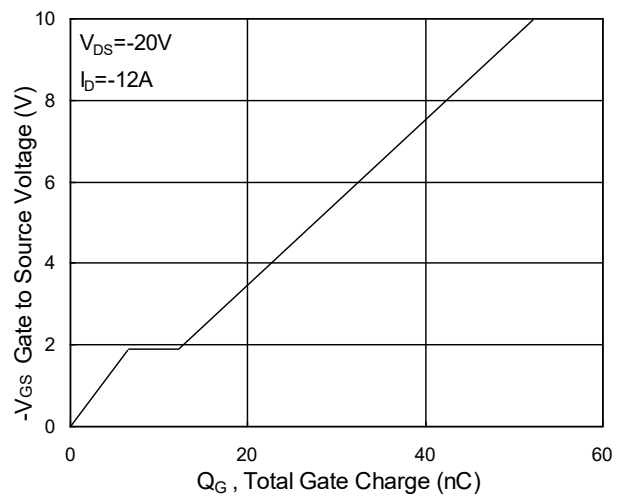


Fig.4 Gate-Charge Characteristics

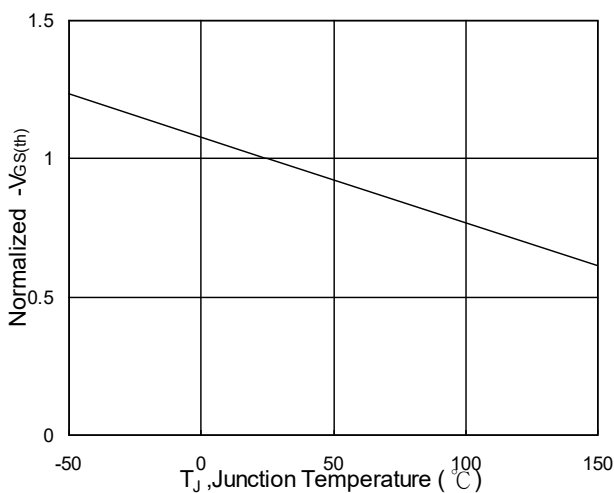


Fig.5 Normalized V_{GS(th)} v.s T_J

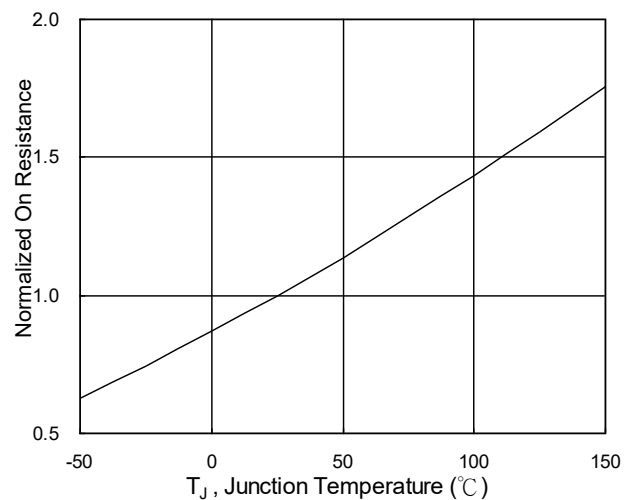


Fig.6 Normalized R_{DS(on)} v.s T_J

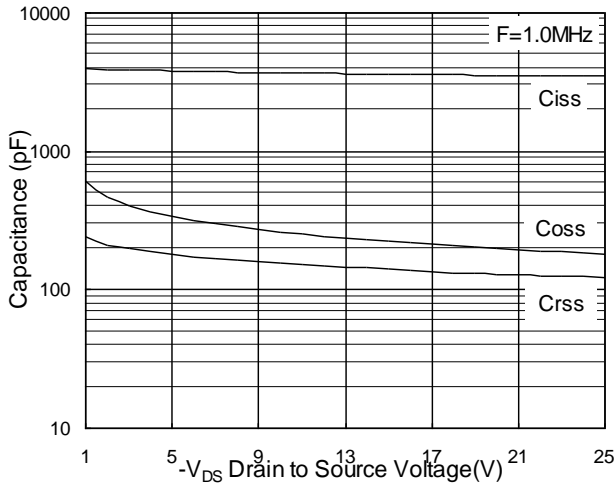


Fig.7 Capacitance

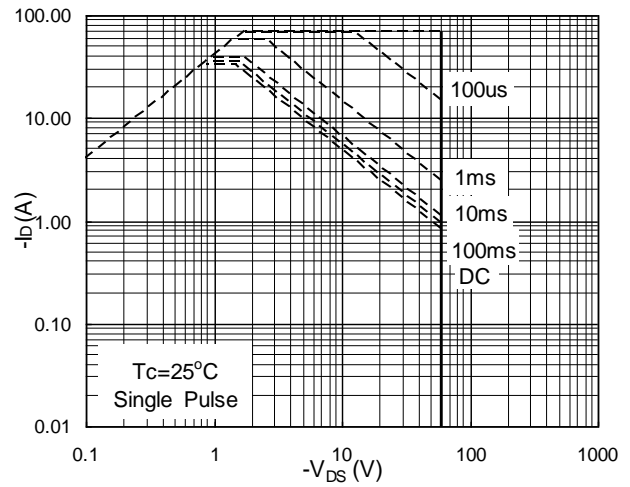


Fig.8 Safe Operating Area

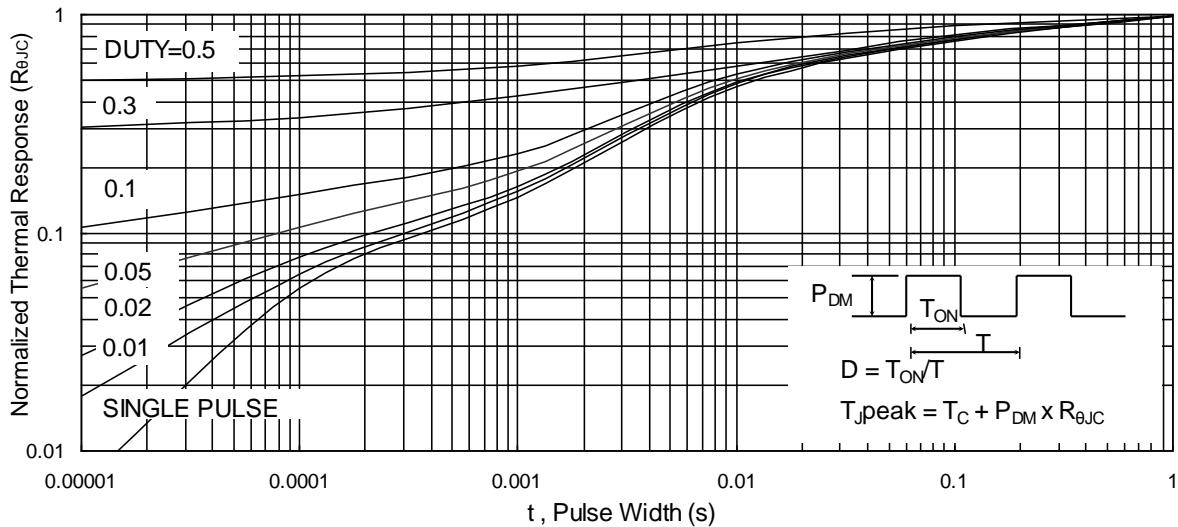


Fig.9 Normalized Maximum Transient Thermal Impedance

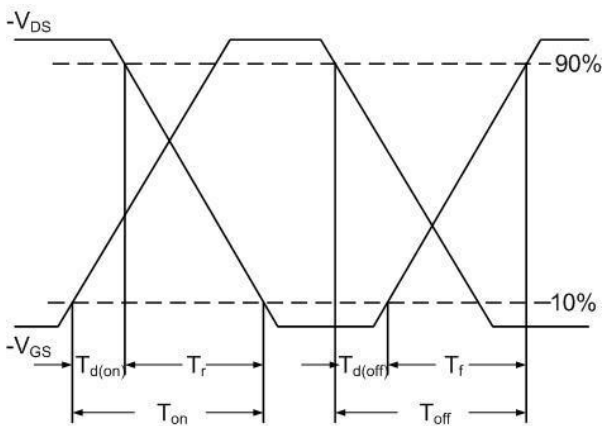


Fig.10 Switching Time Waveform

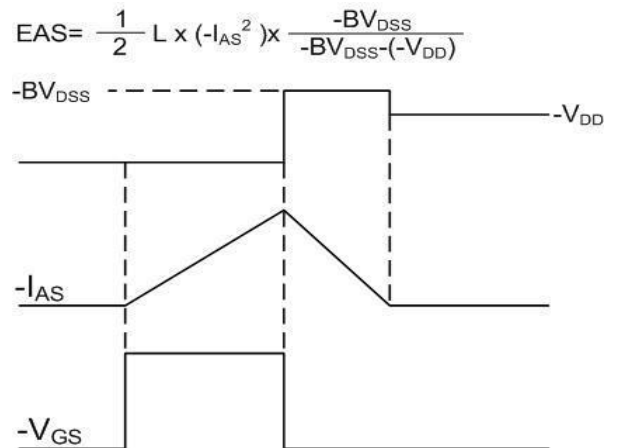


Fig.11 Unclamped Inductive Waveform

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