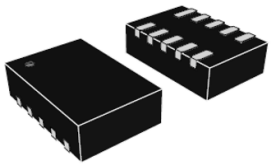
STEF512SRX

Datasheet

Dual electronic fuse for 5 V and 12 V rails with reverse current blocking



DFN10 (2 x 3 mm)

Maturity status link
STEF512SRX

Features

- 5 V and 12 V channels into one chip
- 25 V absolute maximum input voltage
- Precise output overvoltage clamp
- Fixed overcurrent protection for both channels
- Reverse current protection on 5 V channel
- Thermal protection
- Available in auto-retry version
- Input undervoltage lockout
- Adjustable output voltage slew rate
- Integrated 45 mΩ power MOSFETs
- SAS disable pin
- Current monitor pin selection
- Current monitor output in a single pin for both rails
- DFN10 (2 x 3 mm) package

Applications

- HD and SSD
- Hard disk arrays and NAS
- Hot plug protections

Description

The STEF512SRX is an integrated dual electronic fuse, designed to protect circuitry on the output from overcurrent and overvoltage events, in those applications requiring hot swap operation and inrush current control.

The device embeds two electronic fuses, one for the 5 V rail and one for the 12 V rail. Thanks to the very low on-resistance of the integrated power MOSFETs, the voltage drop from the main supply to the load is very low during normal operation.

The 5 V channel provides a reverse blocking feature, preventing current flow to the input in case of brown-out or shutdown.

The start-up time is internally controlled by a dedicated slew rate circuit. In this way the inrush current at startup can be kept under control.

The maximum load current is precisely limited, by utilizing a sense FET topology, to factory-defined values.

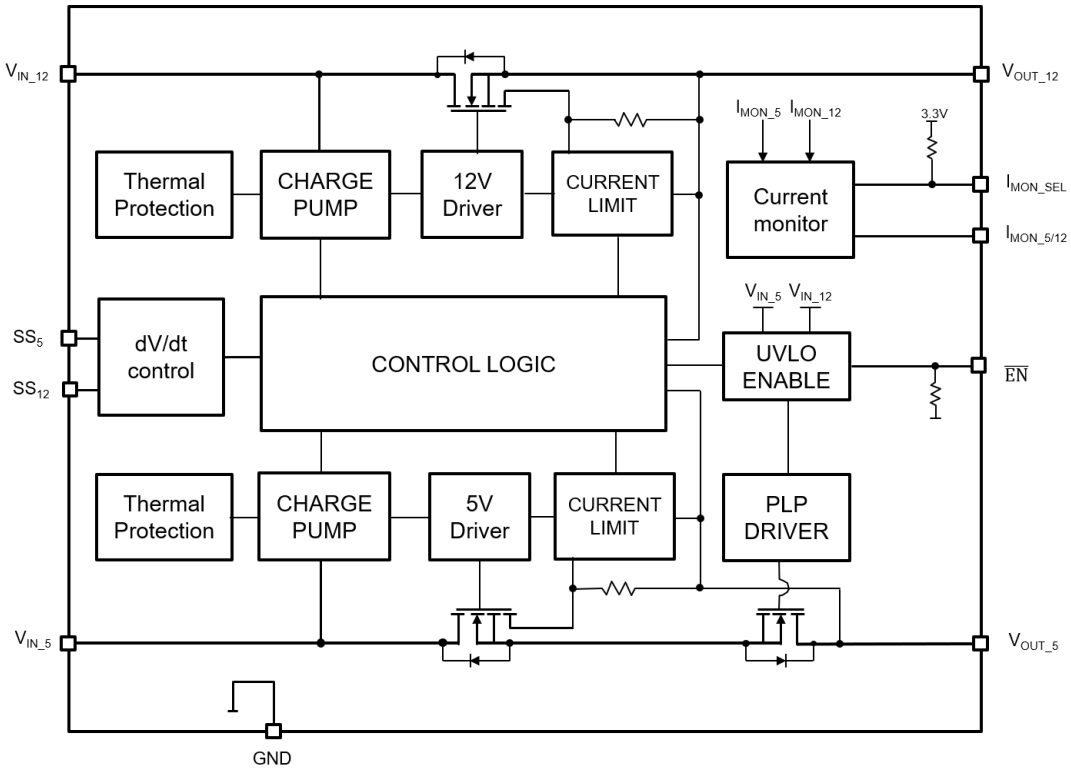
The device also provides precise overvoltage clamp for each channel, preventing the load being damaged from power supply failures, and undervoltage lockout (UVLO), assuring that the input voltage is above the minimum operating threshold, before the power is turned on.

When an overload condition occurs, the STEF512SRX limits the output current to the predefined safe value. If the anomalous overload condition persists, the device goes into thermal shutdown, the internal switch is opened and the load is disconnected from the power supply.

Load current on each channel can be accurately monitored by reading the signal on the $I_{MON\_5/12}$ pin.

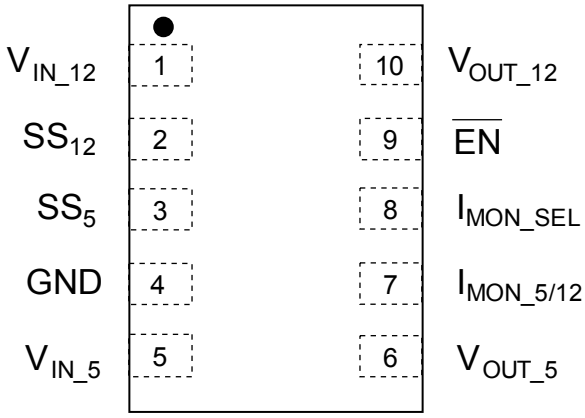
1 Diagram

Figure 1. **Block diagram**



2 Pin configuration

Figure 2. **Pin connection (top view)**



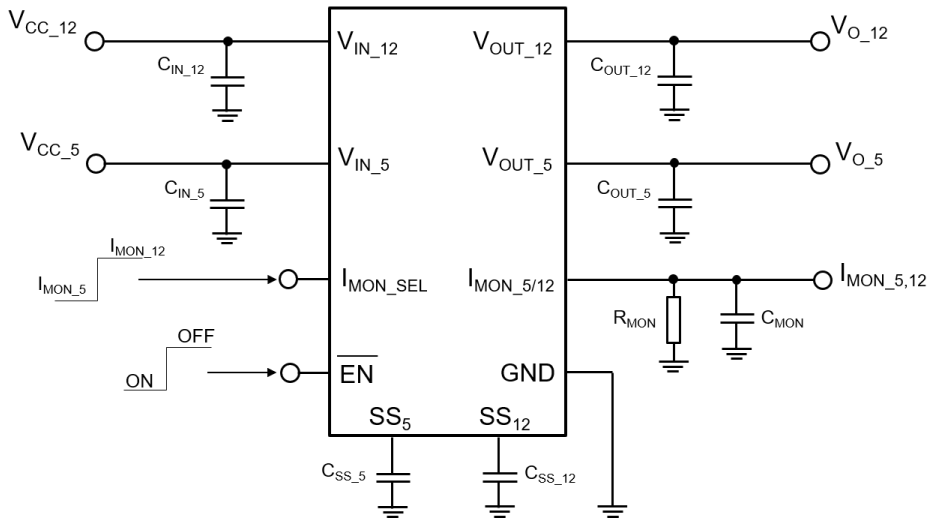
DFN 10 (2 x 3 mm)
Marking view

Table 1. **Pin description**

Symbol	Pin	Description
V_{IN_12}	1	12 V rail supply voltage.
SS_{12}	2	If not connected, default start-up time of 12 V channel is 13 ms. If bypassed to GND with Css, the start-up time can be increased to more than 13 ms. Leave the pin floating if not used.
SS_5	3	If not connected, default start-up time of 5 V channel is 13 ms. If bypassed to GND with Css, the start-up time can be increased to more than 13 ms. Leave the pin floating if not used.
GND	4	Ground.
V_{IN_5}	5	5 V rail supply voltage.
V_{OUT_5}	6	5 V rail output voltage.
$I_{MON\_5/12}$	7	Current monitoring for 5 V or 12 V rail.
I_{MON_SEL}	8	Current monitoring selection pin. If connected to GND, pin 7 shows the I_{MON_5} value. If connected to high level voltage or left floating it shows the I_{MON_12} value. This pin is pulled up to 3.3 V via 750 kΩ resistor.
$\overline{EN}$	9	SAS disable input: set this pin logic-low to turn on the device, high to turn off the device. This pin is internally pulled down to GND via 3.3 MΩ resistor.
V_{OUT_12}	10	12 V rail output voltage.

3 Typical application

Figure 3. **Typical application circuit**



Note: C_{SS_5} and C_{SS_12} are optional.

4 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN_5}	5 V supply voltage	-0.3 to 25	V
	Negative transient tolerance (< 1 ms)	-3	V
V_{IN_12}	12 V supply voltage	-0.3 to 25	V
	Negative transient tolerance (< 1 ms)	-3	V
V_{OUT_5}	5 V output voltage	-0.3 to 7	V
V_{OUT_12}	12 V output voltage	-0.3 to V_{IN} + 0.3 (18 V max.)	V
SSx	Soft-start pin voltage	-0.3 to 7	V
I_{OUT_5}	Continuous output current (1)	3.6	A
I_{OUT_12}	Continuous output current (1)	3.6	A
V_{EN}, I_{MON_SEL}	Enable pin, I_{MON} selection	-0.3 to 7	V
$I_{MON\_5,12}$	Monitor pins voltage	-0.3 to 7	V
ESD	Charge device model	± 500	V
	Human body model	± 2000	
$T_{J\text{-}OP}$	Operating junction temperature (2)	-40 to 125	°C
T_{STG}	Storage temperature	-55 to 150	°C

1. *This value can be applied for guaranteed lifetime. Higher value can be applied for a time lower than 200 ms. The maximum allowable power dissipation is a function of the maximum operative junction temperature of 125 °C, the junction-to-ambient thermal resistance R_{thJA}, and the ambient temperature T_A. It can be estimated by: $P_{D(MAX)} = (125 - T_A) / R_{thJA}$. Exceeding the maximum allowable power dissipation produces overheating that may cause thermal shutdown.*
2. *The thermal limit is set above the maximum thermal rating. It is not recommended to operate the device at temperatures greater than the maximum ratings for extended periods of time.*

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	82	°C/W
R_{thJC}	Thermal resistance junction-case	12	°C/W

1. *Based on JESD51-7, 4-layer PCB.*

5 Electrical characteristics

T_J = 25 °C, V_{IN_5} = 5 V, V_{IN_12} = 12 V, $V_{\overline{EN}}$ = 0 V, C_{IN} = 1 µF, C_{OUT} = 10 µF, unless otherwise specified.

Table 4. Electrical characteristics for STEF512SRX

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
5 V eFuse						
V_{IN_5}	Operating input voltage		4.5		V_{Clamp_5}	V
V_{Clamp_5}	Output clamping voltage	V_{IN_5} = 8 V	5.5	5.7	5.9	V
V_{UVLO_5}	Undervoltage lockout	Turn-on, voltage rising	3.9	4.0	4.1	V
		Hysteresis		0.3		V
R_{DSon_5}	On-resistance	T_J = 25 °C, I_{OUT_05} = 0.5 A		45		mΩ
		T_J = 125 °C (1)			70	
I_{L_5}	Off-state leakage current	$V_{\overline{EN}}$ = 5 V, V_{OUT_5} = GND			1	µA
I_{PLP_5}	PLP reverse leakage current	$V_{\overline{EN}}$ = 0 V, V_{OUT_5} = 5 V, V_{IN_5} < V_{UVLO_5}			1	µA
T_{PLP}	PLP intervention time (2)	$V_{\overline{EN}}$ = 0V, V_{OUT_5} = 5 V, V_{IN_5} < V_{UVLO_5}, I_{PLP_5} < 1 µA, (see Section 6.8)		600		ns
I_{TRIP_5}	Overcurrent trip point (2)			3.6		A
I_{HOLD_5}	Overload current limit	V_{OUT_5} > 2.5 V	2.9	3.1	3.3	A
I_{SHORT_5}	Short-circuit current (2)	V_{OUT_5} < 2.5 V		1.75		A
dV/dt _5	Output voltage ramp time	From 10% to 90% of V_{OUT}, C_{SS_5} floating	10.5	13	15.5	ms
A_{I_5}	Current monitor output current gain I_{MON_5} / I_{OUT_5}	I_{OUT_5} > = 100 mA	26	28.5	31	µA/A
12 V eFuse						
V_{IN_12}	Operating input voltage		10.5		V_{Clamp_12}	V
V_{Clamp_12}	Output clamping voltage	V_{IN_12} = 17 V	14.5	15	15.5	V
V_{UVLO_12}	Undervoltage lockout	Turn-on, voltage rising	7.7	8.5	9.3	V
V_{Hyst_12}	UVLO hysteresis	Turn-off, voltage falling		0.8		V
R_{DSon_12}	On-resistance	T_J = 25 °C, I_{OUT_12} = 0.5 A		40		mΩ
		T_J = 125 °C (1)			70	
I_{L_12}	Off-state leakage current	$V_{\overline{EN}}$ = 5 V, V_{OUT_12} = GND			1	µA
I_{TRIP_12}	Overcurrent trip point (2)			3.6		A
I_{HOLD_12}	Overload current limit	V_{OUT_12} > 7.5 V	2.9	3.1	3.3	A
I_{SHORT_12}	Short-circuit current (2)	V_{OUT_12} < 7.5 V		1.75		A
A_{I_12}	Current monitor output current gain I_{MON_12} / I_{OUT_12}	I_{OUT_12} > = 100 mA	27.5	30	32.5	µA/A

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$dV/dt_{\_12}$	Output voltage ramp time	From 10% to 90% of V_{OUT}, C_{SS_12} floating	10.5	13	15.5	ms
Common features						
V_{IL}	Low level input voltage, $\overline{EN}$ pin	Output enabled			0.7	V
V_{IH}	High level input voltage, $\overline{EN}$ pin	Output disabled	1.7			V
$R_{Pull\text{-}down}$	Pull-down resistor on $\overline{EN}$	Connected to GND		3.3		MΩ
$I_{\overline{EN}}$	$\overline{EN}$ consumption	$V_{\overline{EN}}$ = 5 V		1.5		µA
V_{IL_IMSL}	I_{MON_SEL} low level input voltage	$I_{MON\_5/12}$ pin outputs I_{MON_5}			0.7	V
V_{IH_IMSL}	I_{MON_SEL} high level input voltage	$I_{MON\_5/12}$ pin outputs I_{MON_12}	1.6			V
V_{pull1}	Pull-up (I_{mon_sel})			3.3		V
$R_{Pull\text{-}up}$	Pull-up resistor on I_{mon_sel}			750		kΩ
T_{DELAY} (2)	Startup output delay time	$\overline{EN}$ set to low state		500		µs
I_q	Quiescent current (GND)	Device operating, no load		400	600	µA
		Off-state, $V_{\overline{EN}}$ = 5 V		8		µA
Thermal protection						
TSD (2)	Shutdown temperature			165		°C
	Hysteresis			30		

1. *Values across temperature range are guaranteed by design/correlation and tested in production only at ambient temperature.*
2. *Guaranteed by design, but not tested in production.*

Table 5. Recommended operating condition

Symbol	Parameter	Min.	Typ.	Max	Unit
C_{IN}	Input capacitance	1	10		µF
C_{OUT}	Output capacitance	10	47		
C_{IMON_x}	Monitor pin filter capacitor	1	10		nF
R_{IMONx}	Monitor pin resistor		10		kΩ

6 Device functional description

The STEF512SRX embeds a 5 V and a 12 V electronic fuse (eFuses). Each eFuse can limit the voltage or the current during fault events, such as input overvoltage or output overload, respectively. For this purpose, it contains 2 hysteretic control loops, one limiting the output voltage and one limiting the input current.

The current limiting loop is also used during the start-up phase of the eFuse to limit the inrush current into the output capacitor.

During normal operation, the eFuse behaves as a low-resistance power FET, therefore the output voltage follows the input one. In case of overvoltage or overcurrent event, the eFuse limits the V_{GS} of the internal FET, to clamp the output voltage or current respectively. During such events the die temperature increases due to the power dissipation and so, if the fault persists and the overtemperature threshold is overcome, the device goes into thermal shutdown, the internal FET is turned off and the load disconnected from the power supply.

Each eFuse provides factory-trimmed undervoltage lockout feature.

6.1 Undervoltage lockout

Undervoltage lockout circuit prevents each eFuse from turning on if the supply voltage is below the UVLO rising threshold. During operation, if the input voltage of one channel falls below (V_{UVLO_x} - V_{Hyst_x}), the outputs of both channels are turned off simultaneously.

6.2 Start-up sequence and voltage clamp

The typical start-up sequence of the eFuse is described below and shown in Figure 4, as follows:

- The power supply is connected to the V_{IN_x} pins and both 5 V and 12 V input voltages are higher than the undervoltage lockout threshold.
- The disable pin ($\overline{EN}$) is connected to GND or left floating by the user to enable the device.
- Typically 500 µs after the eFuse starts ramping up the output voltage. Each channel ramps up with the default or user-defined value.
- If the input voltage continues rising, above the overvoltage threshold (V_{Clamp_x}), as a consequence of a failure in the power supply, the eFuse limits the output voltage to V_{Clamp_x}. The eFuse keeps operating in this state until overtemperature threshold is reached and then it shuts down. The power MOSFET remains in an off-state until the die temperature drops below the hysteresis value. Once this happens, the internal auto-retry circuit attempts to reset the device.

6.3 Soft-start function

In order to reduce the inrush current the device starts with a controlled slew rate.

- If SS_{12} and SS_5 pins are floating the device starts with an internal controlled slew rate of 13 ms on both channels.
- The soft-start time can be increased from 13 ms to higher values, by connecting the external C_{SS_X} capacitors.
- At each new startup the internal circuitry choses the longer slew rate between the default internal one (13 ms) and the one set by C_{SS_X}

During the start-up phase the foldback current limit is disabled, the current limit is set to I_{HOLD_x} value.

Given the desired time interval Δt, the capacitance to be added on the C_{SS_X} pin with nominal input voltage V_{IN_12} = 12 V, V_{IN_5} = 5 V can be calculated using the following theoretical formula, valid for C_{SS_X} > 100 nF.

$$\Delta t\ [ms] = C_{SS\_X}\,[nF] \times 0.13 \quad (1)$$

Figure 4. **Typical start-up sequence (Enable after V_{IN} rise)**

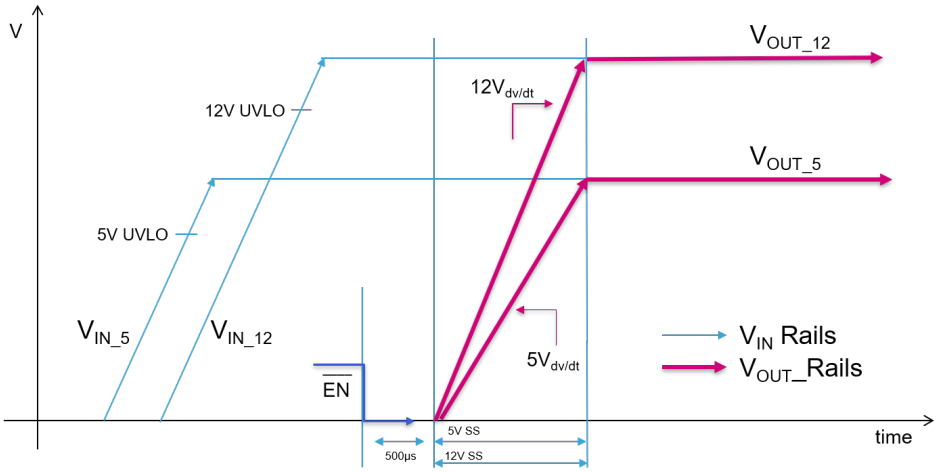
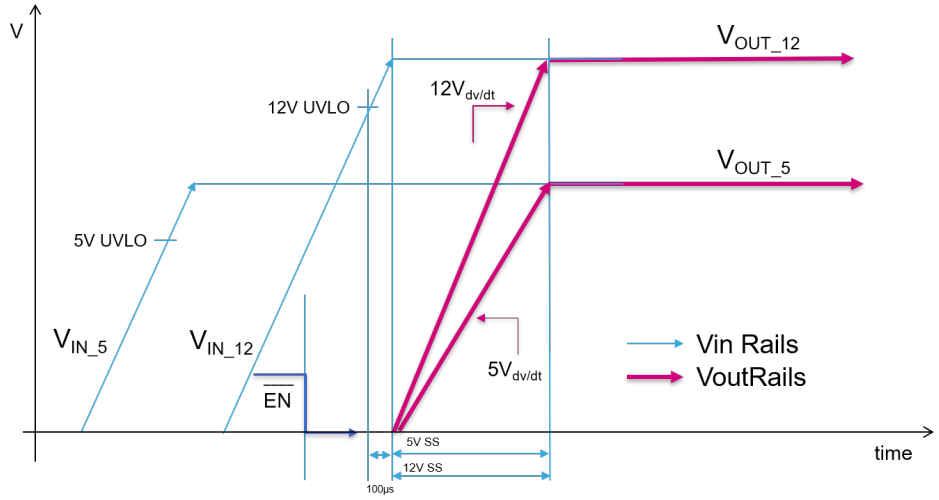


Figure 5. **Typical start-up sequence (Enable during V_{IN} rise)**



6.4 Enable pin

The device provides an SAS-compliant chip disable pin ($\overline{EN}$). The pin is internally pulled down to GND via 3.3 MΩ.

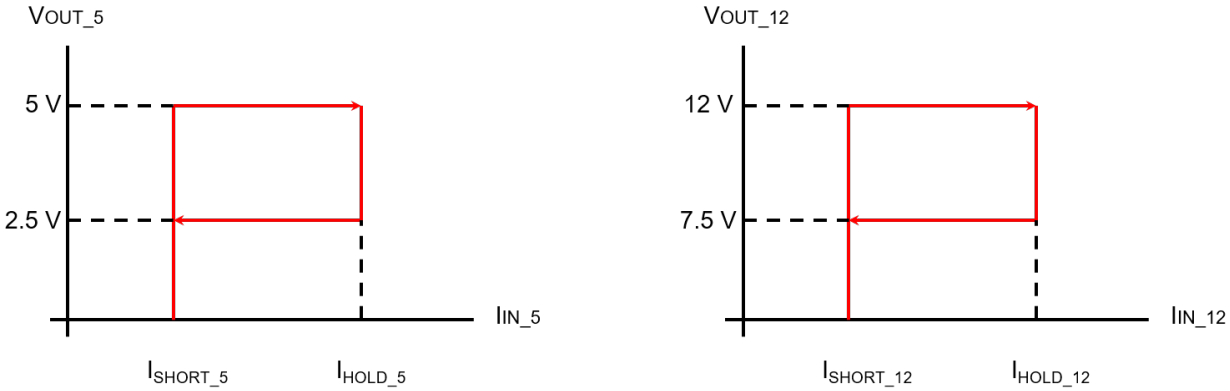
If this function is not needed in the application, it can be left floating. As soon as the input voltage of both channels is higher than the UVLO thresholds, the device ON/OFF status depends on the enable pin as described in the above images.

6.5 Current limit function after startup

Each eFuse provides 2 kinds of current limit protection mechanisms (see Figure 6):

- Operative current limit (I_{HOLD_x}) for both channels, active once the output voltage reaches the input voltage.
- Short-circuit current limit (I_{SHORT_x}) is applied when the output voltage falls below the short-circuit detection thresholds (2.5 V for the 5 V eFuse and 7.5 V for the 12 V eFuse).

Figure 6. **Current limit function graph (5 V and 12 V channels)**



6.6 eFuse current monitor

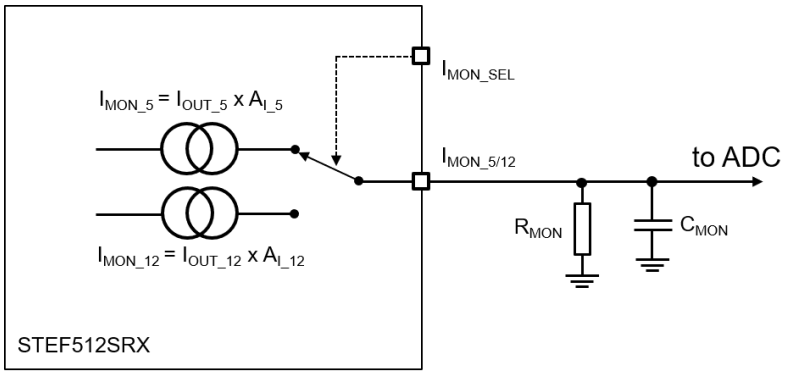
Each channel is equipped with a current monitoring feature that allows the host processor to read the current flowing through the fuse. To use only one ADC converter, the $I_{MON\_5/12}$ pin is able to manage both outputs current information, thanks to a current monitoring selection pin (I_{MON_SEL}).

If I_{MON_SEL} is connected to GND, the pin 7 outputs the I_{MON_5} signal. If I_{MON_SEL} is set to high level, pin 7 outputs the I_{MON_12} signal.

The I_{MON_x} signal is a current proportional to the relevant channel load current, by factor $A_{I\_x} = I_{MON\_x} / I_{OUT\_x}$.

This current is imposed on an external R_{MON_x}, converting the sensing current into voltage for further processing by the host system (see Figure 7).

Figure 7. **Current monitor simplified circuit**



Current monitoring circuit is also equipped with an internal clamp that limits the voltage on the pin at a static value of 1.8 V. Bypassing the pin to GND with a minimum C_{MON} of 1 nF is recommended as it avoids voltage spikes during fast output current transition.

6.7 Thermal shutdown

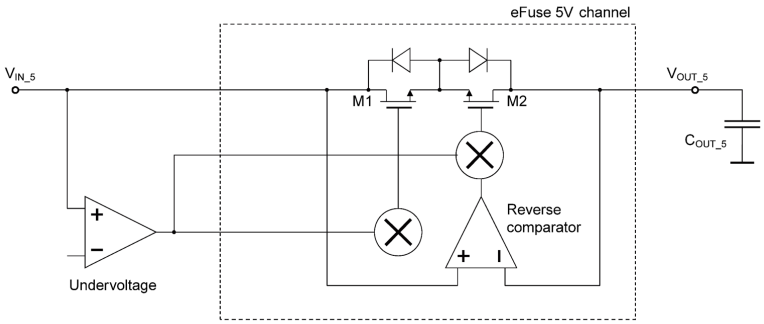
If the device temperature exceeds the thermal threshold, typically 165 °C, the thermal shutdown circuitry turns the power MOSFET off, thus disconnecting the load. The power MOSFET remains in an off-state until the die temperature drops below the hysteresis value. Once this happens, the internal auto-retry circuit attempts to reset the device.

The device is also equipped with a differential thermal protection that avoids damage in case of fast thermal gradients inside the chip. When the differential thermal protection is activated, both the channels are switched off. This protection works in auto-retry mode without soft-start phase.

6.8 Reverse current blocking feature on the 5 V channel

The 5 V eFuse contains a second power transistor (ISOFET) connected in a back-to-back configuration with the main one, to prevent significant current flowing back from the 5 V output into the 5 V input, in case of input short to ground, brown-out or deep input voltage glitch. The simplified structure is shown in Figure 8. The ISOFET is controlled by the UVLO circuit and by a reverse comparator, which continuously monitors the voltage difference between the V_{IN_5} and V_{OUT_5}.

Figure 8. 5 V eFuse diagram



As soon as the reverse comparator detects significant negative voltage across the 5 V eFuse (typically 50 mV), the M2 transistor is turned off immediately. M2 can be turned back on only if the voltage drop across the eFuse has become zero (no negative current). However, in case of slow V_{IN_5} decay, the V_{OUT_5} voltage follows the V_{IN_5} because of the output capacitor being discharged through the eFuse into the V_{IN_5}, hence no significant negative voltage is generated across the eFuse. In that case the UVLO circuit serves as a “stop loss” feature, i.e. the information from the reverse comparator is overridden by the V_{IN_5} undervoltage lockout and M2 is forced to turn off.

As soon as the UVLO threshold has been reached again, the eFuse restarts with normal soft-start cycle.

6.9 External capacitors and application suggestions

Input and output capacitors are mandatory to reduce the transient effects of stray inductances which may be present on the input and output power paths. In fact, when the STEF512SRX interrupts the current flow, input inductance generates a positive voltage spike on the input, and output inductance generates a negative voltage spike on the output. To reduce the effects of such transients, a C_{IN} capacitor of at least 1 µF (including derating effects) must be connected between the input pin and GND and placed as close as possible to the device.

For the same reason, a C_{OUT} capacitor of at least 10 µF must be connected at the output port.

When the device is connected to the power supplies by means of long wires, whose inductance is higher than 1 µH, the input capacitor should be increased.

It is suggested to provide for additional protections and methods for addressing these transients, such as:

- Minimizing inductance of the input and output tracks
- TVS diodes on the input to absorb inductive spikes placed as close as possible to input pins
- Schottky diode on the output to absorb negative spikes
- Combination of ceramic and electrolytic capacitors on the input and output.

7 Typical characteristics

The following plots refer to the typical application circuit with V_{CC_12} = 12 V, V_{CC_5} = 5 V, I_{OUT_12} = I_{OUT_5} = 0 A, SS_5 and SS_12 floating, $\overline{EN}$ set to low state and unless otherwise noted, at T_A = 25 °C.

Figure 9. Quiescent current vs. temperature (ON Mode)

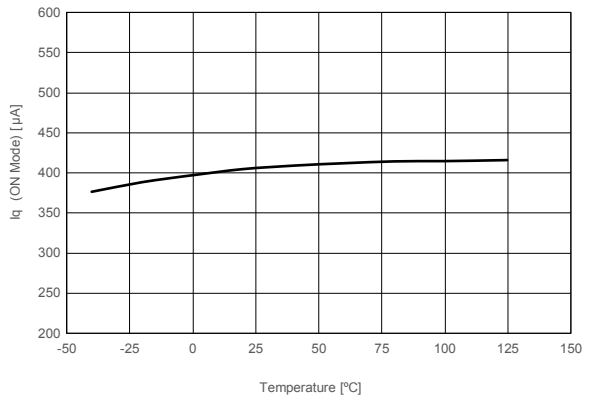


Figure 10. Quiescent current vs. temperature (OFF Mode)

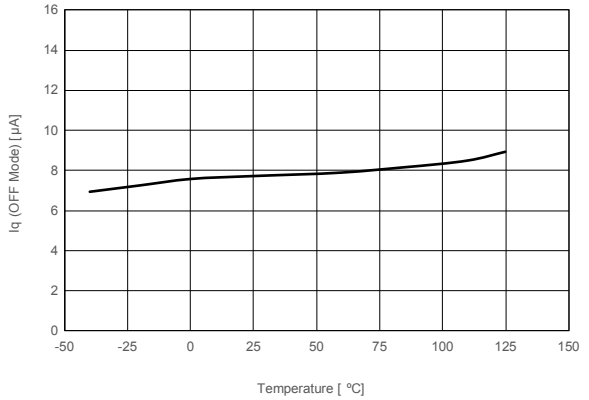


Figure 11. R_{DS_ON} 12 V eFuse vs. temperature

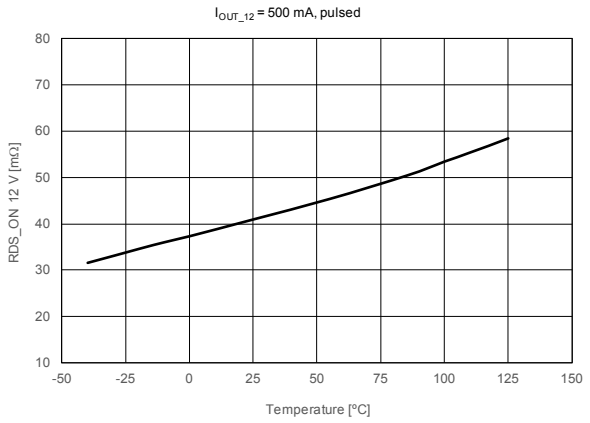


Figure 12. R_{DS_ON} 5 V eFuse vs. temperature

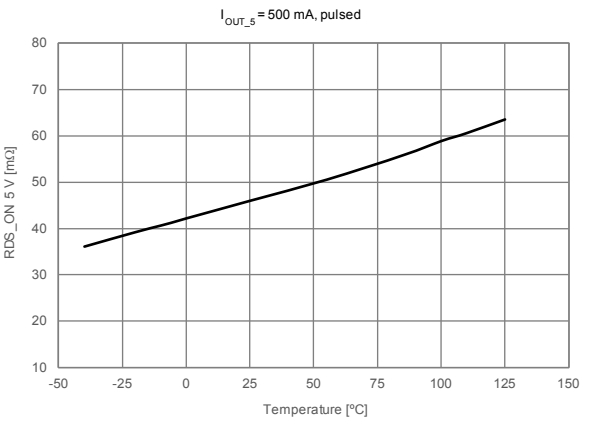


Figure 13. 12 V eFuse voltage clamp vs. temperature

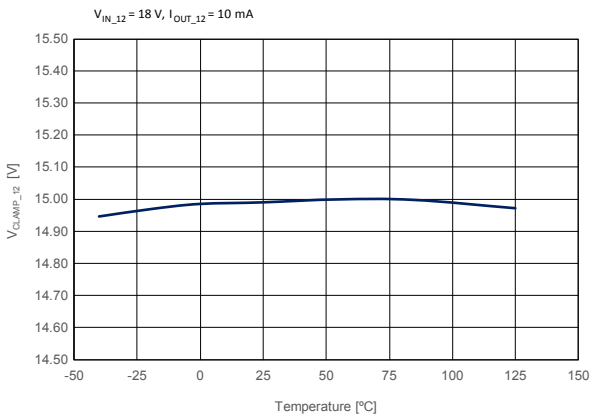


Figure 14. 5 V eFuse voltage clamp vs. temperature

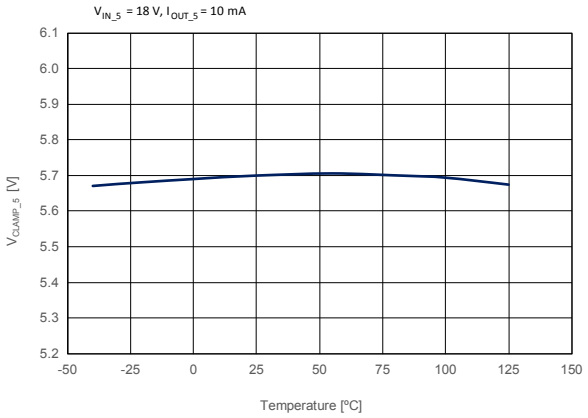


Figure 15. UVLO 5 V eFuse vs. temperature

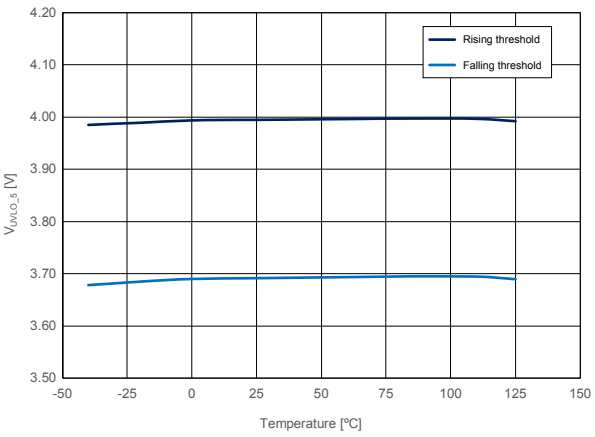


Figure 16. UVLO 12 V eFuse vs. temperature

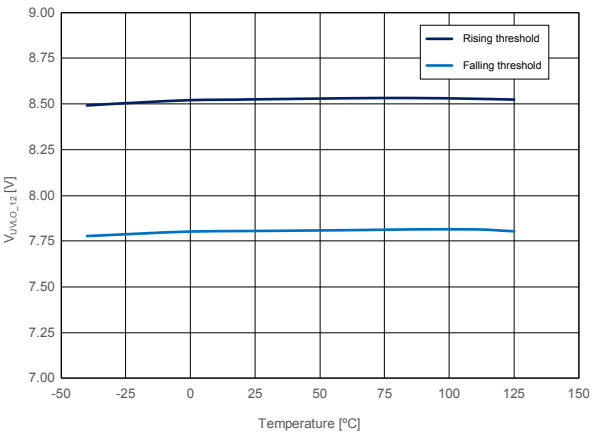


Figure 17. 5 V eFuse overload current limit vs. temperature

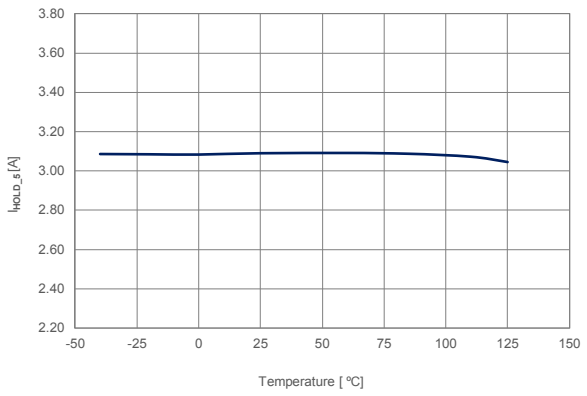


Figure 18. 12 V eFuse overload current limit vs. temperature

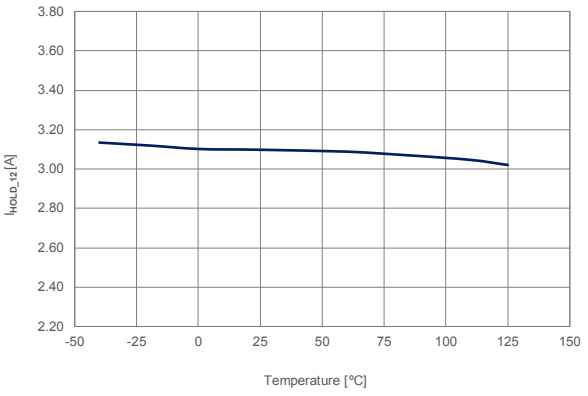


Figure 19. Soft-start time vs. temperature

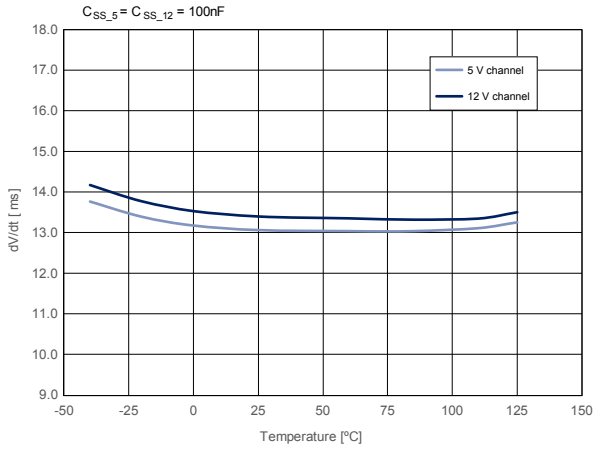


Figure 20. SAS disable pin threshold vs. temperature

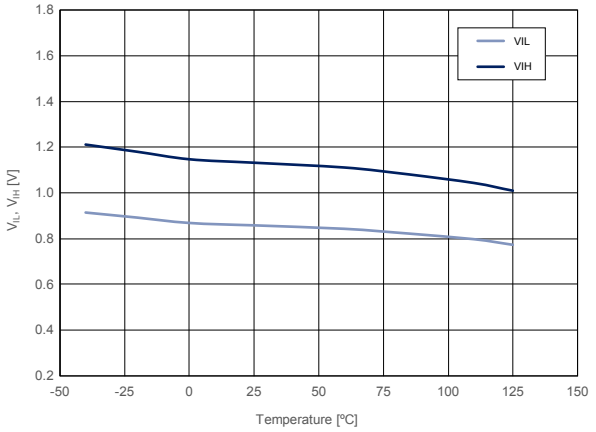


Figure 21. I_{MON_SEL} pin threshold vs. temperature

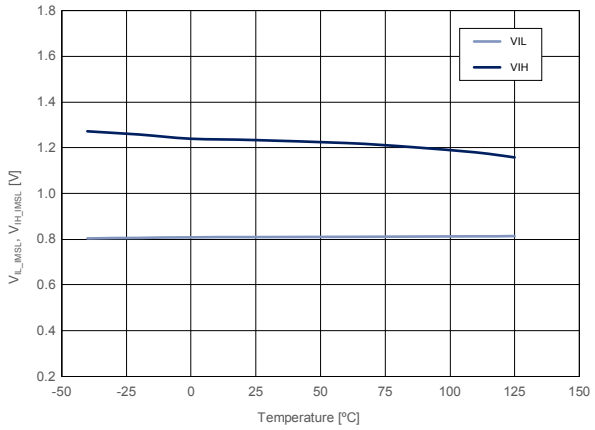


Figure 22. Current monitor gain vs. temperature

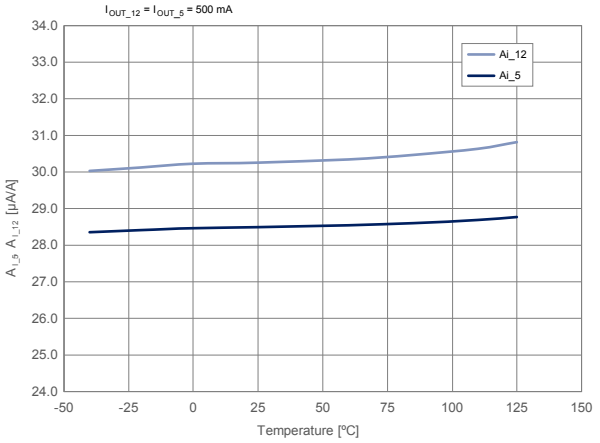


Figure 23. 5 V and 12 V current monitor gain vs. load current

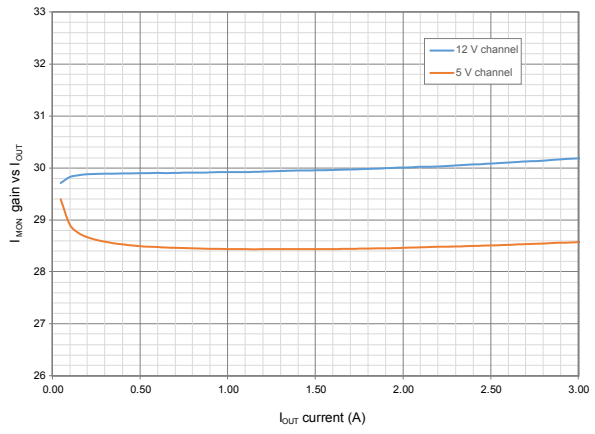


Figure 24. Startup via input voltage

V_{IN_12} = from 0 V to 12 V, V_{IN_5} = from 0 V to 5 V, I_{OUT_12} = 2 mA, I_{OUT_5} = 2 mA

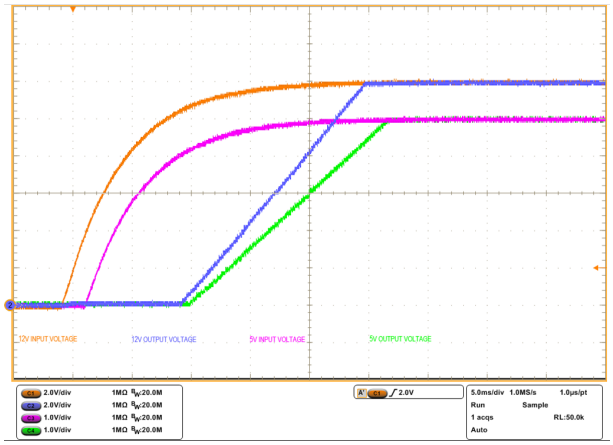


Figure 25. Startup via input voltage (Hot-plug) 5 V

V_{IN_12} = 12 V, V_{IN_5} = from 0 V to 5 V, I_{OUT_12} = 0 mA, I_{OUT_5} = 0 mA

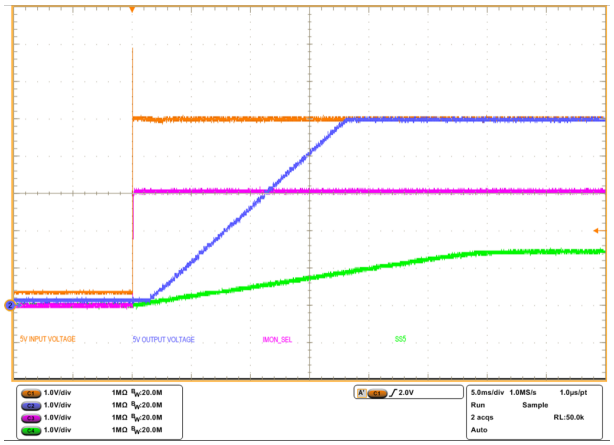


Figure 26. Startup via input voltage (Hot-plug) 12 V

V_{IN_12} = from 0 V to 12 V, V_{IN_5} = 5 V, I_{OUT_12} = 0 mA, I_{OUT_5} = 0 mA

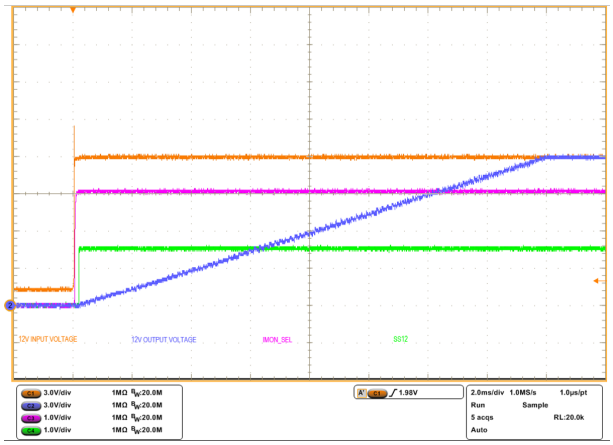


Figure 27. Startup via input voltage (Hot-plug) 5 V & 12 V

V_{IN_12} = from 0 V to 12 V, V_{IN_5} = from 0 V to 5 V, I_{OUT_12} = 0 mA, I_{OUT_5} = 0 mA

Figure 28. Startup via EN_N signal

V_{IN_12} = 12 V, V_{IN_5} = 5 V, V_{EN_N} = from 3.3 V to 0 V, I_{OUT_12} = 10 mA, I_{OUT_5} = 10 mA

Figure 29. Shutdown via EN_N signal

V_{IN_12} = 12 V, V_{IN_5} = 5 V, V_{EN_N} = from 0 V to 3.3 V , trise = 1 µs, I_{OUT_12} = 10 mA, I_{OUT_5} = 10 mA

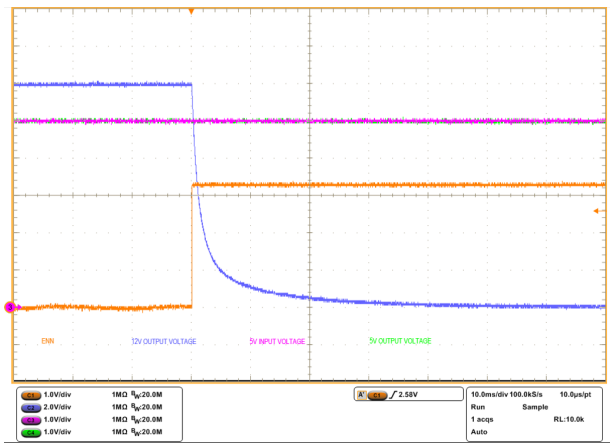


Figure 30. Startup into voltage clamp (5 V eFuse)

V_{IN_12} = from 0 V to 12 V, V_{IN_5} = from 0 V to 12 V, I_{OUT_12} = 0 mA, I_{OUT_5} = 100 mA

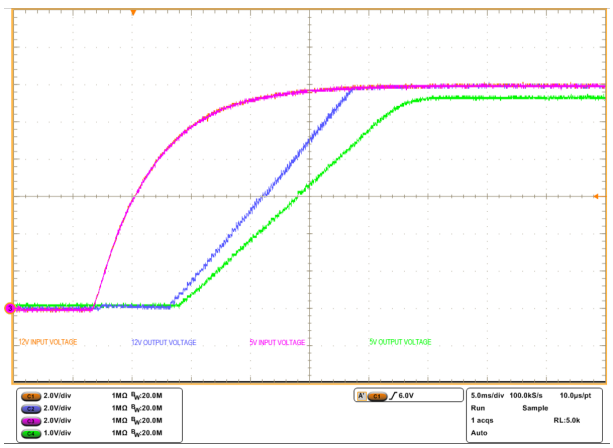


Figure 31. Startup into voltage clamp (12 V eFuse)

V_{IN_12} = from 0 V to 18 V, V_{IN_5} = 5 V, I_{OUT_12} = 100 mA, I_{OUT_5} = 0 mA, trise = 10 µs

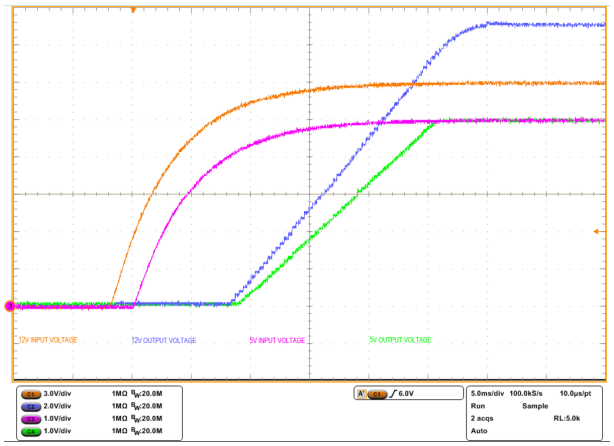


Figure 32. Voltage clamp during operation (5 V eFuse)

V_{IN_12} = 12 V, V_{IN_5} = from 5 V to 8 V, I_{OUT_12} = 0 mA, I_{OUT_5} = 400 mA

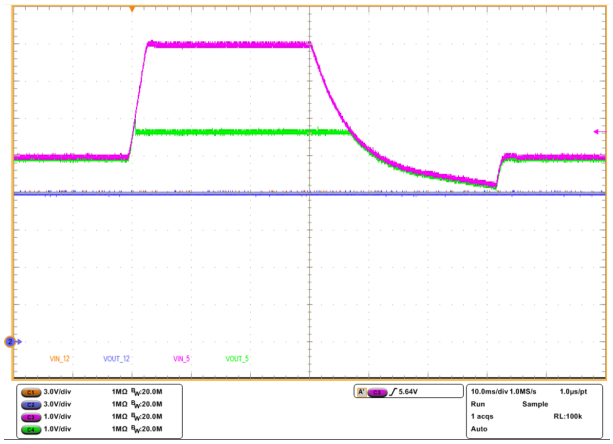


Figure 33. Voltage clamp during operation (12 V eFuse)

V_{IN_12} = from 12 V to 18 V, V_{IN_5} = 5 V, I_{OUT_12} = 400 mA, I_{OUT_5} = 0 mA

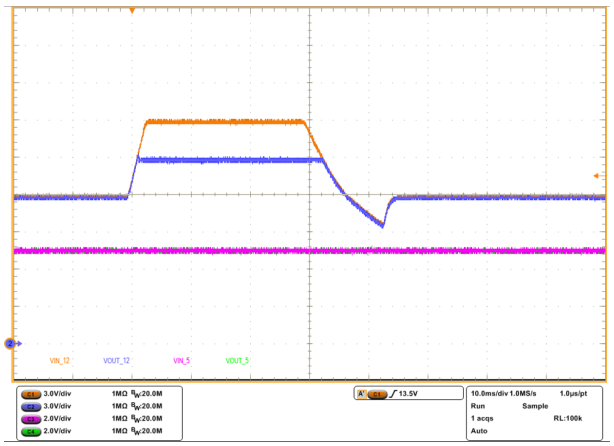


Figure 34. Startup into output short-circuit by EN_N (5 V eFuse)

V_{IN_12} = 12 V, V_{IN_5} = 5 V, I_{OUT_12} = 0 mA, V_{OUT_5} = shorted to GND

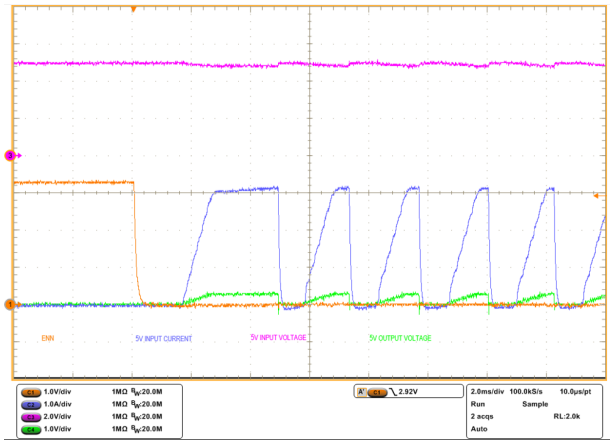


Figure 35. Startup into output short-circuit by EN_N (12 V eFuse)

V_{IN_12} = 12 V, V_{IN_5} = 5 V, I_{OUT_5} = 0 mA, V_{OUT_12} = shorted to GND

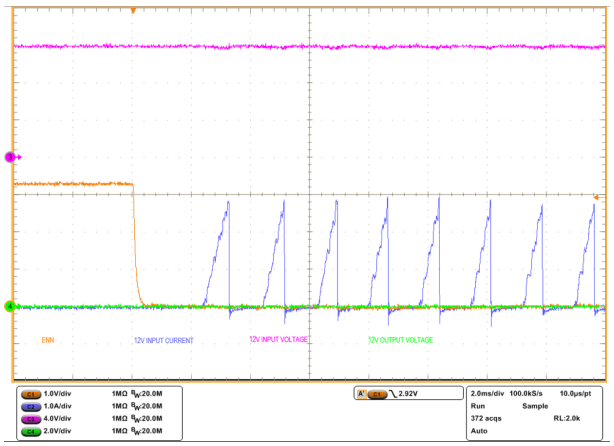


Figure 36. Startup into overload (5 V eFuse)

V_{IN_12} = from 0 V to 12 V, V_{IN_5} = from 0 V to 5 V, R_{OUT_5} = 1 Ω, I_{OUT_12} = 0 mA

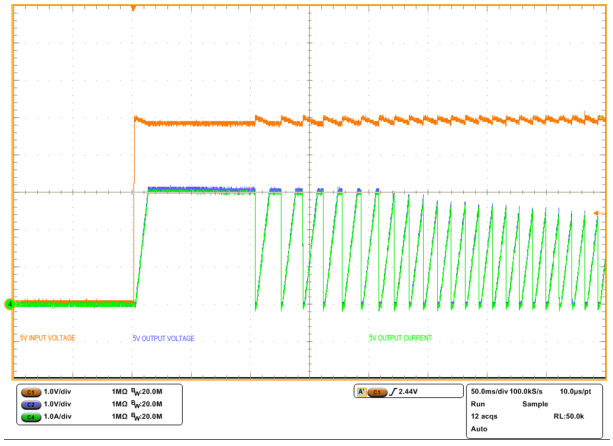


Figure 37. Startup into overload (12 V eFuse)

V_{IN_12} = from 0 V to 12 V, V_{IN_5} = from 0 V to 5 V, R_{OUT_12} = 2.2 Ω, I_{OUT_5} = 0 mA

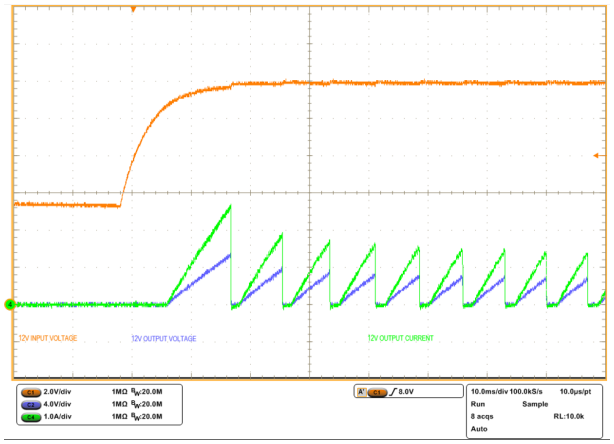


Figure 38. Overcurrent protection during operation (5 V eFuse)

V_{IN_12} = 12 V, V_{IN_5} = 5 V, I_{OUT_12} = 2 A, I_{OUT_5} = from 0 mA to current limit (constant voltage load)

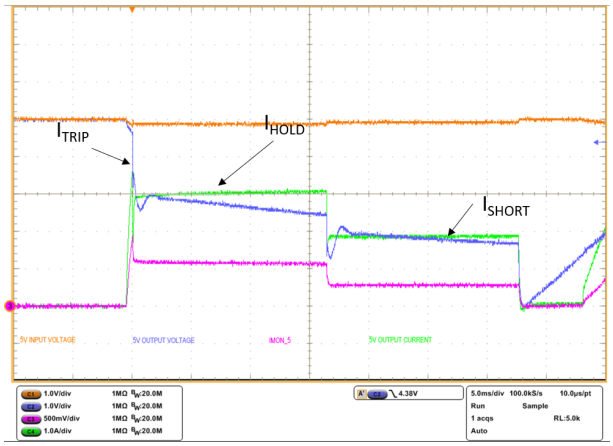


Figure 39. Overcurrent protection during operation (12 V eFuse)

V_{IN_12} = 12 V, V_{IN_5} = 5 V, I_{OUT_5} = 1 A, I_{OUT_12} = from 0 mA to current limit (constant voltage load)

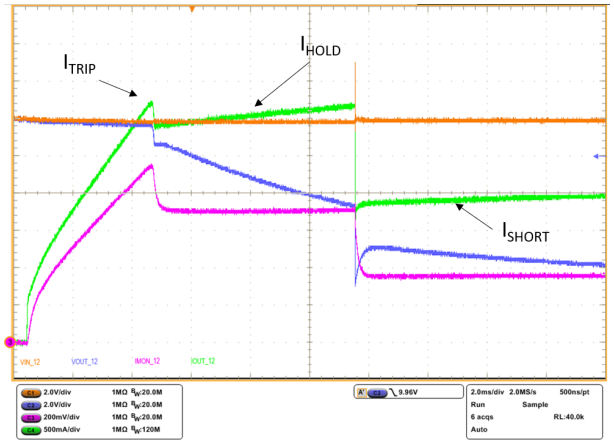


Figure 40. PLP protection through UVLO_5

V_{IN_12} = 12 V, V_{IN_5} = from 5 V to floating, I_{OUT_12} = 0 mA, I_{OUT_5} = 1 A

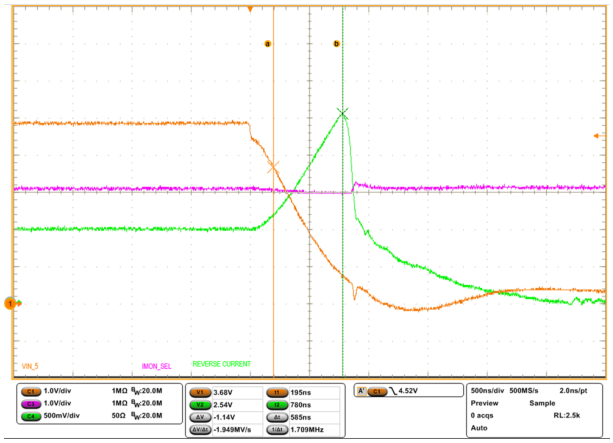


Figure 41. Current monitor response time to load step

I_{out_12} = 1 A to 2 A and back, R_{IMON} = 10 kΩ and C_{IMON} = 10 nF

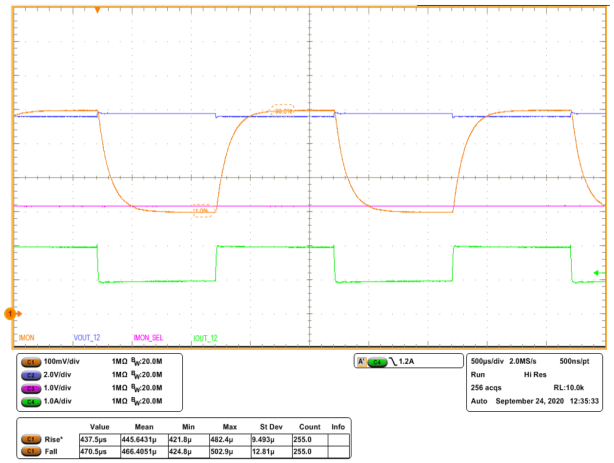
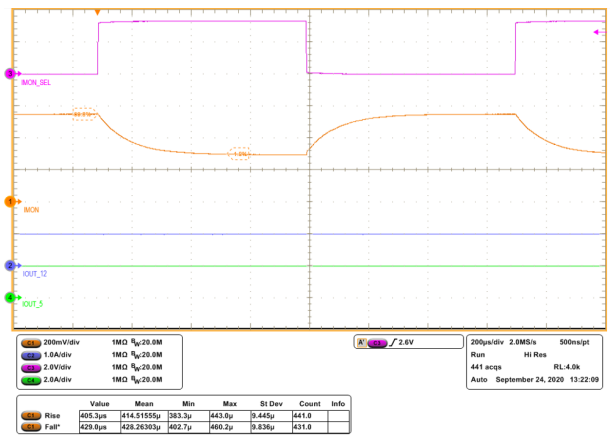


Figure 42. Current monitor response time to channel switch via $I_{MON-SEL}$

I_{out_12} = 1 A, I_{out_5} = 2 A, R_{IMON} = 10 kΩ and C_{IMON} = 10 nF



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 DFN10 (2 x 3 mm) package information

Figure 43. DFN10 (2 x 3 mm) package outline

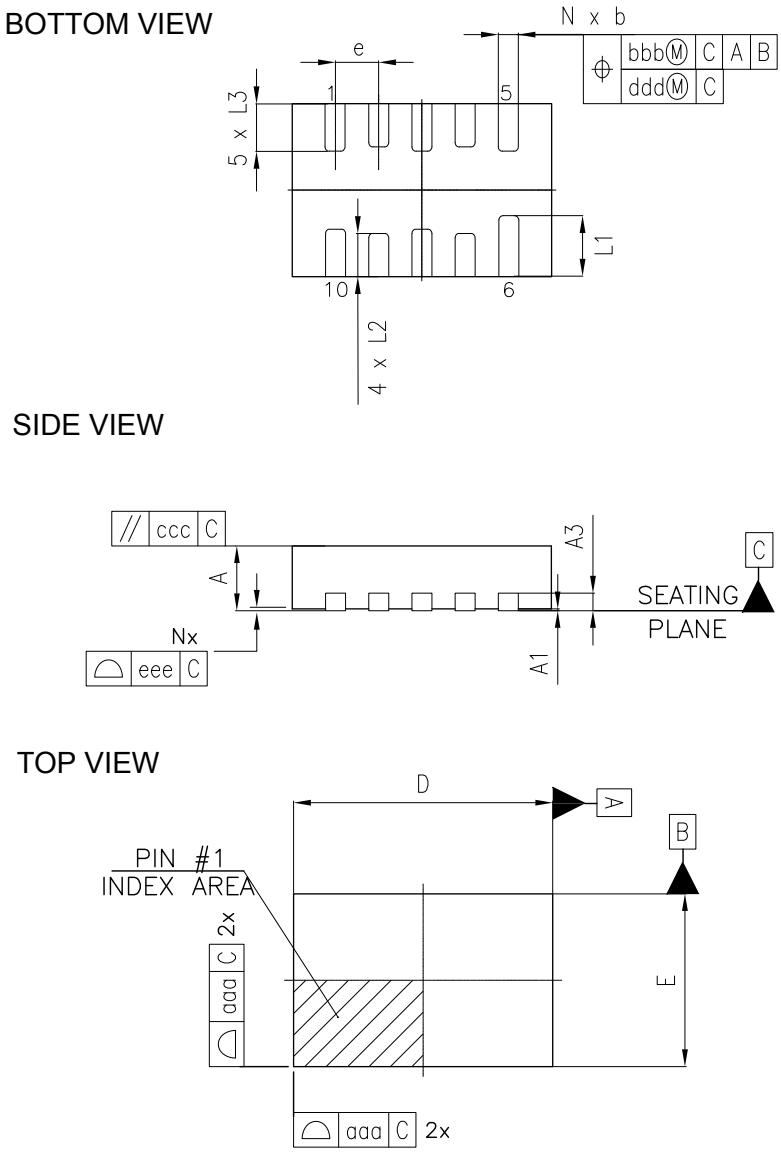
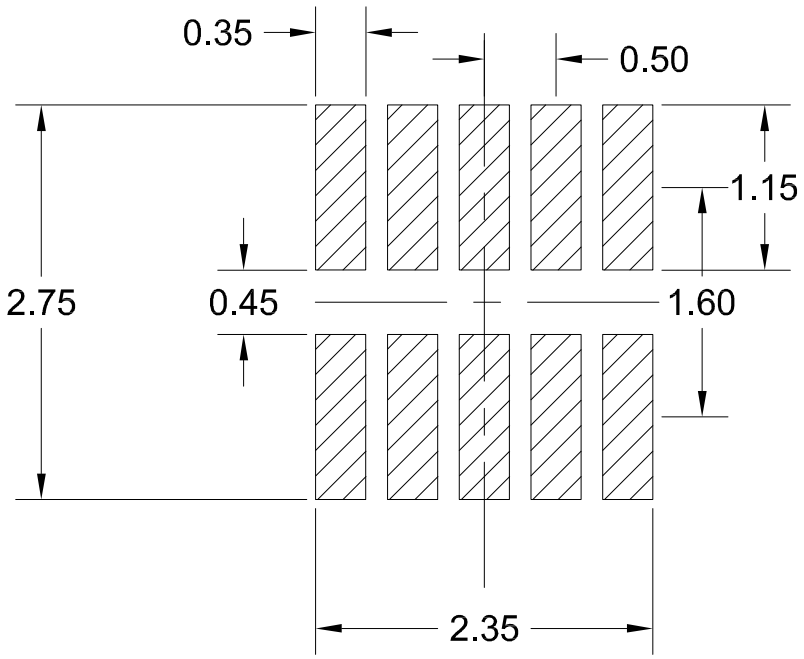


Table 6. **DFN10 (2 x 3 mm) mechanical data**

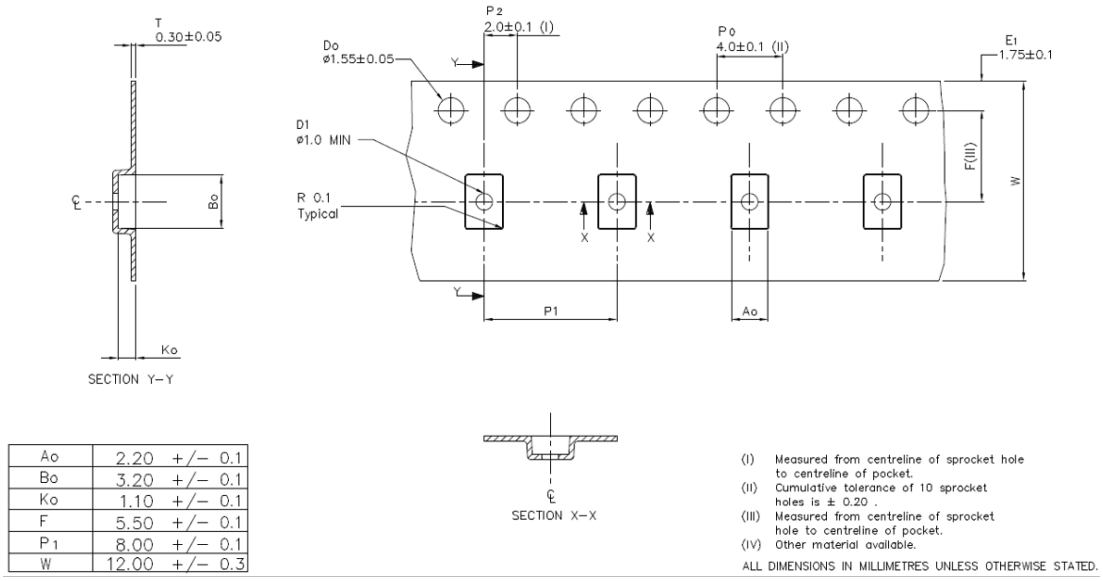
Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 ref.	
b	0.180	0.230	0.280
D		3.00 BSC	
e		0.50 BSC	
E		2.00 BCS	
L1	0.60	0.70	0.80
L2	0.40	0.50	0.60
L3	0.45	0.55	0.65
K	0.20		
N		10	
aaa		0.05	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

Figure 44. **DFN10 (2 x 3 mm) recommended footprint**



8.2 DFN10 (2 x 3) carrier tape information

Figure 45. Carrier tape information



Ao	2.20 +/– 0.1
Bo	3.20 +/– 0.1
Ko	1.10 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

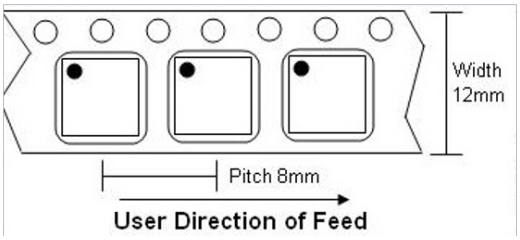


Figure 46. Marking information

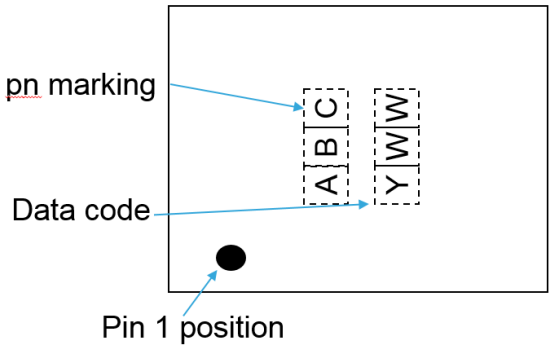
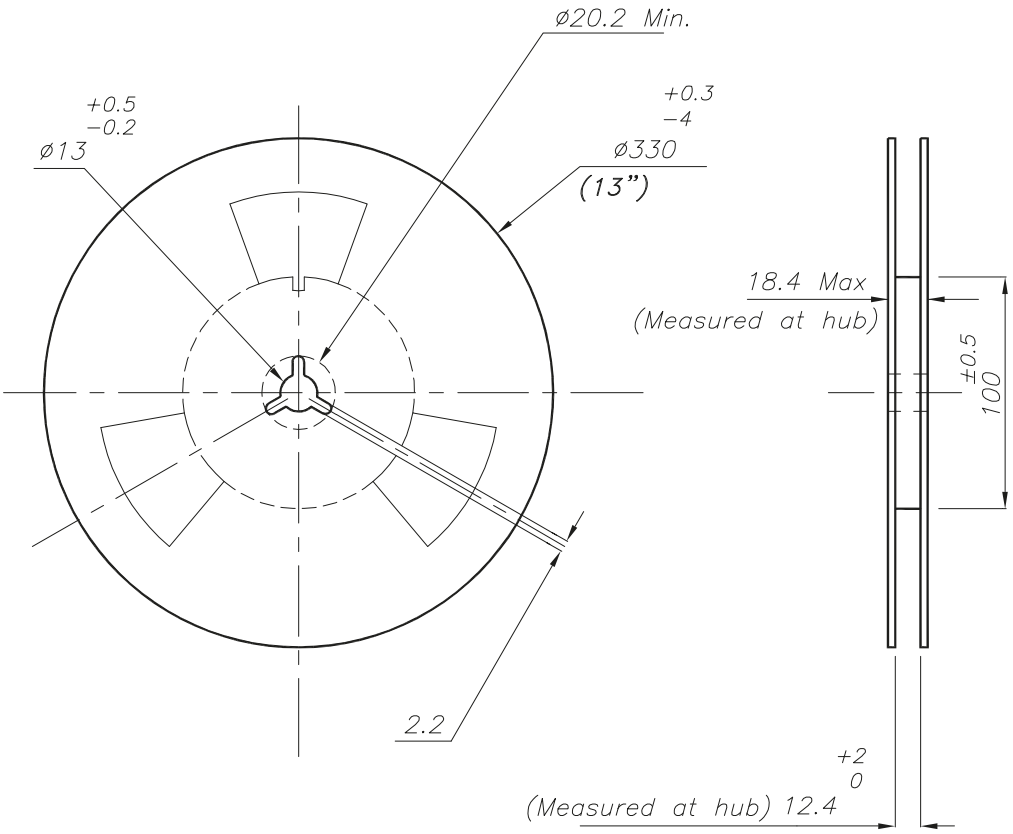


Figure 47. **Reel drawing**



9 Ordering information

Table 7. **Order codes**

Order code	Package	Marking
STEF512SRXCPUR	DFN10 (2 x 3 mm)	EXC

Revision history

Table 8. **Document revision history**

Date	Revision	Changes
31-Jan-2022	1	Initial release.

Contents

List of tables

List of figures