LM723JAN Voltage Regulator

Check for Samples: LM723JAN

FEATURES

- 150 mA output current without external pass transistor
- Output currents in excess of 10A possible by adding external transistors
- Input voltage 40V max
- Output voltage adjustable from 2V to 37V
- Can be used as either a linear or a switching regulator

DESCRIPTION

The LM723 is a voltage regulator designed primarily for series regulator applications. By itself, it will supply output currents up to 150 mA; but external transistors can be added to provide any desired load current. The circuit features extremely low standby current drain, and provision is made for either linear or foldback current limiting.

The LM723 is also useful in a wide range of other applications such as a shunt regulator, a current regulator or a temperature controller.

Connection Diagram

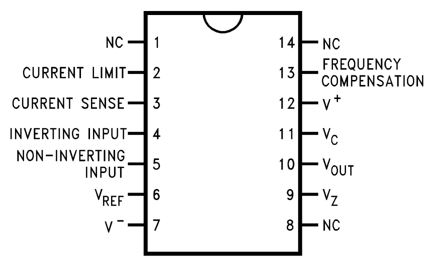
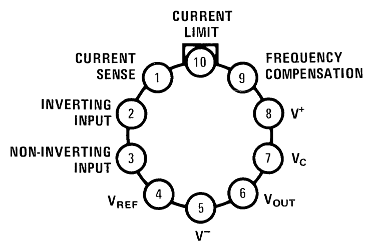


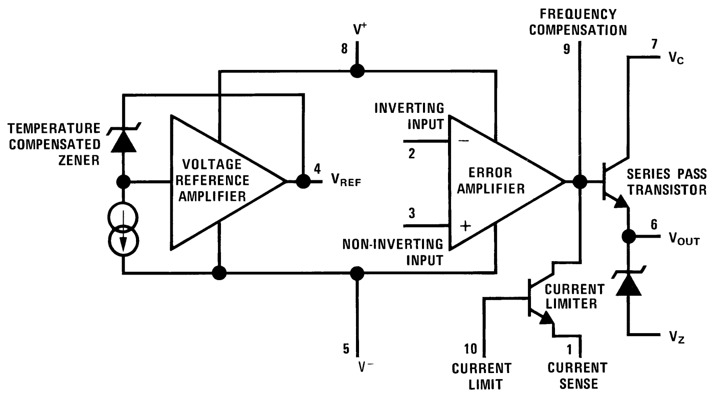
Figure 1. Dual-In-Line Package (Top View)



NOTE: Pin 5 connected to case.

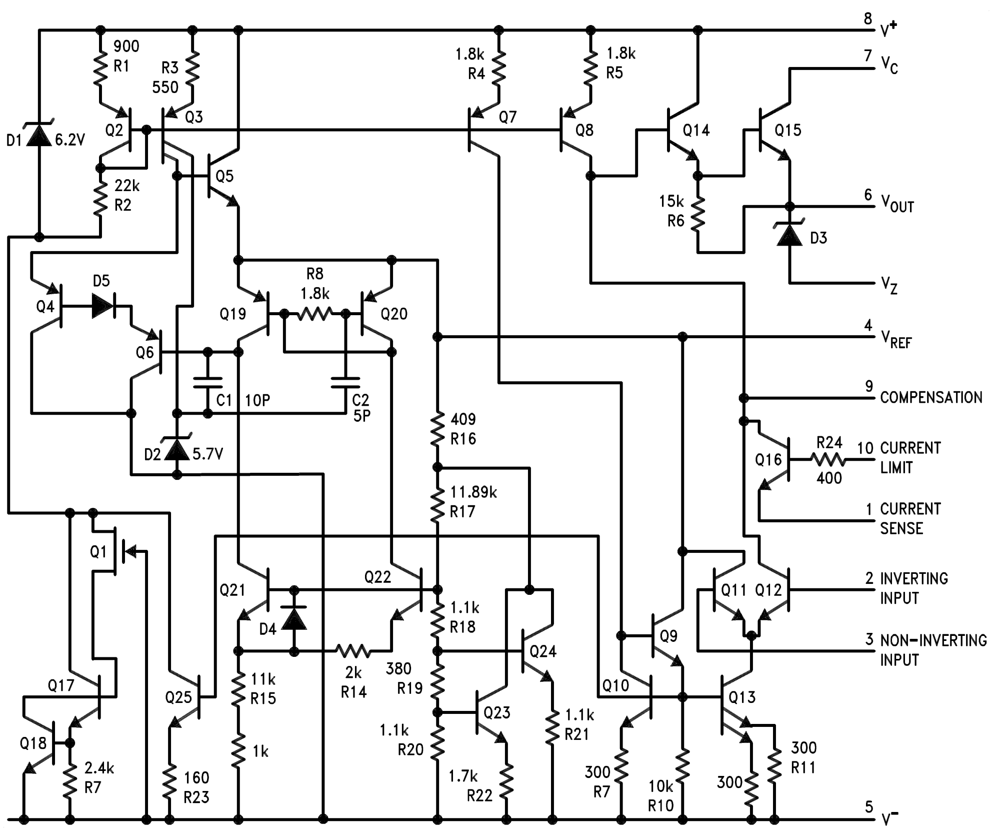
Figure 2. Metal Can Package (Top View)

Equivalent Circuit



(1) Pin numbers refer to metal can package.

Schematic Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings [1]

Pulse Voltage from V^+ to V^- (50 ms)	50V
Continuous Voltage from V^+ to V^-	40V
Input-Output Voltage Differential	40V
Differential Input Voltage	±5V
Voltage between non-inverting input and V^-	+8V
Current from V_Z	25 mA
Current from V_{REF}	15 mA
Internal Power Dissipation (T_A = 125°C) Metal Can [2]	300 mW
Cavity DIP [2]	400 mW
Maximum T_J	+175°C
Storage Temperature Range	−65°C ≤ T_A ≤ +150°C
Lead Temperature (Soldering, 4 sec. max.)	300°C
Thermal Resistance	
θ_{JA}	
Cerdip (Still Air) Cerdip (500LF/ Min Air flow) Metal Can (Still Air) Metal Can (500LF/ Min Air flow)	100°C/W 61°C/W 156°C/W 89°C/W
θ_{JC}	
CERDIP Metal Can	22°C/W 37°C/W
ESD Tolerance [3]	1200V

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is less. See derating curves for maximum power rating above 25°C.
(3) Human body model, 1.5 kΩ in series with 100 pF.

Recommended Operating Conditions

Input Voltage Range	9.5V to 40V $_{DC}$
Output Voltage Range	2V to 37V $_{DC}$
Input-Output Voltage Differential	2.5 V to 38V $_{DC}$
Ambient Operating Temperature Range	−55°C ≤ T_A ≤ +125°C

Quality Conformance Inspection

MIL-STD-883, Method 5004 and Method 5005

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25

Subgroup	Description	Temp (°C)
10	Switching tests at	+125
11	Switching tests at	-55

Electrical Characteristics

DC Parameters [1]

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{Rline}	Line Regulation	$12V \le V_{IN} \le 15V$, $V_{OUT} = 5V$, $I_L = 1mA$		−0.1	0.1	$\%V_{OUT}$	1
				−0.2	0.2	$\%V_{OUT}$	2
				−0.3	0.3	$\%V_{OUT}$	3
		$12V \le V_{IN} \le 40V$, $V_{OUT} = 2V$, $I_L = 1mA$		−0.2	0.2	$\%V_{OUT}$	1
		$9.5V \le V_{IN} \le 40V$, $V_{OUT} = 5V$, $I_L = 1mA$		−0.3	0.3	$\%V_{OUT}$	1
		$12V \le V_{IN} \le 15V$, $V_{OUT} = 5V$, $I_L = 1mA$		−10.0	+10.0	mV	1
				−20.0	+20.0	mV	2
				−30.0	+30.0	mV	3
V_{Rload}	Load Regulation	$1mA \le I_L \le 50mA$, $V_{IN} = 12V$, $V_{OUT} = 5V$		−0.15	0.15	$\%V_{OUT}$	1
				−0.4	0.4	$\%V_{OUT}$	2
				−0.6	0.6	$\%V_{OUT}$	3
		$1mA \le I_L \le 10mA$, $V_{IN} = 40V$, $V_{OUT} = 37V$		−0.5	0.5	$\%V_{OUT}$	1
		$6mA \le I_L \le 12mA$, $V_{IN} = 10V$, $V_{OUT} = 7.5V$		−0.2	0.2	$\%V_{OUT}$	1
		$1mA \le I_L \le 50mA$, $V_{IN} = 12V$, $V_{OUT} = 5V$		−15.0	+15.0	mV	1
				−40.0	+40.0	mV	2
				−60.0	+60.0	mV	3
V_{REF}	Voltage Reference	$I_{REF} = 1mA$, $V_{IN} = 12V$		6.95	7.35	V	1
				6.9	7.4	V	2, 3
I_{SCD}	Standby Current	$V_{IN} = 30V$, $I_L = I_{REF} = 0$, $V_{OUT} = V_{REF}$		0.5	3	mA	1
				0.5	2.4	mA	2
				0.5	3.5	mA	3
I_{OS}	Short Circuit Current	$V_{OUT} = 5V$, $V_{IN} = 12V$, $R_{SC} = 10\Omega$, $R_L = 0$		45	85	mA	1
V_Z	Zener Voltage	$I_Z = 1mA$		[2][3] 5.58	6.82	V	1
V_{OUT}	Output Voltage	$V_{IN} = 12V$, $V_{OUT} = 5V$, $I_L = 1mA$	[4]	4.5	5.5	V	1, 2, 3
Delta V_{OUT} / Delta T	Average Temperature Coefficient of Output Voltage	$25°C \le T_A \le +125°C$, $V_{IN} = 12V$, $V_{OUT} = 5V$, $I_L = 1mA$	[5]	−0.01	0.01	%/°C	8A
		$-55°C \le T_A \le +25°C$, $V_{IN} = 12V$, $V_{OUT} = 5V$, $I_L = 1mA$	[5]	−0.015	0.015	%/°C	8B
Delta V_{OUT} / Delta V_{IN}	Ripple Rejection	f = 10KHz, $C_{REF} = 0F$, $V_{INS} = 2V_{RMS}$		64		dB	4
		f = 10KHz, $C_{REF} = 5\mu F$, $V_{INS} = 2V_{RMS}$		76		dB	4

(1) Unless otherwise specified, $T_A = 25°C$, $V_{IN} = V^+ = V_C = 12V$, $V^- = 0$, $V_{OUT} = 5V$, $I_L = 1$ mA, $R_{SC} = 0$, $C_1 = 100$ pF, $C_{REF} = 0$ and divider impedance as seen by error amplifier ≤ 10 kΩ connected as shown in Figure 3. Line and load regulation specifications are given for the condition of constant chip temperature. Temperature drifts must be taken into account separately for high dissipation conditions.
(2) For metal can applications where V_Z is required, an external 6.2V zener diode should be connected in series with V_{OUT}.
(3) Tested for 14 – lead DIP only.
(4) Setup test for Temp. Coeff.
(5) Calculated parameter

Electrical Characteristics (continued)

DC Parameters (1)

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
N_O	Output Noise Voltage	100Hz ≤ f ≤ 10KHz, V_{INS} = $0V_{RMS}$, C_{REF} = 0µF			120	$µV_{RMS}$	4
		100Hz ≤ f ≤ 10KHz, V_{INS} = $0V_{RMS}$, C_{REF} = 5µF			7	$µV_{RMS}$	4
Delta V_{OUT} / Delta V_{IN}	Line Transient Response	V_{IN} = 12V, V_{OUT} = 5V, I_L = 1mA, C_{REF} = 5µF, R_{SC} = 0Ω, Delta V_{IN} = 3V for 25µsec		0	10	mV/V	4
Delta V_{OUT} / Delta I_L	Load Transient Response	V_{IN} = 12V, V_{OUT} = 5V, I_L = 40mA, C_{REF} = 5µF, R_{SC} = 0Ω, Delta I_L = 10mA for 25µsec		−1.5	0	mV/mA	4

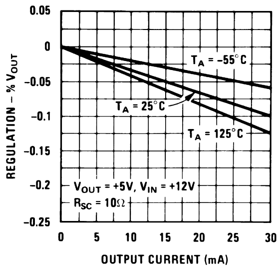
DC Parameters: Drift Values

Delta calculations performed on JAN S and QMLV devices at Group B, Subgroup 5, only.

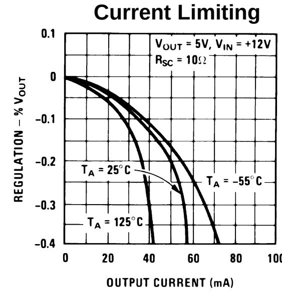
Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{Rline}	Line Regulation	12V ≤ V_{IN} ≤ 15V, V_{OUT} = 5V, I_L = 1mA, ±1mV, or ±15% (whichever is greater)		−1.0	1.0	mV	1
V_{Rload}	Load Regulation	1mA ≤ I_L ≤ 50mA, V_{IN} = 12V, V_{OUT} = 5V, ±1mV, or ±20% (whichever is greater)		−1.0	1.0	mV	1
V_{REF}	Reference Voltage	I_{REF} = 1mA, V_{IN} = 12V		−15	15	mV	1
I_{SCD}	Standby Current Drain	V_{IN} = 30V, I_L = I_{REF} =0, V_{OUT} = V_{REF}		−10	10	%	1

Typical Performance Characteristics

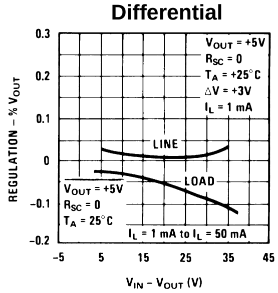
Load Regulation Characteristics with Current Limiting



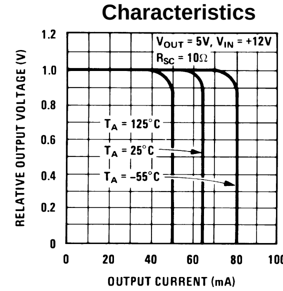
Load Regulation Characteristics with Current Limiting



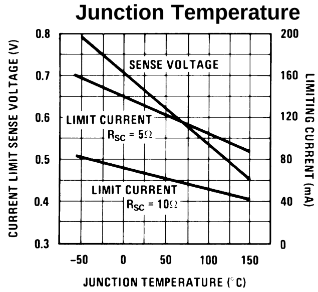
Load & Line Regulation vs Input-Output Voltage Differential



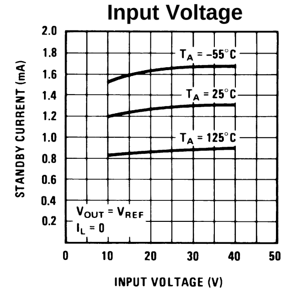
Current Limiting Characteristics



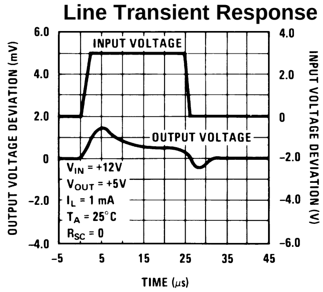
Current Limiting Characteristics vs Junction Temperature



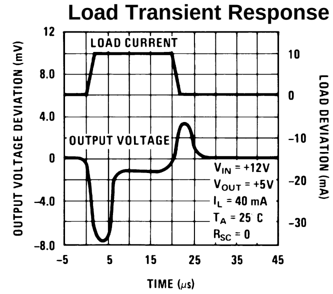
Standby Current Drain vs Input Voltage



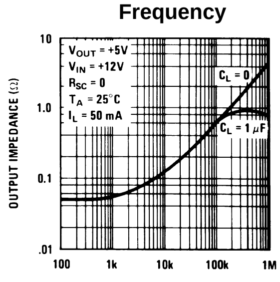
Line Transient Response



Load Transient Response

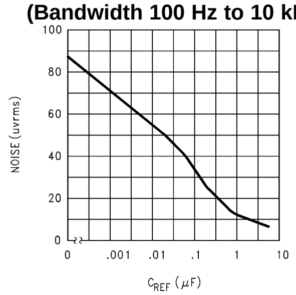


Output Impedence vs Frequency



Maximum Power Ratings

Noise vs Filter Capacitor (C_{REF} in Circuit of Figure 3) (Bandwidth 100 Hz to 10 kHz)



LM723 Power Dissipation vs Ambient Temperature

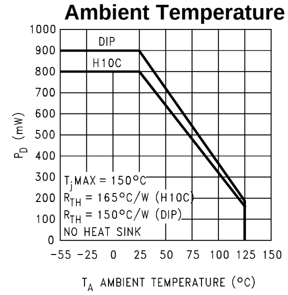


Table 1. Resistor Values (kΩ) for Standard Output Voltage

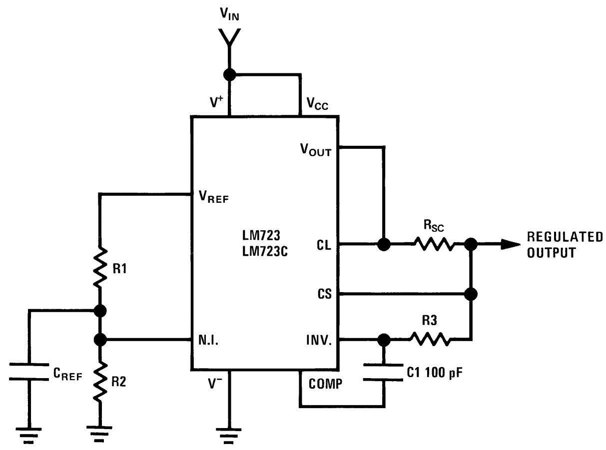
Positive Output Voltage	Applicable Figures (2)	Fixed Output ±5%		Output Adjustable ±10% (1)			Negative Output Voltage	Applicable Figures	Fixed Output ±5%		5% Output Adjustable ±10%		
		R1	R2	R1	P1	R2			R1	R2	R1	P1	R2
+3.0	1, 5, 6, 9, 12 (4)	4.12	3.01	1.8	0.5	1.2	+100	7	3.57	102	2.2	10	91
+3.6	1, 5, 6, 9, 12 (4)	3.57	3.65	1.5	0.5	1.5	+250	7	3.57	255	2.2	10	240
+5.0	1, 5, 6, 9, 12 (4)	2.15	4.99	0.75	0.5	2.2	−6 (3)	3, (10)	3.57	2.43	1.2	0.5	0.75
+6.0	1, 5, 6, 9, 12 (4)	1.15	6.04	0.5	0.5	2.7	−9	3, 10	3.48	5.36	1.2	0.5	2.0
+9.0	2, 4, (5, 6, 9, 12)	1.87	7.15	0.75	1.0	2.7	−12	3, 10	3.57	8.45	1.2	0.5	3.3
+12	2, 4, (5, 6, 9, 12)	4.87	7.15	2.0	1.0	3.0	−15	3, 10	3.65	11.5	1.2	0.5	4.3
+15	2, 4, (5, 6, 9, 12)	7.87	7.15	3.3	1.0	3.0	−28	3, 10	3.57	24.3	1.2	0.5	10
+28	2, 4, (5, 6, 9, 12)	21.0	7.15	5.6	1.0	2.0	−45	8	3.57	41.2	2.2	10	33
+45	7	3.57	48.7	2.2	10	39	−100	8	3.57	97.6	2.2	10	91
+75	7	3.57	78.7	2.2	10	68	−250	8	3.57	249	2.2	10	240

(1) Replace R1/R2 in figures with divider shown in Figure 16.
(2) Figures in parentheses may be used if R1/R2 divider is placed on opposite input of error amp.
(3) V^+ and V_{CC} must be connected to a +3V or greater supply.

Table 2. Formulae for Intermediate Output Voltages

Outputs from +2 to +7 volts	Outputs from +4 to +250 volts	Current Limiting
(Figure 3 Figure 7 Figure 8 Figure 9 Figure 12 Figure 15)	(Figure 10)	
$V_{OUT} = \left(V_{REF} \times \frac{R2}{R1 + R2}\right)$ (1)	$V_{OUT} = \left(\frac{V_{REF}}{2} \times \frac{R2 - R1}{R1}\right); R3 = R4$ (2)	$I_{LIMIT} = \frac{V_{SENSE}}{R_{SC}}$ (3)
Outputs from +7 to +37 volts	**Outputs from −6 to −250 volts**	**Foldback Current Limiting**
(Figure 4 Figure 7 Figure 8 Figure 9 Figure 12 Figure 15)	(Figure 5 Figure 11 Figure 13)	$I_{KNEE} = \left(\frac{V_{OUT}\,R3}{R_{SC}\,R4} + \frac{V_{SENSE}\,(R3 + R4)}{R_{SC}\,R4}\right)$
$V_{OUT} = \left(V_{REF} \times \frac{R1 + R2}{R2}\right)$ (5)	$V_{OUT} = \left(\frac{V_{REF}}{2} \times \frac{R1 + R2}{R1}\right); R3 = R4$ (6)	$I_{SHORT\ CKT} = \left(\frac{V_{SENSE}}{R_{SC}} \times \frac{R3 + R4}{R4}\right)$ (4)

Typical Applications

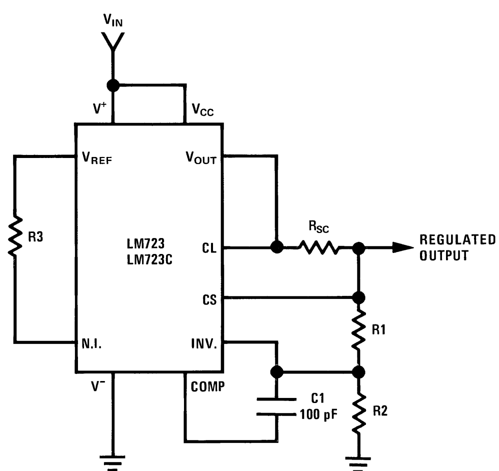


Note: $R3 = \frac{R1\,R2}{R1 + R2}$ for minimum temperature drift

Figure 3. Basic Low Voltage Regulator (V_{OUT} = 2 to 7 Volts)

Table 3. Basic Low Voltage Regulator (V_{OUT} = 2 to 7 Volts)

Typical Performance	
Regulated Output Voltage	5V
Line Regulation (ΔV_{IN} = 3V)	0.5mV
Load Regulation (ΔI_L = 50 mA)	1.5mV



Note: $R3 = \frac{R1\,R2}{R1 + R2}$ for minimum temperature drift.
R3 may be eliminated for minimum component count.

Figure 4. Basic High Voltage Regulator (V_{OUT} = 7 to 37 Volts)

Table 4. Basic High Voltage Regulator (V_{OUT} = 7 to 37 Volts)

Typical Performance	
Regulated Output Voltage	15V
Line Regulation (ΔV_{IN} = 3V)	1.5 mV

Table 4. Basic High Voltage Regulator (V_{OUT} = 7 to 37 Volts) (continued)

Typical Performance	
Load Regulation (ΔI_L = 50 mA)	4.5 mV

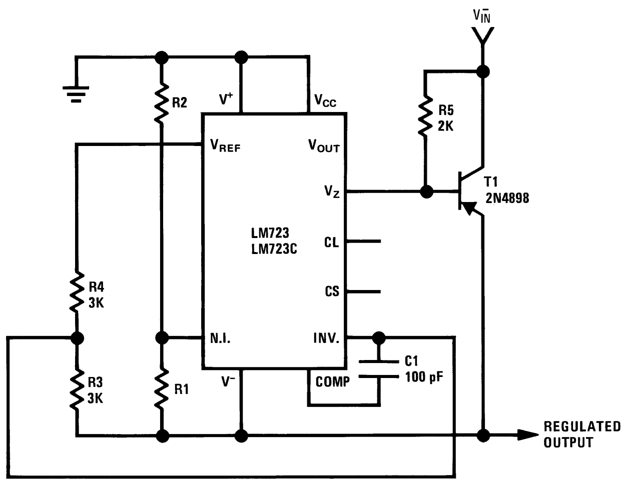


Figure 5. Negative Voltage Regulator

Table 5. Negative Voltage Regulator

Typical Performance	
Regulated Output Voltage	−15V
Line Regulation (ΔV_{IN} = 3V)	1 mV
Load Regulation (ΔI_L = 100 mA)	2 mV

Figure 6.

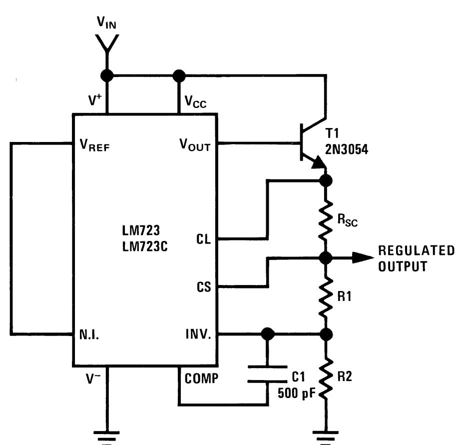


Figure 7. Positive Voltage Regulator (External NPN Pass Transistor)

Table 6. Positive Voltage Regulator (External NPN Pass Transistor)

Typical Performance	
Regulated Output Voltage	+15V
Line Regulation (ΔV_{IN} = 3V)	1.5 mV
Load Regulation (ΔI_L = 1A)	15 mV

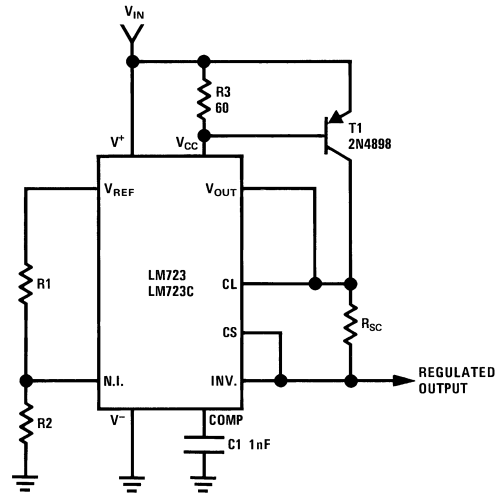


Figure 8. Positive Voltage Regulator (External PNP Pass Transistor)

Table 7. Positive Voltage Regulator (External PNP Pass Transistor)

Typical Performance	
Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 1A)	5 mV

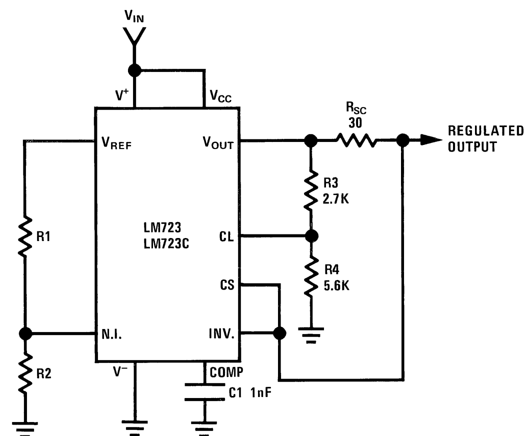


Figure 9. Foldback Current Limiting

Table 8. Foldback Current Limiting

Typical Performance	
Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 10 mA)	1 mV
Short Circuit Current	20 mA

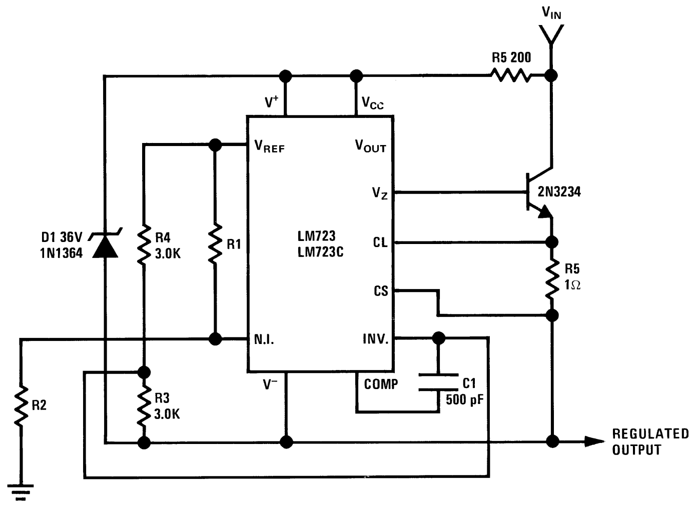


Figure 10. Positive Floating Regulator

Table 9. Positive Floating Regulator

Typical Performance	
Regulated Output Voltage	+50V
Line Regulation (ΔV_{IN} = 20V)	15 mV
Load Regulation (ΔI_L = 50 mA)	20 mV

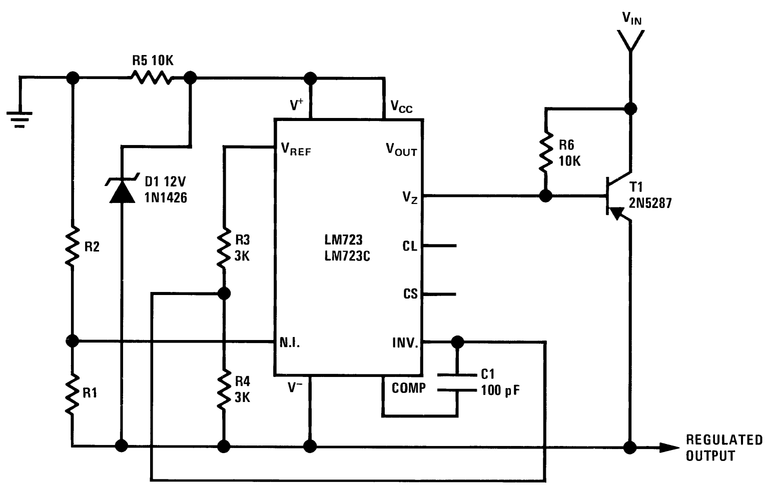


Figure 11. Negative Floating Regulator

Table 10. Negative Floating Regulator

Typical Performance	
Regulated Output Voltage	−100V
Line Regulation (ΔV_{IN} = 20V)	30 mV
Load Regulation (ΔI_L = 100 mA)	20 mV

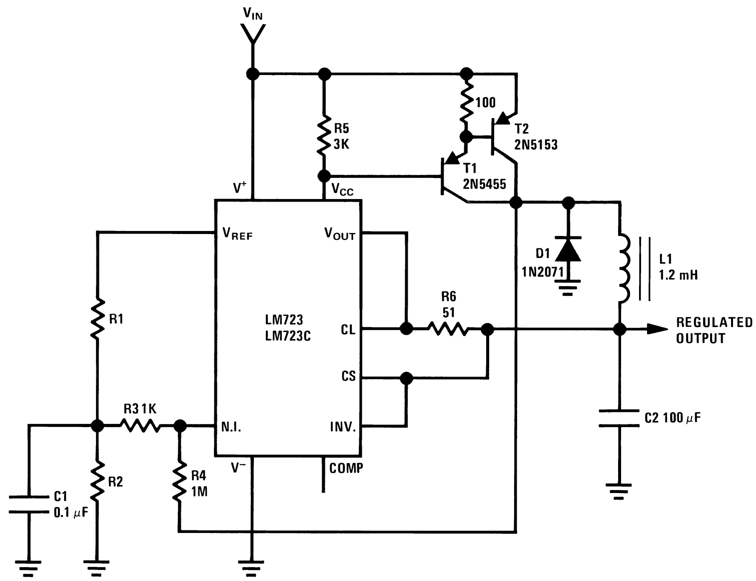


Figure 12. Positive Switching Regulator

Table 11. Positive Switching Regulator(1)

Typical Performance	
Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 30V)	10 mV
Load Regulation (ΔI_L = 2A)	80 mV

(1) L_1 is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009 in. air gap.

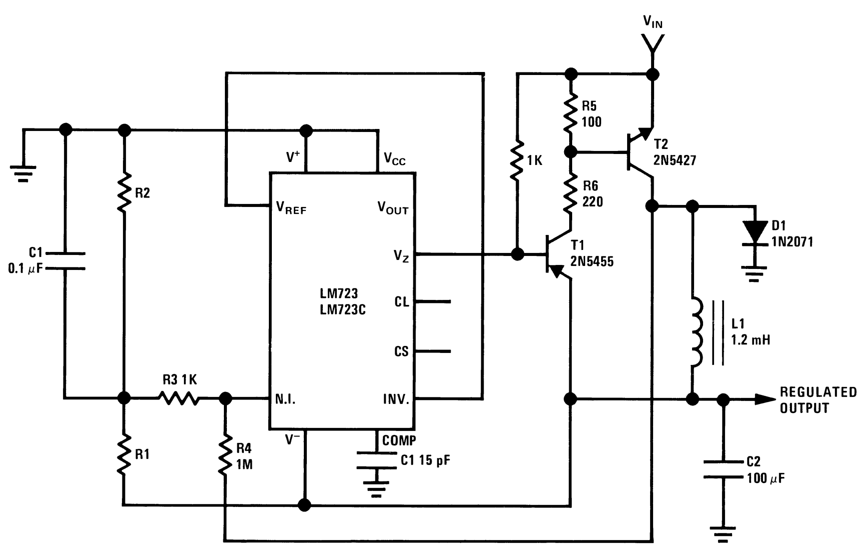


Figure 13. Negative Switching Regulator

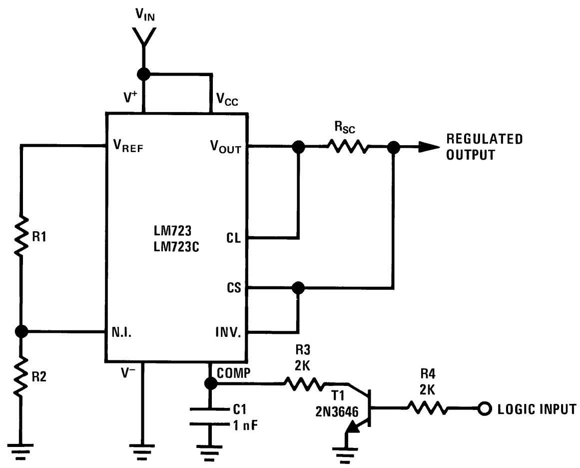
Table 12. Negative Switching Regulator(1)

Typical Performance	
Regulated Output Voltage	−15V

(1) L_1 is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009 in. air gap.

Table 12. Negative Switching Regulator[(1)] (continued)

Typical Performance	
Line Regulation (ΔV_{IN} = 20V)	8 mV
Load Regulation (ΔI_L = 2A)	6 mV



Note: Current limit transistor may be used for shutdown if current limiting is not required.

Figure 14. Remote Shutdown Regulator with Current Limiting

Table 13. Remote Shutdown Regulator with Current Limiting

Typical Performance	
Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 50 mA)	1.5 mV

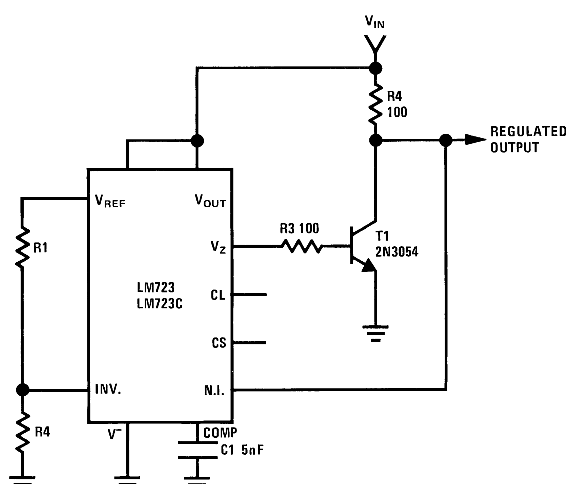
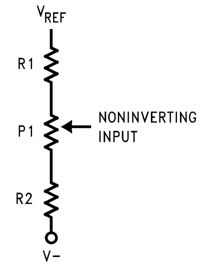


Figure 15. Shunt Regulator

Table 14. Shunt Regulator

Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 10V)	0.5 mV
Load Regulation (ΔI_L = 100 mA)	1.5 mV



NOTE: Replace R1/R2 in figures with divider shown in Figure 16

Figure 16. Output Voltage Adjust

Revision History Section

Date Released	Revision	Section	Originator	Changes
02/15/05	A	New Release, Corporate format	L. Lytle	1 MDS data sheet converted into one Corp. data sheet format. MJLM723-X, Rev. 1A0. MDS data sheet will be archived.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
JL723SCA	ACTIVE	CDIP	J	14	25	TBD	A42 SNPB	Level-1-NA-UNLIM	
JL723SIA	ACTIVE	TO-100	LME	10	20	TBD	POST-PLATE	Level-1-NA-UNLIM	
JM38510/10201SCA	ACTIVE	CDIP	J	14	25	TBD	A42 SNPB	Level-1-NA-UNLIM	
JM38510/10201SIA	ACTIVE	TO-100	LME	10	20	TBD	POST-PLATE	Level-1-NA-UNLIM	
M38510/10201SCA	ACTIVE	CDIP	J	14	25	TBD	A42 SNPB	Level-1-NA-UNLIM	
M38510/10201SIA	ACTIVE	TO-100	LME	10	20	TBD	POST-PLATE	Level-1-NA-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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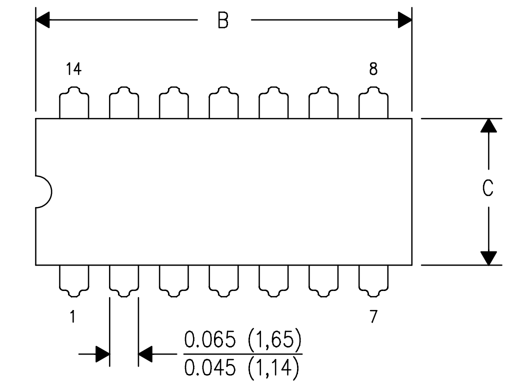
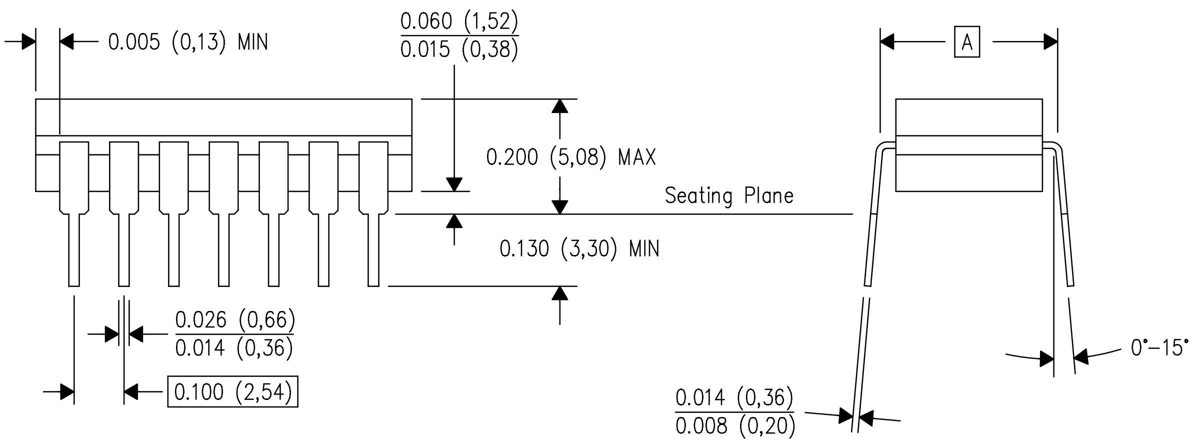
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



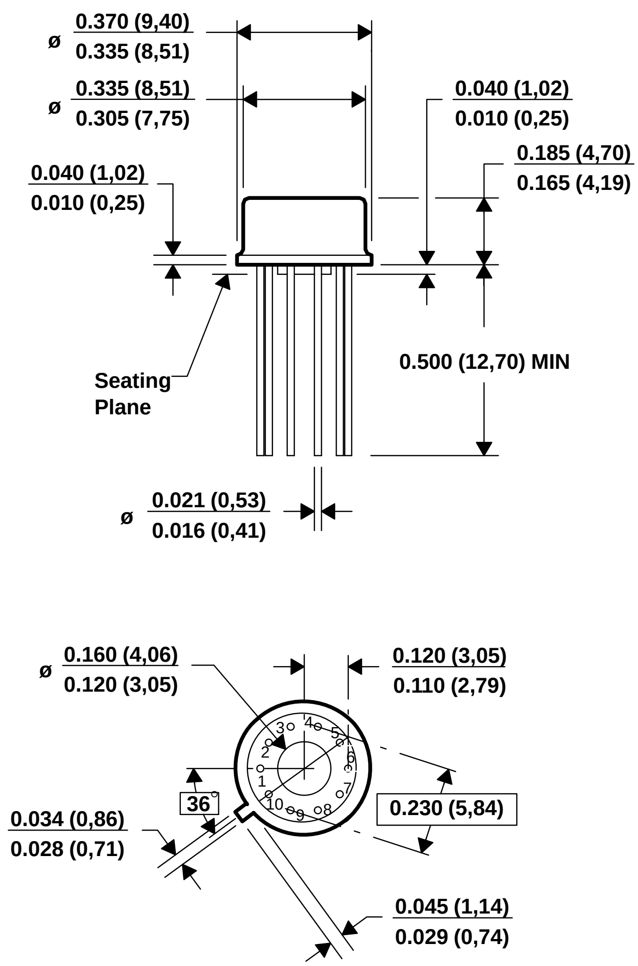
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

LME (O–MBCY–W10) **METAL CYLINDRICAL PACKAGE**



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
- D. Pin numbers shown for reference only. Numbers may not be marked on package.
- E. Falls within JEDEC MO–006/TO-100.

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