Description

The PJ9570 Series are highly precise,low noise,positive voltage LDO regulators manufactured using CMOS processes. The PJ9570 performance is optimized for battery-powered systems to deliver ultra low noise and low quiescent current. Regulator ground current increases only slightly in dropout, further prolonging the battery life. The PJ9570 Series also works with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications, critical in hand-held wireless devices. The PJ9570 Series consumes less than 1μA in shutdown mode and has fast turn-on time less than 50s. The other features include ultra low dropout voltage, high output accuracy, current limiting protection, and high ripple rejection ratio.

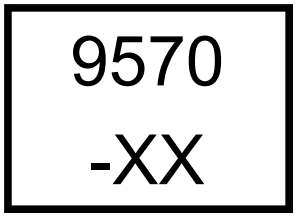
Features

- Ultra Low Noise for RF Application
- Ultra Fast Response in Line/Load Transient
- Low Power Consumption:70uA(Typ.)
- PSRR=75dB@1KHz
- Maximum Output Current: 500mA
- Low Dropout : 100mV @ 100mA at V_{OUT}=3.3V
- Operating Voltage Ranges : 2V to 6.5V
- Over Temperature and Current Limiting Protection
- Thermal Shutdown Protection

Applications

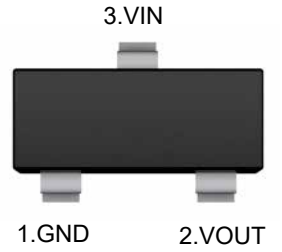
- Battery-Powered Equipment
- CDMA/GSM Cellular Handsets
- Audio/Video Equipment

Marking Code

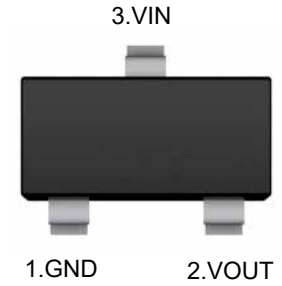


XX:Output Voltage
e.g. 3.0:3.0V 3.3:3.3V

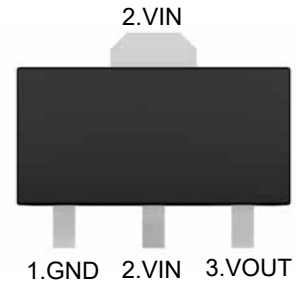
SOT-23



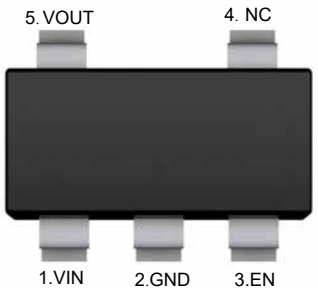
SOT-23-3



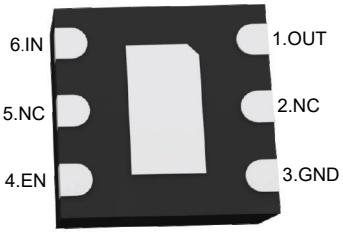
SOT-89



SOT-23-5



DFN2x2C-6L



Functional Pin Description

Pin Name	Pin Function
EN	Chip Enable (Active High). Note that this pin is high impedance
NC	NO Connected
GND	Ground
VOUT	Output Voltage
VIN	Power Input Voltage

Ordering Information

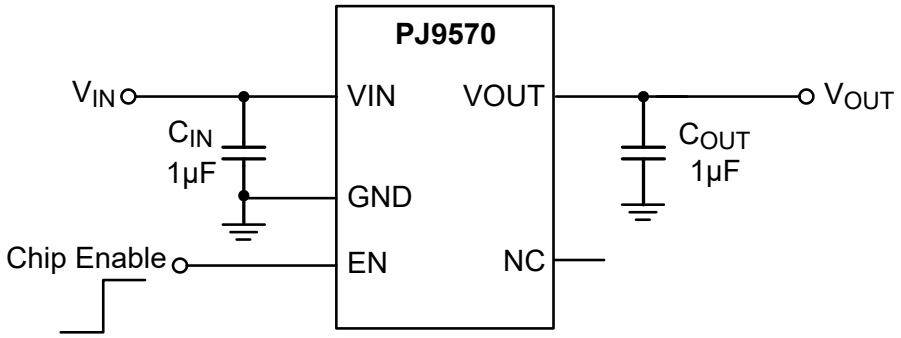
PJ9570- □□□□

Package Type
SA:SOT-23 SC:SOT-23-3
SQ:SOT-89 SE:SOT-23-5
DFC : DFN2x2C-6L

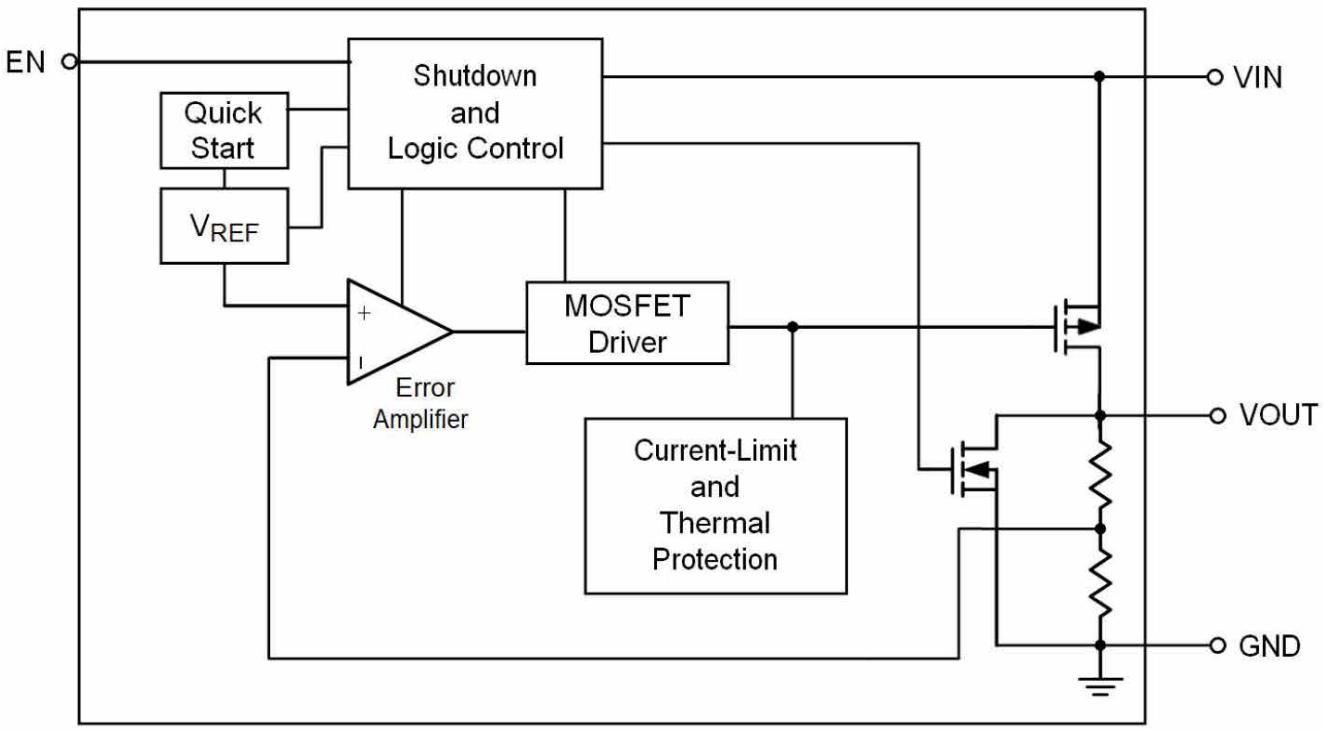
Output Voltage
12 : 1.2V 15 : 1.5V 18 : 1.8V
25 : 2.5V 28 : 2.8V 30 : 3.0V
33 : 3.3V 36 : 3.6V

Output current tap
M : 500mA

Typical Application Circuit



Function Block Diagram



Absolute Maximum Ratings Note1

Ratings at 25℃ ambient temperature unless otherwise specified.

Parameter		Value	Unit
VIN,VEN to GND Voltage	V_{IN}	-0.3 ~ +7	V
	$V_{ON/OFF}$	-0.3 ~ +0.3	V
VOUT to VIN Voltage		-0.3~VIN+0.3	V
Power Dissipation	SOT-23	300	mW
	SOT-89	400	mW
	SOT-23-3	250	mW
	SOT-23-5	250	mW
	DFN2x2C-6L	560	mW
Thermal Resistance,Junction-to-Ambient	SOT-23	330	°C/W
	SOT-89	250	°C/W
	SOT-23-3	400	°C/W
	SOT-23-5	400	°C/W
	DFN2x2C-6L	180	°C/W
Operating Ambient Temperature		-40 ~ +85	°C
Junction temperature		260	°C
Storage temperature range		-40 ~ +125	°C
ESD(HBM) Note2		4	KV
ESD(CDM) Note2		400	V

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

2. ESD testing is performed according to the respective JESD22 JEDEC standard. The human body model is a 100pF capacitor discharged through a 1.5KΩ resistor into each pin.The machine model is a 200pF capacitor discharged into each pin.

Parameter		Value	Unit
Supply Voltage		2 ~ 6.5	V
Operating Junction Temperature Range	T_J	-40 ~ +125	°C
Operating Free Air Temperature Range	T_A	-40 ~ +85	°C

Electrical Characteristics

(V_{IN}=V_{OUT}+1, V_{OUT} = 3.3V, C_{IN}=1μF, C_{OUT}=1μF, T_A=25℃ , unless otherwise noted.)

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Voltage		V_{IN}		-0.3	--	6.5	V
Output Voltage Accuracy		ΔV_{OUT}	I_{OUT}=40mA	-2	--	+2	%
Quiescent Current		I_Q	V_{IN}>V_{OUT},EN=V_{IN} I_{OUT}=0mA	--	70	--	μA
Dropout Voltage Note1		V_{DROP}	I_{OUT}=100mA	--	100	--	mV
			I_{OUT}=200mA	--	220	--	
Line Regulation		ΔV_{LINE}	V_{IN}=V_{OUT}+1 to 7V,I_{OUT}=40mA	--	0.05	--	%/V
Load Regulation		ΔV_{LOAD}	1mA<I_{OUT}<100mA	--	50	--	mV
Short circuit/start carrying current		I_{SHORT}	R_L=1Ω	--	50	--	mA
EN Leakage Current		I_{EN}		--	1	--	μA
Current Limit		I_{LIM}	V_{IN}=V_{OUT}+1	--	600	--	mA
EN Input Threshold	Logic Low	V_{IL}	V_{IN}=3V to 5.5V,Shut down	--	--	0.4	V
	Logic High	V_{IH}	V_{IN}=3V to 5.5V,Start up	1.2	--	--	
Output Noise Voltage		e_{NO}	300Hz to 50KHz, I_{OUT}=40mA	--	50	--	μV_{RMS}
Power Supply Rejection Rate		PSRR	V_{IN}=V_{OUT}+1, f=1KHz,I_{OUT}=40mA	--	75	--	dB
Output Voltage Temperature Coefficient		TC_{VOUT}	I_{OUT}=10mA	--	100	--	ppm/°C

Applications Information

Input Capacitor

A 1μF ceramic capacitor is recommended to connect between VIN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both VIN and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended minimum output capacitance is 1μF, ceramic capacitor is recommended, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to V_{OUT} and GND pins.

Enable Function

The PJ9570 has an EN pin to turn on or turn off the regulator, When the EN pin is in logic high, the regulator will be turned on. The shutdown current is almost 0μA typical. The EN pin may be directly tied to V_{IN} to keep the part on.The Enable input is CMOS logic and cannot be left floating.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula：

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / R_{\theta JA}$

Where TJ(MAX) is the maximum operation junction temperature 125 ℃, T_A is the ambient temperature and the $R_{\theta JA}$ is the junction to ambient thermal resistance.

The power dissipation definition in device is：

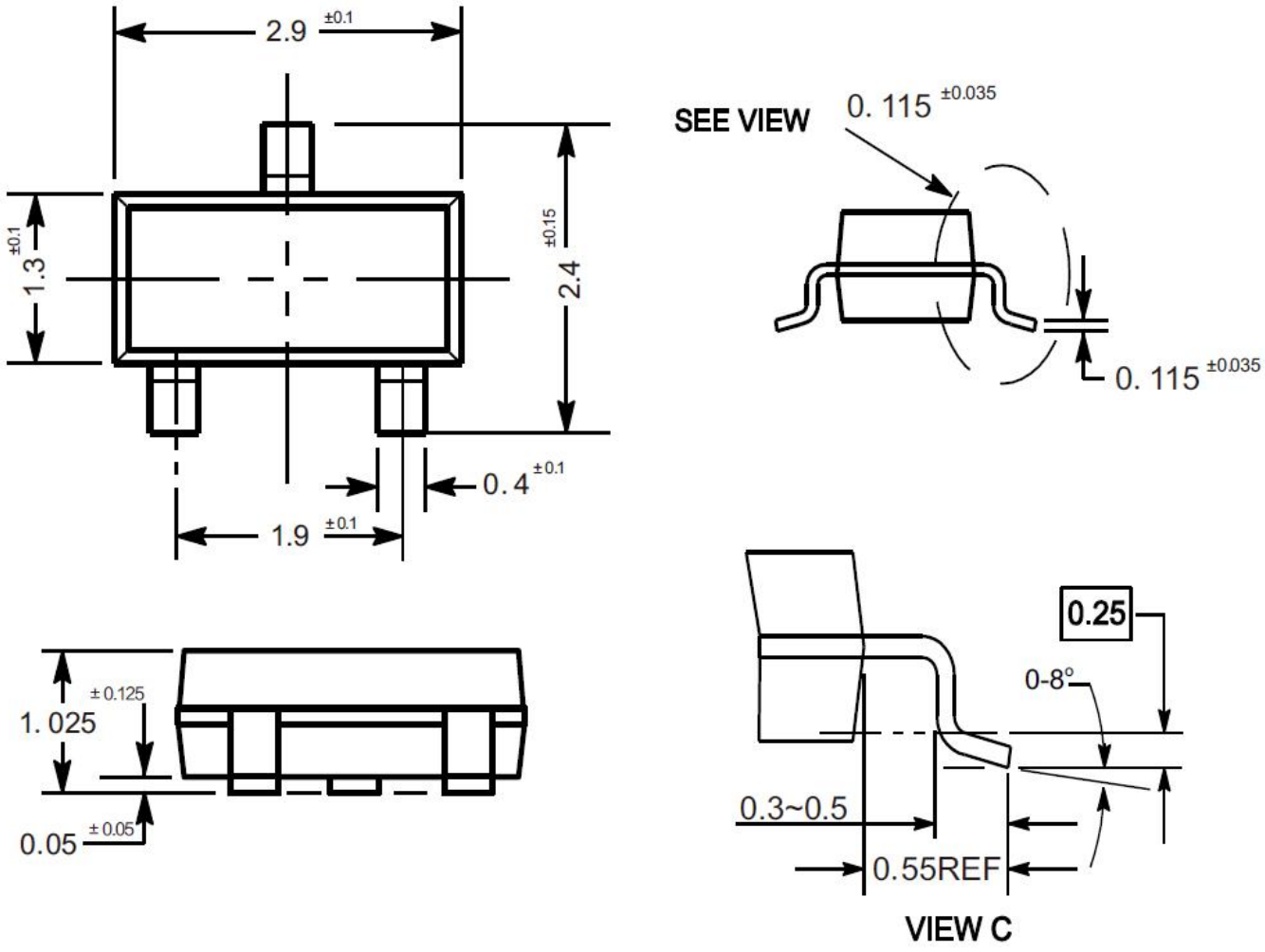
$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$

Layout Consideration

By placing input and output capacitors on the same side of the PCB as the LDO, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the PJ9570 Series ground pin using as wide and as short of a copper trace as is practical.Connections using long trace lengths, narrow trace widths, and connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.

Package Outline

SOT-23
Dimensions in mm



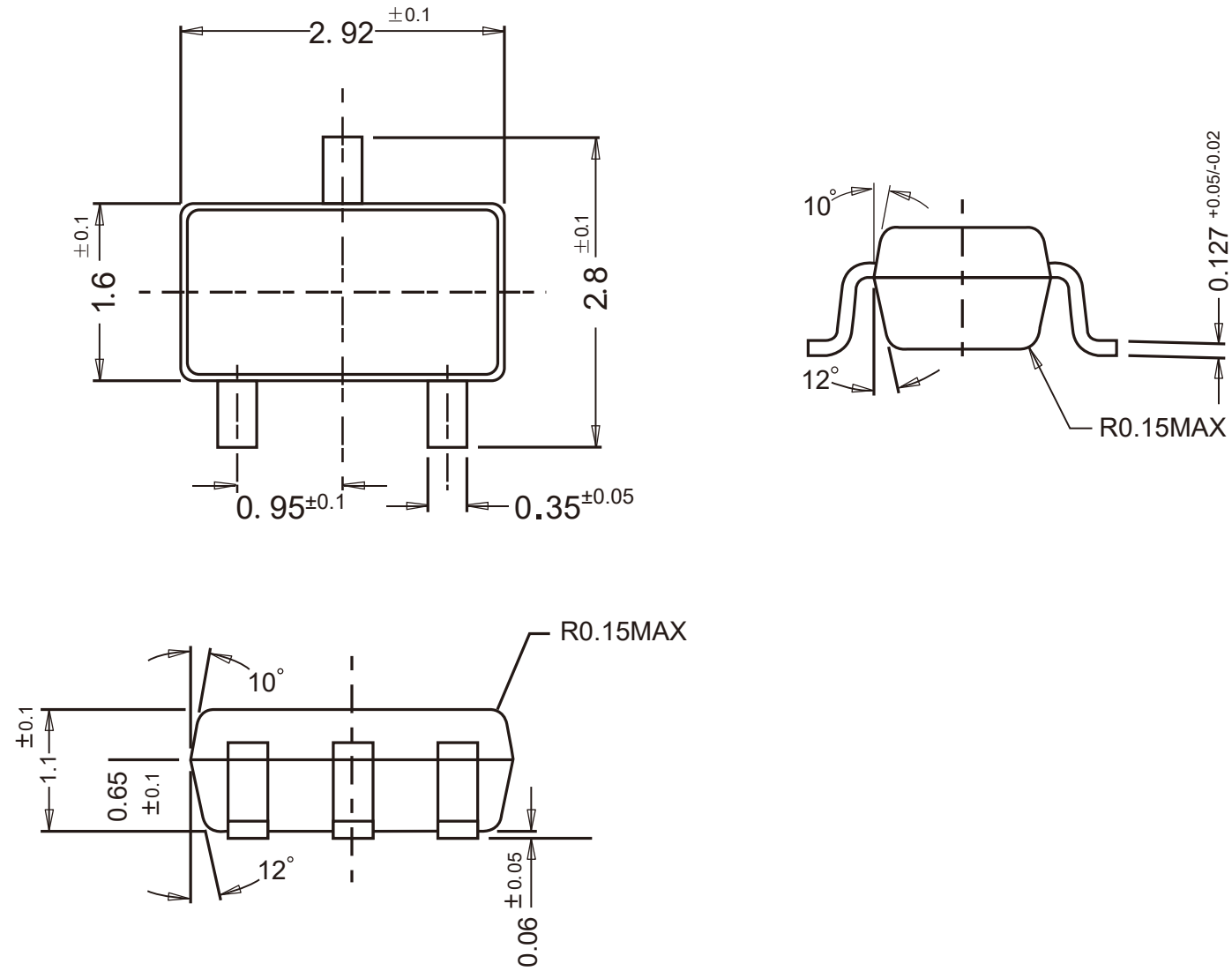
Ordering Information

Device	Package	Shipping
PJ9570 Series	SOT-23	3,000PCS/Reel&7inches

Package Outline

SOT-23-3

Dimensions in mm

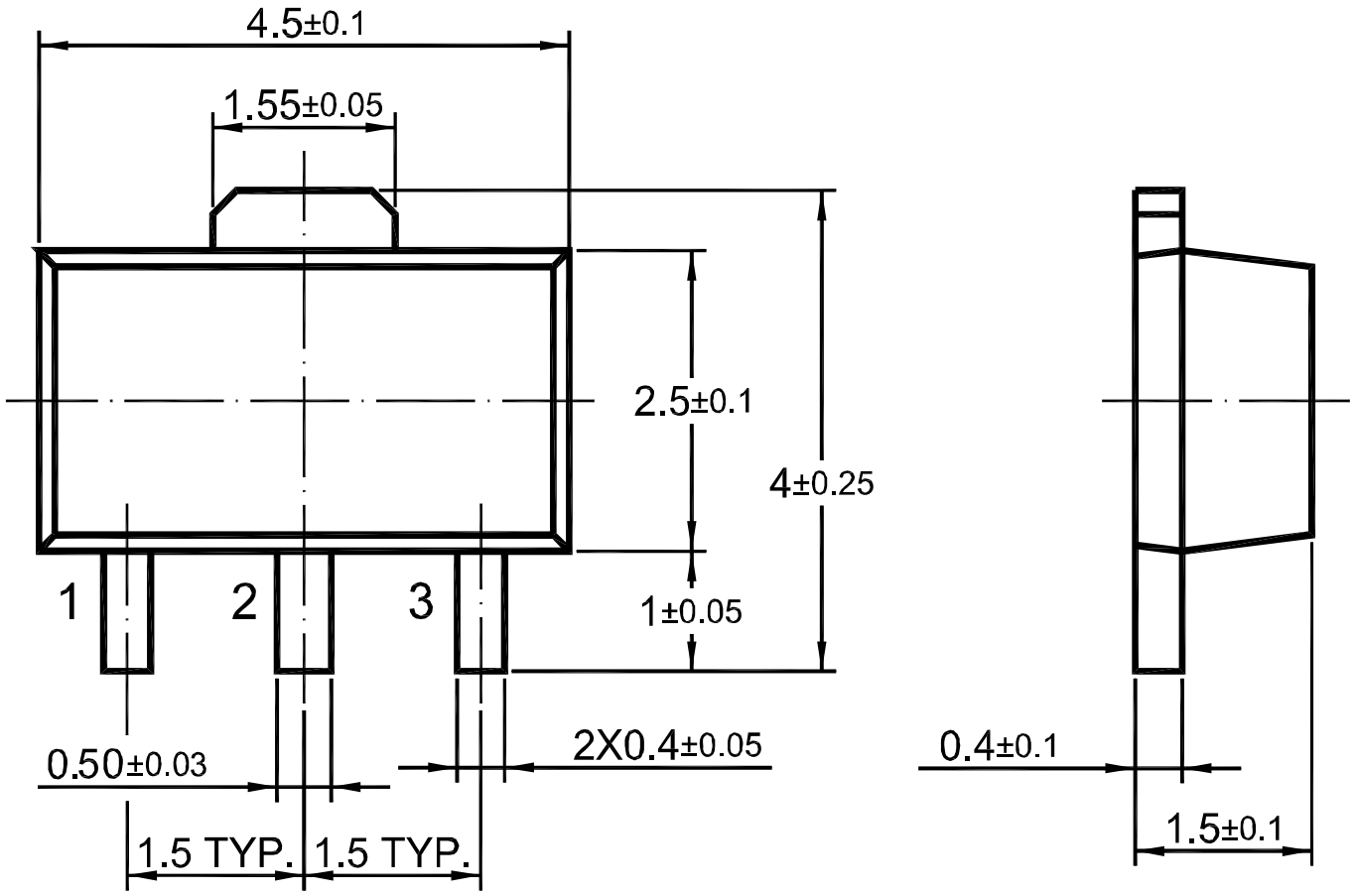


Ordering Information

Device	Package	Shipping
PJ9570 Series	SOT-23-3	3,000PCS/Reel&7inches

Package Outline

SOT-89
Dimensions in mm



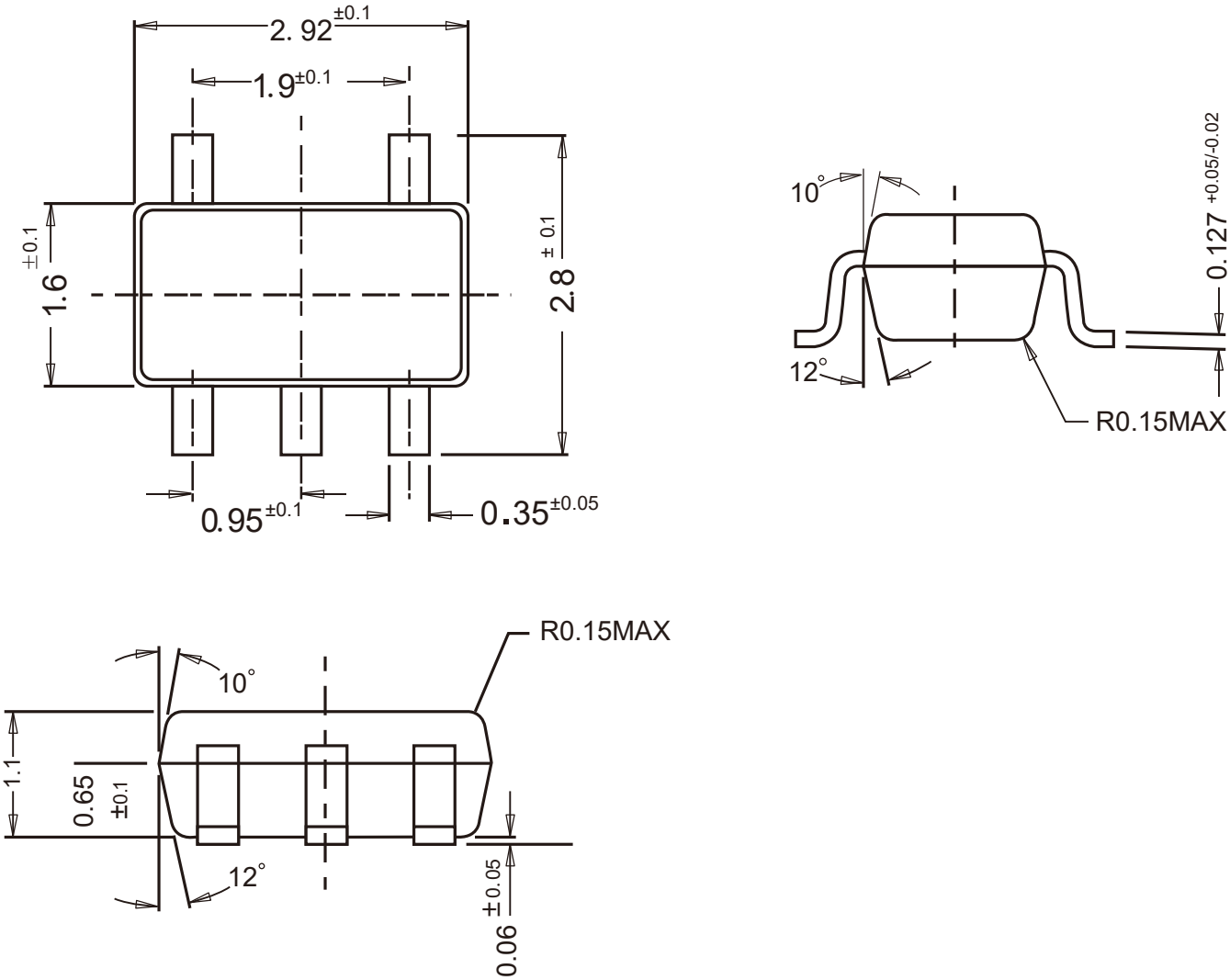
Ordering Information

Device	Package	Shipping
PJ9570 Series	SOT-89	1,000PCS/Reel&7inches
		3,000PCS/Reel&13inches

Package Outline

SOT-23-5

Dimensions in mm

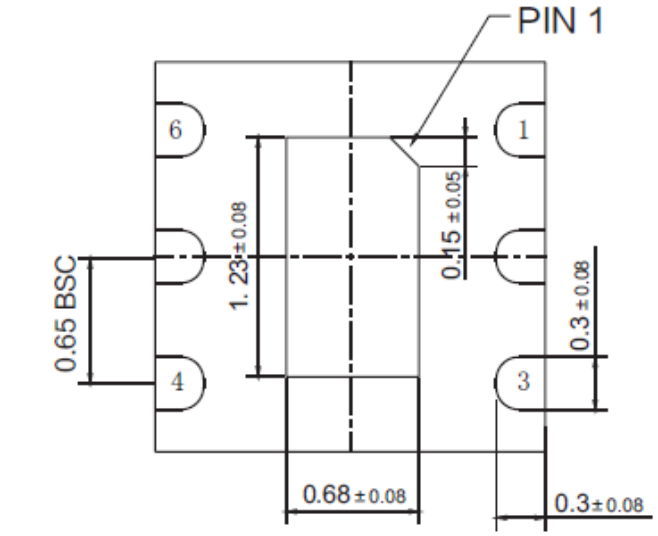


Ordering Information

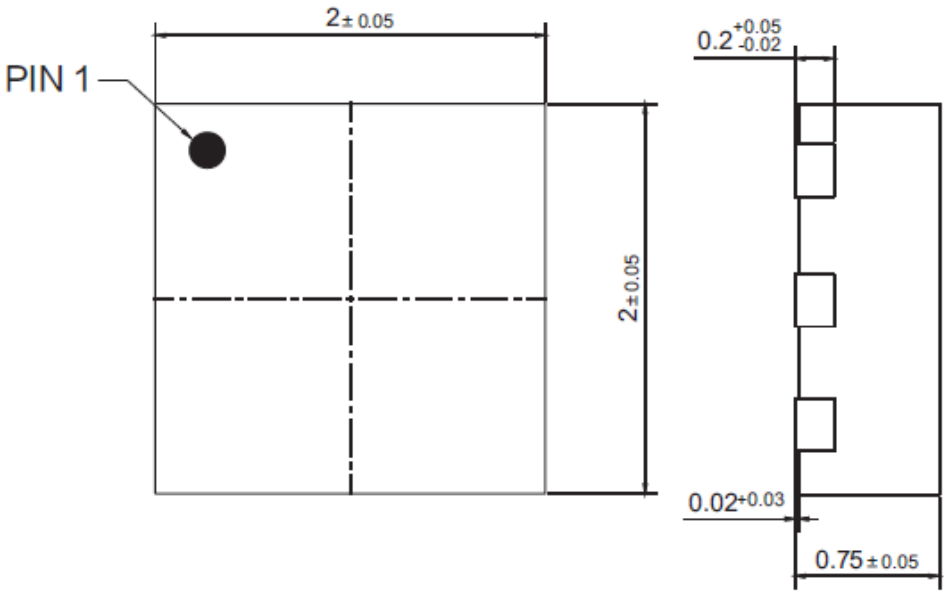
Device	Package	Shipping
PJ9570 Series	SOT-23-5	3,000PCS/Reel&7inches

Package Outline

DFN2x2-6L-0006
Dimensions in mm



BOTTOM VIEW



TOP VIEW SIDE VIEW

Ordering Information

Device	Package	Shipping
PJ9570 Series	DFN2x2C-6L	3,000PCS/Reel&7inches