

General Description

These P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

Features

-30V, -6.5A, RDS(ON) = 30mΩ@VGS = -10V

Fast switching

Green Device Available

Suit for -4.5V Gate Drive Applications

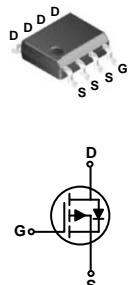
Applications

Notebook

Load Switch

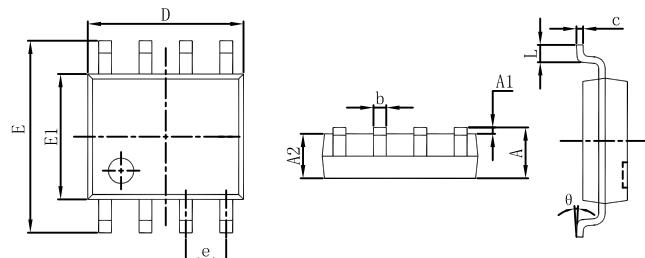
Battery Protection

Hand-held Instruments



BVDSS	RDS(ON)	ID
-30V	30mΩ	-6.5A

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Absolute Maximum Ratings Tc=25°C unless otherwise noted

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	-30	V
VGS	Gate-Source Voltage	±20	V
I _D	Drain Current – Continuous (T _C =25°C)	-6.5	A
	Drain Current – Continuous (T _C =100°C)	-5.5	A
I _{DM}	Drain Current – Pulsed ¹	-30	A
P _D	Power Dissipation (T _C =25°C)	2.1	W
	Power Dissipation – Derate above 25°C	0.017	W/°C
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction to ambient	---	60	°C/W

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Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Off Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_D=-250\mu\text{A}$	-30	---	---	V
$\Delta \text{BV}_{\text{DSS}}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=-1\text{mA}$	---	-0.03	---	$\text{V}/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{\text{DS}}=-30\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=25^\circ\text{C}$	---	---	-1	μA
		$V_{\text{DS}}=-24\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=125^\circ\text{C}$	---	---	-10	μA
I_{GSS}	Gate-Source Leakage Current	$V_{\text{GS}}=\pm 20\text{V}$, $V_{\text{DS}}=0\text{V}$	---	---	± 100	nA

On Characteristics

$R_{\text{DS}(\text{ON})}$	Static Drain-Source On-Resistance	$V_{\text{GS}}=-10\text{V}$, $I_D=-6\text{A}$	---	30	45	$\text{m}\Omega$
		$V_{\text{GS}}=-4.5\text{V}$, $I_D=-5\text{A}$	---	50	70	$\text{m}\Omega$
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{GS}}=V_{\text{DS}}$, $I_D = -250\mu\text{A}$	-1.0	-1.6	-2.5	V
			---	4	---	$\text{mV}/^\circ\text{C}$
g_{fs}	Forward Transconductance	$V_{\text{DS}}=-10\text{V}$, $I_D=-3\text{A}$	---	3.5	---	s

Dynamic and switching Characteristics

Q_g	Total Gate Charge ^{2,3}	$V_{\text{DS}}=-15\text{V}$, $V_{\text{GS}}=-4.5\text{V}$, $I_D=-3\text{A}$	---	5.1	---	nC
Q_{gs}	Gate-Source Charge ^{2,3}		---	2	---	
Q_{gd}	Gate-Drain Charge ^{2,3}		---	2.2	---	
$T_{\text{d}(\text{on})}$	Turn-On Delay Time ^{2,3}	$V_{\text{DD}}=-15\text{V}$, $V_{\text{GS}}=-10\text{V}$, $R_G=6\Omega$ $I_D=-1\text{A}$	---	3.4	---	ns
T_r	Rise Time ^{2,3}		---	10.8	---	
$T_{\text{d}(\text{off})}$	Turn-Off Delay Time ^{2,3}		---	26.9	---	
T_f	Fall Time ^{2,3}		---	6.9	---	
C_{iss}	Input Capacitance		---	1400	---	pF
C_{oss}	Output Capacitance	$V_{\text{DS}}=-10\text{V}$, $V_{\text{GS}}=0\text{V}$, $F=1\text{MHz}$	---	300	---	
C_{rss}	Reverse Transfer Capacitance		---	230	---	

Drain-Source Diode Characteristics and Maximum Ratings

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_s	Continuous Source Current	$V_G=V_D=0\text{V}$, Force Current	---	---	-6.5	A
I_{SM}	Pulsed Source Current		---	---	-13	A
V_{SD}	Diode Forward Voltage	$V_{\text{GS}}=0\text{V}$, $I_s=-1\text{A}$, $T_J=25^\circ\text{C}$	---	---	-1.2	V

RATING AND CHARACTERISTIC CURVES (AO4459)

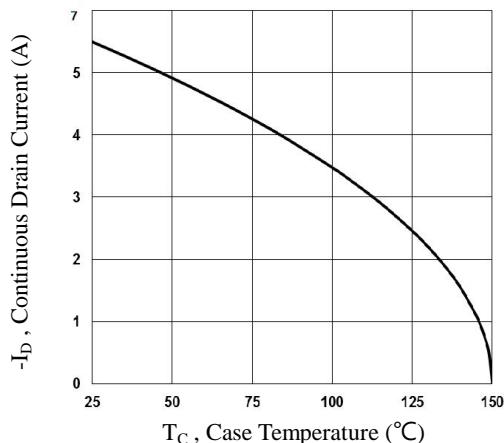


Fig.1 Continuous Drain Current vs. T_C

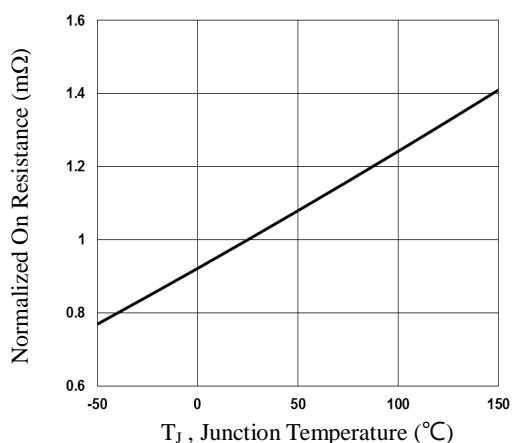


Fig.2 Normalized RDS(ON) vs. T_J

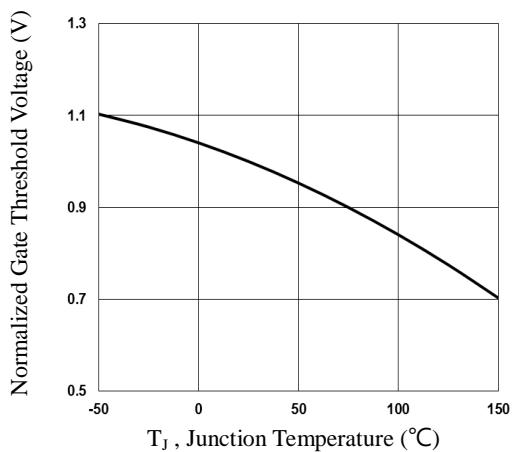


Fig.3 Normalized V_{th} vs. T_J

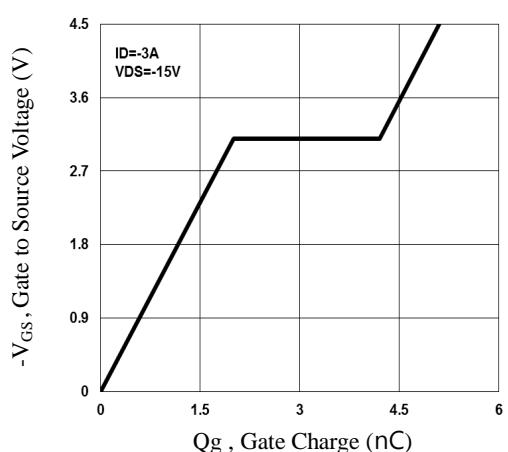


Fig.4 Gate Charge Waveform

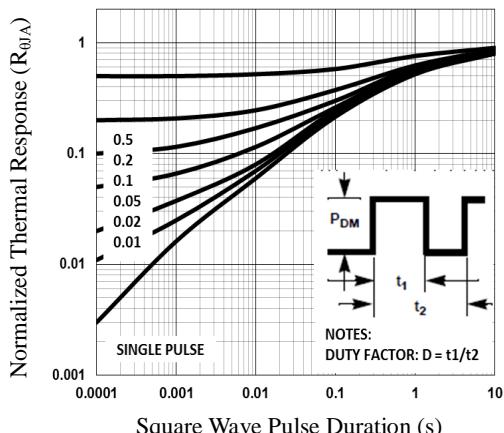


Fig.5 Normalized Transient Impedance

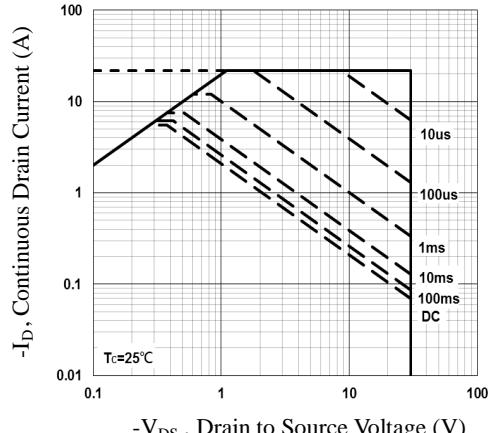


Fig.6 Maximum Safe Operation Area