LM6152/LM6154 Dual and Quad 75 MHz GBW Rail-to-Rail I/O Operational Amplifiers

1 Features

- At V_S = 5V, typical unless noted.
- Greater than Rail-to-rail Input CMVR −0.2 5V to 5.25 V
- Rail-to-rail Output Swing 0.01 V to 4.99 V
- Wide Gain-bandwidth 75 MHz @ 100 kHz
- Slew Rate
  - Small Signal 5 V/µs
  - Large Signal 45 V/µs
- Low Supply Current 1.4 mA/amplifier
- Wide Supply Range 2.7 V to 24 V
- Fast Settling Time of 1.1 µs for 2 V Step (to 0.01%)
- PSRR 91 dB
- CMRR 84 dB

2 Applications

- Portable High Speed Instrumentation
- Signal Conditioning Amplifier/ADC Buffers
- Barcode Scanners

3 Description

Using patented circuit topologies, the LM6152/LM6154 provides new levels of speed vs. power performance in applications where low voltage supplies or power limitations previously made compromise necessary. With only 1.4 mA/amplifier supply current, the 75 MHz gain bandwidth of this device supports new portable applications where higher power devices unacceptably drain battery life. The slew rate of the devices increases with increasing input differential voltage, thus allowing the device to handle capacitive loads while maintaining large signal amplitude.

The LM6152/LM6154 can be driven by voltages that exceed both power supply rails, thus eliminating concerns about exceeding the common-mode voltage range. The rail-to-rail output swing capability provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

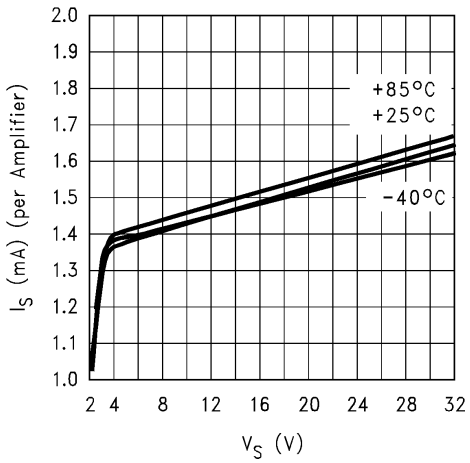
Operating on supplies from 2.7 V to over 24 V, the LM6152/LM6154 is excellent for a very wide range of applications, from battery operated systems with large bandwidth requirements to high speed instrumentation.

Device Information(1)

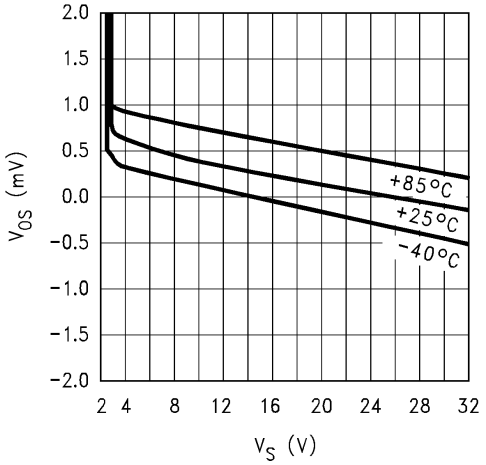
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM6152	SOIC (8)	4.902 mm × 3.912 mm
LM6154	SOIC (14)	8.636 mm × 3.912 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Supply Current vs. Supply Voltage



Offset Voltage vs. Supply voltage



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4 Revision History

Changes from Revision D (March 2013) to Revision E **Page**

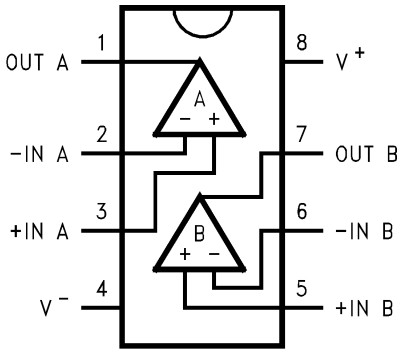
- Changed "Junction Temperature Range" to "Operating Temperature Range" and deleted "T_J" in Recommended Operating Conditions ... 4
- Deleted T_J = 25°C for Electrical Characteristics Tables ... 5

Changes from Revision C (March 2013) to Revision D **Page**

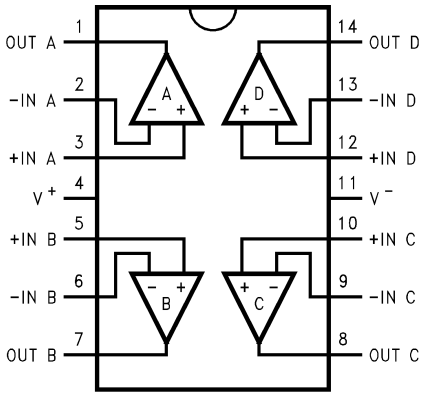
- Changed layout of National Data Sheet to TI format ... 15

5 Pin Configuration and Functions

Package D08A
8-Pin
Top View



Package D14A
14-Pin
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	LM6152	LM6154		
	D08A	D14A		
-IN A	2	2	I	ChA Inverting Input
+IN A	3	3	I	ChA Non-inverting Input
-IN B	6	6	I	ChB Inverting Input
+IN B	5	5	I	ChB Non-inverting Input
-IN C		9	I	ChC Inverting Input
+IN C		10	I	ChC Non-inverting Input
-IN D		13	I	ChD Inverting Input
+IN D		12	I	ChD Non-inverting Input
OUT A	1	1	O	ChA Output
OUT B	7	7	O	ChB Output
OUT C		8	O	ChC Output
OUT D		14	O	ChD Output
V^-	4	11	I	Negative Supply
V^+	8	4	I	Positive Supply

6 Specifications

6.1 Absolute Maximum Ratings[1][2]

	MIN	MAX	UNIT
Differential Input Voltage		±15	V
Voltage at Input/Output Pin		(V^+) + 0.3 (V^-) −0.3	V
Supply Voltage $(V^+ - V^-)$		35	V
Current at Input Pin		±10	mA
Current at Output Pin [3]		±25	mA
Current at Power Supply Pin		50	mA
Lead Temperature (soldering, 10 sec)		260	°C
Junction Temperature [4]		150	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly into a PC board.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		-65	+150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]		2500	V

(1) JEDEC document JEP155 states that 2500-V HBM allows safe manufacturing with a standard ESD control process. Human body model is 1.5 kΩ in series with 100 pF

6.3 Recommended Operating Conditions[1]

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply Voltage		$2.7 \le V^+ \le 24$	V
Operating Temperature Range, LM6152,LM6154	0	+70	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.

6.4 Thermal Information

THERMAL METRIC[1]		D08A	D14A	UNIT
		8 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193°C/W	126°C/W	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 5.0 V DC Electrical Characteristics

Unless otherwise specified, all limits are ensured for V^+ = 5.0V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	TYP(1)	LM6152AC LIMIT(2)	LM6154BC LM6152BC LIMIT(2)	UNIT
V_{OS}	Input Offset Voltage		0.54	2 **4**	5 **7**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		**10**			µV/°C
I_B	Input Bias Current	0V ≤ V_{CM} ≤ 5V	500 **750**	980 **1500**	980 **1500**	nA max
I_{OS}	Input Offset Current		32 **40**	100 **160**	100 **160**	nA max
R_{IN}	Input Resistance, CM	0V ≤ V_{CM} ≤ 4V	30			MΩ
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 4V	94	70	70	dB min
		0V ≤ V_{CM} ≤ 5V	84	60	60	
PSRR	Power Supply Rejection Ratio	5V ≤ V^+ ≤ 24V	91	80	80	dB min
V_{CM}	Input Common-Mode Voltage Range	Low	−0.25	0	0	V
		High	5.25	**5.0**	**5.0**	V
A_V	Large Signal Voltage Gain	R_L = 10 kΩ	214	50	50	V/mV min
V_O	Output Swing	R_L = 100 kΩ	0.006	0.02 **0.03**	0.02 **0.03**	V max
			4.992	4.97 **4.96**	4.97 **4.96**	V min
		R_L = 2 kΩ	0.04	0.10 **0.12**	0.10 **0.12**	V max
			4.89	4.80 **4.70**	4.80 **4.70**	V min
I_{SC}	Output Short Circuit Current	Sourcing	6.2	3 **2.5**	3 **2.5**	mA min
				27 **17**	27 **17**	mA max
		Sinking	16.9	7 **5**	7 **5**	mA min
				40	40	mA max
I_S	Supply Current	Per Amplifier	1.4	2 **2.25**	2 **2.25**	mA max

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.

6.6 5.0 V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for V^+ = 5.0V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	TYP(1)	LM6152AC LIMIT(2)	LM6154BC LM6152BC LIMIT(2)	UNIT
SR	Slew Rate	±4V Step @ V_S = ±6V, R_S < 1 kΩ	30	24 **15**	24 **15**	V/µs min
GBW	Gain-Bandwidth Product	f = 100 kHz	75			MHz
	Amp-to-Amp Isolation	R_L = 10 kΩ	125			dB
e_n	Input-Referred Voltage Noise	f = 1 kHz	9			nV/√Hz
i_n	Input-Referred Current Noise	f = 1 kHz	0.34			pA/√Hz
T.H.D	Total Harmonic Distortion	f = 100 kHz, R_L = 10 kΩ A_V = −1, V_O = 2.5 V_{PP}	−65			dBc
ts	Settling Time	2V Step to 0.01%	1.1			µs

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.

6.7 2.7 V DC Electrical Characteristics

Unless otherwise specified, all limits are ensured for V^+ = 2.7V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	TYP(1)	LM6152AC LIMIT(2)	LM6154BC LM6152BC LIMIT(2)	UNIT
V_{OS}	Input Offset Voltage		0.8	2 **5**	5 **8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		**10**			µV/°C
I_B	Input Bias Current		500			nA
I_{OS}	Input Offset Current		50			nA
R_{IN}	Input Resistance, CM	0V ≤ V_{CM} ≤ 1.8V	30			MΩ
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.8V	88			dB
		0V ≤ V_{CM} ≤ 2.7V	78			
PSRR	Power Supply Rejection Ratio	3V ≤ V^+ ≤ 5V	69			dB
V_{CM}	Input Common-Mode Voltage Range	Low	−0.25	0	0	V
		High	2.95	2.7	2.7	V
A_V	Large Signal Voltage Gain	R_L = 10 kΩ	5.5			V/mV
V_O	Output Swing	R_L = 10 kΩ	0.032	0.07 **0.11**	0.07 **0.11**	V max
			2.68	2.64 **2.62**	2.64 **2.62**	V min
I_S	Supply Current	Per Amplifier	1.35			mA

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.

6.8 2.7 V AC Electrical Characteristics

Unless otherwise specified, all limits are ensured for V^+ = 2.7V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	TYP(1)	LM6152AC LIMIT(2)	LM6154BC LM6152BC LIMIT(2)	UNIT
GBW	Gain-Bandwidth Product	f = 100 kHz	80			MHz

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.

6.9 24 V DC Electrical Characteristics

Unless otherwise specified, all limits are ensured for V^+ = 24V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	TYP(1)	LM6152AC LIMIT(2)	LM6154BC LM6152BC LIMIT(2)	UNIT
V_{OS}	Input Offset Voltage		0.3	2 **4**	7 **9**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		**10**			µV/°C
I_B	Input Bias Current		500			nA
I_{OS}	Input Offset Current		32			nA
R_{IN}	Input Resistance, CM	0V ≤ V_{CM} ≤ 23V	60			Meg Ω
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 23V	94			dB
		0V ≤ V_{CM} ≤ 24V	84			
PSRR	Power Supply Rejection Ratio	0V ≤ V_{CM} ≤ 24V	95			dB
V_{CM}	Input Common-Mode Voltage Range	Low	−0.25	0	0	V
		High	24.25	24	24	V
A_V	Large Signal Voltage Gain	R_L = 10 kΩ	55			V/mV
V_O	Output Swing	R_L = 10 kΩ	0.044	0.075 **0.090**	0.075 **0.090**	V max
			23.91	23.8 **23.7**	23.8 **23.7**	V min
I_S	Supply Current	Per Amplifier	1.6	2.25 **2.50**	2.25 **2.50**	mA max

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.

6.10 24 V AC Electrical Characteristics

Unless otherwise specified, all limits are ensured for V^+ = 24V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	TYP(1)	LM6152AC LIMIT(2)	LM6154BC LM6152BC LIMIT(2)	UNIT
GBW	Gain-Bandwidth Product	f = 100 kHz	80			MHz

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.

6.11 Typical Performance Characteristics

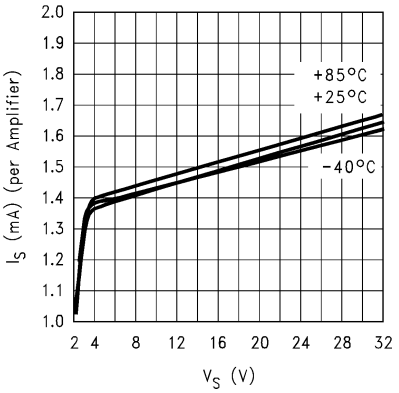


Figure 1. Supply Current vs. Supply Voltage

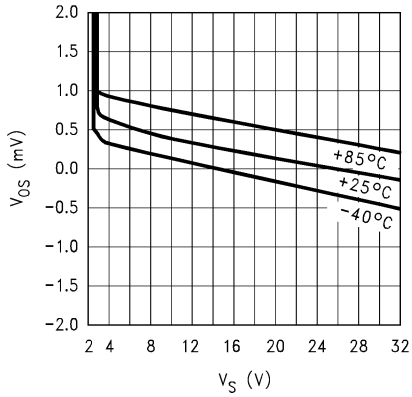


Figure 2. Offset Voltage vs. Supply voltage

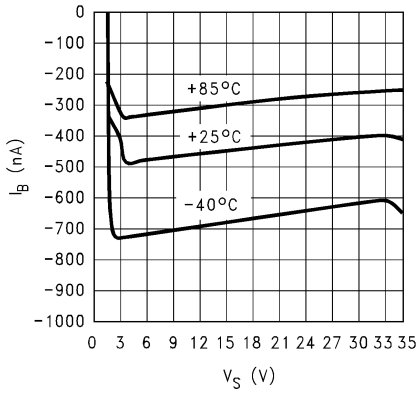


Figure 3. Bias Current vs. Supply voltage

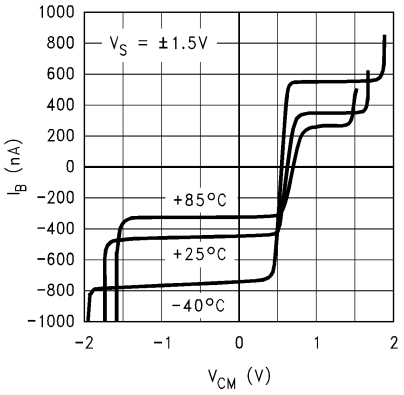


Figure 4. Bias Current vs. V_{CM}

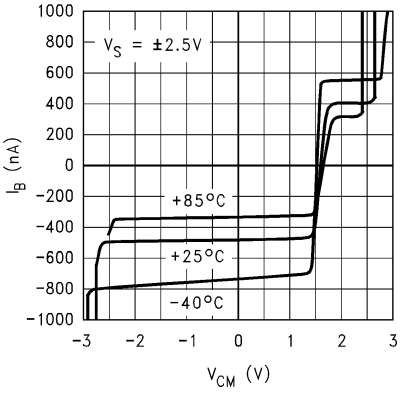


Figure 5. Bias Current vs. V_{CM}

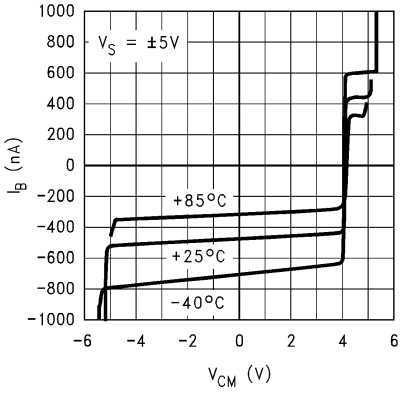


Figure 6. Bias Current vs. V_{CM}

Typical Performance Characteristics (continued)

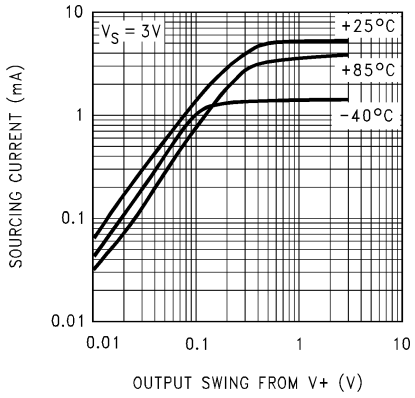


Figure 7. Output Voltage vs. Source Current

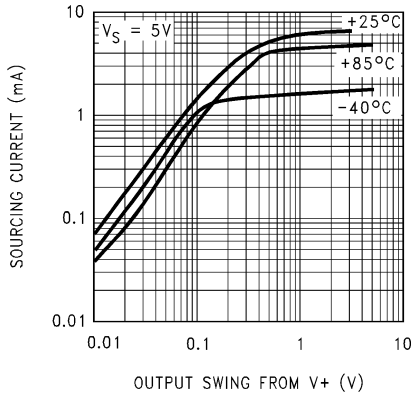


Figure 8. Output Voltage vs. Source Current

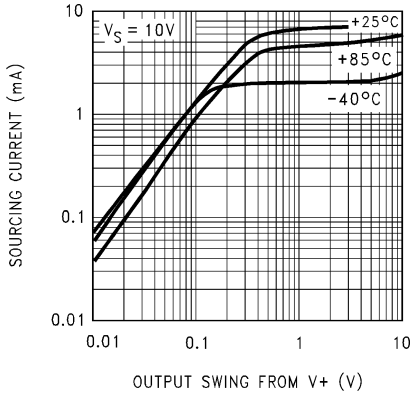


Figure 9. Output Voltage vs. Source Current

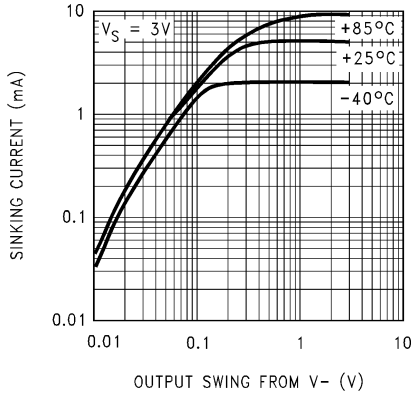


Figure 10. Output Voltage vs. Sink Current

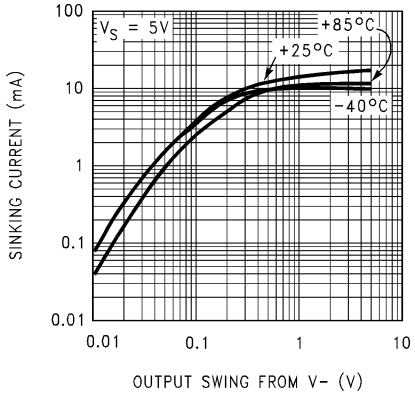


Figure 11. Output Voltage vs. Sink Current

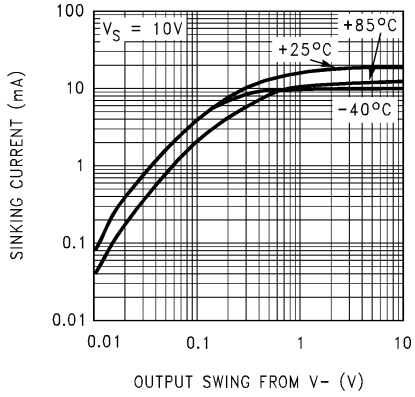


Figure 12. Output Voltage vs. Sink Current

Typical Performance Characteristics (continued)

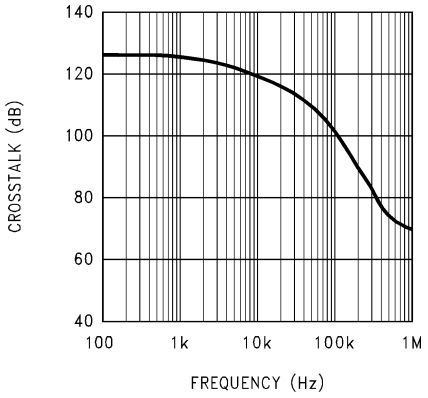


Figure 13. Crosstalk (dB) vs. Frequency

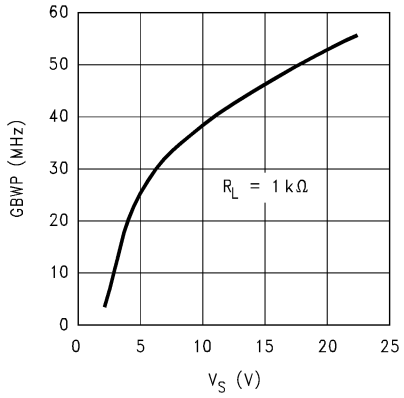


Figure 14. GBWP (@ 100 kHz) vs. Supply Voltage

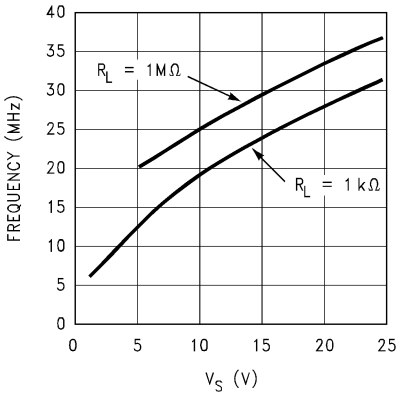


Figure 15. Unity Gain Frequency vs. Supply Voltage for Various Loads

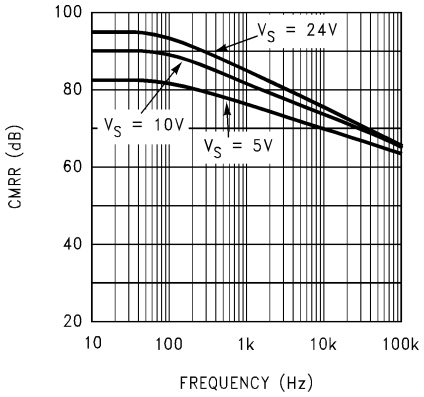


Figure 16. CMRR

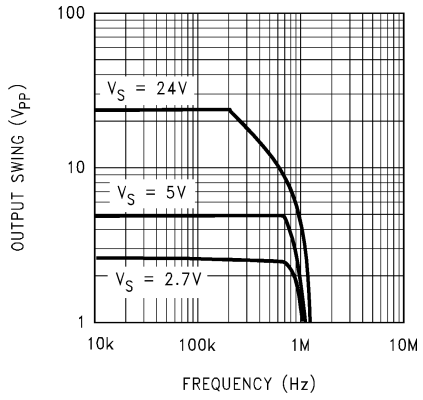


Figure 17. Voltage Swing vs. Frequency (C_L = 100 pF)

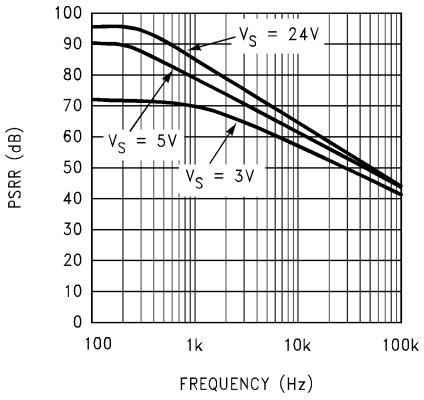


Figure 18. PSRR vs. Frequency

Typical Performance Characteristics (continued)

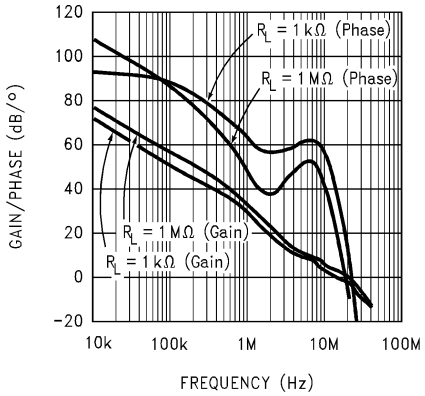


Figure 19. Open Loop Gain/Phase (V_S = 5V)

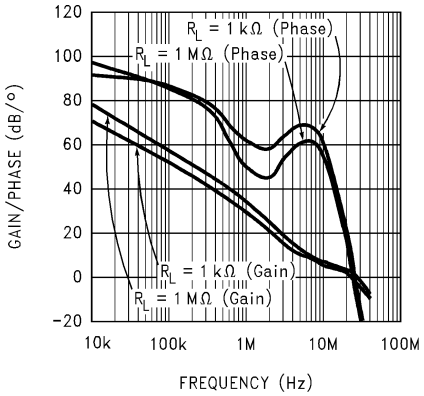


Figure 20. Open Loop Gain/Phase (V_S = 10V)

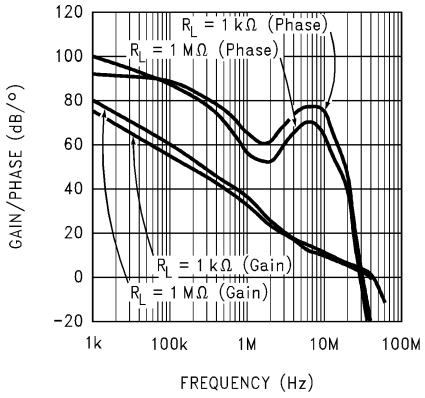


Figure 21. Open Loop Gain/Phase (V_S = 24V)

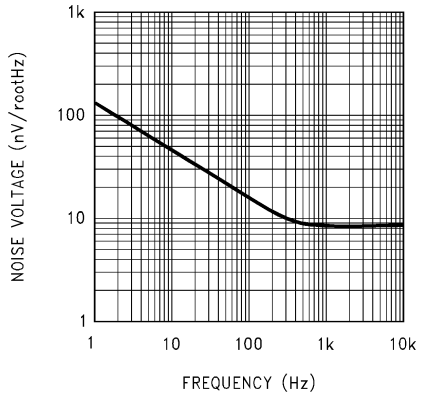


Figure 22. Noise Voltage vs. Frequency

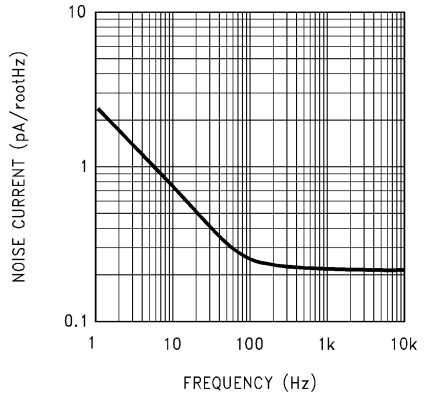


Figure 23. Noise Current vs. Frequency

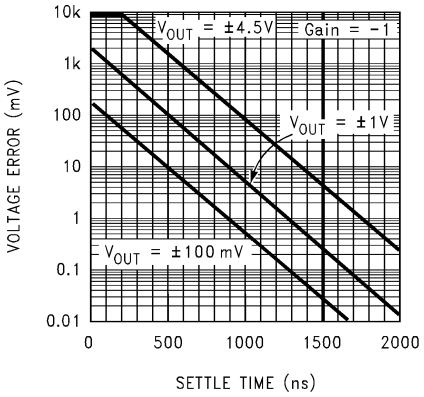


Figure 24. Voltage Error vs. Settle Time

Typical Performance Characteristics (continued)

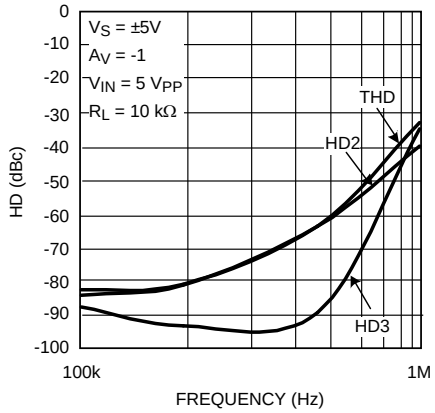


Figure 25. Distortion vs. Frequency

7 Application and Implementation

The LM6152/LM6154 is ideally suited for operation with about 10 kΩ (Feedback Resistor, R_F) between the output and the negative input terminal.

With R_F set to this value, for most applications requiring a close loop gain of 10 or less, an additional small compensation capacitor (C_F) (see Figure 26) is recommended across R_F in order to achieve a reasonable overshoot (10%) at the output by compensating for stray capacitance across the inputs.

The optimum value for C_F can best be established experimentally with a trimmer cap in place since its value is dependant on the supply voltage, output driving load, and the operating gain. Below, some typical values used in an inverting configuration and driving a 10 kΩ load have been tabulated for reference:

Table 1. Typical BW (−3 dB) at Various Supply Voltage and Gains

V_S Volts	GAIN	C_F pF	BW (−3 dB) MHz
3	−1	5.6	4
	−10	6.8	1.97
	−100	None	0.797
24	−1	2.2	6.6
	−10	4.7	2.2
	−100	None	0.962

In the non-inverting configuration, the LM6152/LM6154 can be used for closed loop gains of +2 and above. In this case, also, the compensation capacitor (C_F) is recommended across R_F (= 10 kΩ) for gains of 10 or less.

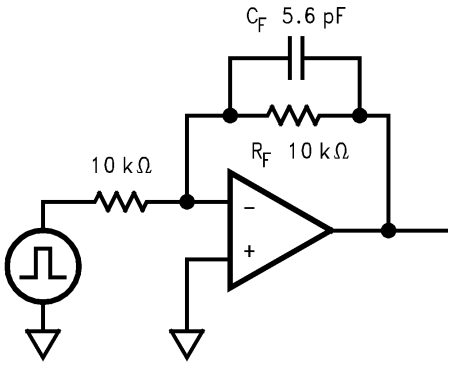


Figure 26. Typical Inverting Gain Circuit A_V = −1

Because of the unique structure of this amplifier, when used at low closed loop gains, the realizable BW will be much less than the GBW product would suggest.

The LM6152/LM6154 brings a new level of ease of use to op amp system design.

The greater than rail-to-rail input voltage range eliminates concern over exceeding the common-mode voltage range. The rail-to-rail output swing provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The high gain-bandwidth with low supply current opens new battery powered applications where higher power consumption previously reduced battery life to unacceptable levels.

The ability to drive large capacitive loads without oscillating functional removes this common problem.

To take advantage of these features, some ideas should be kept in mind.

The LM6152/LM6154, capacitive loads do not lead to oscillations, in all but the most extreme conditions, but they will result in reduced bandwidth. They also cause increased settling time.

Unlike most bipolar op amps, the unique phase reversal prevention/speed-up circuit in the input stage, causes the slew rate to be very much a function of the input pulse amplitude. This results in a 10 to 1 increase in slew rate when the differential input signal increases. Large fast pulses will raise the slew-rate to more than 30 V/µs.

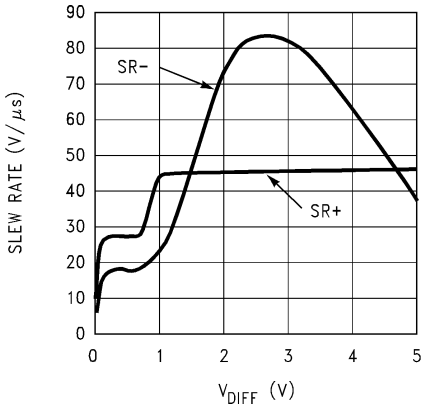


Figure 27. Slew Rate vs. V_{DIFF}

The speed-up action adds stability to the system when driving large capacitive loads.

A conventional op amp exhibits a fixed maximum slew-rate even though the differential input voltage rises due to the lagging output voltage. In the LM6152/LM6154, increasing lag causes the differential input voltage to increase but as it does, the increased slew-rate keeps the output following the input much better. This effectively reduces phase lag. As a result, the LM6152/LM6154 can drive capacitive loads as large as 470 pF at gain of 2 and above, and not oscillate.

Capacitive loads decrease the phase margin of all op amps. This can lead to overshoot, ringing and oscillation. This is caused by the output resistance of the amplifier and the load capacitance forming an R-C phase shift network. The LM6152/6154 senses this phase shift and partly compensates for this effect.

8 Device and Documentation Support

8.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM6152	Click here	Click here	Click here	Click here	Click here
LM6154	Click here	Click here	Click here	Click here	Click here

8.2 Trademarks

All trademarks are the property of their respective owners.

8.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

8.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM6152ACM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	LM61 52ACM	
LM6152ACM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM61 52ACM	Samples
LM6152ACMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM61 52ACM	Samples
LM6152BCM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM61 52BCM	Samples
LM6152BCMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM61 52BCM	Samples
LM6154BCM	NRND	SOIC	D	14	55	TBD	Call TI	Call TI	0 to 70	LM6154BCM	
LM6154BCM/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM6154BCM	Samples
LM6154BCMX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM6154BCM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

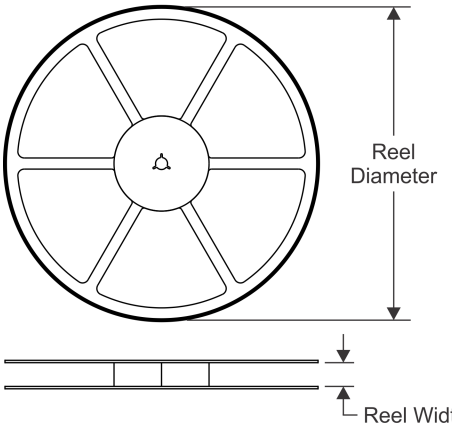
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

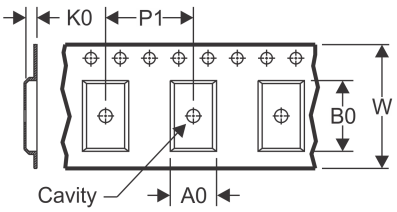
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

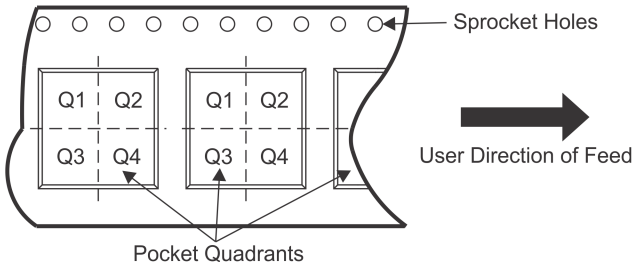


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

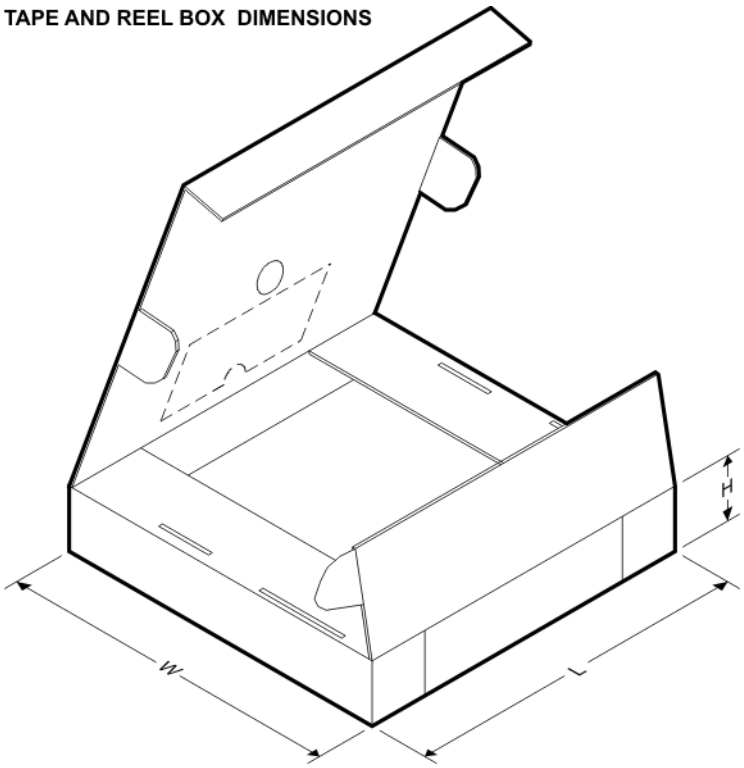
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM6152ACMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM6152BCMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM6154BCMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

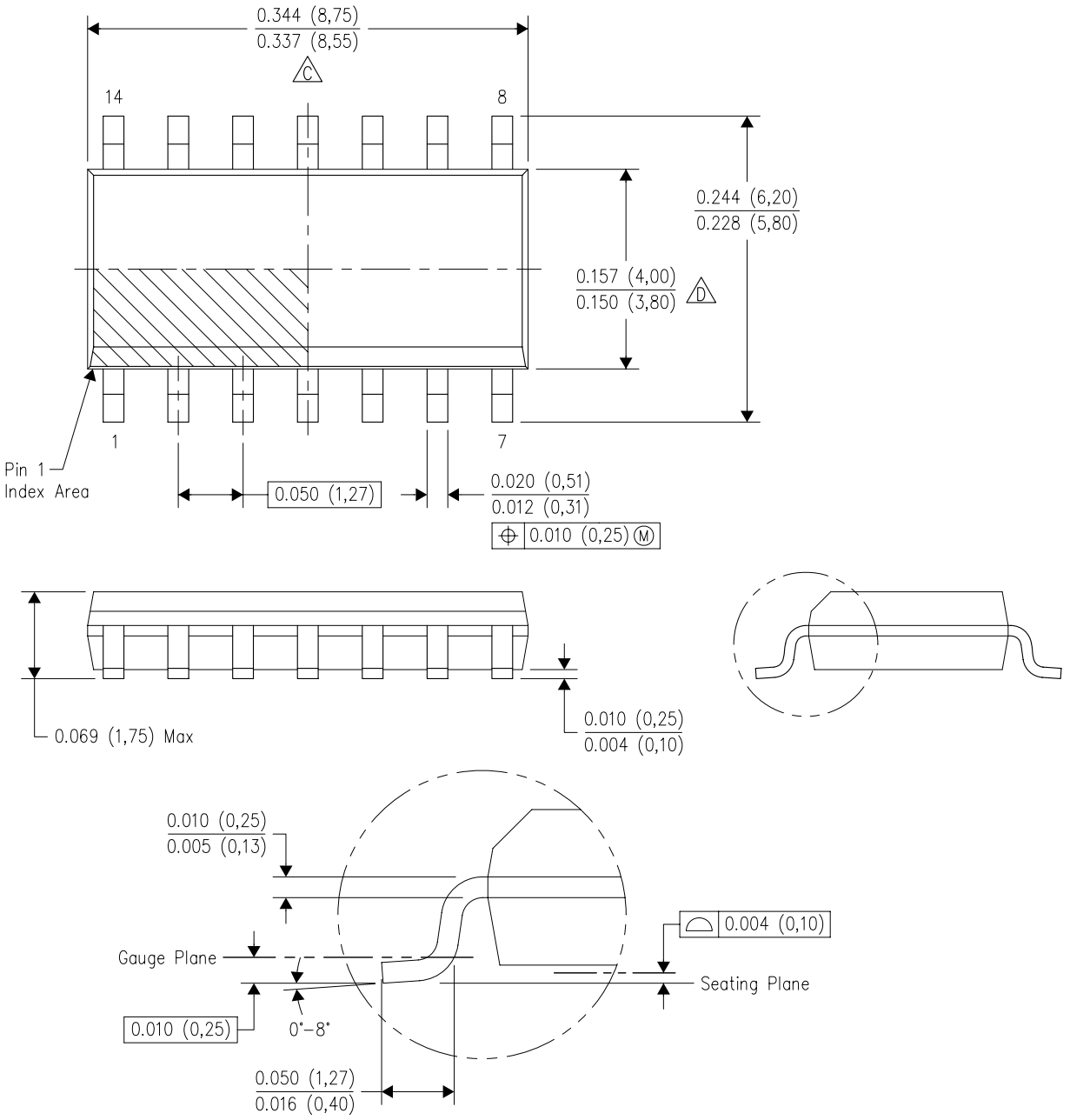
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM6152ACMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM6152BCMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM6154BCMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

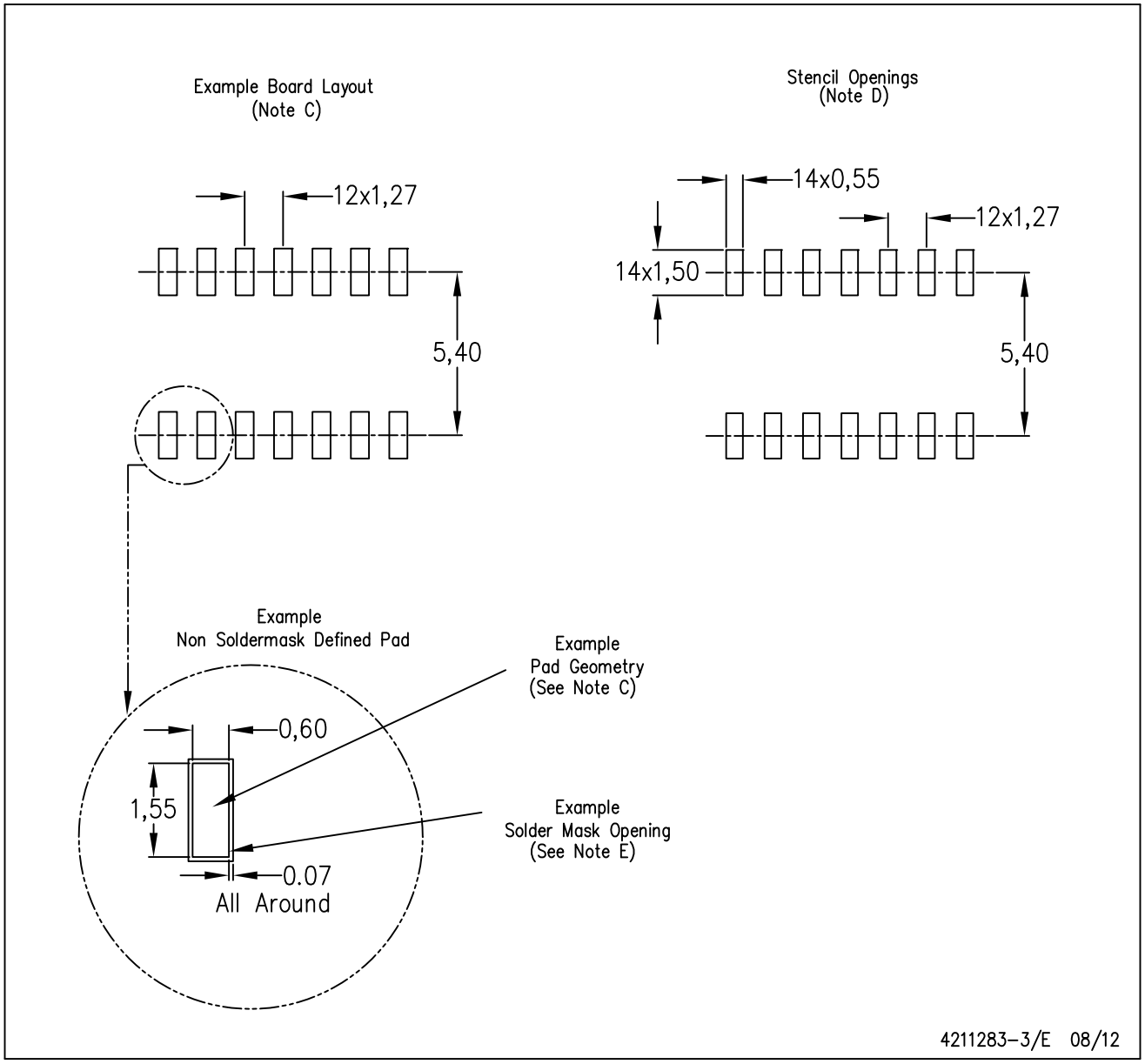
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



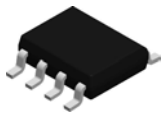
4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

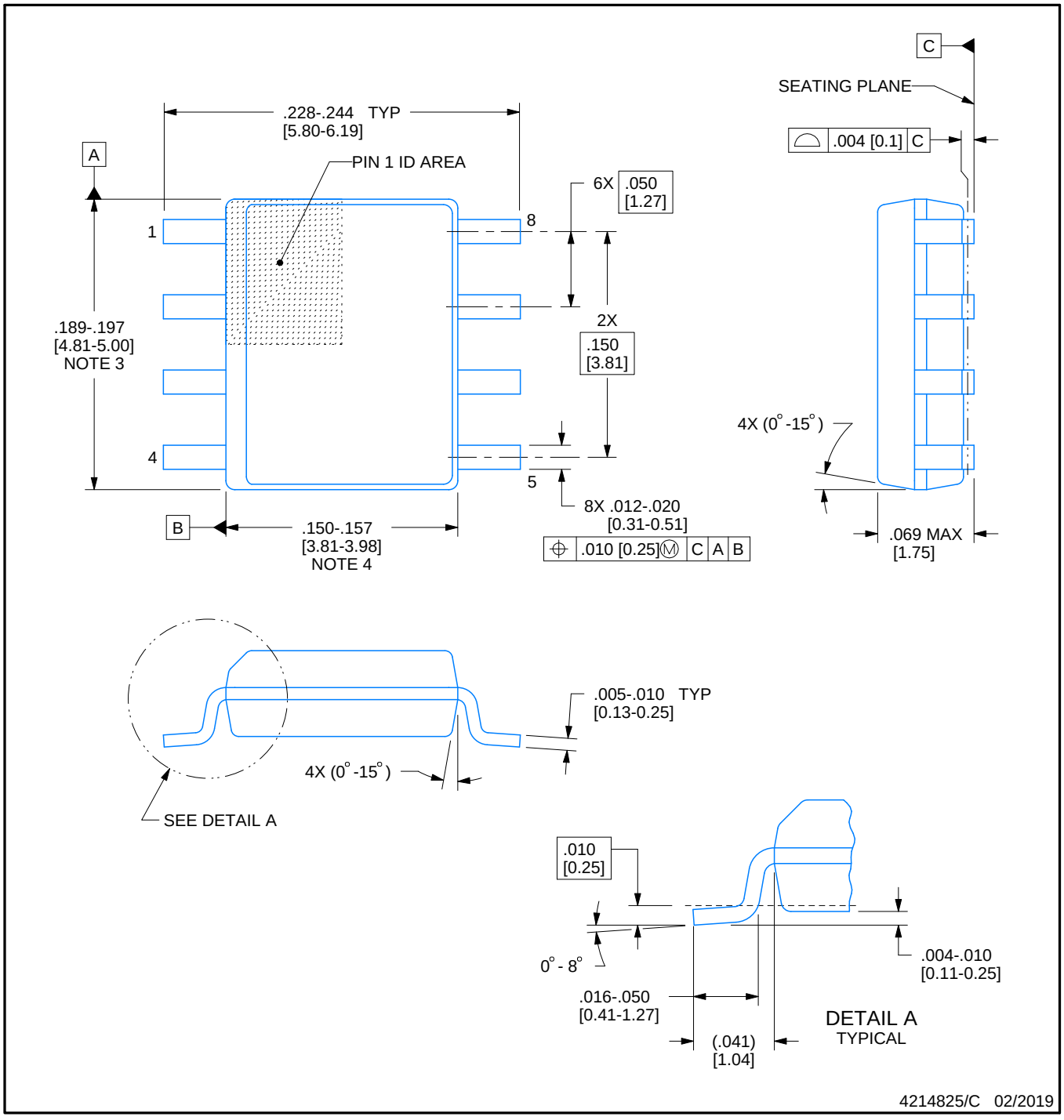


PACKAGE OUTLINE

D0008A

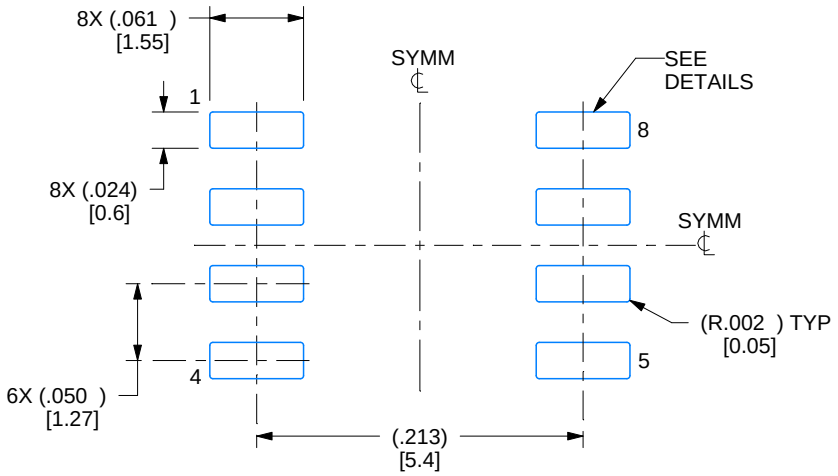
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

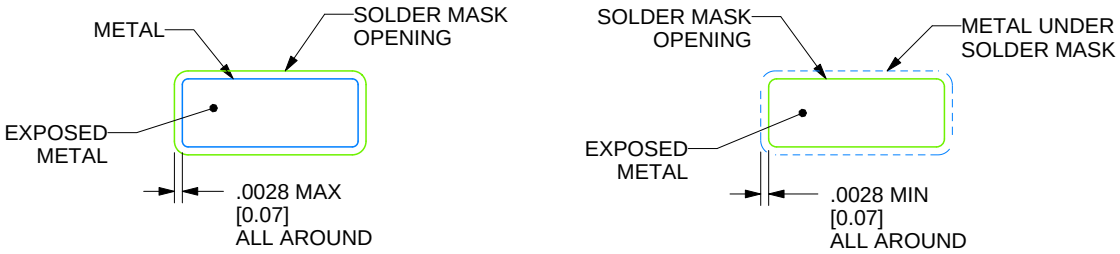


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

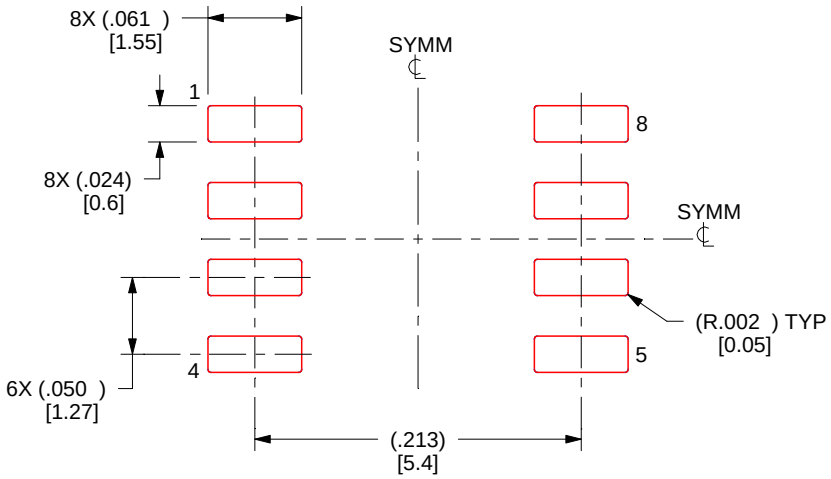
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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