



JM38510/11301/11302

JAN 8-BIT MULTIPLYING
D/A CONVERTERS

Precision Monolithics Inc.

T-51-09-08

GENERAL DESCRIPTION

This data sheet covers the electrical requirements of the monolithic 8-bit digital-to-analog converters found in MIL-M-38510/113. Devices supplied to this data sheet are manufactured and tested at PMI's MIL-M-38510 certified facility and are listed in QPL-38510.

Complete device requirements will be found in MIL-M-38510 and MIL-M-38510/113 for Class B and Class S processed devices.

Device Types shall be as follows:

- 01 D/A Converter, 8 bit, 0.19% linearity
- 02 D/A Converter, 8 bit, 0.10% linearity

GENERIC CROSS-REFERENCE INFORMATION

This cross-reference information is presented for the convenience of the user. The Generic-Industry types listed may not have identical operational performance characteristics across the military temperature range or reliability factors equivalent to the MIL-M-38510/113 devices.

Military Device Type	Generic-Industry Type
01	DAC-08
02	DAC-08A

CASE OUTLINE

Per MIL-M-38510, Appendix C, Case Outline D-2 (16-Lead 1/4" x 7/8", dual-in-line). Package type designator "E".

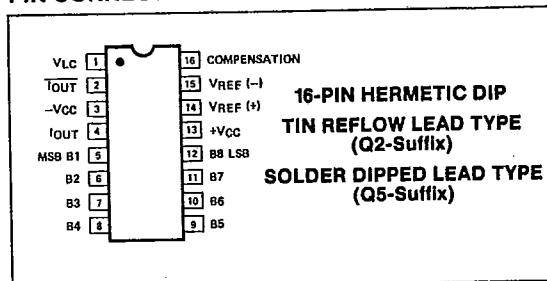
POWER AND THERMAL CHARACTERISTICS

Package	Case outline	Maximum allowable power dissipation	Maximum $\theta_J - C$	Maximum $\theta_J - A$
Dual-in-line	E	400mW at $T_A = 125^\circ\text{C}$	35°C/W	120°C/W

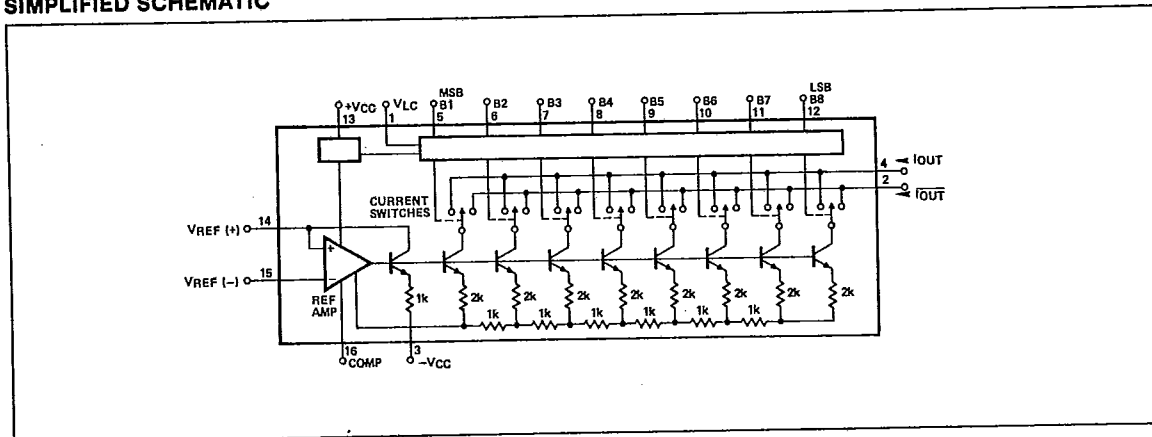
ORDERING INFORMATION

LINEARITY	JAN SLASH SHEET	PMI DEVICE
0.19%	JM38510/11301BEB	DAC08Q2/38510
0.19%	JM38510/11301BEA	DAC08Q5/38510
0.19%	JM38510/11301SEA	DAC08SQ5/38510
0.10%	JM38510/11302BEB	DAC08Q2/38510
0.10%	JM38510/11302BEA	DAC08Q5/38510
0.10%	JM38510/11302SEA	DAC08SQ5/38510

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage [+V_{CC} - (-V_{CC})] 36Vdc
 Voltage, Digital Input to Negative Supply
 [V_{logic} - (-V_{CC})] 0 to 36Vdc
 Voltage, Logic Control (V_{LO}) -V_{CC} to +V_{CC}
 Reference Voltage Input [(V₁₄, V₁₅)] -V_{CC} to +V_{CC}
 Reference Input Current (I₁₄) 5mA
 Reference Input Differential Voltage
 [(V₁₄ - V₁₅)] ±18Vdc
 Lead Temperature (Soldering, 60 sec) 300°C

Junction Temperature 175°C
 Storage Temperature -65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ±5Vdc to ±15Vdc*
 Ambient Temperature Range -55°C to +125°C

***NOTE:**

A slight degradation in linearity can occur when the supply voltage is near the ±5V end of the recommended operating range.

ELECTRICAL CHARACTERISTICS at ±V_{CC} = ±15Vdc; Source resistance = 50 ohms; I_{REF} = 2mA; Figure 1; Ambient temperature range = -55°C to +125°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	01 LIMITS		02 LIMITS		UNITS
			MIN	MAX	MIN	MAX	
Monotonicity	Δ(I)	Measure I _O , (I _{ON} - I _{ON-1}) ≥ 0 at each major carry point	0	16	0	16	μA
	Δ(I)	Measure I _O , (I _{ON} - I _{ON-1}) ≥ 0 at each major carry point	0	16	0	16	
Output Symmetry	ΔI _{FS}	I _{FS} - I _{FS}	-8	8	-4	4	μA
Full-Scale Current Temperature Coefficient	$\frac{T_O(I_{FS})}{T_O(I_{FS})}$	All input bits high, Measure I _O All input bits low, Measure I _O	-50	50	-50	50	ppm/°C
Full-Scale Current	I _{FS}	All input bits high, Measure I _O	1.94	2.04	1.984	2	mA
	I _{FS}	All input bits low, Measure I _O					
Zero-Scale Current	I _{zs}	All input bits low Measure I _O	-2	2	-1	1	μA
	I _{zs}	All input bits high, Measure I _O					
Positive Bit Errors	ΣNL+	Measure I _O (Σ Positive bit errors)/IFS	0	0.19	0	0.10	%
	ΣNL+	Measure I _O (Σ Positive bit errors)/IFS					
Negative Bit Errors	ΣNL-	Measure I _O (Σ Negative bit errors)/IFS	-0.19	0	-0.10	0	%
	ΣNL-	Measure I _O (Σ Negative bit errors)/IFS					
Positive and Negative Bit Error Difference	ΔΣNL	Measure I _O ΣNL+ - ΣNL-	-0.05	0.05	-0.03	0.03	%
	ΔΣNL	Measure I _O ΣNL+ - ΣNL-					
Positive Relative Accuracy	NL+	Measure I _O ΣNL+ + ΔΣNL	0	0.19	0	0.10	%
	NL+	Measure I _O ΣNL+ + ΔΣNL					
Negative Relative Accuracy	NL-	Measure I _O ΣNL- + ΔΣNL	0	0.19	0	0.10	%
	NL-	Measure I _O ΣNL- + ΔΣNL					

Bit Error

Bit error is the deviation of the analog output from its ideal value (after zero-scale and full-scale errors have been calibrated out) when turning on an individual bit. This is measured for all n bits.

$$\text{Bit error (analog value)} = V_n - (\text{FSR}/2^n)$$

Where V_n = analog output with bit n on only.

FSR = full-scale range

n = number of bits

Summation Nonlinearity (ΣNL)

Summation nonlinearity is the sum of all positive bit errors or all negative bit errors, whichever is larger. By summing up all the bit errors in one direction, you obtain the worst possible nonlinearity (i.e. if bit 2 is 1 LSB high and bit 4 is 1/2 LSB high, then bits 2 and 4 together will be 1 1/2 LSBs high. This is essentially the same as integral nonlinearity since the bit errors are superimposed on each other to give the worst case nonlinearity.



ELECTRICAL CHARACTERISTICS at $\pm V_{CC} = \pm 15V_{dc}$; Source resistance = 50 ohms; $I_{REF} = 2.0mA$; Figure 1; Ambient temperature range = $-55^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	01 LIMITS		02 LIMITS		UNITS
			MIN	MAX	MIN	MAX	
Output Current Range	$I_{FS} R_1$	All input bits high, Measure I_O . $-V_{CC} = -10V$, $V_{REF} = 15V$	2.1	—	2.1	—	mA
	$\overline{I_{FS} R_1}$	All input bits low, Measure $\overline{I_O}$. $-V_{CC} = -10V$, $V_{REF} = 15V$	—	—	—	—	
	$I_{FS} R_2$	All input bits high, Measure I_O . $-V_{CC} = -12V$, $V_{REF} = 25V$	4.2	—	4.2	—	
	$\overline{I_{FS} R_2}$	All input bits low, Measure $\overline{I_O}$. $-V_{CC} = -12V$, $V_{REF} = 25V$	—	—	—	—	
Reference Bias Current	I_{REF}	All input bits low	-3	0	-3	0	μA
High Level Input Current	I_{IH}	All input bits $V_{IN} = 18V$, each input measured separately	-0.05	10	-0.05	10	μA
Low Level Input Current	I_{IL}	All input bits $V_{IN} = 10V$, each input measured separately	-10	—	-10	—	μA
Full-Scale Current At +18V Compliance	I_{FS}^{+}	All input bits high, Measure I_O . $V_{IO} = 18V$	1.90	2.08	1.94	2.04	mA
	$\overline{I_{FS}^{+}}$	All input bits low, Measure $\overline{I_O}$. $V_{IO} = 18V$	—	—	—	—	
Full-Scale Current At -10V Compliance	I_{FS}^{-}	All input bits high, Measure I_O . $V_{IO} = -10V$	1.90	2.08	1.94	2.04	mA
	$\overline{I_{FS}^{-}}$	All input bits low, Measure $\overline{I_O}$. $V_{IO} = -10V$	—	—	—	—	
Change In Full Scale Current Due to Voltage Compliance	ΔI_{FSC}	All input bits high, Measure I_O . $25^{\circ}C \leq T_A \leq 125^{\circ}C$	-4	4	-4	4	μA
		$T_A = -55^{\circ}C$	-8	8	-8	8	
	$\Delta \overline{I_{FSC}}$	All input bits low, Measure $\overline{I_O}$. $25^{\circ}C \leq T_A \leq 125^{\circ}C$	-4	4	-4	4	
		$T_A = -55^{\circ}C$	-8	8	-8	8	
Power Supply Sensitivity From + V_{CC}	$P_{SS} I_{FS}^{+1}$	All input bits high, Measure I_O . $+V_{CC} = 4.5V$ to $+5.5V$, $-V_{CC} = -18V$	-4	4	-4	4	μA
	$\overline{P_{SS} I_{FS}^{+1}}$	All input bits low, Measure $\overline{I_O}$. $+V_{CC} = 4.5V$ to $+5.5V$, $-V_{CC} = -18V$	—	—	—	—	
	$P_{SS} I_{FS}^{+2}$	All input bits high, Measure I_O . $+V_{CC} = 12V$ to $18V$, $-V_{CC} = -18V$	-8	8	-8	8	
	$\overline{P_{SS} I_{FS}^{+2}}$	All input bits low, Measure $\overline{I_O}$. $+V_{CC} = 12V$ to $18V$, $-V_{CC} = -18V$	—	—	—	—	
Power Supply Sensitivity From - V_{CC}	$P_{SS} I_{FS}^{-1}$	All input bits high, Measure I_O . $+V_{CC} = 18V$, $-V_{CC} = -12V$ to $-18V$	-8	8	-8	8	μA
	$\overline{P_{SS} I_{FS}^{-1}}$	All input bits low, Measure $\overline{I_O}$. $+V_{CC} = 18V$, $-V_{CC} = -12V$ to $-18V$	—	—	—	—	
	$P_{SS} I_{FS}^{-2}$	All input bits high, Measure I_O . $+V_{CC} = 18V$, $-V_{CC} = -4.5V$ to $-5.5V$ $I_{REF} = 1mA$	-2	2	-2	2	
	$\overline{P_{SS} I_{FS}^{-2}}$	All input bits low, Measure $\overline{I_O}$. $+V_{CC} = 18V$, $-V_{CC} = -4.5V$ to $-5.5V$ $I_{REF} = 1mA$	—	—	—	—	

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ELECTRICAL CHARACTERISTICS at $\pm V_{CC} = \pm 15\text{Vdc}$; Source resistance = 50 ohms; $I_{REF} = 2.0\text{mA}$; Figure 1; Ambient temperature range = -55°C to $+125^\circ\text{C}$, unless otherwise noted.

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PARAMETER	SYMBOL	CONDITIONS	01 LIMITS		02 LIMITS		UNITS
			MIN	MAX	MIN	MAX	
Supply Current From $+V_{CC}$	I_{CC+}	All input bits high	0.4	3.8	0.4	3.8	mA
Supply Current From $-V_{CC}$	I_{CC-}	All input bits high	-7.8	-0.8	-7.8	-0.8	mA
Propagation Delay Time, High-to-Low Level	t_{PHL}	Figure 2, Measure V_O	6	60	6	60	ns
Propagation Delay Time, Low-to-High Level	t_{PLH}	Figure 2, Measure V_O	6	60	6	60	ns
Reference Amplifier Input Slew Rate	dI_O/dt $T_A = 25^\circ\text{C}$	Figure 3, Measure V_O	1.5	—	1.5	—	mA/ μs
Settling Time, High-to-Low Level	t_{SHL} $T_A = 25^\circ\text{C}$	Figure 2, Output within 1/2 LSB of final value of I_O	10	135	10	135	ns
Settling Time, Low-to-High Level	t_{SLH} $T_A = 25^\circ\text{C}$	Figure 2, Output within 1/2 LSB of final value of I_O	10	135	10	135	ns

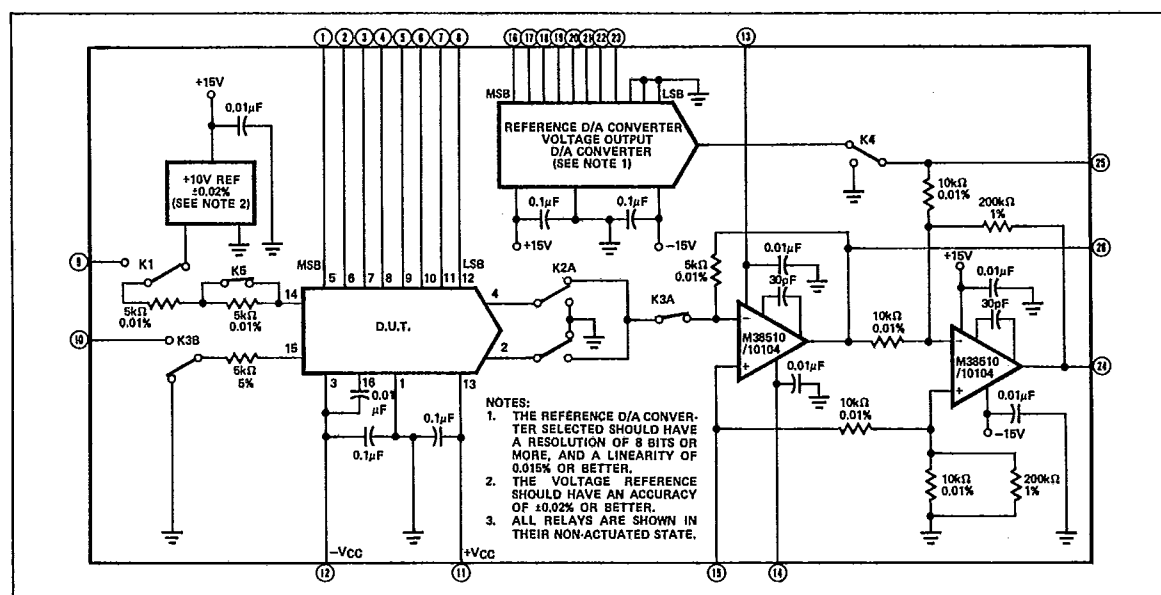


Figure 1. Test Circuit For Static Tests

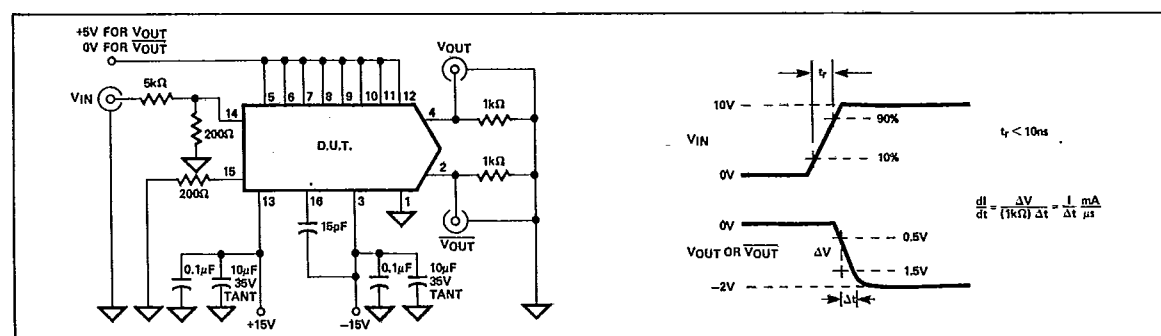


Figure 3. Test Circuit For Slew Rate, Device Types 01, 02

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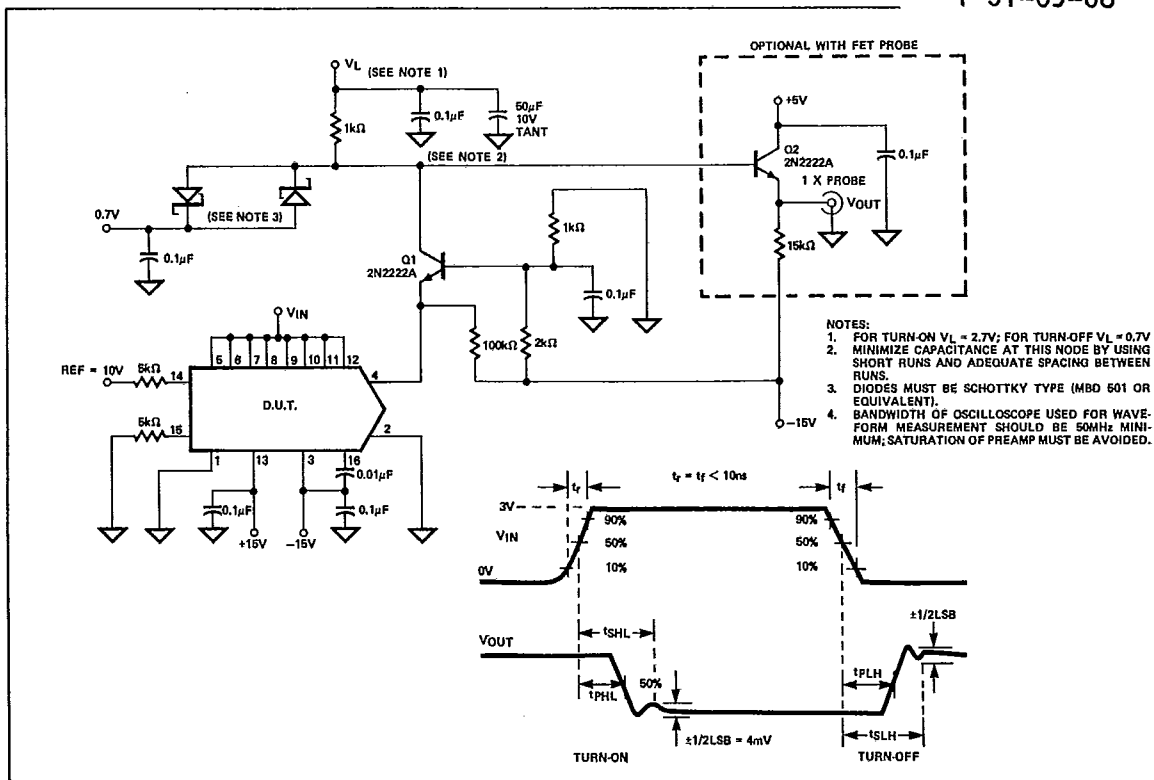


Figure 2. Test Circuit For Propagation Delay and Settling Time, Device Types 01 and 02

BURN-IN

Devices supplied by PMI have been subjected to burn-in per method 1015 of MIL-STD-883 using test condition C or test condition F with the circuit shown in Figure 4.

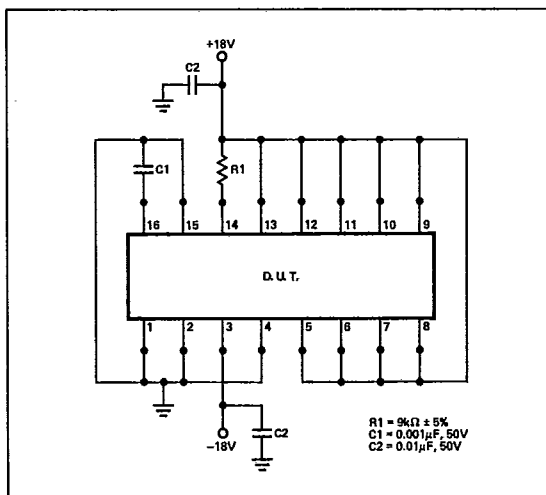


Figure 4. Test Circuit, Burn-In and Operating Life Test

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