General Description

The WSF20N20G is N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching .

performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency..

Product Summery

BVDSS	RDSON	ID
200V	0.12Ω	18A

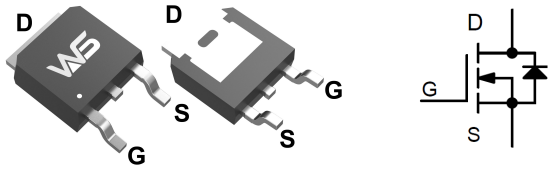
Applications

- Uninterruptible Power Supply(UPS)
- Power Factor Correction (PFC)

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent Cdv/dt effect decline
- Green Device Available

TO-252 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	200	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ 10V[1]	18	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ 10V[1]	10	A
I_{DM}	Pulsed Drain Current[2]	72	A
EAS	Single Pulse Avalanche Energy[3]	340	mJ
I_{AS}	Avalanche Current	15	A
P_D@T_C=25℃	Total Power Dissipation[3]	104	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient [1]	---	60	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	---	1.2	℃/W

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	200	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BVDSS Temperature Coefficient	Reference to 25℃ , I_D=1mA	---	0.25	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V , I_D=4.5A	---	0.12	0.16	Ω
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	2.0	3.5	4.0	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-4.63	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=200V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=160V , V_{GS}=0V , T_J=125℃	---	---	10	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±30V , V_{DS}=0V	---	---	±100	nA
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	0.12	---	Ω
Q_g	Total Gate Charge (10V)	V_{DS}=160V , V_{GS}=10V , I_D=18A	---	40	---	nC
Q_{gs}	Gate-Source Charge		---	5.2	---	
Q_{gd}	Gate-Drain Charge		---	18	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=100V , V_{GS}=10V , R_G=25Ω,I_D=18A	---	24	---	ns
T_r	Rise Time		---	45	---	
$T_{d(off)}$	Turn-Off Delay Time		---	101	---	
T_f	Fall Time		---	95	---	
C_{iss}	Input Capacitance	V_{DS}=25V , V_{GS}=0V , f=1MHz	---	1317	---	pF
C_{oss}	Output Capacitance		---	181	---	
C_{rss}	Reverse Transfer Capacitance		---	76	---	

Guaranteed Avalanche Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy[5]	V_{DD}=25V , L=0.1mH , I_{AS}=15A	250	---	---	mJ

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,6]	V_G=V_D=0V , Force Current	---	---	18	A
I_{SM}	Pulsed Source Current[2,6]		---	---	72	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=18A , T_J=25℃	---	---	1.4	V
t_{rr}	Reverse Recovery Time	IF=15A , dI/dt=100A/μs , T_J=25℃	---	230	---	nS
Q_{rr}	Reverse Recovery Charge		---	1.8	---	uC

Note :
1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper,t<10sec.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=15A
4.The power dissipation is limited by 150℃ junction temperature
5.The Min. value is 100% EAS tested guarantee.
6.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

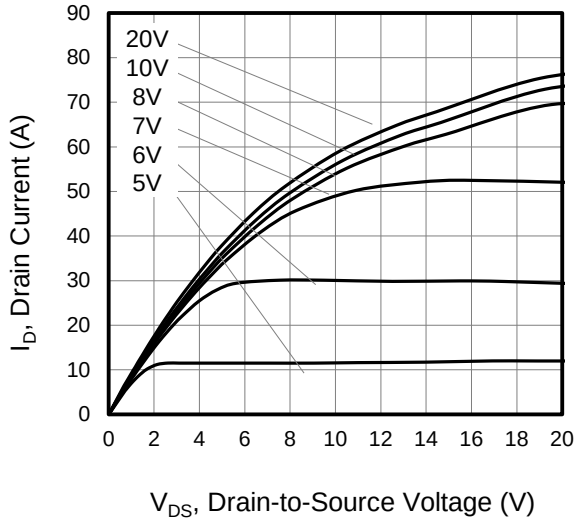


Figure 1. Output Characteristics (T_J = 25ºC)

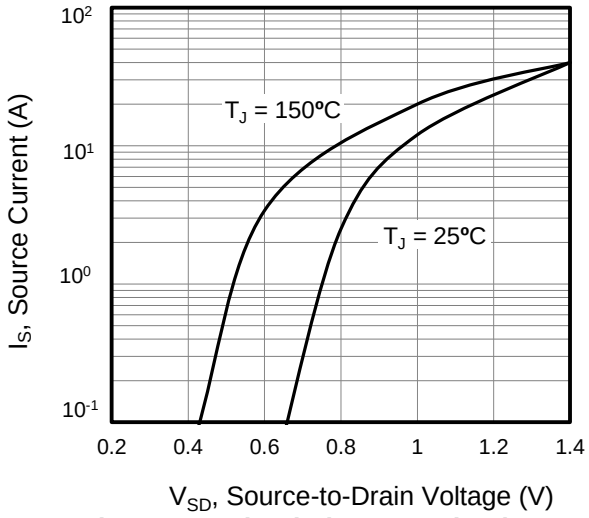


Figure 2. Body Diode Forward Voltage

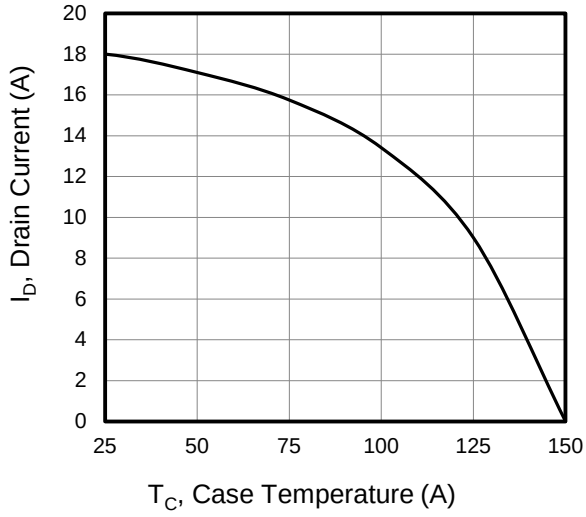


Figure 3. Drain Current vs. Temperature

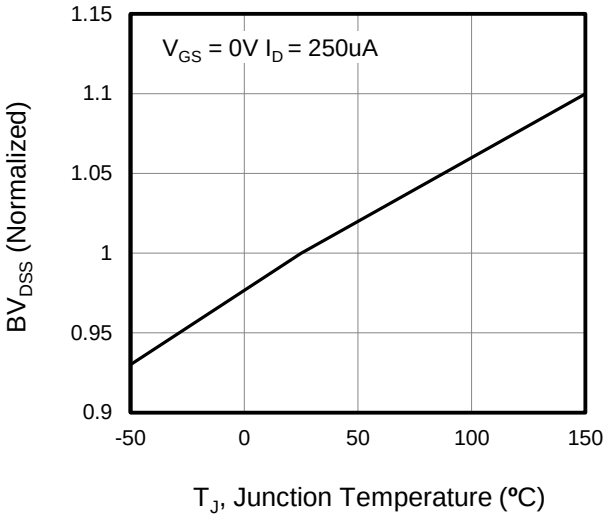


Figure 4. BV_{DSS} Variation vs. Temperature

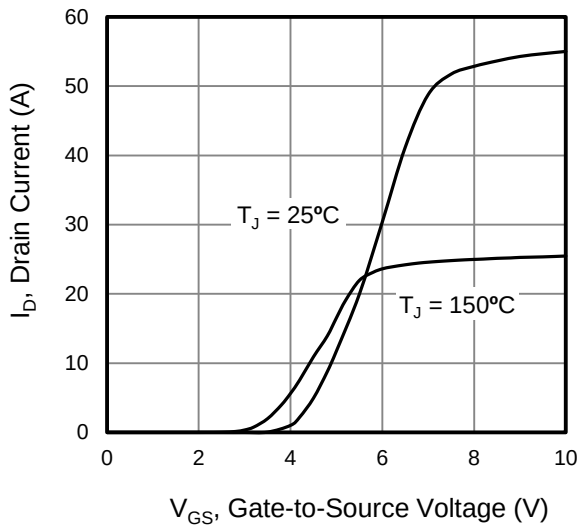


Figure 5. Transfer Characteristics

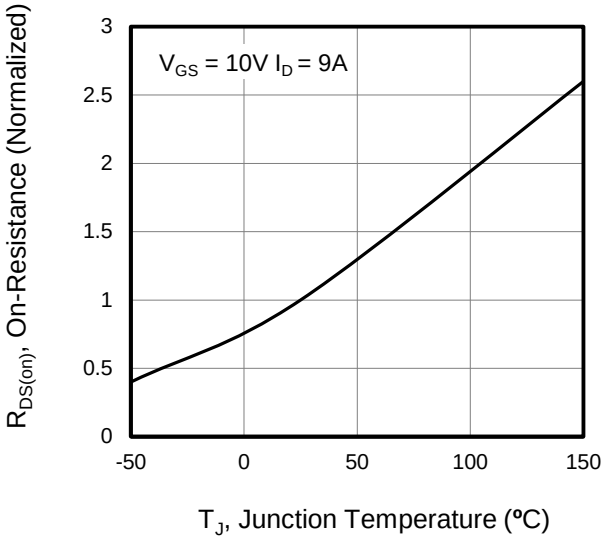


Figure 6. On-Resistance vs. Temperature

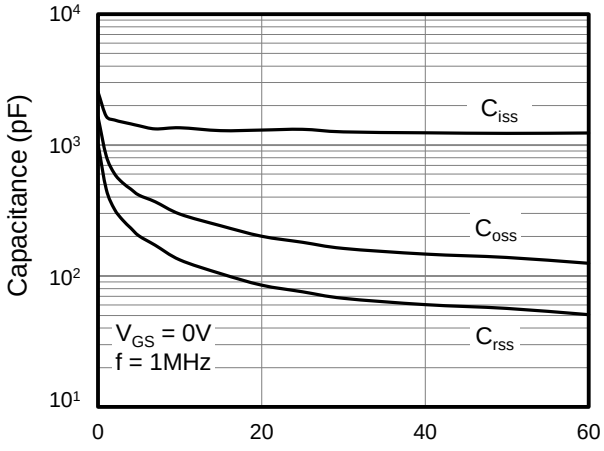


Figure 7. Capacitance

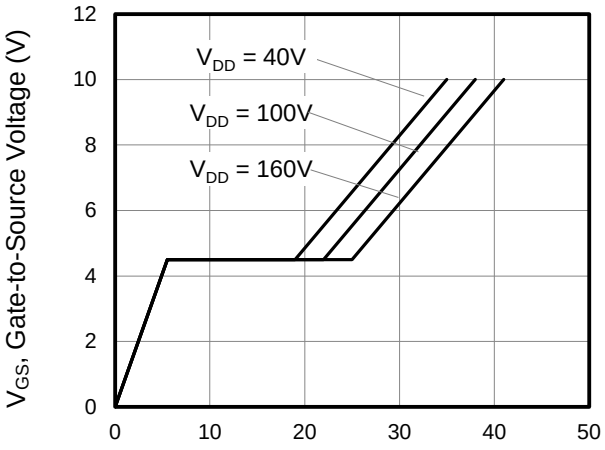


Figure 8. Gate Charge

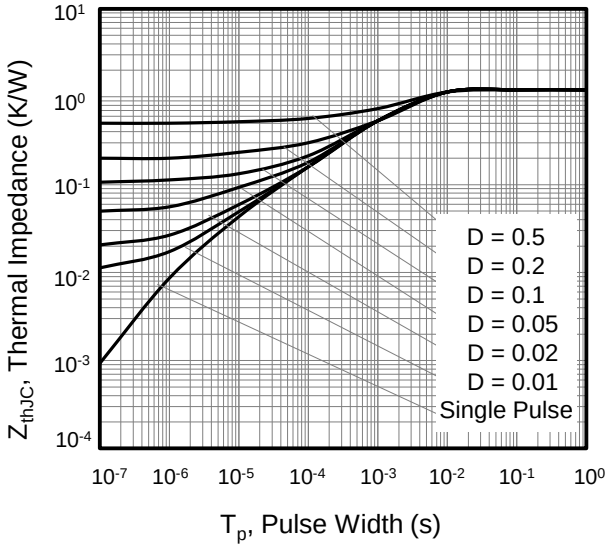


Figure 10. Transient Thermal Impedance

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