DiePlus™ Advantage

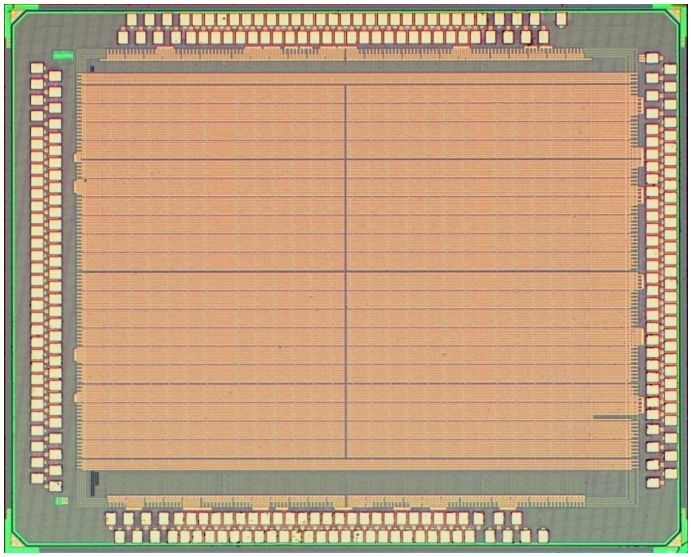
SiliconBlue®

January 25, 2011 (2.0.6) **Data Sheet**

DiePlus Advantage is SiliconBlue's focused program to provide designers with an optimal device mounting solution for mobile handheld applications. This data sheet provides detailed information regarding DiePlus Advantage devices. For general family information, please refer to the iCE65 mobileFPGA Device Family Data Sheet.

- **Smallest possible board footprint**
  - Mechanical package structures such as lead frames and heat slugs are eliminated, as well plastic encapsulation
  - Available as known-good die (KGD) or bumped die using wafer-level chip scale (WLCSP) packaging technology
- **Lowest cost solution, eliminating costs associated with encapsulated packages**
- **Up to 90% less weight than equivalent pin-count packaged devices**
- **Very flexible delivery options for KGD**
  - Whole wafer uncut, with wafer map
  - Cut wafer mounted on blue tape, with wafer map
  - KGD on tape and reel
  - Selectable die thickness: 4.0, 10.0, or 31.0 mil
- **WLCSP redistribution layer technology exhibits excellent electrical characteristics**
  - No signal integrity issues often associated with mounting substrates
  - Robust electrical connections minimize resistance and inductance

Figure 1: **iCE65L04 Known Good Die**



- **WLCSP technology eliminates need for KGD manufacturing flow**
  - Devices use standard PCB reflow mounting methods
  - Eliminates need for wire bonding and lead frames
  - Available in 0.4mm pitch (CS) or 0.5mm pitch (CC)
- **Laser etched custom marking available for WLCSP devices**
- **Full wafer custom programming of Non-Volatile Configuration Memory (NVCM) available**

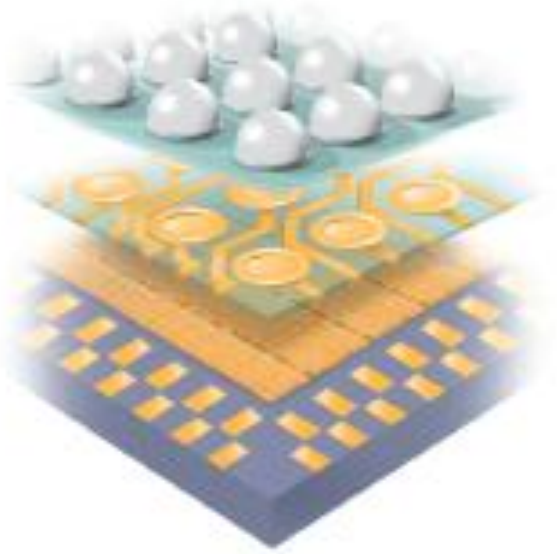
Table 1: **iCE65 Ultra Low-Power Programmable Logic DiePlus Family Summary**

		iCE65L01	iCE65L04	iCE65P04	iCE65L08
Logic Cells (LUT + Flip-Flop)		1,280	3,520	3,520	7,680
RAM4K Memory Blocks		16	20	20	32
Maximum Programmable I/O Pins		95	176	174	222
Maximum Differential Input Pairs		0	20	20	25
Size		2.5mm x 2.5mm	3.9mm x 3.2mm	3.8mm x 3.1mm	4.8mm x 4.4mm
Wafer Level Chip Scale Package, WLCSP	**Package**	CS36	CS63		CC72
	I/O Pins	25(0)	48(4)		55(8)
Known Good Die, KGD	**I/O Pads**	95(0)	176(20)	174(20)	222(25)

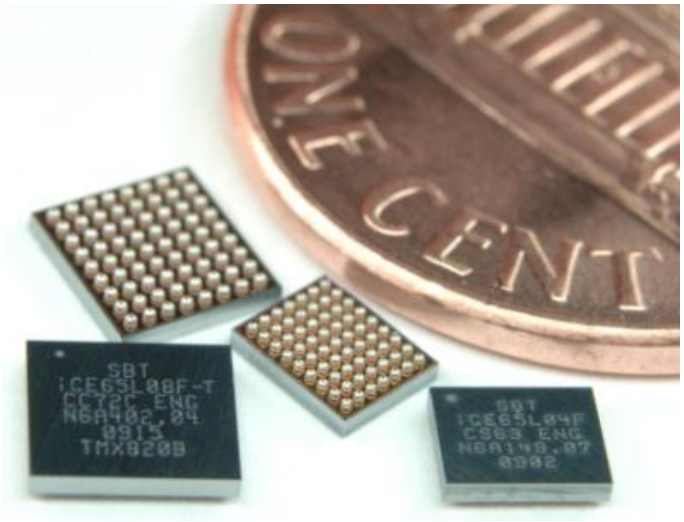
Industry's most advanced packages

The iCE65 mobileFPGA family uses the most advanced packaging technology available,

including Wafer Level Chip Scale Packaging (WLCSP). WLCSP technology adds a redistribution layer to a bare die, allowing standard mounting balls to be added.



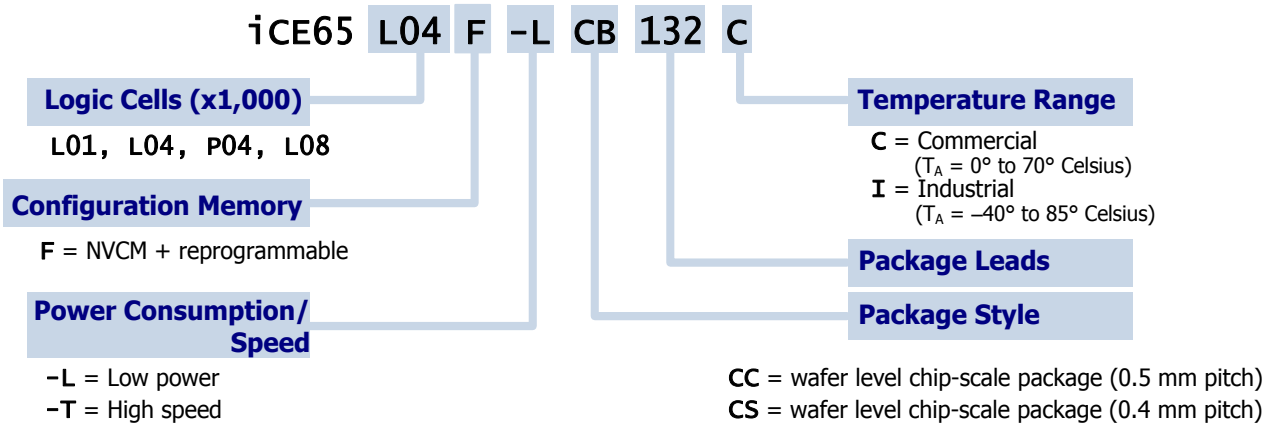
These devices can then be mounted to printed circuit boards just like standard ball grid array devices. By using WLCSP, iCE65 mobileFPGAs offer very small footprints and eliminate standard plastic package costs.



Ordering Information: WLCSP

Figure 2 describes the iCE65 ordering codes for all packaged components. See the separate iCE DiCE data sheets when ordering die-based products.

Figure 2: **iCE65 Ordering Codes (WLCSP)**



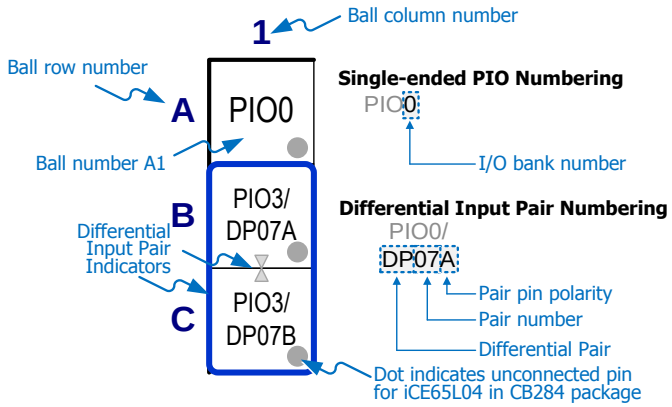
iCE65 devices offer two power consumption, speed options. Standard products ("-L" ordering code) have low standby and dynamic power consumption. The "-T" provides higher-speed logic.

Similarly, iCE65 devices are available in two operating temperature ranges, one for typical commercial applications, the other with an extended temperature range for industrial and telecommunications applications. The ordering code also specifies the device package option.

iCE65 Footprint Diagram Conventions

Figure 3 illustrates the naming conventions used in the following footprint diagrams. Each PIO pin is associated with an I/O Bank. PIO pins in I/O Bank 3 that support differential inputs are also numbered by differential input pair.

Figure 3: **CS and CC Package Footprint Diagram Conventions**



CS36 Wafer-Level Chip-Scale Ball Grid Array

The CS36 package is a wafer-level chip-scale package with 0.4 mm ball pitch. The iCE65L01 is the only device available in this package.

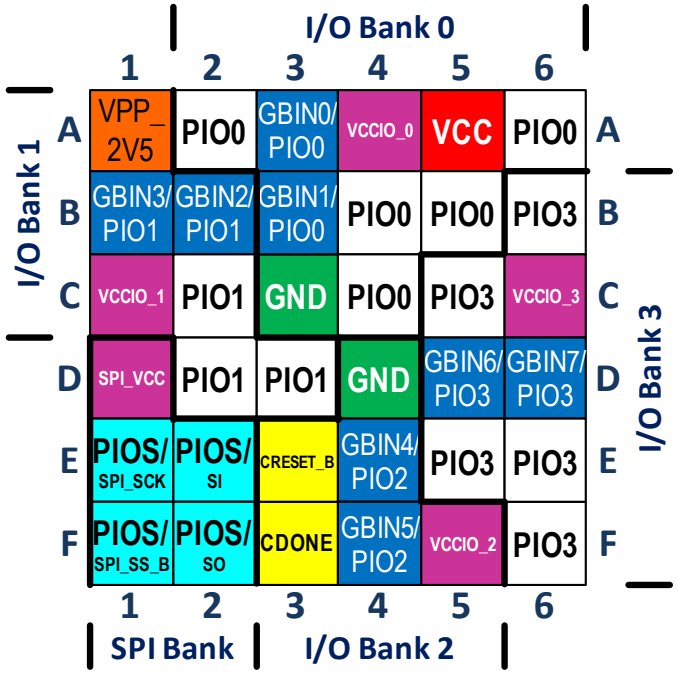
Footprint Diagram

Figure 4 shows the footprint diagram for the 36-ball wafer-level chip-scale package (CS36). Figure 3 shows the conventions used in the diagram. Compared to other packages, the footprint may appear left-right flipped because the balls on the CS36 package are mounted on the same side as the active circuitry. In other packages, the balls are mounted on the opposite side from the active circuitry.

See Table 2 for a complete, detailed pinout for the 36-ball wafer-level chip-scale BGA packages.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 4: **iC65L01 CS36 Wafer-Level Chip-Scale BGA Footprint (Top View)**



Pinout Table

Table 2 provides a detailed pinout table for the CS36 package. Pins are generally arranged by I/O bank, then by ball function. The CS36 package has no JTAG pins. The CS36 has no Cold Boot, CBSEL0 and CBSEL1 pins.

Table 2: **iCE65L01 CS36 Wafer-level Chip-scale BGA Pinout Table**

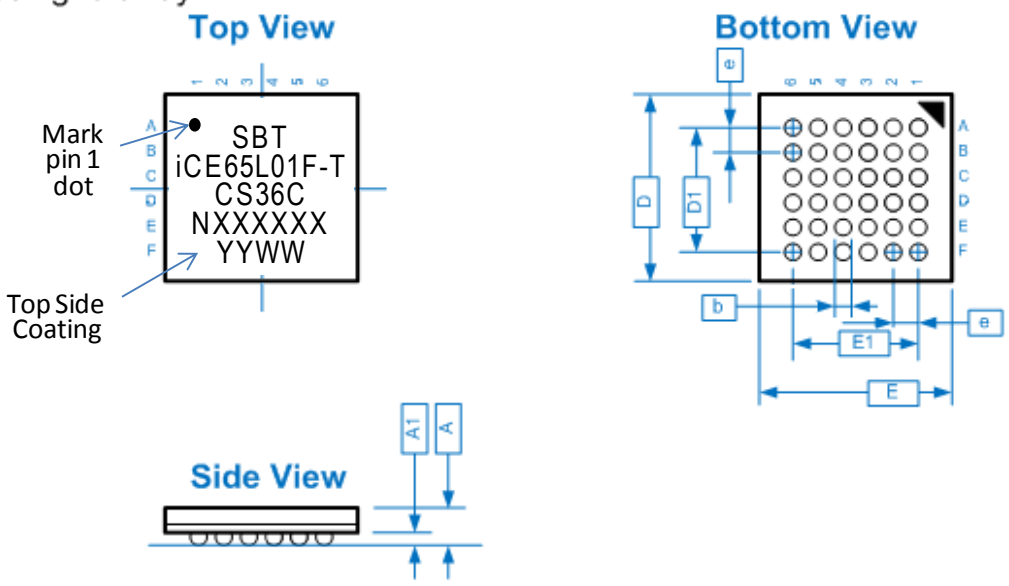
Ball Function	Ball Number	Type	Bank
GBIN0/PIO0	A3	GBIN	0
GBIN1/PIO0	B3	GBIN	0
PIO0	A2	PIO	0
PIO0	A6	PIO	0
PIO0	B4	PIO	0
PIO0	B5	PIO	0
PIO0	C4	PIO	0
VCCIO_0	A4	VCCIO	0
GBIN2/PIO1	B2	GBIN	1
GBIN3/PIO1	B1	GBIN	1
PIO1	C2	PIO	1
PIO1	D2	PIO	1
PIO1	D3	PIO	1
VCCIO_1	C1	VCCIO	1

Ball Function	Ball Number	Type	Bank
CDONE	F3	CONFIG	2
CRESET_B	E3	CONFIG	2
GBIN4/PIO2	E4	GBIN	2
GBIN5/PIO2	F4	GBIN	2
VCCIO_2	F5	VCCIO	2
GBIN7/PIO3	D6	GBIN	3
GBIN6/PIO3	D5	GBIN	3
PIO3	B6	PIO	3
PIO3	C5	PIO	3
PIO3	E5	PIO	3
PIO3	E6	PIO	3
PIO3	F6	PIO	3
VCCIO_3	C6	VCCIO	3
PIOS/SPI_SO	F2	PIO/SPI	SPI
PIOS/SPI_SI	E2	PIO/SPI	SPI
PIOS/SPI_SCK	E1	PIO/SPI	SPI
PIOS/SPI_SS_B	F1	PIO/SPI	SPI
SPI_VCC	D1	SPI	SPI
GND	C3	GND	GND
GND	D4	GND	GND
VCC	A5	VCC	VCC
VPP_2V5	A1	VPP	VPP

Package Mechanical Drawing

Figure 5: **CS36 Package Mechanical Drawing**

CS36: 2.50 x 2.50 mm, 36-ball, 0.4 mm ball-pitch, wafer-level chip-scale ball grid array



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			6		Columns
Number of Ball Rows	Y			6		Rows
Number of Signal Balls		n		36		Balls
Body Size	X	E	—	2.50	2.52	mm
	Y	D	—	2.50	2.52	
Ball Pitch		e	—	0.40	—	
Ball Diameter		b	—	0.25	—	
Edge Ball Center to Center	X	E1	—	2.00	—	
	Y	D1	—	2.00	—	
Package Height		A	0.801	0.840	0.879	
Stand Off		A1	0.17	0.20	0.23	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L01F	Part number
	-T	Power/Speed
3	CS36C	Package type
	ENG	Engineering
4	NXXXXXXX	Lot Number
5	YYWW	Date Code

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
42	34

CS63 Wafer-Level Chip-Scale Ball Grid Array

The CS63 package is a wafer-level chip-scale package with 0.4 mm ball pitch. The iCE65L04 is the only device available in this package.

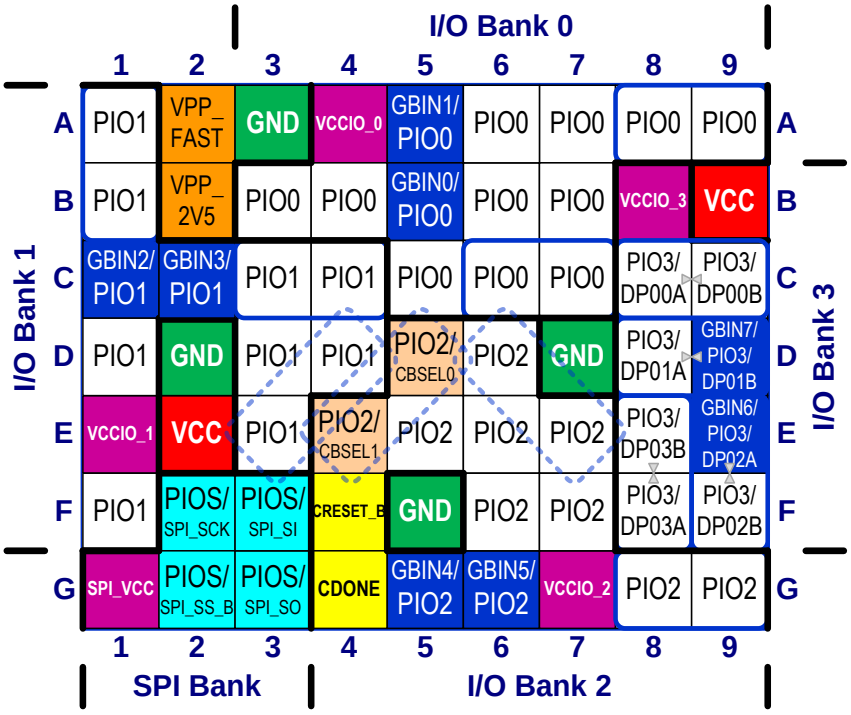
Footprint Diagram

Figure 6 shows the footprint diagram for the 63-ball wafer-level chip-scale package (CS63). Figure 3 shows the conventions used in the diagram. Compared to other packages, the footprint may appear left-right flipped because the balls on the CS63 package are mounted on the same side as the active circuitry. In other packages, the balls are mounted on the opposite side from the active circuitry.

See Table 3 for a complete, detailed pinout for the 63-ball wafer-level chip-scale BGA packages.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 6: **iC65L04 CS63 Wafer-Level Chip-Scale BGA Footprint (Top View)**



Pinout Table

Table 3 provides a detailed pinout table for the CS63 package. Pins are generally arranged by I/O bank, then by ball function. The table also highlights the differential I/O pairs in I/O Bank 3. The CS63 package has no JTAG pins.

Table 3: **iCE65L04 CS63 Wafer-level Chip-scale BGA Pinout Table**

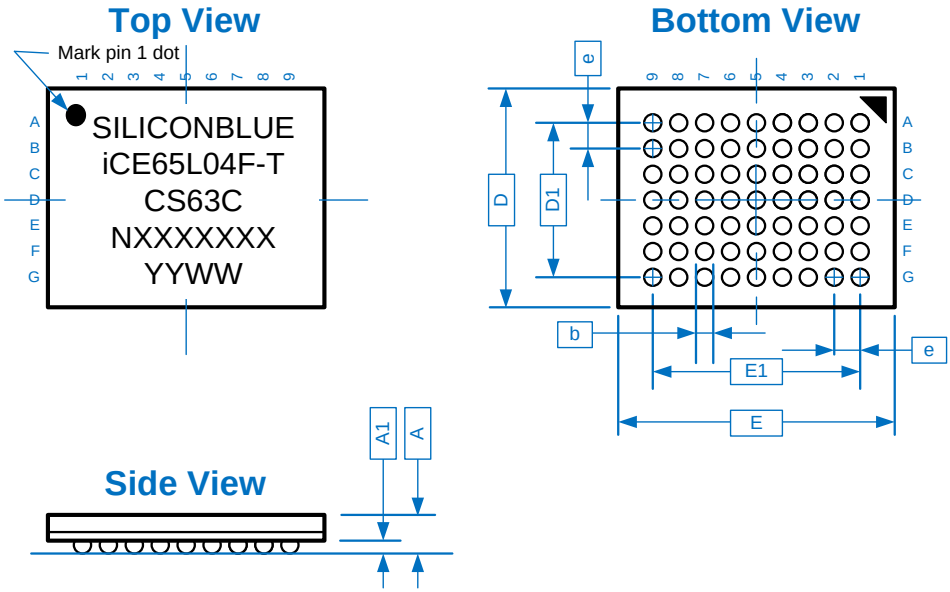
Ball Function	Ball Number	Type	Bank
GBIN0/PIO0	B5	GBIN	0
GBIN1/PIO0	A5	GBIN	0
PIO0	A6	PIO	0
PIO0	A7	PIO	0
PIO0	A8	PIO	0
PIO0	A9	PIO	0
PIO0	B3	PIO	0
PIO0	B4	PIO	0
PIO0	B6	PIO	0
PIO0	B7	PIO	0
PIO0	C5	PIO	0
PIO0	C6	PIO	0
PIO0	C7	PIO	0

Ball Function	Ball Number	Type	Bank
VCCIO_0	A4	VCCIO	0
GBIN2/PIO1	C1	GBIN	1
GBIN3/PIO1	C2	GBIN	1
PIO1	A1	PIO	1
PIO1	B1	PIO	1
PIO1	C3	PIO	1
PIO1	C4	PIO	1
PIO1	D1	PIO	1
PIO1	D3	PIO	1
PIO1	D4	PIO	1
PIO1	E3	PIO	1
PIO1	F1	PIO	1
VCCIO_1	E1	VCCIO	1
CDONE	G4	CONFIG	2
CRESET_B	F4	CONFIG	2
GBIN4/PIO2	G5	GBIN	2
GBIN5/PIO2	G6	GBIN	2
PIO2	D6	PIO	2
PIO2	E5	PIO	2
PIO2	E6	PIO	2
PIO2	E7	PIO	2
PIO2	F6	PIO	2
PIO2	F7	PIO	2
PIO2	G8	PIO	2
PIO2	G9	PIO	2
PIO2/CBSEL0	D5	PIO	2
PIO2/CBSEL1	E4	PIO	2
VCCIO_2	G7	VCCIO	2
PIO3/DP00A	C8	DPIO	3
PIO3/DP00B	C9	DPIO	3
PIO3/DP01A	D8	DPIO	3
GBIN7/PIO3/DP01B	D9	DPIO/GBIN	3
GBIN6/PIO3/DP02A	E9	DPIO/GBIN	3
PIO3/DP02B	F9	DPIO	3
PIO3/DP03B	E8	DPIO	3
PIO3/DP03A	F8	DPIO	3
VCCIO_3	B8	VCCIO	3
PIOS/SPI_SO	G3	PIO/SPI	SPI
PIOS/SPI_SI	F3	PIO/SPI	SPI
PIOS/SPI_SCK	F2	PIO/SPI	SPI
PIOS/SPI_SS_B	G2	PIO/SPI	SPI
SPI_VCC	G1	SPI	SPI
GND	A3	GND	GND
GND	D2	GND	GND
GND	D7	GND	GND
GND	F5	GND	GND
VCC	B9	VCC	VCC
VCC	E2	VCC	VCC
VPP_2V5	B2	VPP	VPP
VPP_FAST	A2	VPP	VPP

Package Mechanical Drawing

Figure 7: **CS63 Package Mechanical Drawing**

CS63: 3.83 x 3.16 mm, 63-ball, 0.4 mm ball-pitch, wafer-level chip-scale ball grid array



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			9		Columns
Number of Ball Rows	Y			7		Rows
Number of Signal Balls		n		63		Balls
Body Size	X	E	3.81	3.83	3.85	mm
	Y	D	3.14	3.16	3.18	
Ball Pitch		e	—	0.40	—	
Ball Diameter		b	0.23	0.25	0.29	
Edge Ball Center to Center	X	E1	—	3.20	—	
	Y	D1	—	2.40	—	
Package Height		A	0.801	0.840	0.879	
Stand Off		A1	0.17	0.20	0.23	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L04F	Part number
	-T	Power/Speed
3	CS63C	Package type
	ENG	Engineering
4	NXXXXXXX	Lot Number
5	YYWW	Date Code

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
40	32

CC72 Wafer-Level Chip-Scale Ball Grid Array

The CC72 package is wafer-level chip-scale ball grid array with 0.5 mm ball pitch. The iCE65L08 is the only device available in this package.

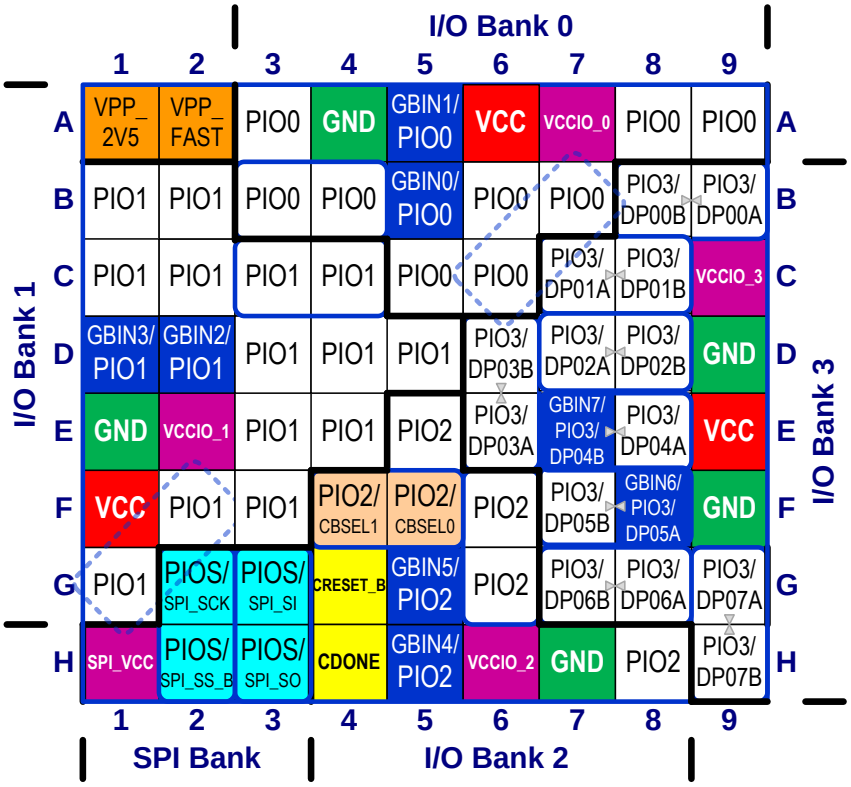
Footprint Diagram

Figure 8 shows the footprint diagram for the 72-ball wafer-level chip-scale package (CC72). Figure 3 shows the conventions used in the diagram. Compared to other packages, the footprint may appear left-right flipped because the balls on the CC72 package are mounted on the same side as the active circuitry. In other packages, the balls are mounted on the opposite side from the active circuitry.

See Table 4 for a complete, detailed pinout for the 72-ball wafer-level chip-scale BGA packages.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 8: **iC65L08 CC72 Wafer-Level Chip-Scale BGA Footprint (Top View)**



Pinout Table

Table 4 provides a detailed pinout table for the CC72 package. Pins are generally arranged by I/O bank, then by ball function. The table also highlights the differential I/O pairs in I/O Bank 3. The CC72 package has no JTAG pins.

Table 4: **iCE65L08 CC72 Wafer-level Chip-scale BGA Pinout Table**

Ball Function	Ball Number	Type	Bank
GBIN0/PIO0	B5	GBIN	0
GBIN1/PIO0	A5	GBIN	0
PIO0	A3	PIO	0
PIO0	A8	PIO	0
PIO0	A9	PIO	0
PIO0	B3	PIO	0
PIO0	B4	PIO	0
PIO0	B6	PIO	0
PIO0	B7	PIO	0
PIO0	C5	PIO	0
PIO0	C6	PIO	0

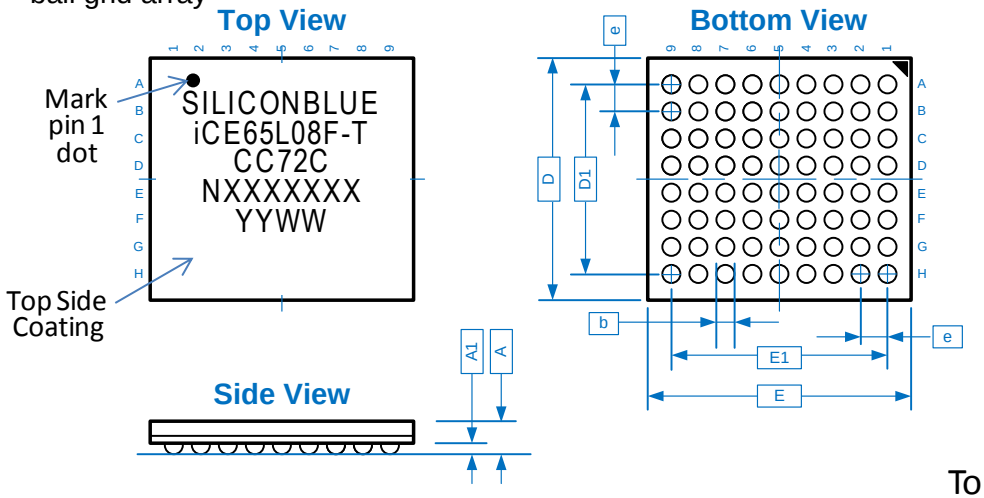
Ball Function	Ball Number	Type	Bank
VCCIO_0	A7	VCCIO	0
GBIN2/PIO1	D2	GBIN	1
GBIN3/PIO1	D1	GBIN	1
PIO1	B1	PIO	1
PIO1	B2	PIO	1
PIO1	C1	PIO	1
PIO1	C2	PIO	1
PIO1	C3	PIO	1
PIO1	C4	PIO	1
PIO1	D3	PIO	1
PIO1	D4	PIO	1
PIO1	D5	PIO	1
PIO1	E3	PIO	1
PIO1	E4	PIO	1
PIO1	F2	PIO	1
PIO1	F3	PIO	1
PIO1	G1	PIO	1
VCCIO_1	E2	VCCIO	1
CDONE	H4	CONFIG	2
CRESET_B	G4	CONFIG	2
GBIN4/PIO2	H5	GBIN	2
GBIN5/PIO2	G5	GBIN	2
PIO2	E5	PIO	2
PIO2	F6	PIO	2
PIO2	G6	PIO	2
PIO2	H8	PIO	2
PIO2/CBSEL0	F5	PIO	2
PIO2/CBSEL1	F4	PIO	2
VCCIO_2	H6	VCCIO	2
PIO3/DP00A	B9	DPIO	3
PIO3/DP00B	B8	DPIO	3
PIO3/DP01A	C7	DPIO	3
PIO3/DP01B	C8	DPIO	3
PIO3/DP02A	D7	DPIO	3
PIO3/DP02B	D8	DPIO	3
PIO3/DP03A	D6	DPIO	3
PIO3/DP03B	E6	DPIO	3
PIO3/DP04A	E8	DPIO	3
GBIN7/PIO3/DP04B	E7	DPIO/GBIN	3
GBIN6/PIO3/DP05A	F8	DPIO/GBIN	3
PIO3/DP05B	F7	DPIO	3
PIO3/DP06A	G8	DPIO	3
PIO3/DP06B	G7	DPIO	3
PIO3/DP07A	G9	DPIO	3
PIO3/DP07B	H9	DPIO	3
VCCIO_3	C9	VCCIO	3
PIOS/SPI_SO	H3	PIO/SPI	SPI
PIOS/SPI_SI	G3	PIO/SPI	SPI
PIOS/SPI_SCK	G2	PIO/SPI	SPI

Ball Function	Ball Number	Type	Bank
PIOS/SPI_SS_B	H2	PIO/SPI	SPI
SPI_VCC	H1	SPI	SPI
GND	A4	GND	GND
GND	D9	GND	GND
GND	E1	GND	GND
GND	F9	GND	GND
GND	H7	GND	GND
VCC	A6	VCC	VCC
VCC	E9	VCC	VCC
VCC	F1	VCC	VCC
VPP_2V5	A1	VPP	VPP
VPP_FAST	A2	VPP	VPP

Package Mechanical Drawing

Figure 9: **iCE65L08 CC72 Package Mechanical Drawing**

CC72: 4.3 x 4.7 mm, 72-ball, 0.5 mm ball-pitch, wafer-level chip-scale ball grid array



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			9		Columns
Number of Ball Rows	Y			8		Rows
Number of Signal Balls		n		72		Balls
Body Size	X	E	—	4.69	4.71	mm
	Y	D	—	4.274	4.29	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.29	0.30	0.35	
Edge Ball Center to Center	X	E1	—	4.00	—	
	Y	D1	—	3.50	—	
Package Height		A	0.841	0.880	0.919	
Stand Off		A1	—	0.25	—	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L08F	Part number
	-T	Power/Speed
3	CC72C	Package type
	ENG	Engineering
4	NXXXXXXX	Lot Number
5	YYWW	Date Code

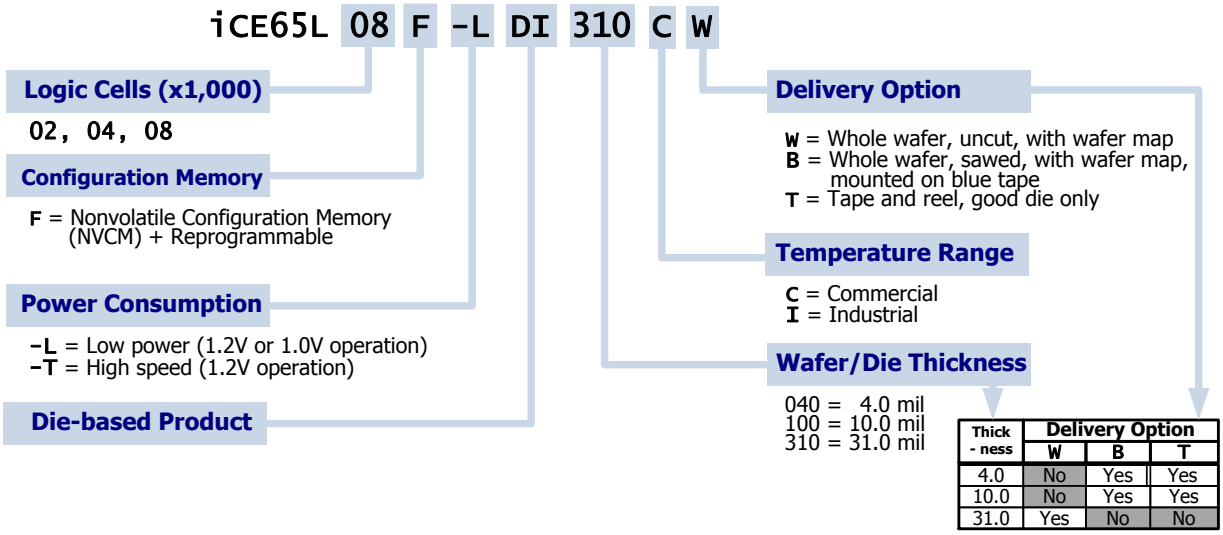
Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
37	30

Ordering Information: KGD

Figure 10 describes the iCE65 Known Good Die product ordering codes.

Figure 10: **iCE65 Ordering Codes (KGD)**



Thick - ness	Delivery Option		
	W	B	T
4.0	No	Yes	Yes
10.0	No	Yes	Yes
31.0	Yes	No	No

iCE65 FPGA devices are available with two power consumption options. Standard products ("-L" ordering code) have low standby and dynamic power consumption. The "-T" option provides higher-speed logic.

Please consult the die distributor or SiliconBlue Technologies Corporation before ordering to verify long-term availability of these die products.

Specifications discussed herein are subject to change without notice. This product is sold "as is" and is delivered with no guarantees or warranties, expressed or implied.

Die Samples

Die samples are available through an authorized SiliconBlue sales representative. Samples are provided untested, but with expected high yield (about 90%).

Functional Specifications

Please refer to the packaged product data sheet found on the SiliconBlue Technologies web site (www.siliconbluetech.com) for functional and parametric specifications. The specifications are provided for reference only.

Physical Specifications

Table 5 lists key physical characteristics of each iCE65 die.

Table 5: **KDG Physical Specifications**

Feature		Dimension
Wafer Diameter		300 mm (12 inches)
Wafer Thickness		31 mil, 10 mil, or 4 mil, specified in order code, Figure 10
Die Size (stepping interval)	iCE65L01	2,490 µm x 2,520 µm
	iCE65L04	3,870 µm x 3,200 µm
	iCE65P04	3,830 µm x 3,080 µm
	iCE65L08	4,810 µm x 4,394 µm
Scribe Width Along X-Axis (dsw_X)		160 µm
Scribe Width Along Y-Axis (dsw_Y)		160 µm
Bond Pad Size (min)		61 µm x 75 µm
Passivation Openings (min)		58 µm x 72 µm
Minimum Bond Pad Pitch (staggered)		35 µm

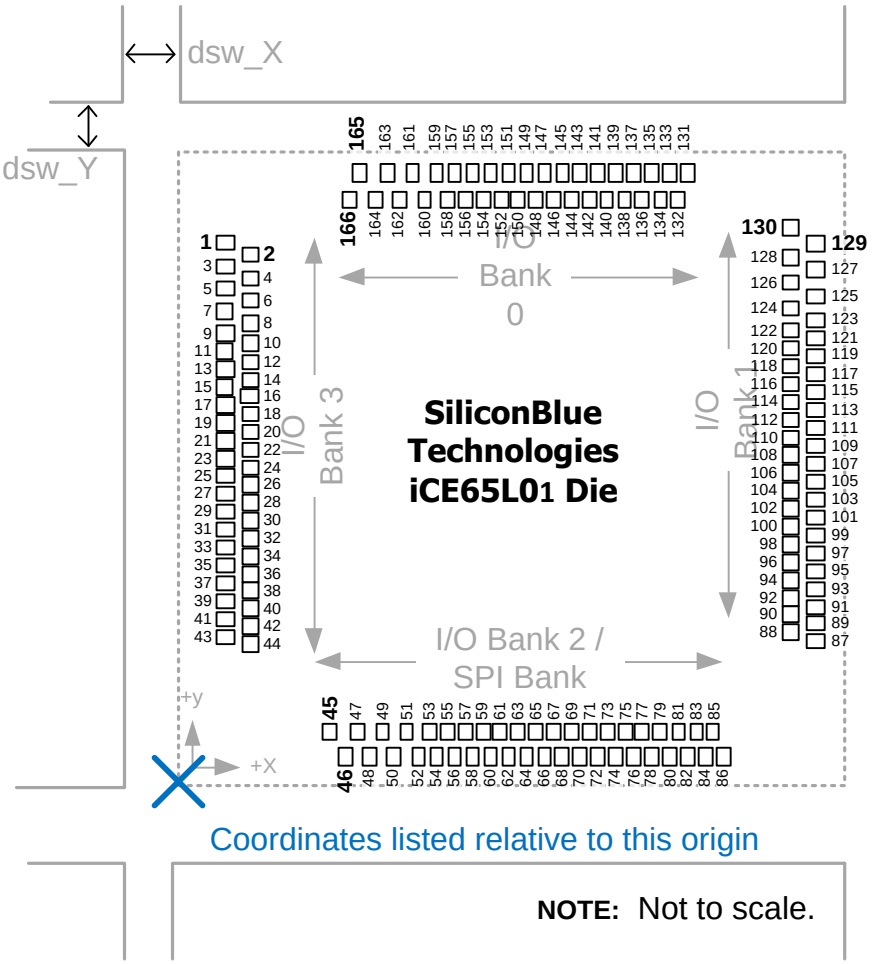
Die Attach Guidelines

- **Bond Wires:** Connect die pads using gold wire. The preferred bond wire diameter is 0.7 mil, not to exceed 0.9 mil.
- **Preferred Attachments:** If possible within the application, attach all pads. If not possible, follow the following connection guidelines.
- **VCC Connections:** A minimum of four VCC attachments are required. The four VCC attachments must use two sets of adjacent VCC pads. Pads 259 and 260 in Table 9 are an example of an adjacent pad set.
- **VCCIO Connections:** A minimum of two VCCIO pads must be attached in every I/O bank used.
  - A minimum of two VCCIO_2 pads in I/O Bank 2 must be attached. The VCCIO_2 connection is required to trigger the Power-On Reset (POR) circuit.
  - A minimum of two VCCIO_1 pads in I/O Bank 1 must be attached unless the TRST_B pad is attached to ground, disabling the JTAG interface.
    - If the JTAG interface is disabled, then ground the JTAG input pins, attached to pads TDI, TMS, TCK and TRST_B to ground.
    - If the JTAG interface is disabled, then leave the JTAG output pin unconnected, pad TDO.
  - If I/O Bank 3 is used in the application, connect the following pads as directed.
    - Attach a minimum of two VCC (Post) pads.
    - Attach a minimum of two GND (Post) pads.
    - Attach a minimum of one VCCIO_3 (Level) pads and electrically connect to other attached VCCIO_3 pads.
    - Attach at least one VCC (Pre) pad.
    - Attach at least one GND (Pre) pad
    - The VCC (Core) and GND (Core) pads may be left unconnected if the required numbers of VCC and GND pads are attached elsewhere.
    - If using an SSTL I/O standard, attach VREF to a valid reference voltage as described in the iCE65 family data sheet and attach GND (Shield) pad to ground.
    - If not using an STTL I/O standard, attach VREF to ground.
  - If unused in the application, the VCCIO connections to I/O Bank 0 and I/O Bank 3 can be left disconnected or attached to ground.
- **VPP_2V5 Connection:** The VPP_2V5 pad must attach to a valid voltage, as described in the iCE65 family data sheet, to trigger the Power-On Reset (POR) circuit.
- **VCC_SPI Connection:** At least one VCC_SPI pad must attach to a valid voltage, as described in the iCE65 family data sheet, to trigger the Power-On Reset (POR) circuit.
- **GND Connections:** A minimum of two GND connections must be attached in every I/O bank used.

Physical Specifications: iCE65L01

Figure 11 shows the physical outlines of iCE65L01 die on a wafer, including pad orientation and physical origin. The bond pad identification and coordinates are provided in Table 6. Table 5 lists key physical characteristics of each iCE65 die.

Figure 11: **iCE65L01 Die Outline**



Bond Pad Listing and Coordinates: iCE68L01

Table 6 lists each of the 166 bonding pads on an iCE65L01 device. The pad number begins in the upper left corner of the die, as shown in Figure 11, and increments in a counter-clockwise direction around the perimeter of the die. . Each bonding pad is identified. Signal names are color-coded by function. I/O pairs are grouped together with a thick surrounding box. These pairs in I/O Bank 3 represent an optional differential input or output. In all other banks, these pairs represent an optional differential output. The pad coordinates are measured relative to the origin, in the lower left corner of the die.

Table 6: **iCE65L01 Bond Pad Listing and Coordinates (Relative to Origin)**

Pad	Signal Name	From Origin	
		X (µm)	Y (µm)
1	PIO3_00	37.5	2060.13
2	PIO3_01	139.5	2010.13
3	PIO3_02	37.5	1960.13
4	PIO3_03	139.5	1910.13
5	GND	37.5	1860.13
6	GND	139.5	1810.13
7	VCCIO_3	37.5	1760.13
8	VCCIO_3	139.5	1710.13
9	PIO3_04	37.5	1660.13
10	PIO3_05	139.5	1610.13
11	PIO3_06	37.5	1575.13
12	PIO3_07	139.5	1540.13
13	PIO3_08	37.5	1505.13
14	PIO3_09	139.5	1470.13
15	GND	37.5	1435.13
16	GND	139.5	1400.13
17	VCC	37.5	1365.13
18	VCC	139.5	1330.13
19	PIO3_10	37.5	1295.13
20	GBIN7/PIO3_11	139.5	1260.13
21	VCCIO_3	37.5	1225.13
22	VCCIO_3	139.5	1190.13
23	VCCIO_3	37.5	1155.13
24	GBIN6/PIO3_12	139.5	1120.13
25	PIO3_13	37.5	1085.13
26	GND	139.5	1050.13
27	GND	37.5	1015.13
28	PIO3_14	139.5	980.13
29	PIO3_15	37.5	945.13
30	PIO3_16	139.5	910.13
31	PIO3_17	37.5	875.13
32	VCC	139.5	840.13
33	PIO3_18	37.5	805.13
34	PIO3_19	139.5	770.13
35	VCCIO_3	37.5	735.13
36	VCCIO_3	139.5	700.13
37	GND	37.5	665.13
38	GND	139.5	615.13
39	PIO3_20	37.5	565.13
40	PIO3_21	139.5	515.13
41	PIO3_22	37.5	465.13
42	PIO3_23	139.5	415.13
43	PIO3_24	37.5	365.13
44	PIO3_25	139.5	315.13
45	PIO2_00	139.5	307
46	PIO2_01	37.5	357
47	PIO2_02	139.5	407
48	PIO2_03	37.5	457
49	PIO2_04	139.5	507
50	PIO2_05	37.5	557
51	PIO2_06	139.5	607
52	PIO2_07	37.5	657
53	VCCIO_2	139.5	692
54	VCCIO_2	37.5	727
55	PIO2_08	139.5	762
56	PIO2_09	37.5	797
57	GND	139.5	832
58	GND	37.5	867
59	GBIN4/PIO2_10	139.5	902
60	PIO2_11	37.5	937
61	VCC	139.5	972
62	VCC	37.5	1007
63	GBIN5/PIO2_12	139.5	1042
64	PIO2_13	37.5	1077
65	VCCIO_2	139.5	1112
66	VCCIO_2	37.5	1147
67	VCCIO_2	139.5	1182
68	PIO2_14	37.5	1217
69	GND	139.5	1252
70	GND	37.5	1287
71	GND	139.5	1322
72	NC	37.5	1357
73	PIO2_15	139.5	1392
74	PIO2_16	37.5	1427
75	PIO2_17	139.5	1462
76	PIO2_18/CBSEL0	37.5	1497
77	PIO2_19/CBSEL1	139.5	1532

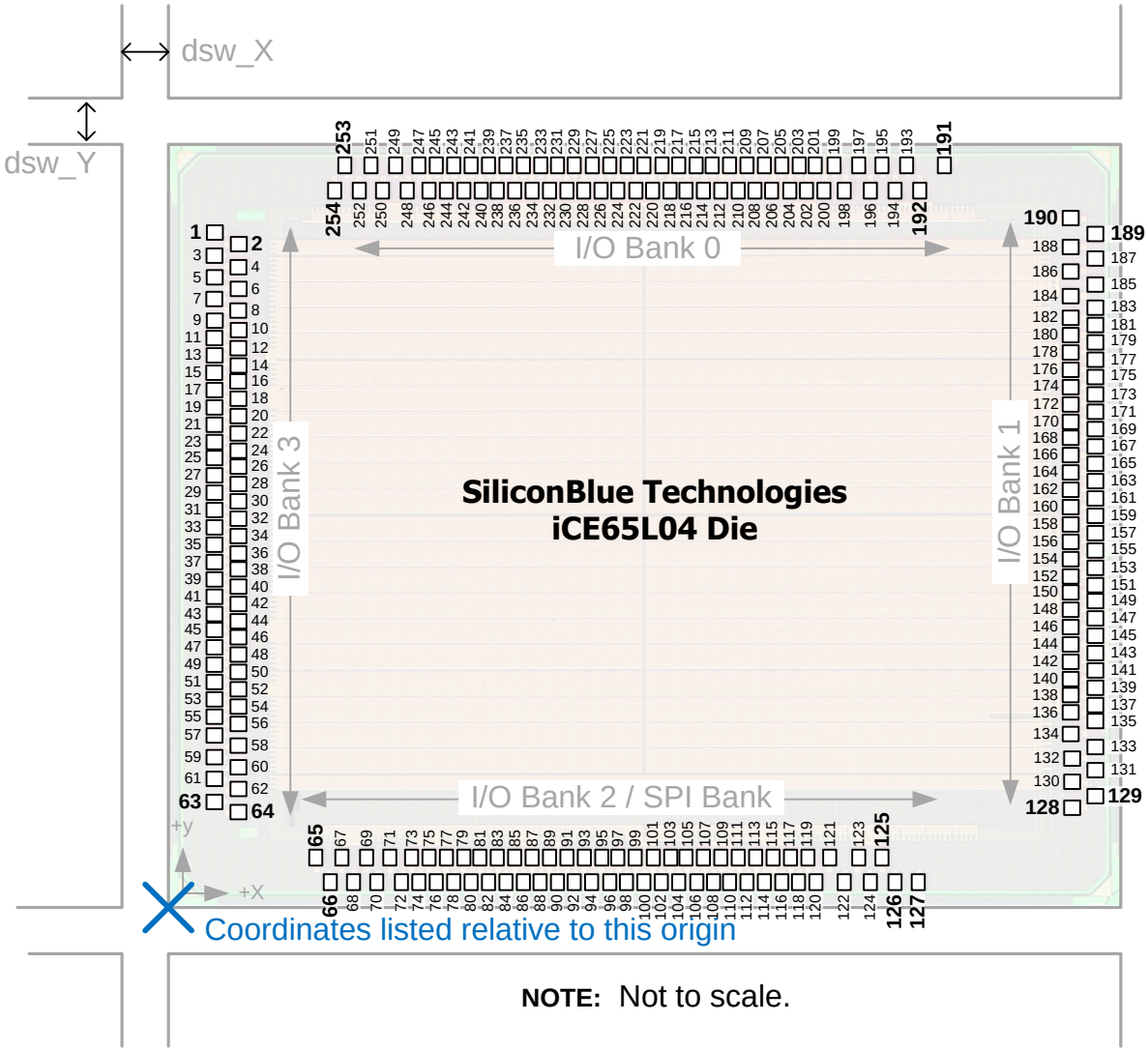
Pad	Signal Name	From Origin X (µm)	From Origin Y (µm)
78	CDONE	37.5	1602
79	CRESET_B	139.5	1652
80	PIOS_00/SPI_SO	37.5	1702
81	PIOS_01/SPI_SI	139.5	1752
82	GND	37.5	1802
83	PIOS_02/SPI_SCK	139.5	1852
84	PIOS_03/SPI_SS_B	37.5	1902
85	SPI_VCC	139.5	1952
86	SPI_VCC_OP	37.5	2002
87	TDI	2155	139.5
88	TMS	2372.5	244.4
89	TCK	2270.5	294.4
90	TDO	2372.5	344.4
91	TRST_B	2270.5	394.4
92	PIO1_00	2372.5	444.4
93	PIO1_01	2270.5	494.4
94	PIO1_02	2372.5	544.4
95	PIO1_03	2270.5	594.4
96	GND	2270.5	679.4
97	GND	2372.5	714.4
98	PIO1_04	2270.5	749.4
99	PIO1_05	2372.5	784.4
100	VCCIO_1	2270.5	819.4
101	VCCIO_1	2372.5	854.4
102	PIO1_06	2270.5	889.4
103	PIO1_07	2372.5	924.4
104	VCC	2270.5	959.4
105	VCC	2372.5	994.4
106	GBIN3/PIO1_08	2270.5	1029.4
107	GBIN2/PIO1_09	2372.5	1064.4
108	GND	2270.5	1259.4
109	GND	2372.5	1294.4
110	PIO1_10	2270.5	1329.4
111	PIO1_11	2372.5	1364.4
112	PIO1_12	2270.5	1399.4
113	PIO1_13	2372.5	1434.4
114	PIO1_14	2270.5	1469.4
115	VCCIO_1	2372.5	1504.4
116	VCCIO_1	2270.5	1539.4
117	PIO1_15	2372.5	1574.4
118	PIO1_16	2270.5	1609.4
119	GND	2372.5	1644.4
120	GND	2270.5	1679.4
121	GND	2372.5	1714.4
122	PIO1_17	2270.5	1749.4
123	PIO1_18	2372.5	1799.4

Pad	Signal Name	From Origin X (µm)	From Origin Y (µm)
124	PIO1_19	2270.5	1849.8
125	PIO1_20	2372.5	1899.8
126	VCCIO_1	2270.5	1949.8
127	VCCIO_1	2372.5	1999.8
128	GND	2270.5	2049.8
129	GND	2372.5	2099.8
130	VPP_2V5	2270.5	2199.8
131	VPP_FAST	1992	2300.5
132	VCC	1884	2402.5
133	VCC	1834	2300.5
134	PIO0_00	1784	2402.5
135	PIO0_01	1734	2300.5
136	PIO0_02	1684	2402.5
137	PIO0_03	1634	2300.5
138	PIO0_04	1584	2402.5
139	PIO0_05	1534	2300.5
140	PIO0_06	1499	2402.5
141	GND	1464	2300.5
142	GND	1429	2402.5
143	PIO0_07	1394	2300.5
144	PIO0_08	1359	2402.5
145	PIO0_09	1324	2300.5
146	PIO0_10	1289	2402.5
147	VCCIO_0	1254	2300.5
148	VCCIO_0	1219	2402.5
149	GBIN1/PIO0_11	1184	2300.5
150	GBIN0/PIO0_12	1149	2402.5
151	GND	865	2300.5
152	GND	830	2402.5
153	PIO0_13	795	2300.5
154	VCCIO_0	760	2402.5
155	VCCIO_0	725	2300.5
156	PIO0_14	690	2402.5
157	PIO0_15	655	2300.5
158	PIO0_16	620	2402.5
159	PIO0_17	585	2300.5
160	PIO0_18	535	2402.5
161	VCCIO_0	760	2402.5
162	GND	435	2402.5
163	PIO0_19	385	2300.5
164	PIO0_20	335	2402.5
165	PIO0_21	285	2300.5
166	PIO0_22	235	2402.5

Physical Specifications: iCE65L04

Figure 12 shows the physical outlines of iCE65L04 die on a wafer, including pad orientation and physical origin. The bond pad identification and coordinates are provided in Table 7. Table 5 lists key physical characteristics of each iCE65 die.

Figure 12: **iCE65L04 Die Outline**



Bond Pad Listing and Coordinates: iCE68L04

Table 7 lists each of the 254 bonding pads on an iCE65L04 device. The pad number begins in the upper left corner of the die, as shown in Figure 12, and increments in a counter-clockwise direction around the perimeter of the die. . Each bonding pad is identified. Signal names are color-coded by function. I/O pairs are grouped together with a thick surrounding box. These pairs in I/O Bank 3 represent an optional differential input or output. In all other banks, these pairs represent an optional differential output. The pad coordinates are measured relative to the origin, in the lower left corner of the die.

Table 7: **iCE65L04 Bond Pad Listing and Coordinates (Relative to Origin)**

Pad	Signal Name	From Origin	
		X (µm)	Y (µm)
1	PIO3_00/DP00A	129.40	2,687.75
2	PIO3_01/DP00B	231.40	2,642.74
3	PIO3_02/DP01A	129.40	2,597.75
4	PIO3_03/DP01B	231.40	2,552.74
5	GND	129.40	2,507.75
6	GND	231.40	2,462.74
7	VCCIO_3	129.40	2,417.75
8	VCCIO_3	231.40	2,372.74
9	PIO3_04/DP02A	129.40	2,327.75
10	PIO3_05/DP02B	231.40	2,292.74
11	PIO3_06/DP03A	129.40	2,257.75
12	PIO3_07/DP03B	231.40	2,222.74
13	VCC	129.40	2,187.75
14	PIO3_08/DP04A	231.40	2,152.74
15	PIO3_09/DP04B	129.40	2,117.75
16	PIO3_10/DP05A	231.40	2,082.74
17	PIO3_11/DP05B	129.40	2,047.75
18	GND	231.40	2,012.74
19	PIO3_12/DP06A	129.40	1,977.75
20	PIO3_13/DP06B	231.40	1,942.74
21	GND	129.40	1,907.75
22	GND	231.40	1,872.74
23	PIO3_14/DP07A	129.40	1,837.75
24	PIO3_15/DP07B	231.40	1,802.74
25	VCCIO_3	129.40	1,767.75
26	VCC	231.40	1,732.74
27	PIO3_16/DP08A	129.40	1,697.75
28	PIO3_17/DP08B	231.40	1,662.74
29	PIO3_18/DP09A	129.40	1,627.75
30	GBIN7/PIO3_19/DP09B	231.40	1,592.74
31	VCCIO_3	129.40	1,557.75
32	VREF	231.40	1,522.74
33	GND	129.40	1,487.75
34	GBIN6/PIO3_20/DP10A	231.40	1,452.74
35	PIO3_21/DP10B	129.40	1,417.75
36	GND	231.40	1,382.74
37	PIO3_22/DP11A	129.40	1,347.75
38	PIO3_23/DP11B	231.40	1,312.74
39	VCCIO_3	129.40	1,277.75
40	VCCIO_3	231.40	1,242.74
41	GND	129.40	1,207.75
42	GND	231.40	1,172.74
43	PIO3_24/DP12A	129.40	1,137.75
44	PIO3_25/DP12B	231.40	1,102.74
45	GND	129.40	1,067.75
46	PIO3_26/DP13A	231.40	1,032.74
47	PIO3_27/DP13B	129.40	997.75
48	PIO3_28/DP14A	231.40	962.74
49	PIO3_29/DP14B	129.40	927.75
50	PIO3_30/DP15A	231.40	892.74
51	PIO3_31/DP15B	129.40	857.75
52	VCC	231.40	822.74
53	PIO3_32/DP16A	129.40	787.75
54	PIO3_33/DP16B	231.40	752.74
55	VCCIO_3	129.40	717.75
56	VCCIO_3	231.40	682.74
57	GND	129.40	637.75
58	GND	231.40	592.74
59	PIO3_34/DP17A	129.40	547.75
60	PIO3_35/DP17B	231.40	502.74
61	PIO3_36/DP18A	129.40	457.75
62	PIO3_37/DP18B	231.40	412.74
63	PIO3_38/DP19A	129.40	367.75
64	PIO3_39/DP19B	231.40	322.74
65	PIO2_00	545.00	139.20
66	PIO2_01	595.00	37.20
67	PIO2_02	645.00	139.20
68	GND	695.00	37.20
69	PIO2_03	745.00	139.20
70	PIO2_04	795.00	37.20
71	PIO2_05	845.00	139.20
72	PIO2_06	895.00	37.20
73	PIO2_07	930.00	139.20
74	PIO2_08	965.00	37.20
75	VCCIO_2	1,000.00	139.20
76	PIO2_09	1,035.00	37.20
77	PIO2_10	1,070.00	139.20

Pad	Signal Name	From Origin X (µm)	From Origin Y (µm)
78	GND	1,105.00	37.20
79	PIO2_11	1,140.00	139.20
80	PIO2_12	1,175.00	37.20
81	PIO2_13	1,210.00	139.20
82	PIO2_14	1,245.00	37.20
83	PIO2_15	1,280.00	139.20
84	PIO2_16	1,315.00	37.20
85	PIO2_17	1,350.00	139.20
86	PIO2_18	1,385.00	37.20
87	GND	1,420.00	139.20
88	PIO2_19	1,455.00	37.20
89	PIO2_20	1,490.00	139.20
90	VCC	1,525.00	37.20
91	PIO2_21	1,560.00	139.20
92	PIO2_22	1,595.00	37.20
93	GBIN5/PIO2_23	1,630.00	139.20
94	GBIN4/PIO2_24	1,665.00	37.20
95	PIO2_25	1,700.00	139.20
96	VCCIO_2	1,735.00	37.20
97	PIO2_26	1,770.00	139.20
98	PIO2_27	1,805.00	37.20
99	GND	1,840.00	139.20
100	PIO2_28	1,875.00	37.20
101	PIO2_29	1,910.00	139.20
102	PIO2_30	1,945.00	37.20
103	PIO2_31	1,980.00	139.20
104	PIO2_32	2,015.00	37.20
105	PIO2_33	2,050.00	139.20
106	PIO2_34	2,085.00	37.20
107	PIO2_35	2,120.00	139.20
108	VCC	2,155.00	37.20
109	VCC	2,190.00	139.20
110	PIO2_36	2,225.00	37.20
111	PIO2_37	2,260.00	139.20
112	VCCIO_2	2,295.00	37.20
113	PIO2_38	2,330.00	139.20
114	GND	2,365.00	37.20
115	PIO2_39	2,400.00	139.20
116	PIO2_40	2,435.00	37.20
117	PIO2_41	2,470.00	139.20
118	PIO2_42/CBSEL0	2,505.00	37.20
119	PIO2_43/CBSEL1	2,540.00	139.20
120	CDONE	2,575.00	37.20
121	CRESET_B	2,625.00	139.20
122	PIOS_00/SPI_SO	2,690.00	37.20
123	PIOS_01/SPI_SI	2,740.00	139.20
124	GND	2,790.00	37.20

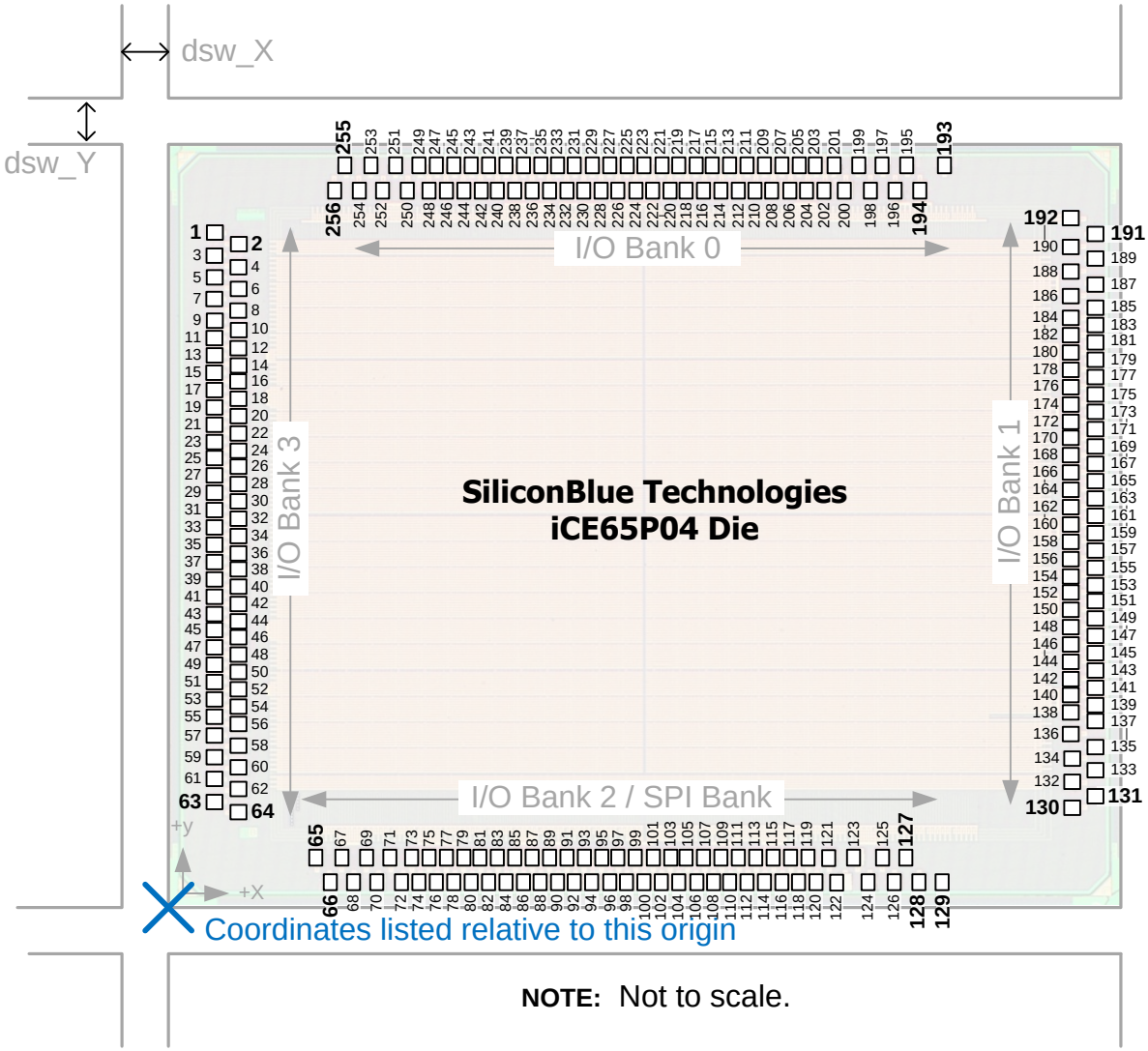
Pad	Signal Name	From Origin X (µm)	From Origin Y (µm)
125	PIOS_02/SPI_SCK	2,840.00	139.20
126	PIOS_03/SPI_SS_B	2,890.00	37.20
127	SPI_VCC	2,990.00	37.20
128	TDI	3,610.80	342.00
129	TMS	3,712.80	392.00
130	TCK	3,610.80	442.00
131	TDO	3,712.80	492.00
132	TRST_B	3,610.80	542.00
133	PIO1_00	3,712.80	592.00
134	PIO1_01	3,610.80	642.00
135	PIO1_02	3,712.80	692.00
136	PIO1_03	3,610.80	727.00
137	GND	3,712.80	762.00
138	GND	3,610.80	797.00
139	PIO1_04	3,712.80	832.00
140	PIO1_05	3,610.80	867.00
141	VCCIO_1	3,712.80	902.00
142	VCCIO_1	3,610.80	937.00
143	PIO1_06	3,712.80	972.00
144	PIO1_07	3,610.80	1,007.00
145	PIO1_08	3,712.80	1,042.00
146	PIO1_09	3,610.80	1,077.00
147	PIO1_10	3,712.80	1,112.00
148	VCC	3,610.80	1,147.00
149	VCC	3,712.80	1,182.00
150	PIO1_11	3,610.80	1,217.00
151	PIO1_12	3,712.80	1,252.00
152	PIO1_13	3,610.80	1,287.00
153	PIO1_14	3,712.80	1,322.00
154	PIO1_15	3,610.80	1,357.00
155	PIO1_16	3,712.80	1,392.00
156	PIO1_17	3,610.80	1,427.00
157	GND	3,712.80	1,462.00
158	GND	3,610.80	1,497.00
159	PIO1_18	3,712.80	1,532.00
160	GBIN3/PIO1_19	3,610.80	1,567.00
161	GBIN2/PIO1_20	3,712.80	1,602.00
162	PIO1_21	3,610.80	1,637.00
163	VCCIO_1	3,712.80	1,672.00
164	VCCIO_1	3,610.80	1,707.00
165	PIO1_22	3,712.80	1,742.00
166	PIO1_23	3,610.80	1,777.00
167	PIO1_24	3,712.80	1,812.00
168	PIO1_25	3,610.80	1,847.00
169	PIO1_26	3,712.80	1,882.00
170	PIO1_27	3,610.80	1,917.00
171	GND	3,712.80	1,952.00

Pad	Signal Name	From Origin	
		X (µm)	Y (µm)
172	GND	3,610.80	1,987.00
173	PIO1_28	3,712.80	2,022.00
174	PIO1_29	3,610.80	2,057.00
175	PIO1_30	3,712.80	2,092.00
176	PIO1_31	3,610.80	2,127.00
177	VCC	3,712.80	2,162.00
178	VCC	3,610.80	2,197.00
179	PIO1_32	3,712.80	2,232.00
180	PIO1_33	3,610.80	2,267.00
181	VCCIO_1	3,712.80	2,302.00
182	VCCIO_1	3,610.80	2,337.00
183	PIO1_34	3,712.80	2,377.00
184	PIO1_35	3,610.80	2,427.00
185	GND	3,712.80	2,477.00
186	PIO1_36	3,610.80	2,527.00
187	PIO1_37	3,712.80	2,577.00
188	PIO1_38	3,610.80	2,627.00
189	PIO1_39	3,712.80	2,677.00
190	VPP_2V5	3,610.80	2,739.68
191	VPP_FAST	3,047.00	2,962.80
192	VCC	2,997.00	2,860.80
193	VCC	2,947.00	2,962.80
194	PIO0_00	2,897.00	2,860.80
195	PIO0_01	2,847.00	2,962.80
196	PIO0_02	2,797.00	2,860.80
197	PIO0_03	2,747.00	2,962.80
198	PIO0_04	2,697.00	2,860.80
199	PIO0_05	2,647.00	2,962.80
200	PIO0_06	2,612.00	2,860.80
201	PIO0_07	2,577.00	2,962.80
202	GND	2,542.00	2,860.80
203	GND	2,507.00	2,962.80
204	PIO0_08	2,472.00	2,860.80
205	PIO0_09	2,437.00	2,962.80
206	PIO0_10	2,402.00	2,860.80
207	PIO0_11	2,367.00	2,962.80
208	PIO0_12	2,332.00	2,860.80
209	PIO0_13	2,297.00	2,962.80
210	PIO0_14	2,262.00	2,860.80
211	PIO0_15	2,227.00	2,962.80
212	VCCIO_0	2,192.00	2,860.80
213	VCCIO_0	2,157.00	2,962.80
214	PIO0_16	2,122.00	2,860.80
215	PIO0_17	2,087.00	2,962.80
216	PIO0_18	2,052.00	2,860.80
217	PIO0_19	2,017.00	2,962.80
218	PIO0_20	1,982.00	2,860.80
219	PIO0_21	1,947.00	2,962.80
220	PIO0_22	1,912.00	2,860.80
221	GBIN1/PIO0_23	1,877.00	2,962.80
222	GND	1,842.00	2,860.80
223	GND	1,807.00	2,962.80
224	GBIN0/PIO0_24	1,772.00	2,860.80
225	PIO0_25	1,737.00	2,962.80
226	PIO0_26	1,702.00	2,860.80
227	PIO0_27	1,667.00	2,962.80
228	VCC	1,632.00	2,860.80
229	VCC	1,597.00	2,962.80
230	PIO0_28	1,562.00	2,860.80
231	PIO0_29	1,527.00	2,962.80
232	PIO0_30	1,492.00	2,860.80
233	PIO0_31	1,457.00	2,962.80
234	GND	1,422.00	2,860.80
235	GND	1,387.00	2,962.80
236	PIO0_32	1,352.00	2,860.80
237	PIO0_33	1,317.00	2,962.80
238	PIO0_34	1,282.00	2,860.80
239	PIO0_35	1,247.00	2,962.80
240	PIO0_36	1,212.00	2,860.80
241	VCCIO_0	1,177.00	2,962.80
242	VCCIO_0	1,142.00	2,860.80
243	PIO0_37	1,107.00	2,962.80
244	PIO0_38	1,072.00	2,860.80
245	PIO0_39	1,037.00	2,962.80
246	PIO0_40	1,002.00	2,860.80
247	PIO0_41	967.00	2,962.80
248	PIO0_42	917.00	2,860.80
249	GND	867.00	2,962.80
250	PIO0_43	817.00	2,860.80
251	PIO0_44	767.00	2,962.80
252	PIO0_45	717.00	2,860.80
253	PIO0_46	667.00	2,962.80
254	PIO0_47	617.00	2,860.80

Physical Specifications: iCE65P04

Figure 13 shows the physical outlines of iCE65P04 die on a wafer, including pad orientation and physical origin. The bond pad identification and coordinates are provided Table 8. Table 5 lists key physical characteristics of each iCE65 die.

Figure 13: **iCE65P04 Die Outline**



Bond Pad Listing and Coordinates: iCE65P04

Table 8 lists each of the 256 bonding pads on an iCE65P04 device. The pad number begins in the upper left corner of the die, as shown in Figure 13, and increments in a counter-clockwise direction around the perimeter of the die. . Each bonding pad is identified. Signal names are color-coded by function. I/O pairs are grouped together with a thick surrounding box. These pairs in I/O Bank 3 represent an optional differential input or output. In all other banks, these pairs represent an optional differential output. The pad coordinates are measured relative to the origin, in the lower left corner of the die.

Table 8: **iCE65P04 Bond Pad Listing and Coordinates (Relative to Origin)**

Pad	Signal Name	From Origin	
		X (µm)	Y (µm)
1	PIO3_00/DP00A	129.4	2687.75
2	PIO3_01/DP00B	231.4	2642.74
3	PIO3_02/DP01A	129.4	2597.75
4	PIO3_03/DP01B	231.4	2552.74
5	GND	129.4	2507.75
6	GND	231.4	2462.74
7	VCCIO_3	129.4	2417.75
8	VCCIO_3	231.4	2372.74
9	PIO3_04/DP02A	129.4	2327.75
10	PIO3_05/DP02B	231.4	2292.74
11	PIO3_06/DP03A	129.4	2257.75
12	PIO3_07/DP03B	231.4	2222.74
13	VCC	129.4	2187.75
14	PIO3_08/DP04A	231.4	2152.74
15	PIO3_09/DP04B	129.4	2117.75
16	PIO3_10/DP05A	231.4	2082.74
17	PIO3_11/DP05B	129.4	2047.75
18	GND	231.4	2012.74
19	PIO3_12/DP06A	129.4	1977.75
20	PIO3_13/DP06B	231.4	1942.74
21	GND	129.4	1907.75
22	GND	231.4	1872.74
23	PIO3_14/DP07A	129.4	1837.75
24	PIO3_15/DP07B	231.4	1802.74
25	VCCIO_3	129.4	1767.75
26	VCC	231.4	1732.74
27	PIO3_16/DP08A	129.4	1697.75
28	PIO3_17/DP08B	231.4	1662.74
29	PIO3_18/DP09A	129.4	1627.75
30	GBIN7/PIO3_19/DP09B	231.4	1592.74
31	VCCIO_3	129.4	1557.75
32	VREF	231.4	1522.74
33	GND	129.4	1487.75
34	GBIN6/PIO3_20/DP10A	231.4	1452.74
35	PIO3_21/DP10B	129.4	1417.75
36	GND	231.4	1382.74
37	PIO3_22/DP11A	129.4	1347.75
38	PIO3_23/DP11B	231.4	1312.74
39	VCCIO_3	129.4	1277.75
40	VCCIO_3	231.4	1242.74
41	GND	129.4	1207.75
42	GND	231.4	1172.74
43	PIO3_24/DP12A	129.4	1137.75
44	PIO3_25/DP12B	231.4	1102.74
45	GND	129.4	1067.75
46	PIO3_26/DP13A	231.4	1032.74
47	PIO3_27/DP13B	129.4	997.75
48	PIO3_28/DP14A	231.4	962.74
49	PIO3_29/DP14B	129.4	927.75
50	PIO3_30/DP15A	231.4	892.74
51	PIO3_31/DP15B	129.4	857.75
52	VCC	231.4	822.74
53	PIO3_32/DP16A	129.4	787.75
54	PIO3_33/DP16B	231.4	752.74
55	VCCIO_3	129.4	717.75
56	VCCIO_3	231.4	682.74
57	GND	129.4	637.75
58	GND	231.4	592.74
59	PIO3_34/DP17A	129.4	547.75
60	PIO3_35/DP17B	231.4	502.74
61	PIO3_36/DP18A	129.4	457.75
62	PIO3_37/DP18B	231.4	412.74
63	PIO3_38/DP19A	129.4	367.75
64	PIO3_39/DP19B	231.4	322.74
65	PIO2_00	440	139.2
66	PIO2_01	490	37.2
67	PIO2_02	540	139.2
68	GND	590	37.2
69	PIO2_03	640	139.2
70	PIO2_04	690	37.2
71	PIO2_05	740	139.2
72	PIO2_06	790	37.2
73	PIO2_07	825	139.2
74	PIO2_08	860	37.2
75	VCCIO_2	895	139.2
76	PIO2_09	930	37.2
77	PIO2_10	965	139.2

Pad	Signal Name	From Origin X (µm)	From Origin Y (µm)
78	GND	1000	37.2
79	PIO2_11	1035	139.2
80	PIO2_12	1070	37.2
81	PIO2_13	1105	139.2
82	PIO2_14	1140	37.2
83	PIO2_15	1175	139.2
84	PIO2_16	1210	37.2
85	PIO2_17	1245	139.2
86	PIO2_18	1280	37.2
87	GND	1315	139.2
88	PIO2_19	1350	37.2
89	PIO2_20	1385	139.2
90	VCC	1420	37.2
91	PIO2_21	1455	139.2
92	PIO2_22	1490	37.2
93	PLLGND	1525	139.2
94	PLLVCC	1595	37.2
95	GBIN5/PIO2_23	1630	139.2
96	GBIN4/PIO2_24	1665	37.2
97	PIO2_25	1700	139.2
98	VCCIO_2	1735	37.2
99	PIO2_26	1770	139.2
100	PIO2_27	1805	37.2
101	GND	1840	139.2
102	PIO2_28	1875	37.2
103	PIO2_29	1910	139.2
104	PIO2_30	1945	37.2
105	PIO2_31	1980	139.2
106	PIO2_32	2015	37.2
107	PIO2_33	2050	139.2
108	PIO2_34	2085	37.2
109	PIO2_35	2120	139.2
110	VCC	2155	37.2
111	VCC	2190	139.2
112	PIO2_36	2225	37.2
113	PIO2_37	2260	139.2
114	VCCIO_2	2295	37.2
115	PIO2_38	2330	139.2
116	GND	2365	37.2
117	PIO2_39	2400	139.2
118	PIO2_40	2435	37.2
119	PIO2_41	2470	139.2
120	PIO2_42/CBSEL0	2505	37.2
121	PIO2_43/CBSEL1	2540	139.2
122	CDONE	2575	37.2
123	CRESET_B	2625	139.2
124	PIOS_00/SPI_SO	2690	37.2
125	PIOS_01/SPI_SI	2740	139.2
126	GND	2790	37.2
127	PIOS_02/SPI_SCK	2840	139.2
128	PIOS_03/SPI_SS_B	2890	37.2
129	SPI_VCC	2990	37.2
130	TDI	3,610.80	342.00
131	TMS	3,712.80	392.00
132	TCK	3,610.80	442.00
133	TDO	3,712.80	492.00
134	TRST_B	3,610.80	542.00
135	PIO1_00	3,712.80	592.00
136	PIO1_01	3,610.80	642.00
137	PIO1_02	3,712.80	692.00
138	PIO1_03	3,610.80	727.00
139	GND	3,712.80	762.00
140	GND	3,610.80	797.00
141	PIO1_04	3,712.80	832.00
142	PIO1_05	3,610.80	867.00
143	VCCIO_1	3,712.80	902.00
144	VCCIO_1	3,610.80	937.00
145	PIO1_06	3,712.80	972.00
146	PIO1_07	3,610.80	1,007.00
147	PIO1_08	3,712.80	1,042.00
148	PIO1_09	3,610.80	1,077.00
149	PIO1_10	3,712.80	1,112.00
150	VCC	3,610.80	1,147.00
151	VCC	3,712.80	1,182.00
152	PIO1_11	3,610.80	1,217.00
153	PIO1_12	3,712.80	1,252.00
154	PIO1_13	3,610.80	1,287.00
155	PIO1_14	3,712.80	1,322.00
156	PIO1_15	3,610.80	1,357.00
157	PIO1_16	3,712.80	1,392.00
158	PIO1_17	3,610.80	1,427.00
159	GND	3,712.80	1,462.00
160	GND	3,610.80	1,497.00
161	PIO1_18	3,712.80	1,532.00
162	GBIN3/PIO1_19	3,610.80	1,567.00
163	GBIN2/PIO1_20	3,712.80	1,602.00
164	PIO1_21	3,610.80	1,637.00
165	VCCIO_1	3,712.80	1,672.00
166	VCCIO_1	3,610.80	1,707.00
167	PIO1_22	3,712.80	1,742.00
168	PIO1_23	3,610.80	1,777.00
169	PIO1_24	3,712.80	1,812.00
170	PIO1_25	3,610.80	1,847.00
171	PIO1_26	3,712.80	1,882.00

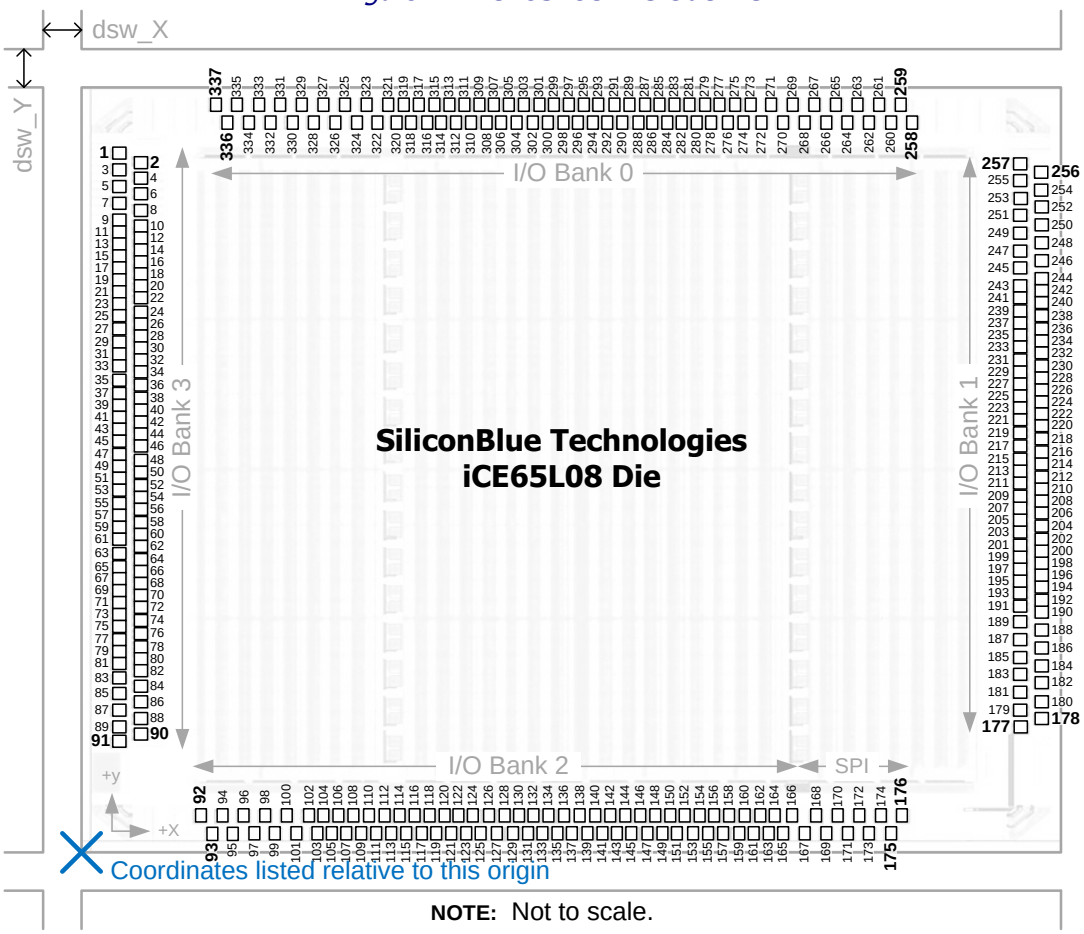
Pad	Signal Name	From Origin X (µm)	From Origin Y (µm)
172	PIO1_27	3,610.80	1,917.00
173	GND	3,712.80	1,952.00
174	GND	3,610.80	1,987.00
175	PIO1_28	3,712.80	2,022.00
176	PIO1_29	3,610.80	2,057.00
177	PIO1_30	3,712.80	2,092.00
178	PIO1_31	3,610.80	2,127.00
179	VCC	3,712.80	2,162.00
180	VCC	3,610.80	2,197.00
181	PIO1_32	3,712.80	2,232.00
182	PIO1_33	3,610.80	2,267.00
183	VCCIO_1	3,712.80	2,302.00
184	VCCIO_1	3,610.80	2,337.00
185	PIO1_34	3,712.80	2,377.00
186	PIO1_35	3,610.80	2,427.00
187	GND	3,712.80	2,477.00
188	PIO1_36	3,610.80	2,527.00
189	PIO1_37	3,712.80	2,577.00
190	PIO1_38	3,610.80	2,627.00
191	PIO1_39	3,712.80	2,677.00
192	VPP_2V5	3,610.80	2,739.68
193	VPP_FAST	3,096.90	2,962.80
194	VCC	2,997.00	2,860.80
195	VCC	2,947.00	2,962.80
196	PIO0_00	2,897.00	2,860.80
197	PIO0_01	2,847.00	2,962.80
198	PIO0_02	2,797.00	2,860.80
199	PIO0_03	2,747.00	2,962.80
200	PIO0_04	2,697.00	2,860.80
201	PIO0_05	2,647.00	2,962.80
202	PIO0_06	2,612.00	2,860.80
203	PIO0_07	2,577.00	2,962.80
204	GND	2,542.00	2,860.80
205	GND	2,507.00	2,962.80
206	PIO0_08	2,472.00	2,860.80
207	PIO0_09	2,437.00	2,962.80
208	PIO0_10	2,402.00	2,860.80
209	PIO0_11	2,367.00	2,962.80
210	PIO0_12	2,332.00	2,860.80
211	PIO0_13	2,297.00	2,962.80
212	PIO0_14	2,262.00	2,860.80
213	PIO0_15	2,227.00	2,962.80
214	VCCIO_0	2,192.00	2,860.80
215	VCCIO_0	2,157.00	2,962.80
216	PIO0_16	2,122.00	2,860.80
217	PIO0_17	2,087.00	2,962.80

Pad	Signal Name	From Origin X (µm)	From Origin Y (µm)
218	PIO0_18	2,052.00	2,860.80
219	PIO0_19	2,017.00	2,962.80
220	PIO0_20	1,982.00	2,860.80
221	PIO0_21	1,947.00	2,962.80
222	PIO0_22	1,912.00	2,860.80
223	GBIN1/PIO0_23	1,877.00	2,962.80
224	GND	1,842.00	2,860.80
225	GND	1,807.00	2,962.80
226	GBIN0/PIO0_24	1,772.00	2,860.80
227	PIO0_25	1,737.00	2,962.80
228	PIO0_26	1,702.00	2,860.80
229	PIO0_27	1,667.00	2,962.80
230	VCC	1,632.00	2,860.80
231	VCC	1,597.00	2,962.80
232	PIO0_28	1,562.00	2,860.80
233	PIO0_29	1,527.00	2,962.80
234	PIO0_30	1,492.00	2,860.80
235	PIO0_31	1,457.00	2,962.80
236	GND	1,422.00	2,860.80
237	GND	1,387.00	2,962.80
238	PIO0_32	1,352.00	2,860.80
239	PIO0_33	1,317.00	2,962.80
240	PIO0_34	1,282.00	2,860.80
241	PIO0_35	1,247.00	2,962.80
242	PIO0_36	1,212.00	2,860.80
243	VCCIO_0	1,177.00	2,962.80
244	VCCIO_0	1,142.00	2,860.80
245	PIO0_37	1,107.00	2,962.80
246	PIO0_38	1,072.00	2,860.80
247	PIO0_39	1,037.00	2,962.80
248	PIO0_40	1,002.00	2, 860.80
249	PIO0_41	967.00	2,962.80
250	PIO0_42	917.00	2,860.80
251	GND	867.00	2,962.80
252	PIO0_43	817.00	2,860.80
253	PIO0_44	767.00	2,962.80
254	PIO0_45	717.00	2,860.80
255	PIO0_46	667.00	2,962.80
256	PIO0_47	617.00	2,860.80

Physical Specifications: iCE65L08

Figure 14 shows the physical outlines of iCE65L08 die on a wafer, including pad orientation and physical origin. The bond pad identification and coordinates are provided in Table 9. Table 5 lists key physical characteristics of each iCE65 die.

Figure 14: **iCE65L08 Die Outline**



Bond Pad Listing and Coordinates

Table 9 lists each of the 337 bonding pads on an iCE65L08 device. The pad number begins in the upper left corner of the die, as shown in Figure 14 and increments in a counter-clockwise direction around the perimeter of the die. Each bonding pad is identified. Signal names are color-coded by function. I/O pairs are grouped together with a thick surrounding box. These pairs in I/O Bank 3 represent an optional differential input or output. In all other banks, these pairs represent an optional differential output. The pad coordinates are measured relative to the origin, in the lower left corner of the die.

Table 9: **iCE65L08 Bond Pad Listing and Coordinates (Relative to Origin)**

Pad	Signal Name	From Origin X (µm)	From Origin Y (µm)
1	PIO3_00/DP00A	129.735	3,882.665
2	PIO3_01/DP00B	231.735	3,837.665
3	PIO3_02/DP01A	129.735	3,792.665
4	PIO3_03/DP01B	231.735	3,747.665
5	GND (Post)	129.735	3,702.665
6	GND (Post)	231.735	3,657.665
7	VCCIO_3 (Post)	129.735	3,612.665
8	VCCIO_3 (Post)	231.735	3,567.665
9	PIO3_04/DP02A	129.735	3,512.665
10	PIO3_05/DP02B	231.735	3,477.665
11	PIO3_06/DP03A	129.735	3,442.665
12	PIO3_07/DP03B	231.735	3,407.665
13	VCC (Core)	129.735	3,372.665
14	VCC (Pre)	231.735	3,337.665
15	PIO3_08/DP04A	129.735	3,302.665
16	PIO3_09/DP04B	231.735	3,267.665
17	PIO3_10/DP05A	129.735	3,232.665
18	PIO3_11/DP05B	231.735	3,197.665
19	GND (Pre)	129.735	3,162.665
20	GND (Core)	231.735	3,127.665
21	PIO3_12/DP06A	129.735	3,092.665
22	PIO3_13/DP06B	231.735	3,057.665
23	GND (Post)	129.735	3,022.665
24	GND (Post)	231.735	2,987.665
25	PIO3_14/DP07A	129.735	2,952.665
26	PIO3_15/DP07B	231.735	2,917.665
27	VCCIO_3 (Post)	129.735	2,882.665
28	VCCIO_3 (Post)	231.735	2,847.665
29	VCC (Pre)	129.735	2,812.665
30	VCC (Pre)	231.735	2,777.665
31	PIO3_16/DP08A	129.735	2,742.665
32	PIO3_17/DP08B	231.735	2,707.665
33	VCCIO_3 (Level)	129.735	2,672.665
34	VCCIO_3 (Level)	231.735	2,637.665
35	GND (Pre)	129.735	2,602.665
36	GND (Pre)	231.735	2,567.665
37	PIO3_18/DP09A	129.735	2,532.665
38	PIO3_19/DP09B	231.735	2,497.665
39	PIO3_20/DP10A	129.735	2,462.665
40	PIO3_21/DP10B	231.735	2,427.665
41	PIO3_22/DP11A	129.735	2,392.665
42	PIO3_23/DP11B	231.735	2,357.665
43	VCCIO_3 (Level)	129.735	2,322.665
44	VCCIO_3 (Level)	231.735	2,287.665
45	VREF	129.735	2,252.665
46	VREF	231.735	2,217.665
47	GND (Shield)	129.735	2,182.665
48	GND (Pre)	231.735	2,147.665
49	VCCIO_3 (Post)	129.735	2,112.665
50	VCCIO_3 (Post)	231.735	2,077.665
51	GND (Post)	129.735	2,042.665
52	GND (Post)	231.735	2,007.665
53	PIO3_24/DP12A	129.735	1,972.665
54	GBIN7/ PIO3_25/DP12B	231.735	1,937.665
55	GND (Core)	129.735	1,902.665
56	GBIN6/ PIO3_26/DP13A	231.735	1,867.665
57	PIO3_27/DP13B	129.735	1,832.665
58	PIO3_28/DP14A	231.735	1,798.665
59	PIO3_29/DP14B	129.735	1,762.665
60	PIO3_30/DP15A	231.735	1,727.665
61	PIO3_31/DP15B	129.735	1,692.665
62	GND (Pre)	231.735	1,657.665
63	GND (Pre)	129.735	1,622.665
64	PIO3_32/DP16A	231.735	1,587.665
65	PIO3_33/DP16B	129.735	1,552.665
66	VCCIO_3 (Post)	231.735	1,517.665
67	VCCIO_3 (Post)	129.735	1,482.665
68	GND (Post)	231.735	1,447.665
69	GND (Post)	129.735	1,412.665
70	PIO3_34/DP17A	231.735	1,377.665
71	PIO3_35/DP17B	129.735	1,342.665
72	PIO3_36/DP18A	231.735	1,307.665
73	PIO3_37/DP18B	129.735	1,272.665
74	PIO3_38/DP19A	231.735	1,237.665
75	PIO3_39/DP19B	129.735	1,202.665
76	PIO3_40/DP20A	231.735	1,167.665

Pad	Signal Name	From Origin X (µm)	From Origin Y (µm)
77	PIO3_41/DP20B	129.735	1,132.665
78	VCC (Pre)	231.735	1,097.665
79	VCC (Core)	129.735	1,062.665
80	PIO3_42/DP21A	231.735	1,027.665
81	PIO3_43/DP21B	129.735	992.665
82	VCCIO_3 (Post)	231.735	957.665
83	VCCIO_3 (Post)	129.735	912.665
84	GND (Post)	231.735	867.665
85	GND (Post)	129.735	822.67
86	PIO3_44/DP22A	231.735	777.67
87	PIO3_45/DP22B	129.735	732.67
88	PIO3_46/DP23A	231.735	687.67
89	PIO3_47/DP23B	129.735	642.67
90	PIO3_48/DP24A	231.735	597.67
91	PIO3_49/DP24B	129.735	552.665
92	PIO2_00	510.0	139.5
93	PIO2_01	560.0	37.5
94	PIO2_02	610.0	139.5
95	GND	660.0	37.5
96	GND	710.0	139.5
97	PIO2_03	760.0	37.5
98	PIO2_04	810.0	139.5
99	PIO2_05	859.3	37.5
100	PIO2_06	910.0	139.5
101	PIO2_07	960.0	37.5
102	PIO2_08	1,012.5	139.5
103	VCCIO_2	1,047.5	37.5
104	VCCIO_2	1,082.5	139.5
105	PIO2_09	1,117.5	37.5
106	PIO2_10	1,152.5	139.5
107	GND	1,187.5	37.5
108	GND	1,222.5	139.5
109	PIO2_11	1,257.5	37.5
110	PIO2_12	1,292.5	139.5
111	PIO2_13	1,327.5	37.5
112	PIO2_14	1,362.5	139.5
113	PIO2_15	1,397.5	37.5
114	PIO2_16	1,432.5	139.5
115	PIO2_17	1,467.5	37.5
116	PIO2_18	1,502.3	139.5
117	GND	1,537.3	37.5
118	GND	1,572.5	139.5
119	PIO2_19	1,607.5	37.5
120	PIO2_20	1,642.5	139.5
121	VCC	1,677.5	37.5
122	VCC	1,712.5	139.5
123	PIO2_21	1,747.5	37.5
124	PIO2_22	1,782.5	139.5
125	PIO2_23	1,817.5	37.5
126	PIO2_24	1,852.5	139.5
127	PIO2_25	1,887.5	37.5
128	PIO2_26	1,922.5	139.5
129	PIO2_27	1,957.5	37.5
130	VCCIO_2	1,992.5	139.5
131	VCCIO_2	2,027.5	37.5
132	PIO2_28	2,062.5	139.5
133	GBIN5/PIO2_29	2,097.5	37.5
134	GBIN4/PIO2_30	2,132.5	139.5
135	GND	2,167.5	37.5
136	GND	2,202.5	139.5
137	PIO2_31	2,237.5	37.5
138	PIO2_32	2,272.5	139.5
139	PIO2_33	2,307.5	37.5
140	PIO2_34	2,342.5	139.5
141	PIO2_35	2,377.5	37.5
142	PIO2_36	2,412.5	139.5
143	PIO2_37	2,447.5	37.5
144	PIO2_38	2,482.5	139.5
145	PIO2_39	2,517.5	37.5
146	PIO2_40	2,552.5	139.5
147	PIO2_41	2,587.5	37.5
148	PIO2_42	2,622.5	139.5
149	PIO2_43	2,657.5	37.5
150	PIO2_44	2,692.5	139.5
151	VCC	2,727.5	37.5
152	VCC	2,762.5	139.5
153	PIO2_45	2,797.5	37.5
154	PIO2_46	2,832.5	139.5
155	VCCIO_2	2,867.5	37.5
156	VCCIO_2	2,902.5	139.5
157	PIO2_47	2,937.5	37.5
158	GND	2,972.5	139.5
159	GND	3,007.5	37.5
160	PIO2_48	3,042.5	139.5
161	PIO2_49	3,077.5	37.5
162	PIO2_50	3,112.5	139.5
163	PIO2_51/CBSEL0	3,147.5	37.5
164	PIO2_52/CBSEL1	3,182.5	139.5
165	CDONE	3,217.5	37.5
166	CRESET_B	3,260.0	139.5
167	PIOS_00/SPI_SO	3,320.0	37.5
168	PIOS_01/SPI_SI	3,370.0	139.5
169	GND	3,420.0	37.5
170	GND	3,470.0	139.5

Pad	Signal Name	From Origin	
		X (µm)	Y (µm)
171	PIOS_02/SPI_SCK	3,520.0	37.5
172	PIOS_03/SPI_SS_B	3,570.0	139.5
173	VCC	3,620.0	37.5
174	VCC	3,670.0	139.5
175	SPI_VCC	3,720.0	37.5
176	SPI_VCC	3,770.0	139.5
177	TDI	4,470.5	634.615
178	TMS	4,572.5	684.615
179	TCK	4,470.5	734.615
180	TDO	4,572.5	784.615
181	TRST_B	4,470.5	834.615
182	PIO1_00	4,572.5	884.615
183	PIO1_01	4,470.5	934.615
184	PIO1_02	4,572.5	984.615
185	PIO1_03	4,470.5	1,034.615
186	GND	4,572.5	1,084.615
187	GND	4,470.5	1,134.615
188	PIO1_04	4,572.5	1,184.615
189	PIO1_05	4,470.5	1,234.62
190	VCCIO_1	4,572.5	1,287.115
191	VCCIO_1	4,470.5	1,322.115
192	PIO1_06	4,572.5	1,357.115
193	PIO1_07	4,470.5	1,392.115
194	PIO1_08	4,572.5	1,427.115
195	PIO1_09	4,470.5	1,462.115
196	PIO1_10	4,572.5	1,497.115
197	VCC	4,470.5	1,532.115
198	VCC	4,572.5	1,567.115
199	PIO1_11	4,470.5	1,602.115
200	PIO1_12	4,572.5	1,637.115
201	PIO1_13	4,470.5	1,672.115
202	PIO1_14	4,572.5	1,707.115
203	PIO1_15	4,470.5	1,742.115
204	PIO1_16	4,572.5	1,777.115
205	PIO1_17	4,470.5	1,812.115
206	PIO1_18	4,572.5	1,847.115
207	GND	4,470.5	1,882.115
208	GND	4,572.5	1,917.110
209	PIO1_19	4,470.5	1,952.115
210	PIO1_20	4,572.5	1,987.115
211	PIO1_21	4,470.5	2,022.115
212	PIO1_22	4,572.5	2,057.115
213	VCCIO_1	4,470.5	2,092.115
214	VCCIO_1	4,572.5	2,127.115
215	PIO1_23	4,470.5	2,162.115
216	PIO1_24	4,572.5	2,197.115
217	PIO1_25	4,470.5	2,232.115
218	PIO1_26	4,572.5	2,267.115
219	GBIN3/PIO1_27	4,470.5	2,302.11
220	GBIN2/PIO1_28	4,572.5	2,337.115
221	PIO1_29	4,470.5	2,372.115
222	PIO1_30	4,572.5	2,407.115
223	PIO1_31	4,470.5	2,442.115
224	PIO1_32	4,572.5	2,477.115
225	PIO1_33	4,470.5	2,512.115
226	PIO1_34	4,572.5	2,547.115
227	PIO1_35	4,470.5	2,582.115
228	GND	4,572.5	2,617.115
229	GND	4,470.5	2,652.115
230	PIO1_36	4,572.5	2,687.12
231	VCCIO_1	4,470.5	2,722.12
232	VCCIO_1	4,572.5	2,757.12
233	PIO1_37	4,470.5	2,792.12
234	PIO1_38	4,572.5	2,827.12
235	PIO1_39	4,470.5	2,862.12
236	PIO1_40	4,572.5	2,897.12
237	PIO1_41	4,470.5	2,932.12
238	PIO1_42	4,572.5	2,967.12
239	PIO1_43	4,470.5	3,002.12
240	PIO1_44	4,572.5	3,037.12
241	PIO1_45	4,470.5	3,072.12
242	PIO1_46	4,572.5	3,107.12
243	VCC	4,470.5	3,142.12
244	VCC	4,572.5	3,177.12
245	PIO1_47	4,470.5	3,229.615
246	PIO1_48	4,572.5	3,279.615
247	VCCIO_1	4,470.5	3,329.615
248	VCCIO_1	4,572.5	3,379.615
249	PIO1_49	4,470.5	3,429.62
250	PIO1_50	4,572.5	3,479.615
251	GND	4,470.5	3,529.615
252	GND	4,572.5	3,579.615
253	PIO1_51	4,470.5	3,629.615
254	PIO1_52	4,572.5	3,679.595
255	PIO1_53	4,470.5	3,729.595
256	PIO1_54	4,572.5	3,779.595
257	VPP_2V5	4,470.5	3,879.575
258	VPP_FAST	3,866.975	4,054.5
259	VCC	3,766.98	4,156.5
260	VCC	3,716.98	4,054.5
261	PIO0_00	3,666.98	4,156.5
262	PIO0_01	3,616.98	4,054.5
263	PIO0_02	3,566.98	4,156.5
264	PIO0_03	3,516.98	4,054.5
265	PIO0_04	3,466.98	4,156.5
266	VCCIO_0	3,416.98	4,054.5

Pad	Signal Name	From Origin	
		X (µm)	Y (µm)
267	PIO0_05	3,366.98	4,156.5
268	PIO0_06	3,316.98	4,054.5
269	PIO0_07	3,266.98	4,156.5
270	GND	3,216.98	4,054.5
271	GND	3,166.98	4,156.5
272	PIO0_08	3,116.98	4,054.5
273	PIO0_09	3,064.48	4,156.5
274	PIO0_10	3,029.48	4,054.5
275	PIO0_11	2,994.48	4,156.5
276	PIO0_12	2,959.48	4,054.5
277	PIO0_13	2,924.48	4,156.5
278	PIO0_14	2,889.48	4,054.5
279	PIO0_15	2,854.48	4,156.5
280	VCCIO_0	2,819.48	4,054.5
281	VCCIO_0	2,784.48	4,156.5
282	PIO0_16	2,749.48	4,054.5
283	PIO0_17	2,714.48	4,156.5
284	PIO0_18	2,679.48	4,054.5
285	PIO0_19	2,644.48	4,156.5
286	PIO0_20	2,609.48	4,054.5
287	PIO0_21	2,574.48	4,156.5
288	PIO0_22	2,539.48	4,054.5
289	PIO0_23	2,504.48	4,156.5
290	PIO0_24	2,469.48	4,054.5
291	PIO0_25	2,434.48	4,156.5
292	GND	2,399.48	4,054.5
293	GND	2,364.48	4,156.5
294	PIO0_26	2,329.48	4,054.5
295	PIO0_27	2,294.48	4,156.5
296	PIO0_28	2,259.48	4,054.5
297	GBIN1/PIO0_29	2,224.48	4,156.5
298	GBIN0/PIO0_30	2,189.48	4,054.5
299	PIO0_31	2,154.48	4,156.5
300	VCCIO_0	2,119.48	4,054.5
301	VCCIO_0	2,084.48	4,156.5
302	PIO0_32	2,049.48	4,054.5
303	PIO0_33	2,014.48	4,156.5
304	PIO0_34	1,979.48	4,054.5
305	PIO0_35	1,944.48	4,156.5

Pad	Signal Name	From Origin	
		X (µm)	Y (µm)
306	VCC	1,909.48	4,054.5
307	VCC	1,874.48	4,156.5
308	PIO0_36	1,839.48	4,054.5
309	PIO0_37	1,804.48	4,156.5
310	PIO0_38	1,769.48	4,054.5
311	PIO0_39	1,734.48	4,156.5
312	GND	1,699.48	4,054.5
313	GND	1,664.48	4,156.5
314	PIO0_40	1,629.48	4,054.5
315	PIO0_41	1,594.48	4,156.5
316	PIO0_42	1,559.48	4,054.5
317	PIO0_43	1,524.48	4,156.5
318	PIO0_44	1,489.48	4,054.5
319	PIO0_45	1,454.48	4,156.5
320	PIO0_46	1,419.48	4,054.5
321	PIO0_47	1,384.48	4,156.5
322	PIO0_48	1,331.98	4,054.5
323	VCCIO_0	1,281.98	4,156.5
324	VCCIO_0	1,231.98	4,054.5
325	PIO0_49	1,181.98	4,156.5
326	PIO0_50	1,131.98	4,054.5
327	PIO0_51	1,081.98	4,156.5
328	PIO0_52	1,031.98	4,054.5
329	PIO0_53	981.98	4,156.5
330	PIO0_54	931.98	4,054.5
331	GND	881.98	4,156.5
332	GND	831.98	4,054.5
333	PIO0_55	781.98	4,156.5
334	PIO0_56	731.98	4,054.5
335	PIO0_57	681.98	4,156.5
336	PIO0_58	631.98	4,054.5
337	PIO0_59	581.98	4,156.5

Die Testing Procedures

SiliconBlue Technologies die products are tested to ensure product functionality in our standard package. Each die has gone through wafer probe test of various functional and parametric conditions.

SiliconBlue Technologies retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed. SiliconBlue Technologies reserves the right to change the probe program at any time for continuous product improvement.

Die users may experience differences in performance relative to SiliconBlue Technologies' data sheets. This is due to differences in package capacitance, inductance, resistance, and trace length.

Product Reliability Monitors

Reliability of all packaged products is monitored by ongoing QRA reliability evaluations. From these evaluations, samples are subjected to a battery of tests known as "Accelerated Life and Environmental Stress Tests." During these tests, devices are stressed for many hours under conditions designed to simulate years of normal field use. A summary of these product family evaluations is published on a regular basis.

Storage Requirements

SiliconBlue Technologies' die products are packaged in a cleanroom environment for shipping. Upon receipt, transfer the die or wafers to a similar environment for storage. SiliconBlue Technologies recommends that the die or wafers be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30% ±10% relative humidity. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

Revision History

Version	Date	Description
2.0.6	25-JAN-2011	Removed P, Waffle Pack option from Ordering Codes Figure 10. Updated CC72 Ball Diameter Figure 9
2.0.5	7-JAN-2011	Made minor correction to Figure 13.
2.0.4	23-AUG-2010	Updated Figure 7 CS63 Package Mechanical Drawing
2.0.3	1-JUL-2010	Removed *Production Qualification scheduled to complete in June 2010. Table 1 Increased WLCSP thickness with Top-side coating, Figures 5, 7, & 9
2.0.2	1-JUN-2010	Changed iCE65P04 Known Good Die, KGD I/O Pads from 174 to 176 in Table 1.
2.0.1	1-JUN-2010	Changed Wafer Thickness in Table 5 to 31 mil, 10 mil, or 4 mil.
2.0	13-MAY-2010	Removed PRELIMINARY. Added devices: iCE65L01 die and WLCSP CS36, iCE65P04 die.
1.0	28-JAN-2010	Initial DiePlus Release combines WLCSP from May 7, 2009 (1.5) iCE65 Family Data Sheet, February 24, 2009 (1.5.1) iCE DiCE iCE65L04 Data Sheet and July 27, 2009 (1.1) iCE DiCE iCE65L08 Data Sheet.

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