MachXO3D Device Family

Data Sheet

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AES	Advanced Encryption Standard
BGA	Ball Grid Array
BLVDS	Bidirectional Low Voltage Differential Signaling
CMOS	Complementary Metal Oxide Semiconductor
EBR	Embedded Block RAM
ECDSA	Elliptic Curve Digital Signature Algorithm
ECDH	Elliptic Curve Diffie-Hellman
ECIES	Elliptic Curve Integrated Encryption Scheme
ECLK	Edge Clock
ESB	Embedded Security Block
FIPS	Federal Information Processing Standard
HMAC	Hash Message Authentication Code
HSP	High Speed Port
I^2C	Inter-Integrated Circuit
I3C	Improved Inter-Integrated Circuit
IP	Intellectual Property
JTAG	Joint Test Action Group
LED	Light-emitting Diode
LUT	Look Up Table
LVCMOS	Low Voltage CMOS
LVDS	Low Voltage Differential Signaling
LVPECL	Low Voltage Positive Emitter Coupled Logic
LVTTL	Low Voltage Transistor-Transistor Logic
MIPI	Mobile Industry Processor Interface
MLVDS	Multipoint Low-Voltage Differential Signaling
MES	Manufacture Electronic Signature
OTP	One Time Programmable
PCLK	Primary Clock
PFU	Programmable Functional Unit
PLL	Phase Locked Loop
POR	Power On Reset
RAM	Random Access Memory
SHA	Secure Hash Algorithm
SPI	Serial Peripheral Interface
TransFR	Transparent Field Reconfiguration
TRNG	True Random Number Generator
TTL	Transistor-Transistor Logic
UFM	User Flash Memory

1. Introduction

The MachXO3D™ device family is the next generation of Lattice Semiconductor Low Density PLDs including enhanced security features and on-chip dual boot flash. The enhanced security features include Advanced Encryption Standard (AES) AES-128/256, Secure Hash Algorithm (SHA) SHA-256, Elliptic Curve Digital Signature Algorithm (ECDSA), Elliptic Curve Integrated Encryption Scheme (ECIES), Hash Message Authentication Code (HMAC) HMAC-SHA256, Public Key Cryptography, and Unique Secure ID. The MachXO3D family is a Root-of-Trust hardware solution that can easily scale to protect the whole system with its enhanced bitstream security and user mode functions. MachXO3D device provides breakthrough I/O density with high number of options for I/O programmability. The device I/O features the support for latest industry standard I/O, including programmable slew-rate enhancements and I3C support.

The MachXO3D family of low power, instant-on, Flash based PLDs have two devices with densities of 4300 and 9400 Look-Up Tables (LUTs). MachXO3D devices include on-chip dual boot configuration flash as well as multi-sectored User Flash Memory (UFM). In addition to LUT-based programmable logic, these devices feature Embedded Block RAM (EBR), Distributed RAM, Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support, advanced configuration support including on-chip dual-boot capability and hardened versions of commonly used functions such as SPI controller, I^2C controller, and timer/counter.

The MachXO3D devices are designed on a 65-nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/O and the ability to turn off I/O banks, on-chip PLLs and oscillators dynamically. These features help manage static and dynamic power consumption resulting in low power for all members of the family.

The MachXO3D devices are available in two performance levels: ultra low power (ZC) and high performance (HC). The ultra low power devices are offered in two speed grades: –2 and –3, with –3 being the fastest. Similarly, the high-performance devices are offered in two speed grades: –5 and –6, with –6 being the fastest. ZC/HC devices have an internal linear voltage regulator, which supports external VCC supply voltages of 3.3 V or 2.5 V. With the exception of power/performance profiles, the two types of devices, ZC and HC, are pin compatible with each other.

The MachXO3D PLDs are available in a broad range of advanced halogen-free packages ranging from the space saving 10 x 10 mm QFN to the 19 x 19 mm caBGA. MachXO3D devices support density migration within the same package. Table 1.1 shows the LUT densities, package and I/O options, along with other key parameters.

The MachXO3D devices offer enhanced I/O features such as drive strength control, finer slew rate control, I3C compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs, and hot socketing. Pull-up, pull-down, and bus-keeper features are controllable on a *per-pin* basis.

A user-programmable internal oscillator is included in MachXO3D devices. The clock output from this oscillator may be divided by the timer or counter for use as clock input in functions such as LED control, key-board scanner, and similar state machines.

The MachXO3D devices also provide flexible, reliable, and secure configuration from on-chip Flash with the encryption and authentication options. These devices can also configure themselves from external SPI Flash or be configured by an external master through the JTAG test access port or through the SPI/I^2C port. Additionally, MachXO3D devices support on-chip dual-boot capability to reduce the system cost and remote field upgrade TransFR capability.

Lattice Semiconductor provides a variety of design tools that allow complex designs to be efficiently implemented using the MachXO3D family of devices. Popular logic synthesis tools provide synthesis library support for MachXO3D devices. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the MachXO3D device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice Semiconductor provides many pre-engineered Intellectual Property (IP) LatticeCORE™ modules, including a number of reference designs licensed free of charge, optimized for the MachXO3D PLD family. By using these configurable soft core IP cores as standardized blocks, you are free to concentrate on the unique aspects of their design, increasing their productivity.

1.1. Features

1.1.1. Solutions

- Best-In-Class control PLD with advanced security functions, provide secure/authenticated boot and root of trust function
- Optimized footprint, logic density, I/O count, I/O performance devices for I/O management and logic applications
- High I/O logic, high I/O devices for I/O expansion applications

1.1.2. Flexible Architecture

- Logic Density ranging from 4.3K to 9.4K LUT4
- High I/O to LUT ratio with up to 383 I/O pins

1.1.3. Dedicated Embedded Security Block

- Advanced Encryption Standard (AES): AES-128/256 Encryption/Decryption
- Secure Hash Algorithm (SHA): SHA-256
- Elliptic Curve Digital Signature Algorithm (ECDSA): ECDSA-based authentication
- Hash Message Authentication Code (HMAC): HMAC-SHA256
- Elliptic Curve Integrated Encryption Scheme (ECIES): ECIES Encryption and Decryption
- True Random Number Generator (TRNG)
- Key Management using Elliptic Curve Diffie-Hellman (ECDH) Public Key Cryptography
- Unique Secure ID
- Guard against malicious attacks
- Interface for user logic via WISHBONE and High Speed Port (HSP)
- Federal Information Processing Standard (FIPS) supported Security Protocols

1.1.4. Pre-Engineered Source Synchronous I/O

- DDR registers in I/O cells
- Dedicated gearing logic
- 7:1 Gearing for Display I/O
- Generic DDR, DDRx2, DDRx4

1.1.5. High Performance, Flexible I/O Buffer

- Programmable sysI/O™ buffer supports wide range of interfaces:
  - LVCMOS 3.3/2.5/1.8/1.5/1.2
  - LVTTL
  - LVDS, Bus-LVDS, MLVDS, LVPECL
  - MIPI D-PHY Emulated
  - Schmitt trigger inputs, up to 0.5 V hysteresis
- Ideal for I/O bridging applications
- I3C compatible on selective I/O
- Slew rate control as Slow/Fast
- I/O support hot socketing
- On-chip differential termination
- Programmable pull-up or pull-down mode

1.1.6. Flexible On-Chip Clocking

- Eight primary clocks
- Up to two edge clocks for high-speed I/O interfaces (top and bottom sides only)
- Two analog PLLs per device with fractional-n frequency synthesis
  - Wide input frequency range (7 MHz to 400 MHz).

1.1.7. Non-volatile, Reconfigurable

- Instant-on
  - Powers up in microseconds
- On-chip dual boot
- Multi-sectored UFM for customer data storage
- Single-chip, secure solution
- Programmable through JTAG, SPI or I^2C
- Reconfigurable Flash
  - Supports background programming of non-volatile memory

1.1.8. TransFR Reconfiguration

- In-field logic update while I/O holds the system state

1.1.9. Enhanced System Level Support

- On-chip hardened functions: SPI, I^2C, and timer/counter
- On-chip oscillator with 5.5% accuracy
- Unique TraceID for system tracking
- Single power supply with extended operating range
- IEEE Standard 1149.1 boundary scan
- IEEE 1532 compliant in-system programming

1.1.10. Advanced Packaging

- 0.5 mm pitch: 4.3K to 9.4K densities with up to 58 I/O in QFN packages
- 0.8 mm pitch: 4.3K to 9.4K densities with up to 383 I/O in BGA packages
- Pin-compatible with MachXO3LF product family of devices

1.1.11. Applications

- Secure boot and Root of Trust
- Consumer Electronics
- Compute and Storage
- Wireless Communications
- Industrial Control Systems
- Automotive System

Table 1.1. MachXO3D Family Selection Guide

Features		MachXO3D-4300	MachXO3D-9400
LUTs		4300	9400
Distributed RAM (kbits)		34	73
EBR SRAM (kbits)		92	432
UFM (kbits)		367/1122[4]	1088/2693[4]
Number of PLLs		2	2
Hardened Functions	Security	1	1
	I^2C	2	2
	SPI	1	1
	Timer/ Counter	1	1
	Oscillator	1	1
On-chip Dual-boot		Yes	Yes
I3C compatible I/O		Yes[1]	Yes[1]
MIPI D-PHY Support[2]		Yes	Yes
Core Vcc	2.5 – 3.3V	ZC/HC	ZC/HC
Temperature	Commercial	Yes	Yes
	Industrial	Yes	Yes
	Automotive	Yes[3]	No

Packages	I/O	
72 QFN (10 mm x 10 mm, 0.5 mm)	58 (HC/ZC)	58 (HC/ZC)
256-ball caBGA (14 mm x 14 mm, 0.8 mm)	206 (HC/ZC)	206 (HC/ZC)
400-ball caBGA (17 mm x 17 mm, 0.8 mm)	—	335 (HC/ZC)
484-ball caBGA (19 mm x 19 mm, 0.8 mm)	—	383 (HC)

Notes:
1. 4 pairs of I/O in bank 3 with I3C dynamic pull up capability.
2. HC device only.
3. ZC lowest speed grade device only.
4. When dual-boot is disabled, image space can be repurposed as extra UFM. Refer to Table 2.17 for more details.

2. Architecture

2.1. Architecture Overview

The MachXO3D family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). All logic density devices in this family have sysCLOCK™ PLLs and blocks of sysMEM Embedded Block RAM (EBRs).

Figure 2.1 shows the block diagrams of the various family members.

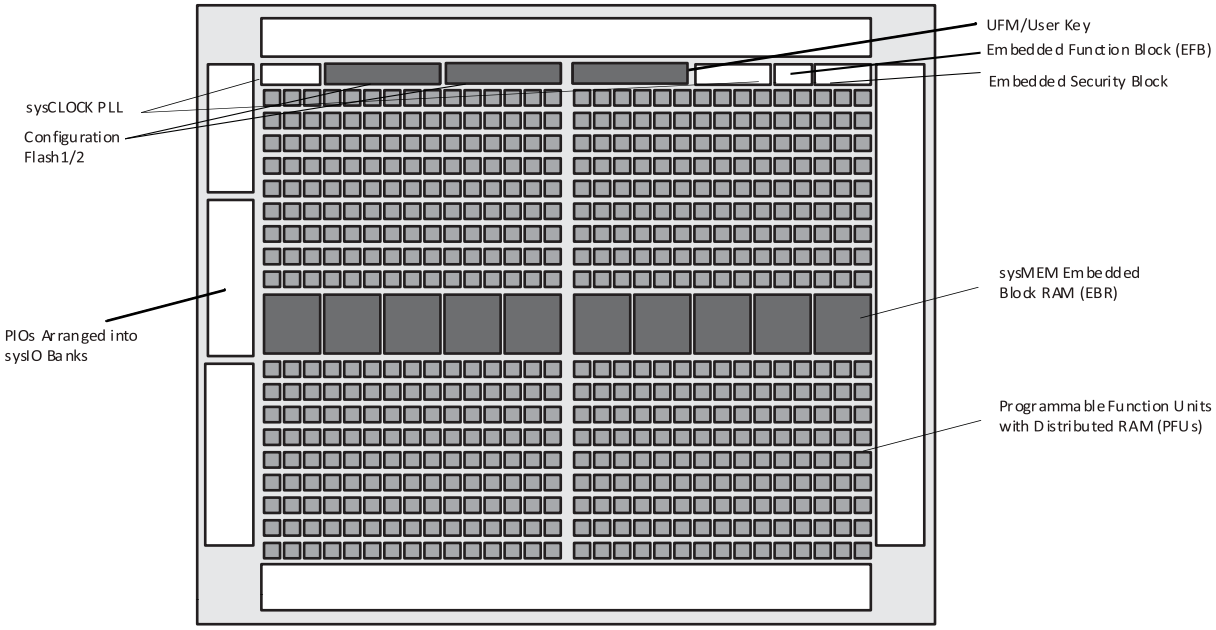


Figure 2.1. Top View of the MachXO3D Device

The logic blocks, Programmable Functional Unit (PFU) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each row has either the logic blocks or the EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysI/O buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the MachXO3D family, the number of sysI/O banks varies by device. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag “hard” control logic to minimize LUT usage.

The MachXO3D registers in PFU and sysI/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

The MachXO3D architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks. These blocks are located at the ends of the on-chip Flash block. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

The Embedded Security Block (ESB) integrates multiple security blocks used for authenticated boot function of the MachXO3D device. User IP located in the fabric can also use these hardened blocks for implementing system level security functions.

MachXO3D devices provide commonly used hardened functions such as SPI controller, I^2C controller, and timer/counter.

MachXO3D devices also provide multiple blocks of User Flash Memory (UFM). These hardened functions and the UFM interface to the core logic and routing through a WISHBONE interface. The UFM space also provides the User Key storage for customer security functions. The UFM can also be accessed through the SPI, I^2C, and JTAG ports.

Every device in the family has a JTAG port that supports programming and configuration of the device as well as access to the user logic. The MachXO3D devices are available for operation from 3.3 V and 2.5 V power supplies, providing easy integration into the overall system.

2.2. PFU Blocks

The core of the MachXO3D device consists of PFU blocks, which can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. Each PFU block consists of four interconnected slices numbered 0 to 3 as shown in Figure 2.2. Each slice contains two LUTs and two registers. There are 53 inputs and 25 outputs associated with each PFU block.

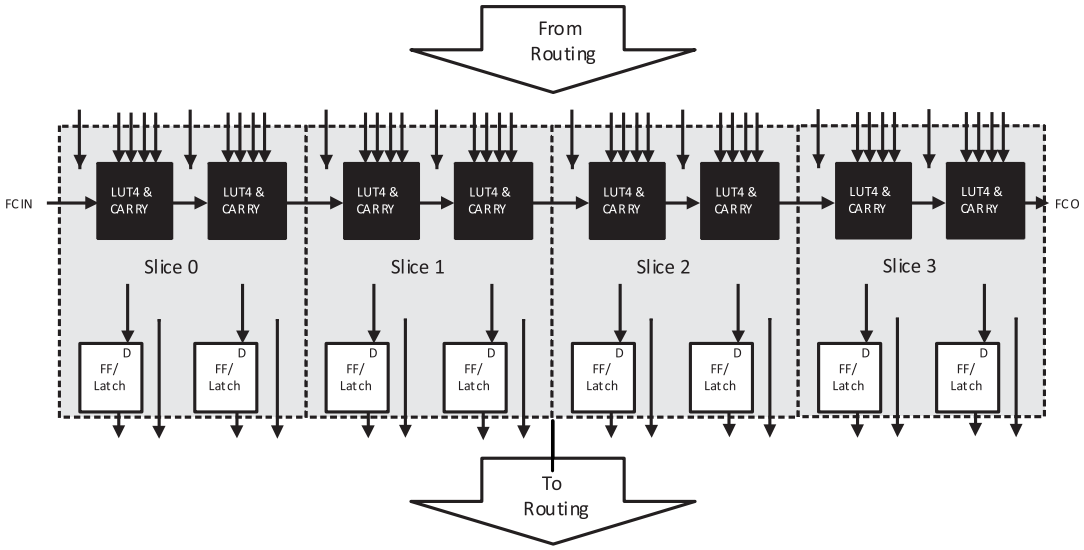


Figure 2.2. PFU Block Diagram

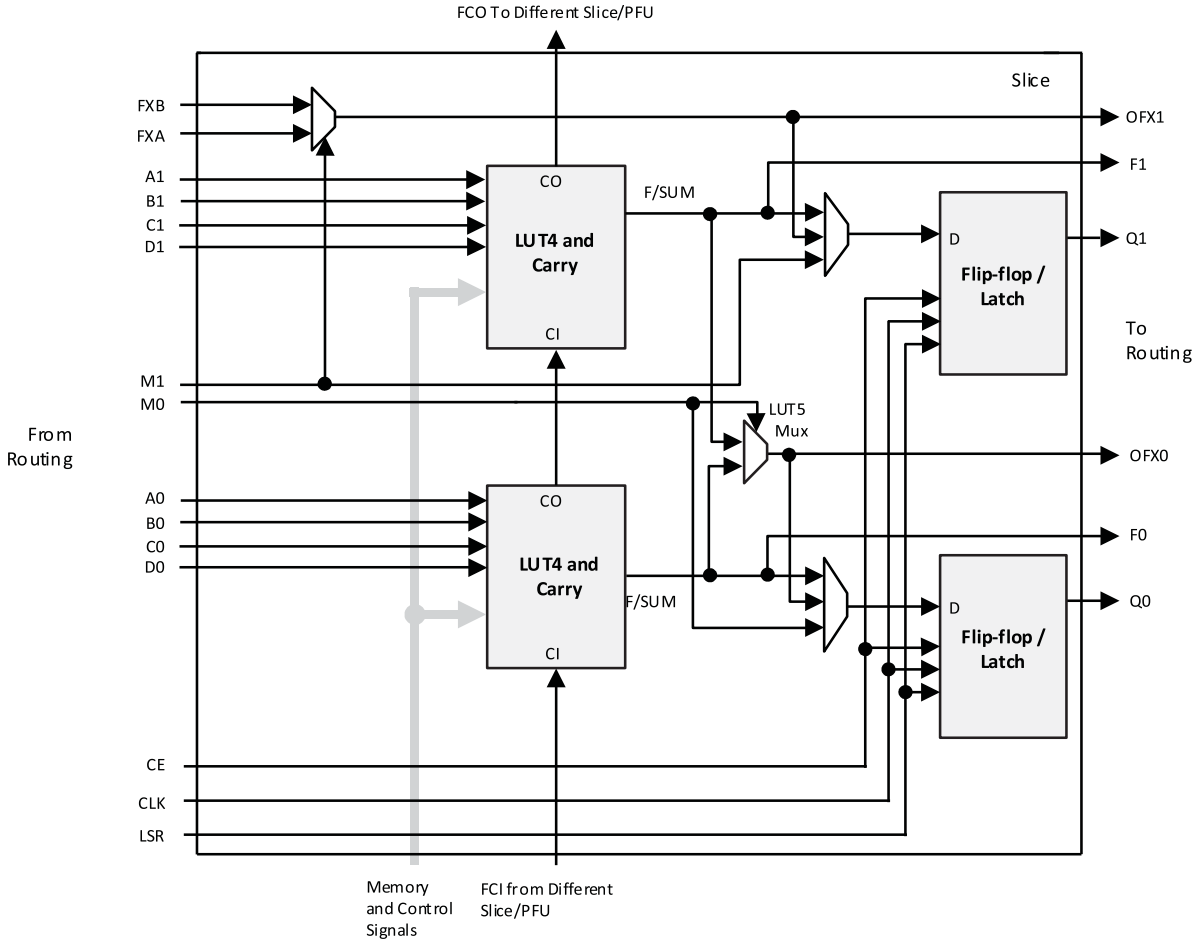
2.2.1. Slices

Slices 0-3 contain two LUT4s feeding two registers. Slices 0-2 can be configured as distributed memory. Table 2.1 shows the capability of the slices in PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. The control logic performs set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions.

Table 2.1. Resources and Modes Available per Slice

Slice	PFU Block	
	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM

Figure 2.3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks. All slices have 15 inputs from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six for routing and one to carry-chain (to the adjacent PFU). Table 2.2 lists the signals associated with Slices 0-3.



For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:
- WCK is CLK
- WRE is from LSR
- DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2
- WAD [A:D] is a 4-bit address from slice 2 LUT input

Figure 2.3. Slice Diagram

Table 2.2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0/M1	Multi-purpose input
Input	Control signal	CE	Clock enable
Input	Control signal	LSR	Local set/reset
Input	Control signal	CLK	System clock
Input	Inter-PFU signal	FCIN	Fast carry in[1]
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice
Output	Inter-PFU signal	FCO	Fast carry out[1]

Notes:
1. See Figure 2.22 for connection details.
2. Requires two PFUs.

2.2.2. Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

2.2.2.1. Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7, and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

2.2.2.2. Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In Ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/down counter with asynchronous clear
- Up/down counter with preload (sync)
- Ripple mode multiplier building block Multiplier support
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Ripple mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode), two additional signals, Carry Generate and Carry Propagate, are generated on a per-slice basis to allow fast arithmetic functions to be constructed by concatenating slices.

2.2.3. RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed by using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address and control signals.

MachXO3D devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software constructs these using distributed memory primitives that represent the capabilities of the PFU. Table 2.3 shows the number of slices required to implement different distributed RAM primitives.

Table 2.3. Number of Slices Required For Implementing Distributed RAM

	SPR 16 x 4	PDPR 16 x 4
Number of slices	3	3

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

2.2.4. ROM Mode

ROM mode uses the LUT logic; hence, slices 0-3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

2.3. Routing

There are many resources provided in the MachXO3D devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The design tools take the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

2.4. Clock/Control Distribution Network

Each MachXO3D device has eight clock inputs (PCLK [T, C] [Banknum]_[2..0]) – three pins on the left side, two pins each on the bottom and top sides and one pin on the right side. These clock inputs drive the clock nets. These eight inputs can be differential or single-ended and may be used as general purpose I/O if they are not used to drive the clock nets. When using a single ended clock input, only the PCLKT input can drive the clock tree directly.

The MachXO3D architecture has three types of clocking resources: edge clocks, primary clocks, and secondary high fanout nets. MachXO3D devices have two edge clocks each on the top and bottom edges. Edge clocks are used to clock I/O registers and have low injection time and skew. Edge clock inputs are from PLL outputs, primary clock pads, edge clock bridge outputs and CIB sources.

The eight primary clock lines in the primary clock network drive throughout the entire device and can provide clocks for all resources within the device including PFUs, EBRs and PICs. In addition to the primary clock signals, MachXO3D devices also have eight secondary high fanout signals, which can be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, etc. Internal logic can drive the global clock network for internally-generated global clocks and control signals.

The maximum frequency for the primary clock network is shown in the MachXO3D External Switching Characteristics table.

Primary clock signals for the MachXO3D devices are generated from eight 27:1 muxes. The available clock sources include eight I/O sources, 11 routing inputs, eight clock divider inputs and up to eight sysCLOCK PLL outputs.

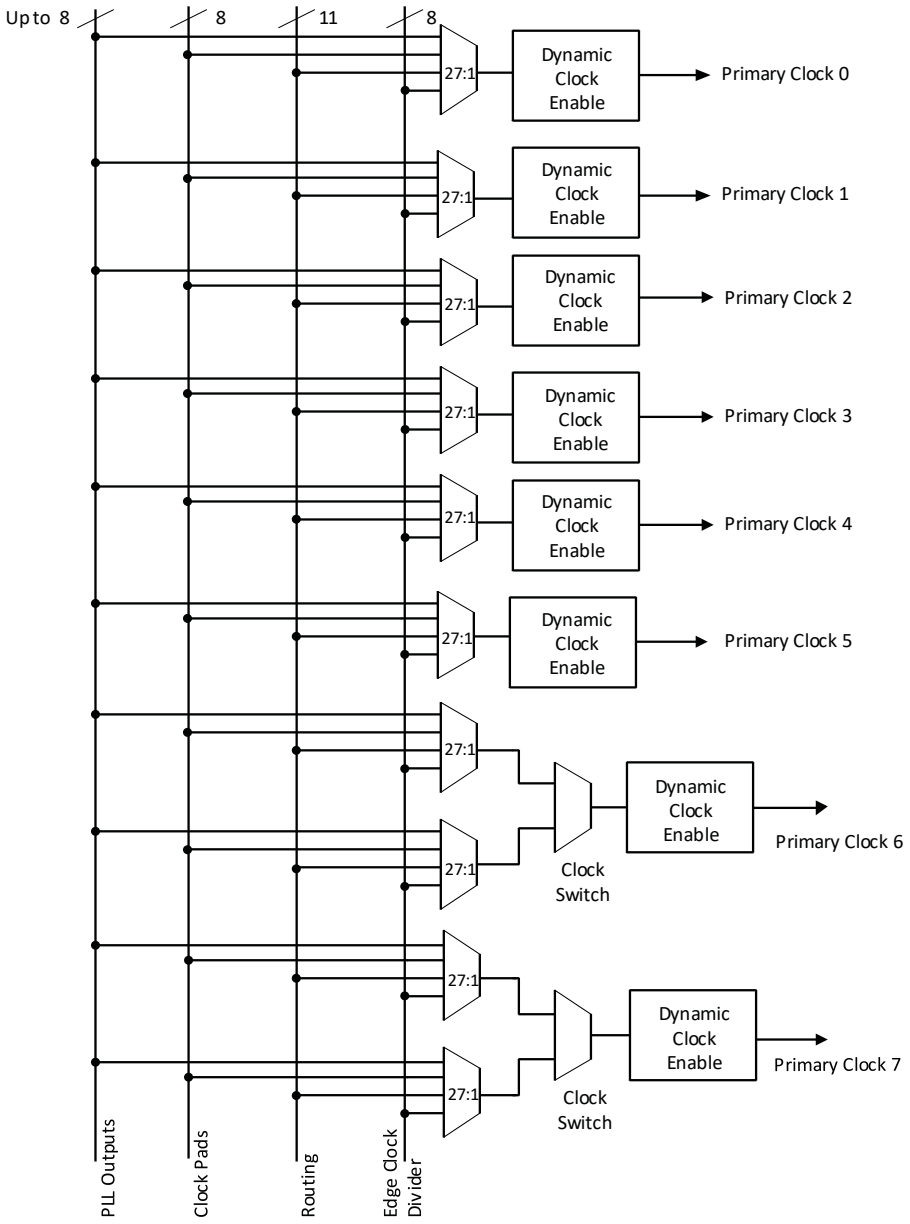


Figure 2.4. Primary Clocks for MachXO3D Devices

Eight secondary high fanout nets are generated from eight 8:1 muxes as shown in Figure 2.5. One of the eight inputs to the secondary high fanout net input mux comes from dual function clock pins and the remaining seven come from internal routing. The maximum frequency for the secondary clock network is shown in MachXO3D External Switching Characteristics table.

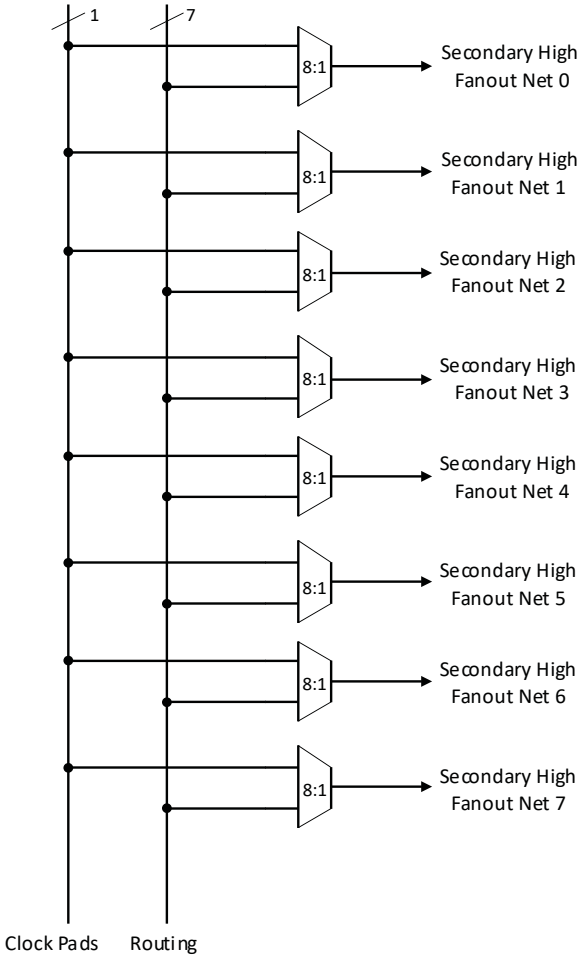


Figure 2.5. Secondary High Fanout Nets for MachXO3D Devices

2.4.1. sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. All MachXO3D devices have one or more sysCLOCK PLL. CLKI is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. CLKFB is the feedback signal to the PLL, which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The MachXO3D sysCLOCK PLLs support high resolution (16-bit) fractional-N synthesis. Fractional-N frequency synthesis allows you to generate an output clock, which is a non-integer multiple of the input frequency.

Each output has its own output divider, thus allowing the PLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. The output dividers may also be cascaded together to generate low frequency clocks. The CLKOP, CLKOS, CLKOS2, and CLKOS3 outputs can all be used to drive the MachXO3D clock distribution network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and deasserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2.6.

The setup and hold times of the device can be improved by programming a phase shift into the CLKOS, CLKOS2, and CLKOS3 output clock, which advance or delay the output clock with reference to the CLKOP output clock.

This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the t_{LOCK} parameter has been satisfied.

The MachXO3D also has a feature that allows you to select between two different reference clock sources dynamically. This feature is implemented using the PLLREFCS primitive. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

The MachXO3D PLL contains a WISHBONE port feature that allows the PLL settings, including divider values, to be dynamically changed from the user logic. When using this feature the EFB block must also be instantiated in the design to allow access to the WISHBONE ports. Similar to the dynamic phase adjustment, when PLL settings are updated through the WISHBONE port, the PLL may lose lock and not relock until the t_{LOCK} parameter has been satisfied. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

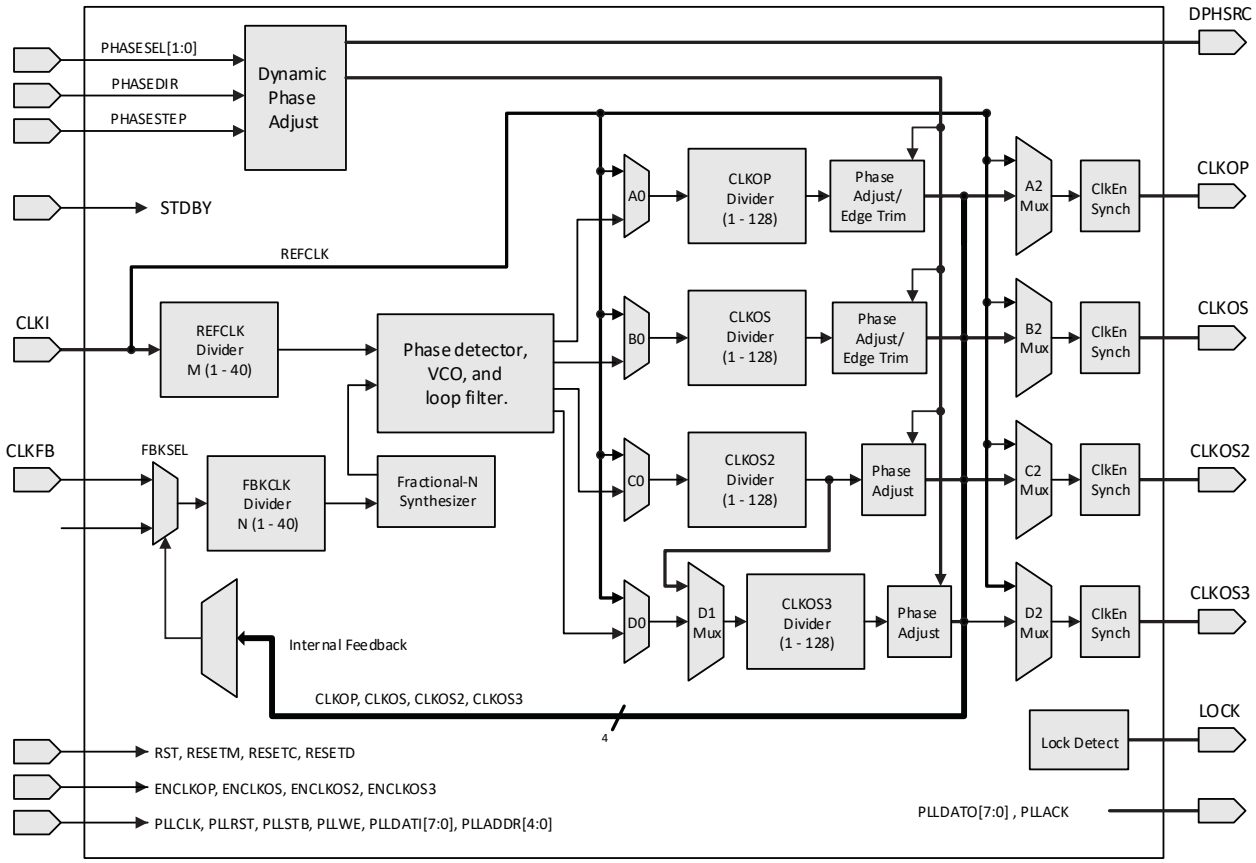


Figure 2.6. PLL Diagram

Table 2.4 provides signal descriptions of the PLL block.

Table 2.4. PLL Signal Descriptions

Port Name	I/O	Description
CLKI	I	Input clock to PLL
CLKFB	I	Feedback clock
PHASESEL[1:0]	I	Select which output is affected by Dynamic Phase adjustment ports
PHASEDIR	I	Dynamic Phase adjustment direction
PHASESTEP	I	Dynamic Phase step – toggle shifts VCO phase adjust by one step.
CLKOP	O	Primary PLL output clock (with phase shift adjustment)
CLKOS	O	Secondary PLL output clock (with phase shift adjust)
CLKOS2	O	Secondary PLL output clock2 (with phase shift adjust)
CLKOS3	O	Secondary PLL output clock3 (with phase shift adjust)
LOCK	O	PLL LOCK, asynchronous signal. Active high indicates PLL is locked to input and feed- back signals.
DPHSRC	O	Dynamic Phase source – ports or WISHBONE is active
STDBY	I	Standby signal to power down the PLL
RST	I	PLL reset without resetting the M-divider. Active high reset.
RESETM	I	PLL reset – includes resetting the M-divider. Active high reset.
RESETC	I	Reset for CLKOS2 output divider only. Active high reset.
RESETD	I	Reset for CLKOS3 output divider only. Active high reset.
ENCLKOP	I	Enable PLL output CLKOP
ENCLKOS	I	Enable PLL output CLKOS when port is active
ENCLKOS2	I	Enable PLL output CLKOS2 when port is active
ENCLKOS3	I	Enable PLL output CLKOS3 when port is active
PLLCLK	I	PLL data bus clock input signal
PLLRST	I	PLL data bus reset. This resets only the data bus not any register values.
PLLSTB	I	PLL data bus strobe signal
PLLWE	I	PLL data bus write enable signal
PLLADDR [4:0]	I	PLL data bus address
PLLDATI [7:0]	I	PLL data bus data input
PLLDATO [7:0]	O	PLL data bus data output
PLLACK	O	PLL data bus acknowledge signal

2.5. sysMEM Embedded Block RAM Memory

The MachXO3D devices contain sysMEM Embedded Block RAMs (EBRs). The EBR consists of a 9 kb RAM, with dedicated input and output registers. This memory can be used for a wide variety of purposes including data buffering, PROM for the soft processor and FIFO.

2.5.1. sysMEM Memory Block

The sysMEM block can implement single port, dual port, pseudo dual port, or FIFO memories. Each block can be used in a variety of depths and widths as shown in Table 2.5.

Table 2.5. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
True Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
FIFO	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18

2.5.2. Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

2.5.3. RAM Initialization and ROM Operation

If desired, the contents of the RAM can be preloaded during device configuration. EBR initialization data can be loaded from the Configuration Flash.

MachXO3D EBR initialization data can also be loaded from the UFM. To maximize the number of UFM bits, initialize the EBRs used in your design to an all-zero pattern. Initializing to an all-zero pattern does not use up UFM bits. MachXO3D devices have been designed such that multiple EBRs share the same initialization memory space if they are initialized to the same pattern.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

2.5.4. Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

2.5.5. Single, Dual, Pseudo-Dual Port and FIFO Modes

Figure 2.7 shows the five basic memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the memory array output.

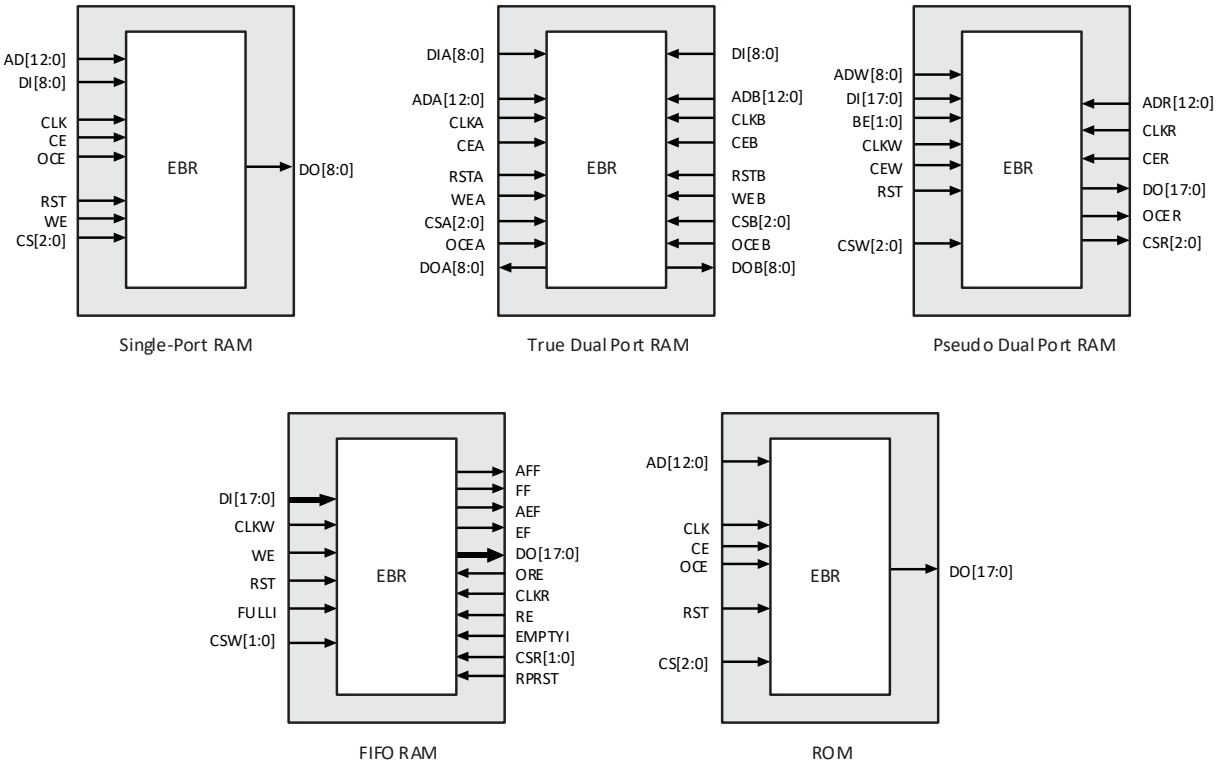


Figure 2.7. sysMEM Memory Primitives

Table 2.6. EBR Signal Descriptions

Port Name	Description	Active State
CLK	Clock	Rising Clock Edge
CE	Clock Enable	Active High
OCE[1]	Output Clock Enable	Active High
RST	Reset	Active High
BE[1]	Byte Enable	Active High
WE	Write Enable	Active High
AD	Address Bus	—
DI	Data In	—
DO	Data Out	—
CS	Chip Select	Active High
AFF	FIFO RAM Almost Full Flag	—
FF	FIFO RAM Full Flag	—
AEF	FIFO RAM Almost Empty Flag	—
EF	FIFO RAM Empty Flag	—
RPRST	FIFO RAM Read Pointer Reset	—

Notes:

1. Optional signals.
2. For dual port EBR primitives a trailing ‘A’ or ‘B’ in the signal name specifies the EBR port A or port B respectively.
3. For FIFO RAM mode primitive, a trailing ‘R’ or ‘W’ in the signal name specifies the FIFO read port or write port respectively.
4. For FIFO RAM mode primitive, FULLI has the same function as CSW(2) and EMPTYI has the same function as CSR(2).
5. In FIFO mode, CLKW is the write port clock, CSW is the write port chip select, CLKR is the read port clock, CSR is the chip select, ORE is the output read enable.

The EBR memory supports three forms of write behavior for single or dual port operation:

1. Normal – Data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. Write Through – A copy of the input data appears at the output of the same port. This mode is supported for all data widths.
3. Read-Before-Write – When new data is being written, the old contents of the address appears at the output.

2.5.6. FIFO Configuration

The FIFO has a write port with data-in, CEW, WE and CLKW signals. There is a separate read port with data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. Table 2.7 shows the range of programming values for these flags.

Table 2.7. Programmable FIFO Flag Ranges

Flag Name	Programming Range
Full (FF)	1 to max (up to 2^N–1)
Almost Full (AF)	1 to Full–1
Almost Empty (AE)	1 to Full–1
Empty (EF)	0

N = Address bit width.

The FIFO state machine supports two types of reset signals: RST and RPRST. The RST signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset state. The RPRST signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications, it is important to keep careful track of when a packet is written into or read from the FIFO.

2.5.7. Memory Core Reset

The memory core contains data output latches for ports A and B. These are simple latches that can be reset synchronously or asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with port A and port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2.8.

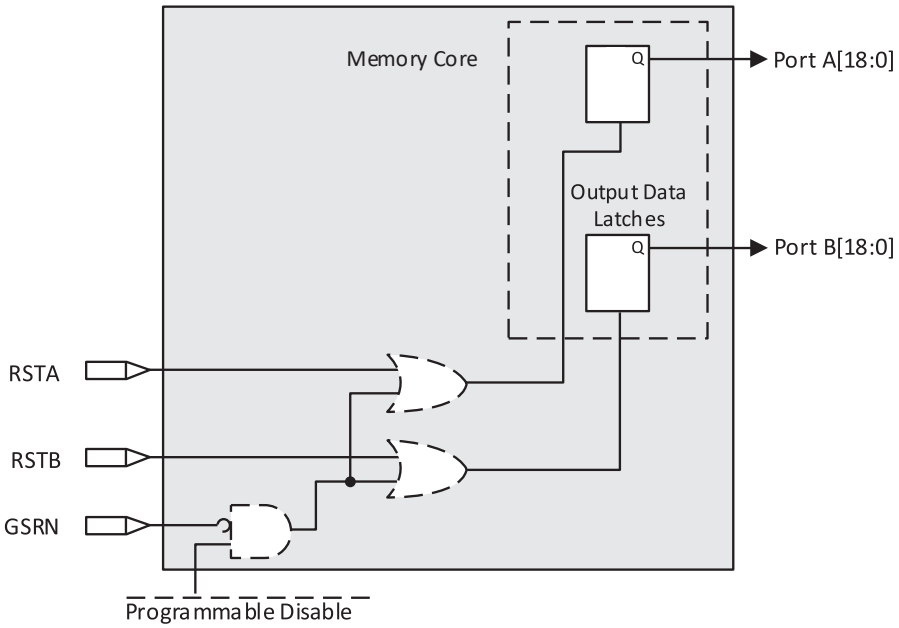


Figure 2.8. Memory Core Reset

2.5.8. EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2.9. The GSR input to the EBR is always asynchronous.

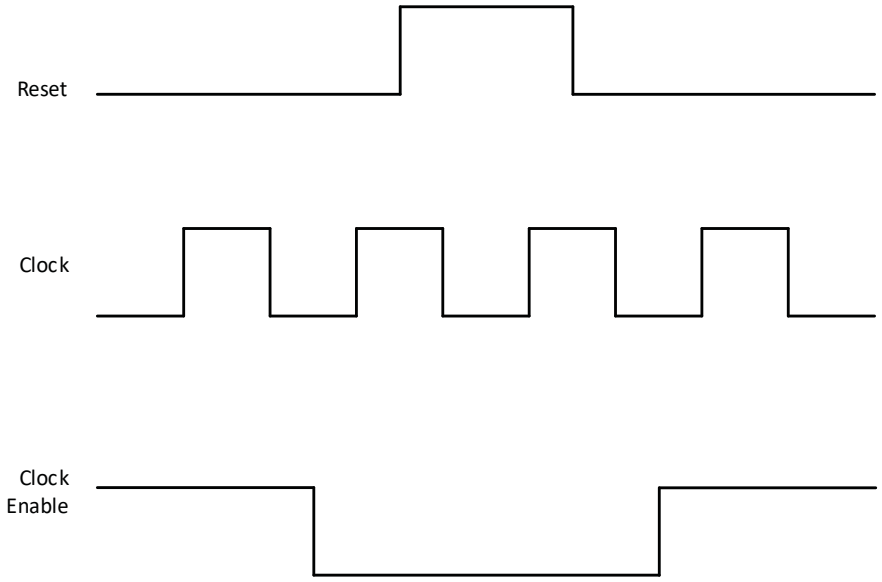


Figure 2.9. EBR Asynchronous Reset (Including GSR) Timing Diagram

If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of 1/fMAX (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is preloaded during configuration, the GSR input must be disabled or the release of the GSR during device wake up must occur before the release of the device I/O becoming active.

These instructions apply to all EBR RAM, ROM and FIFO implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2.9. The reset timing rules apply to the RPReset input versus the RE input and the RST input versus the WE and RE inputs. Both RST and RPReset are always asynchronous EBR inputs.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

2.6. Programmable I/O Cells (PIC)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysI/O buffers and pads. On the MachXO3D devices, the PIO cells are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the MachXO3D devices, two adjacent PIO can be combined to provide a complementary output driver pair.

All PIO pairs can implement differential receivers. Half of the PIO pairs on the top edge of these devices can be configured as true LVDS transmit pairs. The PIO pairs on the bottom edge of these devices have on-chip differential termination.

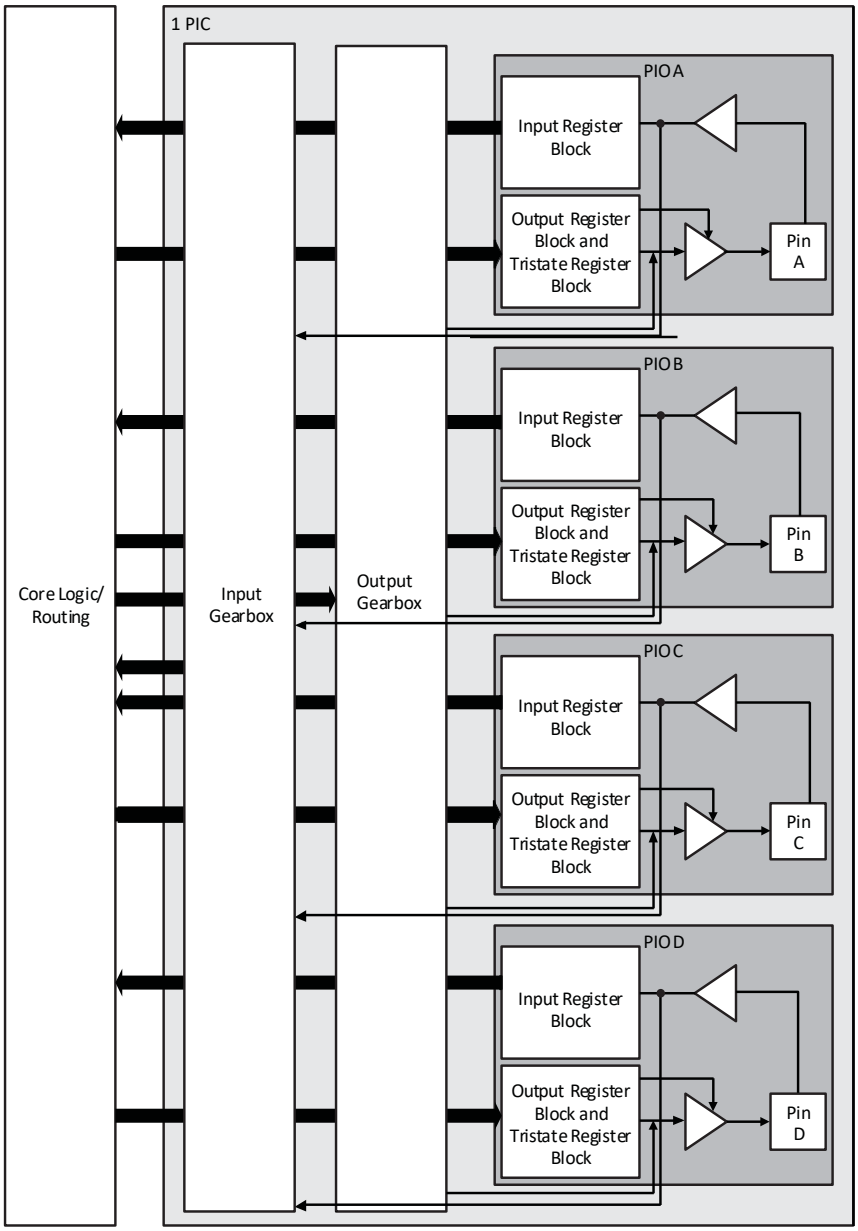


Figure 2.10. Group of Four Programmable I/O Cells

2.7. PIO

The PIO contains three blocks: an input register block, output register block, and tri-state register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

Table 2.8. PIO Signal List

Pin Name	I/O Type	Description
CE	Input	Clock Enable
D	Input	Pin input from sysI/O buffer
INDD	Output	Register bypassed input
INCK	Output	Clock input
Q0	Output	DDR positive edge input
Q1	Output	Registered input/DDR negative edge input
D0	Input	Output signal from the core (SDR and DDR)
D1	Input	Output signal from the core (DDR)
TD	Input	Tri-state signal from the core
Q	Output	Data output signals to sysI/O Buffer
TQ	Output	Tri-state output signals to sysI/O Buffer
SCLK	Input	System clock for input and output/tri-state blocks.
RST	Input	Local set reset signal

2.7.1. Input Register Block

The input register blocks for the PIO on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core.

2.7.1.1. Left, Top, Bottom Edges

Input signals are fed from the sysI/O buffer to the input register block (as signal D). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), and a clock (INCK). If an input delay is desired, users can select a fixed delay. I/O on the bottom edge also have a dynamic delay, DEL[4:0]. The delay, if selected, reduces input register hold time requirements when using a global clock. The input block allows two modes of operation. In single data rate (SDR) the data is registered with the system clock (SCLK) by one of the registers in the single data rate sync register block. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock (SCLK) signal, creating two data streams.

2.7.2. Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysI/O buffers.

2.7.2.1. Left, Top, Bottom Edges

In SDR mode, D0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type register or latch.

In DDR generic mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge, the registered D1 input is registered into the register Q1. A multiplexer running off the same clock is used to switch the mux between the outputs of registers Q0 and Q1 that feeds the output.

Figure 2.11 shows the output register block on the left, top and bottom edges.

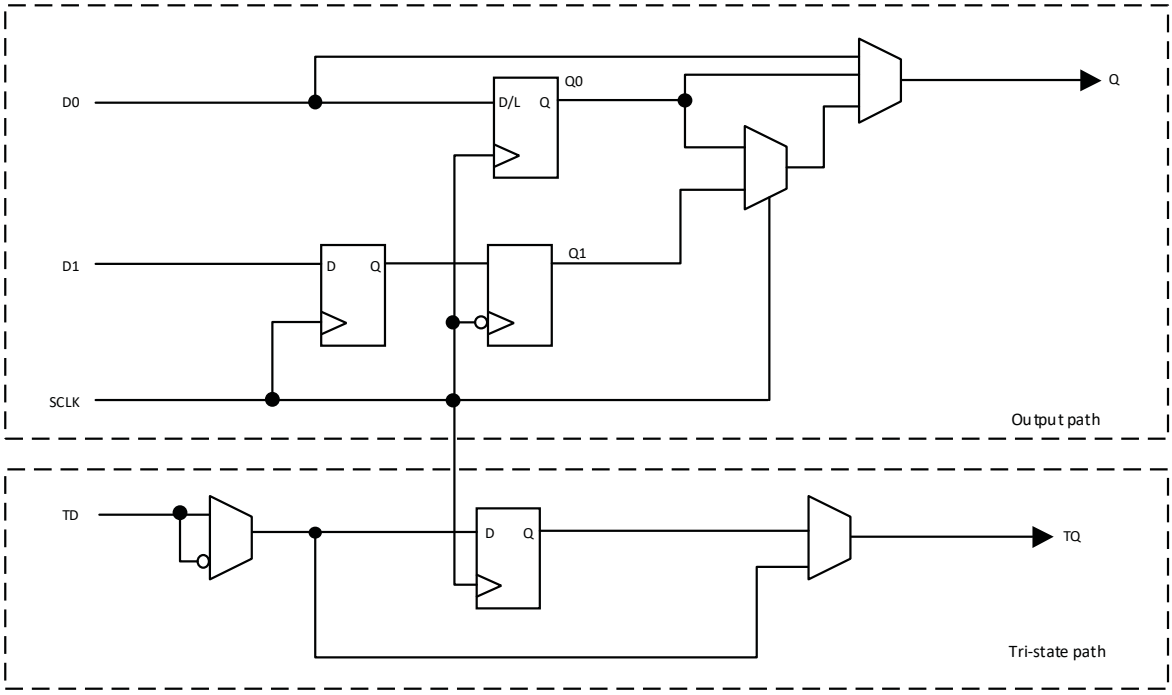


Figure 2.11. MachXO3D Output Register Block Diagram (PIO on the Left, Top and Bottom Edges)

2.7.3. Tri-state Register Block

The tri-state register block registers tri-state control signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output.

2.8. Input Gearbox

Each PIC on the bottom edge has a built-in 1:8 input gearbox. Each of these input gearboxes may be programmed as a 1:7 de-serializer or as one IDDRX4 (1:8) gearbox or as two IDDRX2 (1:4) gearboxes. Table 2.9 shows the gearbox signals.

Table 2.9. Input Gearbox Signal List

Name	I/O Type	Description
D	Input	High-speed data input after programmable delay in PIO A input register block
ALIGNWD	Input	Data alignment signal from device core
SCLK	Input	Slow-speed system clock
ECLK[1:0]	Input	High-speed edge clock
RST	Input	Reset
Q[7:0]	Output	Low-speed data to device core: Video RX(1:7): Q[6:0] GDDRX4(1:8): Q[7:0] GDDRX2(1:4)(IOL-A): Q4, Q5, Q6, Q7 GDDRX2(1:4)(IOL-C): Q0, Q1, Q2, Q3

These gearboxes have three stage pipeline registers. The first stage registers sample the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals UPDATE and SEL0 from the control block. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. Figure 2.12 shows a block diagram of the input gearbox.

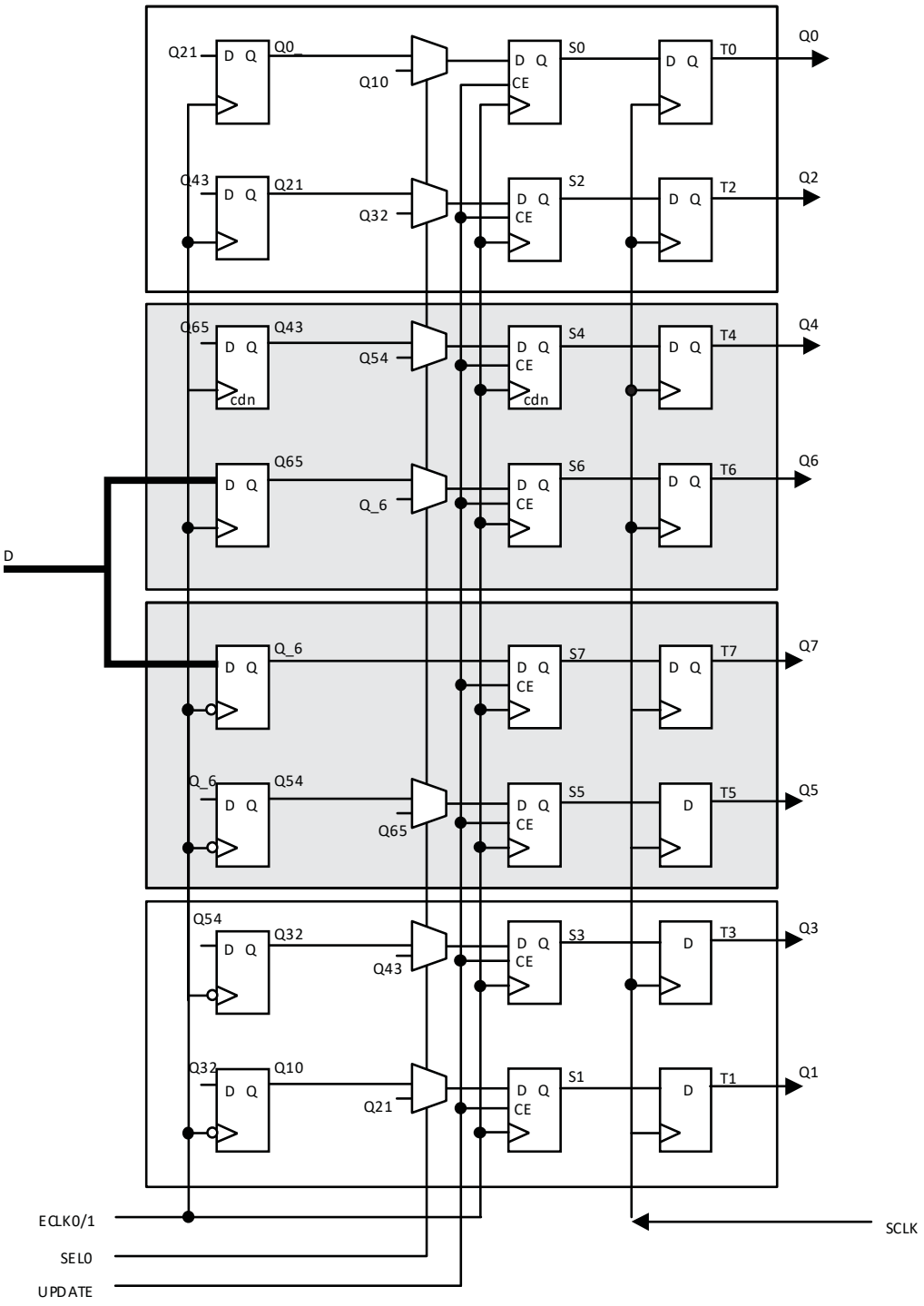


Figure 2.12. Input Gearbox

2.9. Output Gearbox

Each PIC on the top edge has a built-in 8:1 output gearbox. Each of these output gearboxes may be programmed as a 7:1 serializer or as one ODDRX4 (8:1) gearbox or as two ODDRX2 (4:1) gearboxes. Table 2.10 shows the gearbox signals.

Table 2.10. Output Gearbox Signal List

Name	I/O Type	Description
Q	Output	High-speed data output
D[7:0]	Input	Low-speed data from device core
Video TX(7:1): D[6:0]	—	—
GDDRX4(8:1): D[7:0]	—	—
GDDRX2(4:1)(IOL-A): D[3:0]	—	—
GDDRX2(4:1)(IOL-C): D[7:4]	—	—
SCLK	Input	Slow-speed system clock
ECLK [1:0]	Input	High-speed edge clock
RST	Input	Reset

The gearboxes have three stage pipeline registers. The first stage registers sample the low-speed input data on the low-speed system clock. The second stage registers transfer data from the low-speed clock registers to the high-speed clock registers. The third stage pipeline registers controlled by high-speed edge clock shift and mux the high-speed data out to the sysI/O buffer. Figure 2.13 shows the output gearbox block diagram.

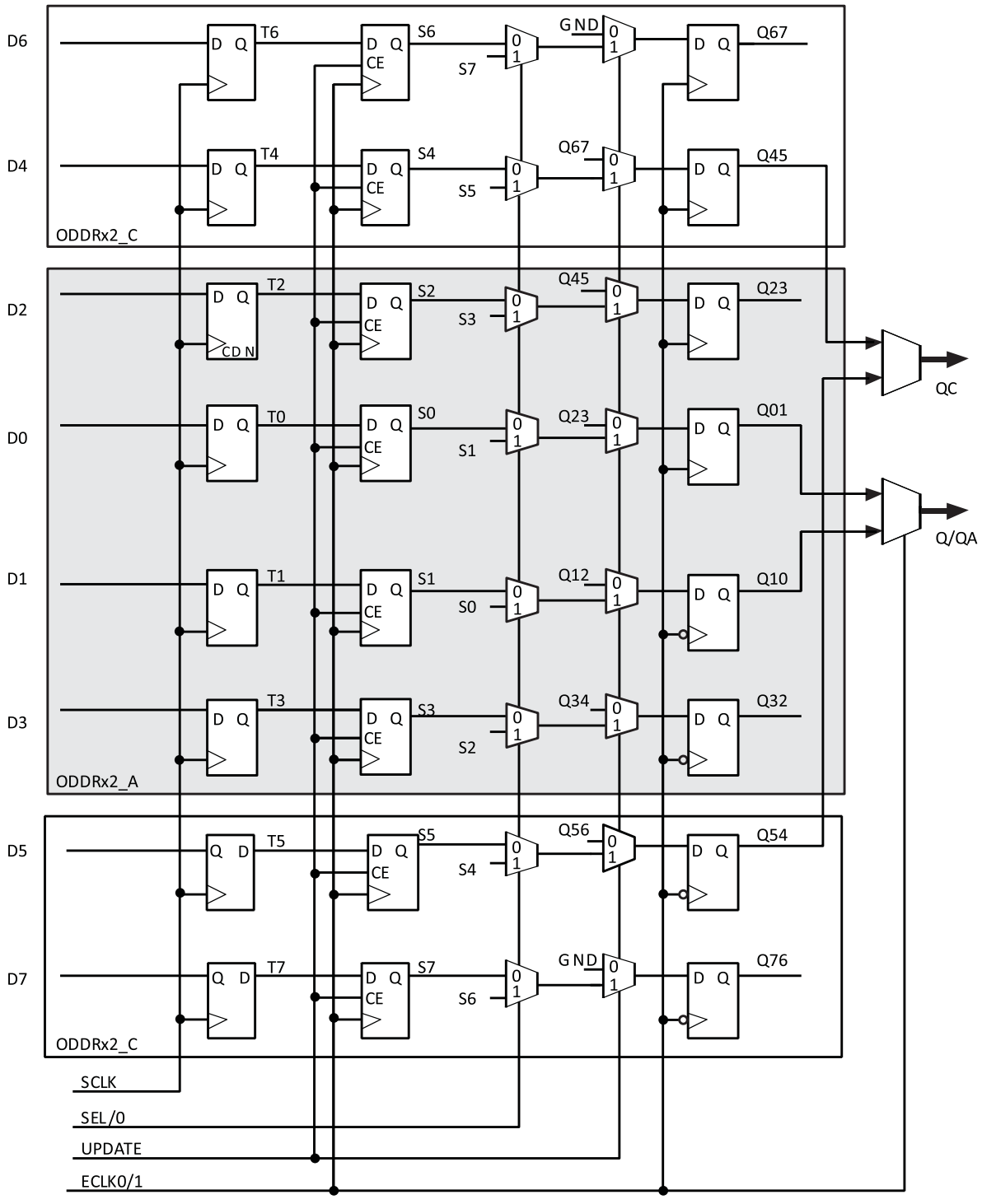


Figure 2.13. Output Gearbox

2.10. sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement a wide variety of standards that are found in today's systems including LVCMOS, TTL, LVDS, BLVDS, MLVDS, LVPECL, and I3C.

Each bank is capable of supporting multiple I/O standards. In the MachXO3D devices, single-ended output buffers, ratioed input buffers (LVTTL, LVCMOS), differential (LVDS) input buffers are powered using I/O supply voltage (V_{CCIO}). Each sysI/O bank has its own V_{CCIO}.

MachXO3D devices contain three types of sysI/O buffer pairs.

1. **Left and Right sysI/O Buffer Pairs**

   The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the left and right of the devices also have differential input buffers. The selective I/O pairs of Bank 3 support I3C dynamic pull up capability.

2. **Bottom sysI/O Buffer Pairs**

   The sysI/O buffer pairs in the bottom bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the bottom also have differential input buffers. Only the I/O on the bottom banks have differential input termination.

3. **Top sysI/O Buffer Pairs**

   The sysI/O buffer pairs in the top bank of the device consist of two single-ended output drivers and two single- ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the top also have differential I/O buffers. Half of the sysI/O buffer pairs on the top edge have true differential outputs. The sysI/O buffer pair comprising of the A and B PIOs in every PIC on the top edge have a differential output driver.

2.10.1. Typical I/O Behavior during Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} and V_{CCIO0} have reached VPORUP level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. You need to ensure that all VCCIO banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a blank device is tri-state with a weak pull-down to GND (some pins such as PROGRAMN and the JTAG pins have weak pull-up to VCCIO as the default functionality). The I/O pins maintain the blank configuration until VCC and VCCIO (for I/O banks containing configuration I/O) reach VPORUP levels at which time the I/O takes on the user-configured settings only after a proper download/configuration.

There are various ways for you to ensure that there are no spurious signals on critical outputs as the device powers up.

2.10.2. Supported Standards

The MachXO3D sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and I3C. The buffer supports the LVTTL, I3C, LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, bus-keeper latch or none) and open drain. BLVDS, MLVDS and LVPECL output emulation is supported on all devices. The MachXO3D devices support on-chip LVDS output buffers on approximately 50% of the I/O on the top bank. Differential receivers for LVDS, BLVDS, MLVDS, and LVPECL are supported on all banks of MachXO3D devices. I3C support is provided with selective I/O in the left bank of the MachXO3D devices.

Table 2.11 summarizes the I/O characteristics of the MachXO3D PLDs and shows the I/O standards, together with their supply and reference voltages, supported by the MachXO3D devices.

Table 2.11. Supported Input Standards

	V_{CCIO} (Typ.)				
Input Standard	**3.3 V**	**2.5 V**	**1.8 V**	**1.5 V**	**1.2 V**
Single-Ended Interfaces					
LVTTL	Yes	Yes[2]	Yes[2]	Yes[2]	—
LVCMOS33	Yes	Yes[2]	Yes[2]	Yes[2]	—
LVCMOS25	Yes[2]	Yes	Yes[2]	Yes[2]	—
LVCMOS18	Yes[2]	Yes[2]	Yes	Yes[2]	—
LVCMOS15	Yes[2]	Yes[2]	Yes[2]	Yes	Yes[2]
LVCMOS12	Yes[2]	Yes[2]	Yes[2]	Yes[2]	Yes
LVCMOS10R25	—	Yes[3]	—	—	—
LVCMOS10R33	Yes[3]	—	—	—	—
I3C33	Yes	—	—	—	—
I3C18	—	—	Yes	—	—
I3C12	—	—	—	—	Yes
Differential Interfaces					
LVDS	Yes	Yes	—	—	—
BLVDS, MLVDS, LVPECL, RSDS	Yes	Yes	—	—	—
MIPI[1]	Yes	Yes	—	—	—
LVTTLD	Yes	Yes[2]	—	—	—
LVCMOS33D	Yes	—	—	—	—
LVCMOS25D	Yes	Yes	—	—	—
LVCMOS18D	Yes	Yes	Yes	—	—

Notes:

1. These interfaces can be emulated with external resistors in all devices.
2. For reduced functionality, refer to MachXO3D sysI/O Technical Note (FPGA-TN-02068) for more details.
3. This input standard can be supported with the referenced input buffer.

Table 2.12. Supported Output Standards

Output Standard	V_{CCIO} (Typ.)
Single-Ended Interfaces	
LVTTL	3.3
LVCMOS33	3.3
LVCMOS25	2.5
LVCMOS18	1.8
LVCMOS15	1.5
LVCMOS12	1.2
LVCMOS10R25, Open Drain	—
LVCMOS10R33, Open Drain	—
LVCMOS33, Open Drain	—
LVCMOS25, Open Drain	—
LVCMOS18, Open Drain	—
LVCMOS15, Open Drain	—
LVCMOS12, Open Drain	—
I3C33	3.3
I3C25	2.5

Output Standard	V_{CCIO} (Typ.)
I3C12	1.2
Differential Interfaces	
LVDS*	2.5, 3.3
BLVDS, MLVDS, RSDS*	2.5
LVPECL*	3.3
MIPI*	2.5
LVTTLD	3.3
LVCMOS33D	3.3
LVCMOS25D	2.5
LVCMOS18D	1.8

***Note**: These interfaces can be emulated with external resistors in all devices.

2.10.3. sysI/O Buffer Banks

MachXO3D device has six I/O banks, one bank on the top, right and bottom side and three banks on the left side. Figure 2.14 shows the sysI/O banks and their associated supplies for all devices.

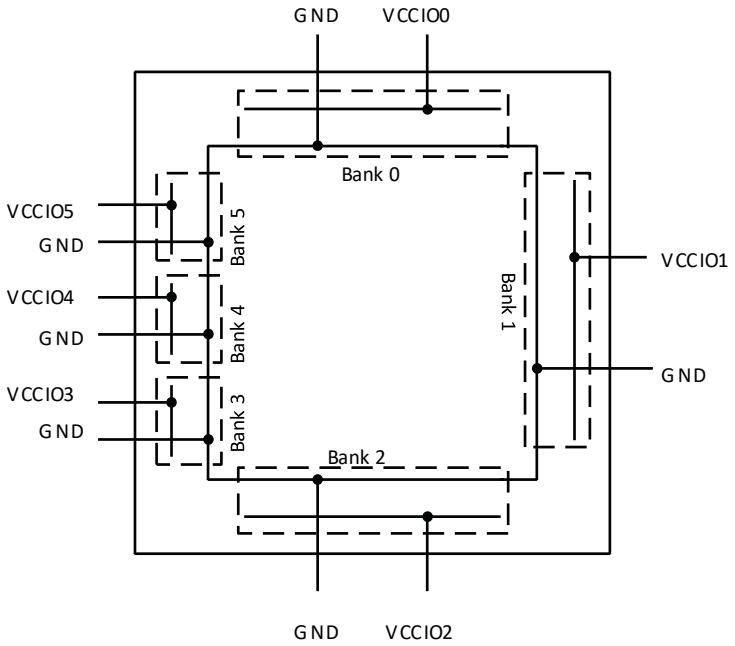


Figure 2.14. MachXO3D I/O Banks

2.11. Hot Socketing

The MachXO3D devices have been carefully designed to ensure predictable behavior during power-up and power-down. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the MachXO3D device ideal for many multiple power supply and hot-swap applications.

2.12. On-chip Oscillator

Every MachXO3D device has an internal CMOS oscillator. The oscillator output can be routed as a clock to the clock tree or as a reference clock to the sysCLOCK PLL using general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit and a user input to enable/disable the oscillator. The oscillator

frequency ranges from 2.08 MHz to 133 MHz. The software default value of the Master Clock (MCLK) is nominally 2.08 MHz. When a different MCLK is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal MCLK frequency of 2.08 MHz.
2. During configuration, users select a different master clock frequency.
3. The MCLK frequency changes to the selected frequency once the clock configuration bits are received.
4. If you do not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.08 MHz.

Table 2.13 lists all the available MCLK frequencies.

Table 2.13. Available MCLK Frequencies

MCLK (MHz, Nominal)	MCLK (MHz, Nominal)	MCLK (MHz, Nominal)
2.08 (default)	9.17	33.25
2.46	10.23	38
3.17	13.3	44.33
4.29	14.78	53.2
5.54	20.46	66.5
7	26.6	88.67
8.31	29.56	133

2.13. Embedded Hardened IP Functions

All MachXO3D devices provide embedded hardened functions such as Security, SPI, I^2C, Timer/Counter, and User Flash Memory (UFM). These embedded blocks interface through the WISHBONE interface with routing as shown in Figure 2.15. For security block, it also has the high-speed interface with routing.

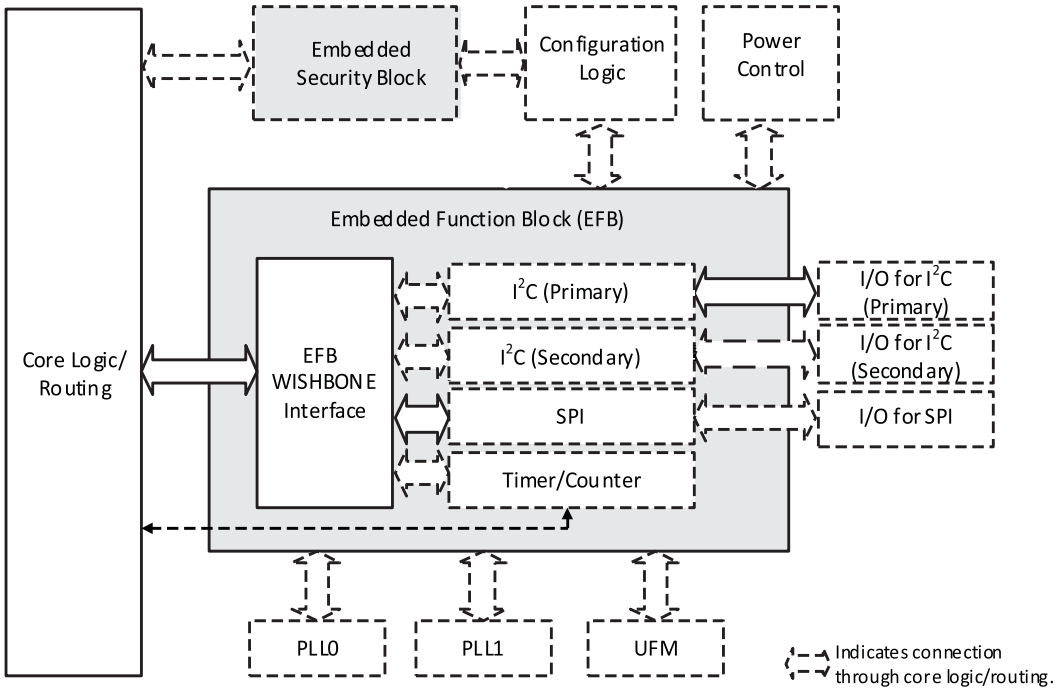


Figure 2.15. Embedded Function Block Interface

2.13.1. Embedded Security Block (ESB) IP Core

Every MachXO3D device contains one ESB IP core. The core is responsible for all the security related functions, including encryption, authentication, and key generation in both configuration and user modes.

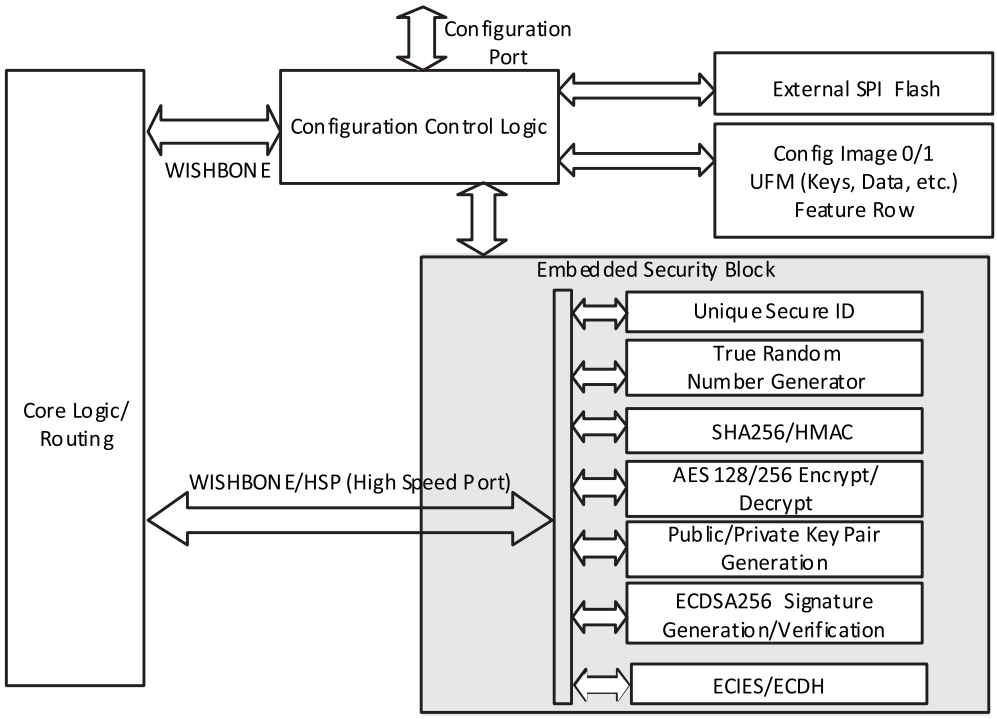


Figure 2.16. ESB Core Block Diagram

The ESB provides the following major functions:

- Secure Hash Algorithm (SHA) — 256 bits
- Elliptic Curve Digital Signature Algorithm (ECDSA) — Generation and verification
- Message Authentication Codes (MACs) — Hash-based MAC (HMAC)
- Elliptic Curve Diffie-Hellman (ECDH) Scheme
- Elliptic Curve Cryptography (ECC) Key Pair Generation — Public key/Private key
- Elliptic Curve Illustrated Encryption Standard (ECIES) Encryption/Decryption
- True Random Number Generator (TRNG)
- Advanced Encryption Standard (AES) — 128/256 bits
- Authentication controller for configuration engine
- WISHBONE interface to user logic
- High Speed Port (HSP) for FIFO-based streaming data transfer
- Unique Secure ID

To ensure the security and authenticity of the configuration bitstream, MachXO3D devices offer the following features:

- Bitstream Encryption
- Bitstream Authentication
- Bitstream Encryption and Authentication

When encryption is enabled, Diamond software encrypts the bitstream using AES key. When authentication is enabled, Lattice Diamond software attaches a certificate, which is based on the bitstream digest to the bitstream using customer's private key from the public/private ECDSA key pair. When both features are enabled, Lattice Diamond

software generates the bitstream digest and attaches the ECDSA certificate/signature to this bitstream first. In the second step, this bitstream with the signature is encrypted using the AES Key.

When programming the bitstream to the configuration image space, AES decryption and authentication are executed based on the associated AES/ECDSA public key. Once the authentication is successful, the programming is complete and the "Done" bit is set. If the authentication is unsuccessful, the MachXO3D device stays in an unprogrammed state.

After programming successfully, the MachXO3D SRAM is configured from flash to enter normal mode after power-cycling, refresh, or ProgramN toggling. It is optional to run the authentication again for each configuration with the selection of fast boot.

There are multiple hard/soft lock controls to enable the reading and writing of specific Flash location, configuration or UFM, for the high security application with the OTP option to prevent any further change to the device.

MachXO3D device provides a unique, immutable key known with Unique Secure ID. Unique Secure ID is used by ESB to generate paired public key, to perform AES encryption and decryption, and to provide other security related functions. This Unique Secure ID is unique for every device, never leaves the device and is inaccessible. No peripheral can reach the Unique Secure ID including the device own fabric.

User logic in the fabric can also access security functions in the ESB through the WISHBONE interface for the control and status register access. Payload data transfer in and out of the ESB is enabled through a FIFO-based pipelined High Speed Port. For example, the MachXO3D device can be used to authenticate the microcontroller firmware image stored in the SPI memory chip attached to the MachXO3D device before booting the microcontroller. Here the High Speed Port with the ESB can be used to transfer the contents stored in the SPI memory into the ESB for digesting of the firmware image, a step associated with the overall ECDSA authentication of the microcontroller firmware.

2.13.2. Hardened I²C IP Core

Every MachXO3D device contains two I²C IP cores. These are the primary and secondary I²C IP cores. Either of the two cores can be configured either as an I²C master or as an I²C slave. The only difference between the two IP cores is that the primary core has pre-assigned I/O pins whereas users can assign I/O pins for the secondary core.

When the IP core is configured as a master, it is able to control other devices on the I²C bus through the interface. When the core is configured as the slave, the device is able to provide I/O expansion to an I²C Master. The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Up to 400 kHz data transfer speed general call support
- On-chip spike/glitch rejection to preserve data integrity
- Interface to custom logic through 8-bit WISHBONE interface

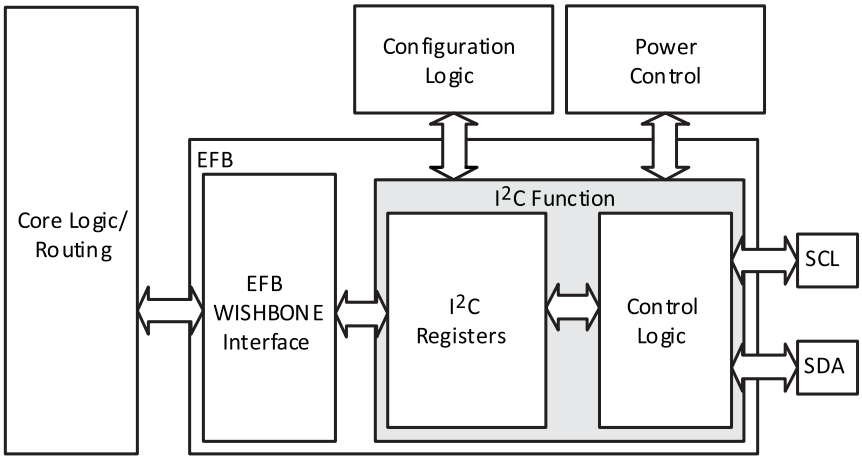


Figure 2.17. I²C Core Block Diagram

Table 2.14 describes the signals interfacing with the I²C cores.

Table 2.14. I²C Core Signal Description

Signal Name	I/O	Description
i2c_scl	Bi-directional	Bidirectional clock line of the I²C core. The signal is an output if the I²C core is in master mode. The signal is an input if the I²C core is in slave mode. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pin Information Summary section of this document for detailed pad and pin locations of I²C ports in each MachXO3D device.
i2c_sda	Bi-directional	Bidirectional data line of the I²C core. The signal is an output when data is transmitted from the I²C core. The signal is an input when data is received into the I²C core. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pin Information Summary section of this document for detailed pad and pin locations of I²C ports in each MachXO3D device.
i2c_irqo	Output	Interrupt request output signal of the I²C core. The intended usage of this signal is for it to be connected to the WISHBONE master controller (i.e. a microcontroller or state machine) and request an interrupt when a specific condition is met. These conditions are described with the I²C register definitions.
cfg_wake	Output	Wake-up signal – To be connected only to the power module of the MachXO3D device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I²C Tab.
cfg_stdby	Output	Stand-by signal – To be connected only to the power module of the MachXO3D device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I²C Tab.

2.13.3. Hardened SPI IP Core

Every MachXO3D device has a hard SPI IP core that can be configured as an SPI master or slave. When the IP core is configured as a master, it is able to control other SPI enabled chips connected to the SPI bus. When the core is configured as the slave, the device is able to interface to an external SPI master. The SPI IP core on MachXO3D devices supports the following functions:

- Configurable Master and Slave modes
- Full-duplex data transfer
- Mode fault error flag with CPU interrupt capability double-buffered data register
- Serial clock with programmable polarity and phase
- LSB first or MSB first data transfer
- Interface to custom logic through 8-bit WISHBONE interface

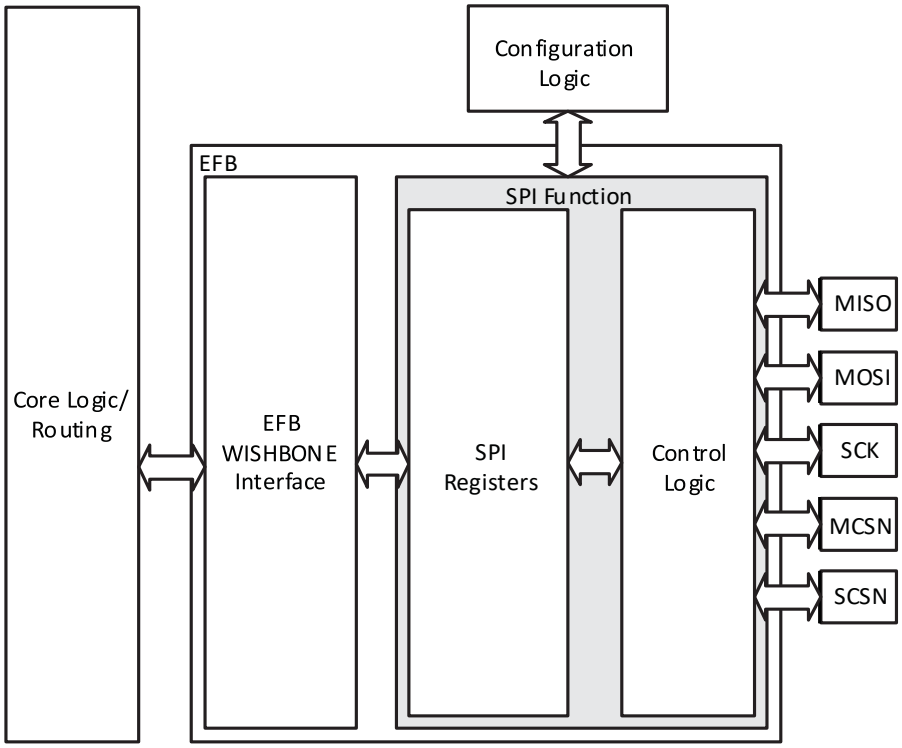


Figure 2.18. SPI Core Block Diagram

Table 2.15 describes the signals interfacing with the SPI cores.

Table 2.15. SPI Core Signal Description

Signal Name	I/O	Master/Slave	Description
spi_csn[0]	O	Master	SPI master chip-select output
spi_csn[1..7]	O	Master	Additional SPI chip-select outputs (total up to eight slaves)
spi_scsn	I	Slave	SPI slave chip-select input
spi_irq	O	Master/Slave	Interrupt request
spi_clk	I/O	Master/Slave	SPI clock. Output in master mode. Input in slave mode.
spi_miso	I/O	Master/Slave	SPI data. Input in master mode. Output in slave mode.
spi_mosi	I/O	Master/Slave	SPI data. Output in master mode. Input in slave mode.
sn	I	Slave	Configuration Slave Chip Select (active low), dedicated for selecting the Configuration Logic.
cfg_stdby	O	Master/Slave	Stand-by signal – To be connected only to the power module of the MachXO3D device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, SPI Tab.
cfg_wake	O	Master/Slave	Wake-up signal – To be connected only to the power module of the MachXO3D device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, SPI Tab.

2.13.4. Hardened Timer/Counter

MachXO3D devices provide a hard Timer/Counter IP core. This Timer/Counter is a general purpose, bidirectional, 16-bit timer/counter module with independent output compare units and PWM support. The Timer/Counter supports the following functions:

- Supports the following modes of operation:
  - Watchdog timer
  - Clear timer on compare match
  - Fast PWM
  - Phase and Frequency Correct PWM
- Programmable clock input source
- Programmable input clock prescaler
- One static interrupt output to routing
- One wake-up interrupt to on-chip standby mode controller
- Three independent interrupt sources: overflow, output compare match, and input capture
- Automatically reloading
- Time-stamping support on the input capture unit
- Waveform generation on the output
- Glitch-free PWM waveform generation with variable PWM period
- Internal WISHBONE bus access to the control and status registers
- Stand-alone mode with preloaded control registers and direct reset input

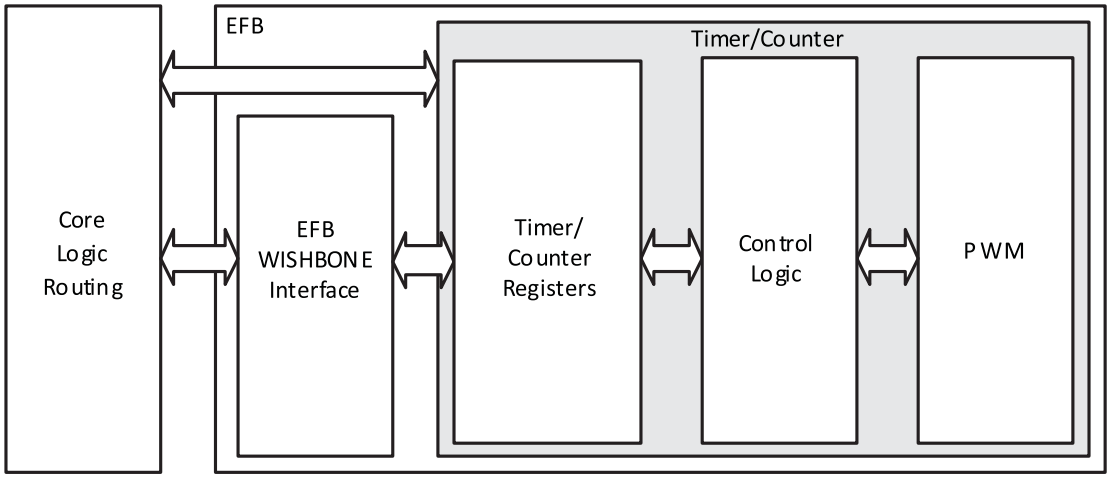


Figure 2.19. Timer/Counter Block Diagram

Table 2.16. Timer/Counter Signal Description

Port	I/O	Description
tc_clki	I	Timer/Counter input clock signal
tc_rstn	I	Register tc_rstn_ena is preloaded by configuration to always keep this pin enabled
tc_ic	I	Input capture trigger event, applicable for non-pwm modes with WISHBONE interface. If enabled, a rising edge of this signal is detected and synchronized to capture tc_cnt value into tc_icr for time-stamping.
tc_int	O	Without WISHBONE – Can be used as overflow flag With WISHBONE – Controlled by three IRQ registers
tc_oc	O	Timer counter output signal

2.14. User Flash Memory (UFM)

MachXO3D devices provide a UFM block that can be used for a variety of applications including storing a portion of the configuration image, initializing EBRs to store PROM data or, as a general purpose user Flash memory. It also has a dedicated block for the user key storage and lock control. The UFM block connects to the device core through the embedded function block WISHBONE interface. You can also access the UFM block through the JTAG, I^2C, and SPI interfaces of the device. The UFM block offers the following features:

- Non-volatile storage up to 1088 kb
- Dedicated 172 kb non-volatile storage (UFM2/3) for user key
- 100K write cycles
- Write access is performed page-wise; each page has 128 bits (16 bytes)
- Auto-increment addressing
- WISHBONE interface

Table 2.17. MachXO3D UFM Size

Device	UFM0 (kbit)	UFM1 (kbit)	UFM2 (kbit)	UFM3 (kbit)	CFG1 (kbit)*
MACHXO3D-4300	98	98	147	24	755
MACHXO3D-9400	458	458	147	24	1,605

***Note:** When the dual boot feature is disabled, the CFG1 space can be repurposed as the additional UFM usage.

2.15. Standby Mode and Power Saving Options

MachXO3D devices are available in two options for maximum flexibility: ZC and HC devices. The ZC devices have ultra low static and dynamic power consumption. The HC devices are designed to provide high performance. The HC devices have a built-in voltage regulator to allow for 2.5 V VCC and 3.3 V VCC.

MachXO3D devices have been designed with features that allow users to meet the static and dynamic power requirements of their applications by controlling various device subsystems such as the bandgap, power-on-reset circuitry, I/O bank controllers, power guard, on-chip oscillator, PLLs, etc. In order to maximize power savings, MachXO3D devices support a low power Stand-by mode.

In the stand-by mode, the MachXO3D devices are powered on and configured. Internal logic, I/O and memories are switched on and remain operational, as the user logic waits for an external input. The device enters this mode when the standby input of the standby controller is toggled or when an appropriate I^2C or JTAG instruction is issued by an external master. Various subsystems in the device such as the band gap, power-on-reset circuitry can be configured such that they are automatically turned “off” or go into a low power consumption state to save power when the device enters this state. Note that the MachXO3D devices are powered on when in standby mode and all power supplies should remain in the Recommended Operating Conditions.

Table 2.18. MachXO3D Power Saving Features Description

Device Subsystem	Feature Description
Bandgap	The bandgap can be turned off in standby mode. When the Bandgap is turned off, analog circuitry such as the POR, PLLs, on-chip oscillator, and differential I/O buffers are also turned off.
Power-On-Reset (POR)	The POR can be turned off in standby mode. This monitors VCC levels. In the event of unsafe VCC drops, this circuit reconfigures the device. When the POR circuitry is turned off, limited power detector circuitry is still active. This option is only recommended for applications in which the power supply rails are reliable.
On-Chip Oscillator	The on-chip oscillator has two power saving features. It may be switched off if it is not needed in your design. It can also be turned off in Standby mode.
PLL	Similar to the on-chip oscillator, the PLL also has two power saving features. It can be statically switched off if it is not needed in a design. It can also be turned off in Standby mode. The PLL waits until all output clocks from the PLL are driven low before powering off.
I/O Bank Controller	Differential I/O buffers (used to implement standards such as LVDS) consume more than ratioed single-ended I/O such as LVCMOS and LVTTL. The I/O bank controller allows you to turn these I/O off dynamically on a per bank selection.
Dynamic Clock Enable for Primary Clock Nets	Each primary clock net can be dynamically disabled to save power.
Power Guard	Power Guard is a feature implemented in input buffers. This feature allows users to switch off the input buffer when it is not needed. This feature can be used in both clock and data paths. Its biggest impact is that in the standby mode it can be used to switch off clock inputs that are distributed using general routing resources.

2.16. Power On Reset

MachXO3D devices have power-on reset circuitry to monitor V_{CCINT} and V_{CCIO} voltage levels during power-up and operation. At power-up, the POR circuitry monitors V_{CCINT} and V_{CCIO0} (controls configuration) voltage levels. It then triggers download from the on-chip configuration Flash memory after reaching the V_{PORUP} level specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. For “C” devices with voltage regulators, V_{CCINT} is regulated from the V_{CC} supply voltage. From this voltage reference, the time taken for configuration and entry into user mode is specified as Flash Download Time ($t_{REFRESH}$) in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/O are held in tri-state. I/O are released to user functionality once the device has finished configuration. Note that for “C” devices, a separate POR circuit monitors external V_{CC} voltage in addition to the POR circuit that monitors the internal post-regulated power supply voltage level.

Once the device enters into user mode, the POR circuitry can optionally continue to monitor V_{CCINT} levels. If V_{CCINT} drops below $V_{PORDNBG}$ level (with the bandgap circuitry switched on) or below $V_{PORDNSRAM}$ level (with the bandgap circuitry switched off to conserve power) device functionality cannot be guaranteed. In such a situation the POR issues a reset and begins monitoring the V_{CCINT} and V_{CCIO} voltage levels. $V_{PORDNBG}$ and $V_{PORDNSRAM}$ are both specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet.

When the bandgap circuitry is switched off, the POR circuitry also shuts down. The device is designed such that a minimal, low power POR circuit is still operational (this corresponds to the $V_{PORDNSRAM}$ reset point described in the paragraph above). However, this circuit is not as accurate as the one that operates when the bandgap is switched on. The low power POR circuit emulates an SRAM cell and is biased to trip before the vast majority of SRAM cells flip. If you are concerned about the V_{CC} supply dropping below V_{CC} (min), they should not shut down the bandgap or POR circuit.

2.17. Configuration and Testing

This section describes the configuration and testing features of the MachXO3D family.

2.17.1. IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO3D devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/O: TDI, TDO, TCK and TMS. The test access port shares its power supply with V_{CCIO} Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see Boundary Scan Testability with Lattice sysI/O Capability (AN8066) and Minimizing System Interruption During Configuration Using TransFR Technology (TN1087).

2.17.2. Device Configuration

All MachXO3D devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port, which supports serial configuration through I^2C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO3D device:

- Internal Flash Download
- JTAG
- Standard Serial Peripheral Interface (Master SPI mode) – interface to boot PROM memory
- System microprocessor to drive a serial slave SPI port (SSPI mode)
- Standard I^2C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it remains active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally, the device can run a CRC check upon entering the user mode. This ensures that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins, which can be used as general purpose I/O, if they are not required for configuration.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO3D devices. Use of this technology allows Lattice Semiconductor to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip Flash, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip Flash.

2.17.2.1. Encryption & Authentication

With the Embedded Security Block, MachXO3D device can provide highly secured control for the device programming and configuration. It uses ECDSA256 algorithm for Configuration Image Authentication. It has the AES256 encryption for additional security and IP protection.

2.17.2.2. Transparent Field Reconfiguration (TransFR)

TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details, refer to Minimizing System Interruption During Configuration Using TransFR Technology (TN1087) for details.

2.17.2.3. Lock Bits and Lock Control Policy

MachXO3D device has read, program, and erase permission control for external CFG ports and for internal WISHBONE bus to access Flash sectors. External CFG ports include JTAG, slave SPI, and slave I^2C. The way to support this feature is to deploy three permission control setting bits for each sectors as SEC_READ, SEC_PROG, and SEC_ERASE.

- SEC_READ — Disable the READ access. This prevents user content from being exposed to external CFG port.
- SEC_PROG— Disable the PROGRAM access. This prevents unexpected incremental programming to modify the current user setting, such as AES KEY, ECDSA PUBLIC KEY or authenticated Bitstream, and others.
- SEC_ERASE— Disable the ERASE access. This prevents unexpected incremental programming to modify the current user setting, such as AES KEY, ECDSA PUBLIC KEY or authenticated Bitstream, and others. This also ensures a safe boot up.

MachXO3D device also provides *Hard Lock* and *Soft Lock* modes for flexible permission control. *Soft Lock* means the security setting bits can be modified by internal WISHBONE bus. In this way, user logic can enable or disable the access by altering the security control bits through internal WISHBONE Bus. *Hard Lock* mode means user logic cannot alter permission control bits through internal WISHBONE bus. The SEC_HLOCK bit is used to choose between the *Soft Lock* and *Hard Lock* modes.

For detailed information regarding Lock Bits and Lock Control Policy, refer to MachXO3D Programming and Configuration Usage Guide (FPGA-TN-02069).

2.17.2.4. Tamper Detection and Response

Configuration logic automatically detects a variety of threat from configuration ports. These threats include any commands/instructions that:

- Try to access Flash/SRAM without entering password or with entering wrong password, if password protection is enabled.
- Try to access Flash/SRAM that is under Soft/Hard Lock protection.
- Attempt to enter MANUFACTURE mode.
- Shift in a wrong password by LSC_SHIFT_PASSWORD.

The Configuration module asserts *threat detect* to user logic once the enabled type of threat has been detected. Also, the Configuration module reports which type of threat is detected and from which configuration port the threat comes.

Once a certain threat has been detected, User logic may inform the Configuration module to disable configuration ports to avoid a dictionary style attack.

2.17.2.5. Password

The MachXO3D device maintains the legacy support, as in the previous generation, for password-based security access feature also known as Flash Protect Key. The Flash Protect Key feature provides a method of controlling access to the Configuration and Programming modes of the device. When enabled, the Configuration and Programming edit mode operations including Write, Verify and Erase operations are allowed only when coupled with a Flash Protect Key, which matches that expected by the device. Without a valid Flash Protect Key, you can perform only rudimentary non-configuration operations such as Read Device ID.

2.17.2.6. On-chip Dual Boot

MachXO3D devices can optionally boot from two patterns, a primary bitstream and a golden bitstream. If the primary bitstream is found to be corrupt while being downloaded into the SRAM, the device shall then automatically re-boot from the golden bitstream. MachXO3D device also supports the option to boot from the latest image in a ping-pong style, or user select for the boot image.

Beyond the On-chip boot, MachXO3D device also provides the external SPI flash boot option. Together with the On-chip boot flash, MachXO3D device can enable the flexible multi-boot function.

2.17.2.7. Soft Error Detection

The Soft Error Detection (SED) feature is a CRC check of the SRAM cells after the device is configured. This check ensures that the SRAM cells were configured successfully. This feature is enabled by a configuration bit option. The Soft Error Detection (SED) can also be initiated in user mode via an input to the fabric. The clock for the Soft Error Detection (SED) circuit is generated using a dedicated divider. The undivided clock from the on-chip oscillator is the input to this divider. For low power applications, you can switch off the Soft Error Detection circuit.

2.17.2.8. Soft Error Correction

The MachXO3D device supports Soft Error Correction (SEC). When BACKGROUND_RECONFIG is enabled using the Lattice Diamond Software in a design, asserting the PROGRAMN pin or issuing the REFRESH sysConfig command refreshes the SRAM array from configuration memory. Only the detected error bit is corrected. No other SRAM cells are changed, allowing the user design to function uninterrupted.

During the project design phase, if the overall system cannot guarantee containment of the error or its subsequent effects on downstream data or control paths, Lattice Semiconductor recommends using SED only. MachXO3D device can then be soft-reset by asserting PROGRAMN or issuing the Refresh command over a sysConfig port in response to SED. Soft-reset additionally erases the SRAM array prior to the SRAM refresh, and asserts internal Reset circuitry to guarantee a known state.

2.18. TraceID

Each MachXO3D device contains a unique (per device) TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the EFB WISHBONE interface and can also be accessed through the SPI, I^2C, or JTAG interfaces.

2.19. Density Shifting

The MachXO3D family has been designed to enable density migration within the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization impact the likely success in each case. When migrating from lower to higher density or higher to lower density, ensure to review all the power supplies and NC pins of the chosen devices.

3. DC and Switching Characteristics

3.1. Absolute Maximum Rating

Table 3.1. Absolute Maximum Rating[1,2,3]

	MachXO3D ZC/HC (2.5 V/3.3 V)
Supply Voltage V_{CC}	–0.5 V to 3.75 V
Output Supply Voltage V_{CCIO}	–0.5 V to 3.75 V
I/O Tri-state Voltage Applied [4,5]	–0.5 V to 3.75 V
Dedicated Input Voltage Applied[4]	–0.5 V to 3.75 V
Storage Temperature (Ambient)	–55 °C to 125 °C
Junction Temperature (T_J)	–40 °C to 125 °C

Notes:

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management (FPGA-TN-02044) document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of –2 V to (VIHMAX + 2) volts is permitted for a duration of <20 ns.
5. The dual function I^2C pins SCL and SDA are limited to –0.25 V to 3.75 V or to –0.3 V with a duration of <20 ns.

3.2. Recommended Operating Conditions

Table 3.2. Recommended Operating Conditions[1]

Symbol	Parameter	Min.	Max.	Units
V_{CC}[1]	Core Supply Voltage for 2.5 V/3.3 V Devices	2.375	3.465	V
V_{CCIO}[1,2,3]	I/O Driver Supply Voltage	1.14	3.465	V
t_{JCOM}	Junction Temperature Commercial Operation	0	85	°C
t_{JIND}	Junction Temperature Industrial Operation	–40	100	°C
t_{JAUTO}	Junction Temperature Automotive Operation	–40	125	°C

Notes:

1. Like power supplies must be tied together. For example, if V_{CCIO} and V_{CC} are both the same voltage, they must also be the same supply.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.

3.3. Power Supply Ramp Rates

Table 3.3. Power Supply Ramp Rates*

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{RAMP}	Power supply ramp rates for all power supplies.	0.01	—	40	V/ms

***Note:** Assumes monotonic ramp rates.

3.4. Power-On-Reset Voltage Levels

Table 3.4. Power-On Reset Voltage Levels[1,2,3,4]

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{PORUP}	Power-On-Reset ramp up trip point (band gap based circuit monitoring V_{CCINT} and V_{CCIO0})	0.90	—	1.06	V

Symbol	Parameter	Min.	Typ.	Max.	Units
$V_{PORUPEXT}$	Power-On-Reset ramp up trip point (band gap based circuit monitoring external V_{CC} power supply)	1.50	—	2.10	V
V_{PORNBG}	Power-On-Reset ramp down trip point (band gap based circuit monitoring V_{CCINT})	0.75	—	1.04	V
$V_{PORDNBGEXT}$	Power-On-Reset ramp down trip point (band gap based circuit monitoring V_{CC})	0.98	—	1.44	V
$V_{PORDNSRAM}$	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V_{CCINT})	—	0.84	—	V
$V_{PORDNSRAMEXT}$	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V_{CC})	—	1.16	—	V

Notes:
1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
2. For devices without voltage regulators V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators, V_{CCINT} is regulated from the V_{CC} supply voltage.
3. Note that V_{PORUP} (min.) and $V_{PORDNBG}$ (max.) are in different process corners. For any given process corner $V_{PORDNBG}$ (max.) is always 12.0 mV below VPORUP(min.).
4. V_{CCIO0} does not have a Power-On-Reset ramp down trip point. V_{CCIO0} must remain within the Recommended Operating Conditions to ensure proper operation.

3.5. Hot Socketing Specifications

Table 3.5. Hot Socketing Specifications[1,2,3]

Symbol	Parameter	Condition	Max.	Units
I_{DK}	Input or I/O leakage Current	$0 < V_{IN} < V_{IH}$ (MAX)	± 1000	µA

Notes:
1. Insensitive to sequence of V_{CC} and V_{CCIO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCIO}.
2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCIO} < V_{CCIO}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}.

3.6. Programming/Erase Specifications

Table 3.6. Programming/Erase Specifications

Symbol	Parameter	Min	Max.	Units
$N_{PROGCYC}$	Flash Programming cycles per $t_{RETENTION}$	—	10,000	Cycles
	Flash Write/Erase cycles	—	100,000	
$t_{RETENTION}$	Data retention at 100°C junction temperature	10	—	Years
	Data retention at 85°C junction temperature	20	—	

Notes:
1. Maximum Flash memory reads are limited to 7.5E13 cycles over the lifetime of the product.
2. A Write/Erase cycle is defined as any number of writes over time followed by any erase cycle.

3.7. ESD Performance

Refer to the MachXO3D Product Family Qualification Summary for complete qualification data, including ESD performance.

3.8. DC Electrical Characteristics

Over Recommended Operating Conditions

Table 3.7. DC Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 4]	Input or I/O Leakage	Clamp OFF and $V_{CCIO} < V_{IN} < V_{IH}$ (MAX)	—	—	175	µA
		Clamp OFF and $V_{IN} = V_{CCIO}$	–10	—	10	µA
		Clamp OFF and V_{CCIO} - 0.97 V < $V_{IN} < V_{CCIO}$	–175	—	—	µA
		Clamp OFF and 0 V < $V_{IN} < V_{CCIO}$ – 0.97 V	—	—	10	µA
		Clamp OFF and V_{IN} = GND	—	—	10	µA
		Clamp ON and 0 V < $V_{IN} < V_{CCIO}$	—	—	10	µA
I_{PU}	I/O Active Pull-up Current	0 < V_{IN} < 0.7 V_{CCIO}	–30	—	–309	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) < $V_{IN} < V_{CCIO}$	30	—	305	µA
I_{BHLS}	Bus Hold Low sustaining current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High sustaining current	V_{IN} = 0.7V_{CCIO}	–30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive current	0 ≤ $V_{IN} ≤ V_{CCIO}$	—	—	305	µA
I_{BHHO}	Bus Hold High Overdrive current	0 ≤ $V_{IN} ≤ V_{CCIO}$	—	—	–309	µA
V_{BHT}[3]	Bus Hold Trip Points	—	VIL (MAX)	—	VIH (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = Typ., V_{IO} = 0 to V_{IH} (MAX)	3	5	9	pf
V_{HYST}	Hysteresis for Schmitt Trigger Inputs[5]	V_{CCIO} = 3.3 V, Hysteresis = Large	—	450	—	mV
		V_{CCIO} = 2.5 V, Hysteresis = Large	—	250	—	mV
		V_{CCIO} = 1.8 V, Hysteresis = Large	—	125	—	mV
		V_{CCIO} = 1.5 V, Hysteresis = Large	—	100	—	mV
		V_{CCIO} = 3.3 V, Hysteresis = Small	—	250	—	mV
		V_{CCIO} = 2.5 V, Hysteresis = Small	—	150	—	mV
		V_{CCIO} = 1.8 V, Hysteresis = Small	—	60	—	mV
		V_{CCIO} = 1.5 V, Hysteresis = Small	—	40	—	mV

Notes:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25 °C, f = 1.0 MHz.
3. Refer to V_{IL} and V_{IH} in the sysI/O Single-Ended DC Electrical Characteristics table of this document.
4. When V_{IH} is higher than V_{CCIO}, a transient current typically of 30 ns in duration or less with a peak current of 6 mA can occur on the high-to- low transition. For true LVDS output pins in MachXO3D devices, V_{IH} must be less than or equal to V_{CCIO}.
5. With bus keeper circuit turned on.

3.9. Static Supply Current

Table 3.8. Static Supply Current [1,2,3,6]

Symbol	Parameter	Device	Typ.[4]	Units
I_{CC}	Core Power Supply	MACHXO3D-4300HC	—	mA
		MACHXO3D-4300ZC	—	mA
		MACHXO3D-9400HC	20	mA
		MACHXO3D-9400ZC	12	mA
I_{CCIO}	Bank Power Supply[5] V_{CCIO} = 2.5 V	All devices	10	uA

Notes:

1. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip oscillator is off, on-chip PLL is off.
2. Frequency = 0 MHz.
3. T_J = 25 °C, power supplies at nominal voltage.
4. Does not include pull-up/pull-down.
5. To determine the MachXO3D peak start-up current data, use the Power Calculator tool.
6. Determination of safe ambient operating conditions requires use of the Diamond Power Calculator tool.

3.10. Programming and Erase Supply Current

Table 3.9. Programming and Erase Supply Current[1,2,3,4]

Symbol	Parameter	Device	Typ.[4]	Units
I_{CC}	Core Power Supply	MACHXO3D-4300HC	—	mA
		MACHXO3D-4300ZC	—	mA
		MACHXO3D-9400HC	71	mA
		MACHXO3D-9400ZC	64	mA
I_{CCIO}	Bank Power Supply[5] V_{CCIO} = 2.5 V	All devices	10	uA

Notes:

1. Assumes all inputs are held at V_{CCIO} or GND and all outputs are tri-stated.
2. Typical user pattern.
3. JTAG programming is at 25 MHz.
4. T_J = 25 °C, power supplies at nominal voltage.
5. Per bank. V_{CCIO} = 2.5 V. Does not include pull-up/pull-down.

3.11. sysI/O Recommended Operating Conditions

Table 3.10. sysI/O Recommended Operating Conditions

Standard	V_{CCIO} (V)			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3	3.135	3.3	3.465	—	—	—
LVCMOS 2.5	2.375	2.5	2.625	—	—	—
LVCMOS 1.8	1.71	1.8	1.89	—	—	—
LVCMOS 1.5	1.425	1.5	1.575	—	—	—
LVCMOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.465	—	—	—
LVDS25[1, 2]	2.375	2.5	2.625	—	—	—
LVDS33[1, 2]	3.135	3.3	3.465	—	—	—
LVPECL[1]	3.135	3.3	3.465	—	—	—
BLVDS[1]	2.375	2.5	2.625	—	—	—
MIPI[3]	2.375	2.5	2.625	—	—	—
MIPI_LP[3]	1.14	1.2	1.26	—	—	—
I3C33	3.135	3.3	3.465	—	—	—
I3C18	171	1.8	1.89	—	—	—
I3C12	1.14	1.2	1.26	—	—	—
LVCMOS25R33	3.135	3.3	3.465	1.1	1.25	1.4
LVCMOS18R33	3.135	3.3	3.465	0.75	0.9	1.05
LVCMOS18R25	2.375	2.5	2.625	0.75	0.9	1.05
LVCMOS15R33	3.135	3.3	3.465	0.6	0.75	0.9
LVCMOS15R25	2.375	2.5	2.625	0.6	0.75	0.9
LVCMOS12R33[4]	3.135	3.3	3.465	0.45	0.6	0.75
LVCMOS12R25[4]	2.375	2.5	2.625	0.45	0.6	0.75
LVCMOS10R33[4]	3.135	3.3	3.465	0.35	0.5	0.65
LVCMOS10R25[4]	2.375	2.5	2.625	0.35	0.5	0.65

Notes:

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.
2. For the dedicated LVDS buffers.
3. Requires the addition of external resistors.
4. Supported only for inputs and BIDIs for –6 speed grade devices.

3.12. sysI/O Single-Ended DC Electrical Characteristics

Table 3.11. sysI/O Single-Ended DC Electrical Charateristics[1,2]

Input/Output Standard	V_{IL}		V_{IH}		VOL Max. (V)	VOH Min. (V)	IOL Max.[4] (mA)	IOH Max.[4] (mA)
	Min. (V)[3]	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3 LVTTL	–0.3	0.8	2.0	3.6	0.4	V_{CCIO} – 0.4	4	–4
							8	–8
							12	–12
							16	–16
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 2.5	–0.3	0.7	1.7	3.6	0.4	V_{CCIO} – 0.4	4	–4
							8	–8
							12	–12
							16	–16
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.8	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.6	0.4	V_{CCIO} – 0.4	4	–4
							8	–8
							12	–12
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.5	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.6	0.4	V_{CCIO} – 0.4	4	–4
							8	–8
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.2	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.6	0.4	V_{CCIO} – 0.4	4	–2
							8	–6
					0.2	V_{CCIO} – 0.2	0.1	–0.1
I3C33	–0.3	0.8	2.0	3.6	0.27	V_{CCIO} – 0.27	4	–4
I3C18	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.6	0.27	V_{CCIO} – 0.27	4	–4
I3C12	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.6	0.18	V_{CCIO} – 0.19	2	–2
LVCMOS25R33	–0.3	V_{REF} – 0.1	V_{REF}+0.1	3.6	NA	NA	NA	NA
LVCMOS18R33	–0.3	V_{REF} – 0.1	V_{REF}+0.1	3.6	NA	NA	NA	NA
LVCMOS18R25	–0.3	V_{REF} – 0.1	V_{REF}+0.1	3.6	NA	NA	NA	NA
LVCMOS15R33	–0.3	V_{REF} – 0.1	V_{REF}+0.1	3.6	NA	NA	NA	NA
LVCMOS15R25	–0.3	V_{REF} – 0.1	V_{REF}+0.1	3.6	NA	NA	NA	NA
LVCMOS12R33	–0.3	V_{REF} – 0.1	V_{REF}+0.1	3.6	0.40	NA	24, 16, 12, 8, 4	NA
LVCMOS12R25	–0.3	V_{REF} – 0.1	V_{REF}+0.1	3.6	0.40	NA	16, 12, 8, 4	NA
LVCMOS10R33	–0.3	V_{REF} – 0.1	V_{REF}+0.1	3.6	0.40	NA	24, 16, 12, 8, 4	NA
LVCMOS10R25	–0.3	V_{REF} – 0.1	V_{REF}+0.1	3.6	0.40	NA	16, 12, 8, 4	NA

Notes:

1. MachXO3D devices allow LVCMOS inputs to be placed in I/O banks where VCCIO is different from what is specified in the applicable JEDEC specification. This is referred to as a ratioed input buffer. In a majority of cases, this operation follows or exceeds the applicable JEDEC specification.
2. MachXO3D devices allow for LVCMOS referenced I/O, which follow applicable JEDEC specifications.
3. The dual function I^2C pins SCL and SDA are limited to a V_{IL} min of –0.25 V or to –0.3 V with a duration of <10 ns.
4. For electromigration, the average DC current sourced or sinked by I/O pads between two consecutive V_{CCIO} or GND pad connections, or between the last V_{CCIO} or GND in an I/O bank and the end of an I/O bank, as shown in the Logic Signal Connections table (also shown as I/O grouping) shall not exceed a maximum of n * 8 mA. “n” is the number of I/O pads between the two consecutive bank V_{CCIO} or GND connections or between the last V_{CCIO} and GND in a bank and the end of a bank. I/O Grouping can be found in the Data Sheet Pin Tables, which can also be generated from the Lattice Diamond software.

3.13. sysI/O Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of the MachXO3D PLD family.

3.13.1. LVDS

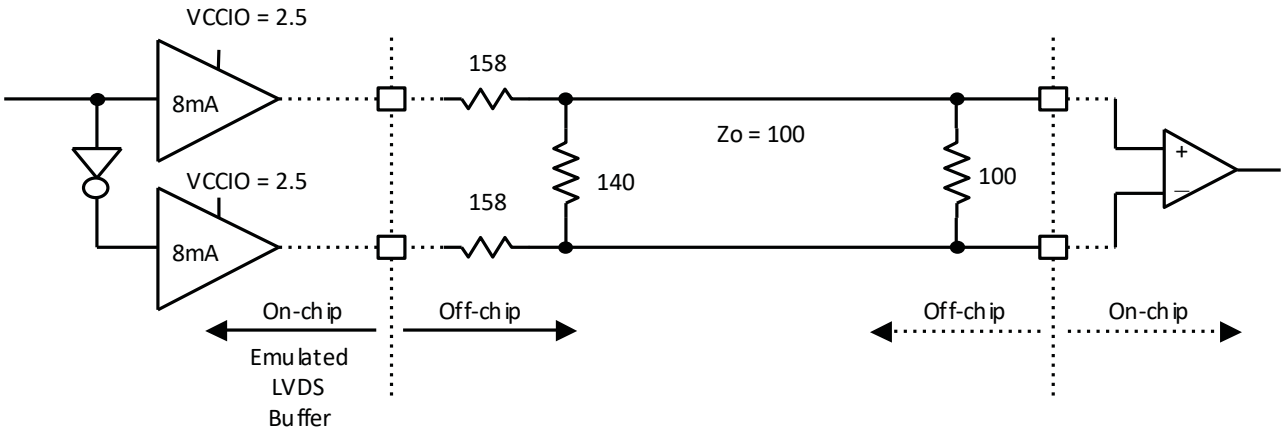
Over Recommended Operating Conditions.

Table 3.12. LVDS

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage	V_{CCIO} = 3.3 V	0	—	2.6	V
		V_{CCIO} = 2.5 V	0	—	2.0	V
V_{THD}	Differential Input Threshold	—	±100	—		mV
V_{CM}	Input Common Mode Voltage	V_{CCIO} = 3.3 V	0.05	—	2.6	V
		V_{CCIO} = 2.5 V	0.05	—	2.0	V
I_{IN}	Input current	Power on	—	—	±10	µA
V_{OH}	Output high voltage for V_{OP} or V_{OM}	R_T = 100 Ω	—	1.375	—	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	R_T = 100 Ω	0.9	1.025	—	V
V_{OD}	Output voltage differential	(V_{OP} - V_{OM}), R_T = 100 Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low	—	—	—	50	mV
V_{OS}	Output voltage offset	(V_{OP} - V_{OM})/2, R_T = 100 Ω	1.1	1.20	1.395	V
ΔV_{OS}	Change in V_{OS} between H and L	—	—	—	50	mV
I_{OSD}	Output short circuit current	V_{OD} = 0 V driver outputs shorted	—	—	24	mA

3.13.2. LVDS Emulation

MachXO3D devices can support LVDS outputs via emulation (LVDS25E). The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3.1 is one possible solution for LVDS standard implementation. Resistor values in Figure 3.1 are industry standard values for 1% resistors.



Note: All resistors are ±1%.

Figure 3.1. LVDS Using External Resistors (LVDS25E)

3.13.3. LVDS25E DC Conditions

Over Recommended Operating Conditions

Table 3.13. LVDS25E DC Conditions

Parameter	Description	Typ.	Units
Z_{OUT}	Output impedance	20	Ω
R_S	Driver series resistor	158	Ω
R_P	Driver parallel resistor	140	Ω
R_T	Receiver termination	100	Ω
V_{OH}	Output high voltage	1.43	V
V_{OL}	Output low voltage	1.07	V
V_{OD}	Output differential voltage	0.35	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	100	Ω
I_{DC}	DC output current	6.03	mA

3.13.4. BLVDS

The MachXO3D family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3.2 is one possible solution for bi-directional multi-point differential signals.

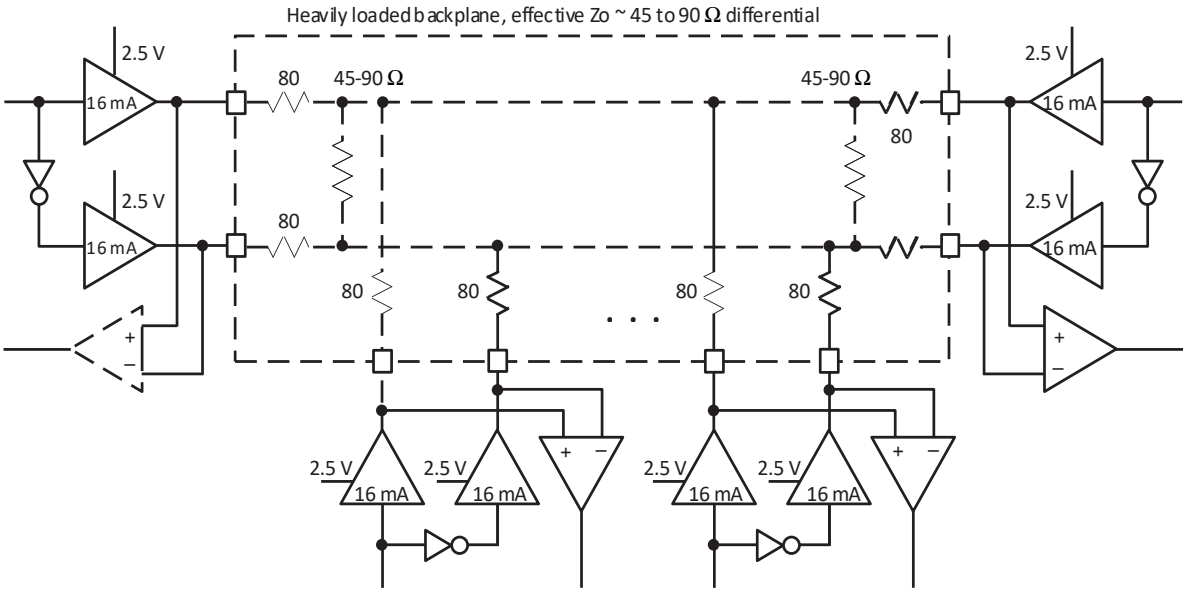


Figure 3.2. BLVDS Multi-point-Output Example

3.13.5. BLVDS DC Condition

Over Recommend Operating Conditions

Table 3.14. BLVDS DC Conditions*

Symbol	Description	Nominal		Units
		Zo = 45	Zo = 90	
Z_{OUT}	Output impedance	20	20	Ω
R_S	Driver series resistance	80	80	Ω
R_{TLEFT}	Left end termination	45	90	Ω
R_{TRIGHT}	Right end termination	45	90	Ω
V_{OH}	Output high voltage	1.375	1.480	V
V_{OL}	Output low voltage	1.125	1.020	V
V_{OD}	Output differential voltage	0.25	0.46	V
V_{CM}	Output common mode voltage	1.250	1.250	V
I_{DC}	DC output current	11.24	10.20	mA

***Note**: For input buffer, see Table 3.12.

3.13.6. LVPECL

The MachXO3D family supports the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Differential LVPECL is one possible solution for point-to-point signals.

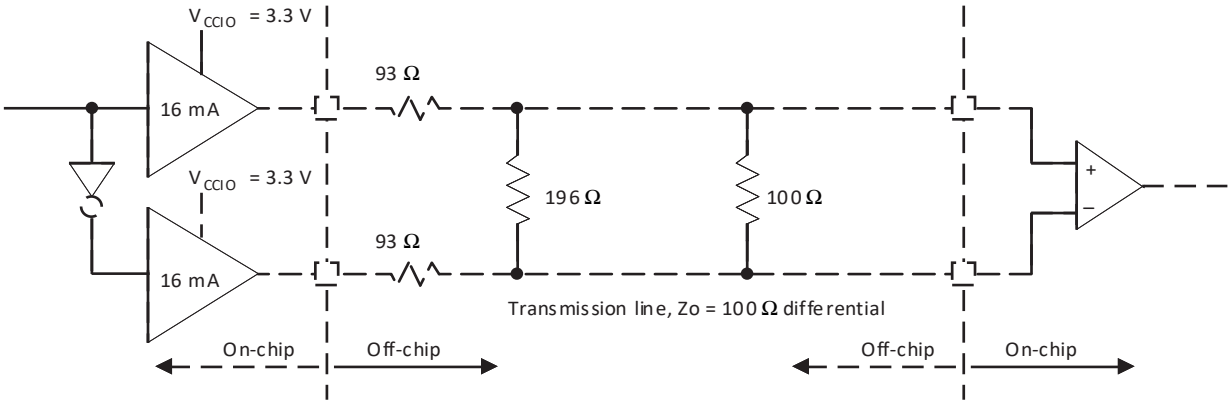


Figure 3.3. Differential LVPECL

3.13.7. LVPECL DC Conditions

Over Recommended Operating Conditions

Table 3.15. LVPECL DC Conditions*

Symbol	Description	Nominal	Units
Z_{OUT}	Output impedance	20	Ω
RS	Driver series resistor	93	Ω
RP	Driver parallel resistor	196	Ω
RT	Receiver termination	100	Ω
VOH	Output high voltage	2.05	V
VOL	Output low voltage	1.25	V
VOD	Output differential voltage	0.80	V
VCM	Output common mode voltage	1.65	V
ZBACK	Back impedance	100	Ω
IDC	DC output current	12.11	mA

***Note**: For input buffer, see Table 3.12.

For further information on LVPECL, BLVDS and other differential interfaces, see details of additional technical documentation at the end of the data sheet.

3.13.8. MIPI D-PHY Emulation

MachXO3D devices can support MIPI D-PHY unidirectional High Speed (HS) and bidirectional Low Power (LP) inputs and outputs via emulation. In conjunction with external resistors, High Speed I/O use the LVDS25E buffer and Low Power I/O use the LVCMOS buffers. The scheme shown in Figure 3.4 is one possible solution for MIPI D-PHY Receiver implementation. The scheme shown in Figure 3.5 is one possible solution for MIPI D-PHY Transmitter implementation.

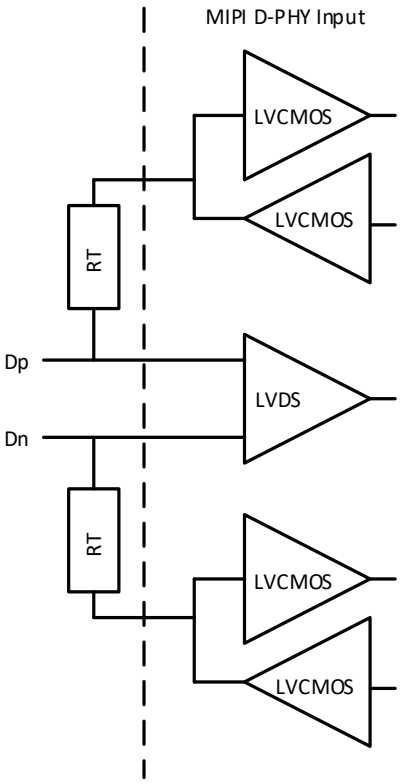


Figure 3.4. MIPI D-PHY Input Using External Resistors

Over recommended operating conditions.

Table 3.16. MIPI DC Conditions

Symbol	Description	Min.	Typ.	Max.	Units
Receiver					
External Termination					
RT	1% external resistor with V_{CCIO}=2.5 V	—	50	—	Ω
	1% external resistor with V_{CCIO}=3.3 V	—	50	—	Ω
High Speed					
V_{CCIO}	V_{CCIO} of the Bank with LVDS Emulated input buffer	—	2.5	—	V
	V_{CCIO} of the Bank with LVDS Emulated input buffer	—	3.3	—	V
V_{CMRX}	Common-mode voltage HS receive mode	150	200	250	mV
V_{IDTH}	Differential input high threshold	—	—	100	mV
V_{IDTL}	Differential input low threshold	–100	—	—	mV
V_{IHHS}	Single-ended input high voltage	—	—	300	mV
V_{ILHS}	Single-ended input low voltage	100	—	—	mV
ZID	Differential input impedance	80	100	120	Ω
Low Power					
V_{CCIO}	V_{CCIO} of the Bank with LVCMOS12D 6 mA drive bidirectional I/O buffer	—	1.2	—	V
V_{IH}	Logic 1 input voltage	—	—	0.88	V
V_{IL}	Logic 0 input voltage, not in ULP State	0.55	—	—	V
V_{HYST}	Input hysteresis	25	—	—	mV

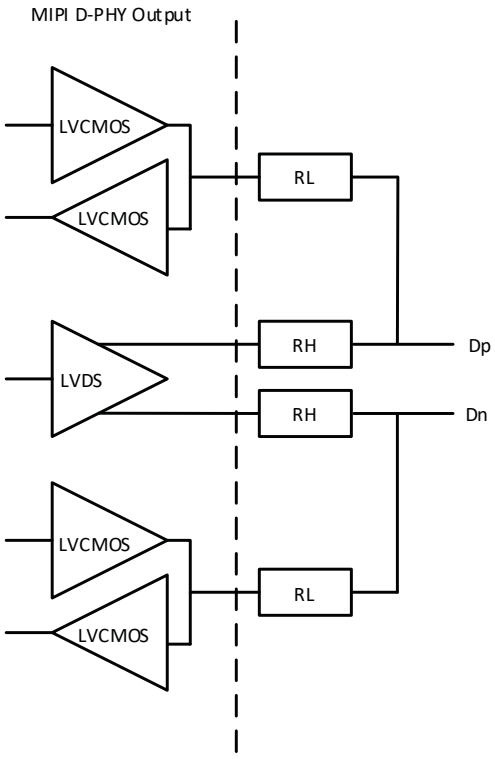


Figure 3.5. MIPI D-PHY Output Using External Resistors

Over recommended operating conditions.

Table 3.17. MIPI D-PHY Output DC Conditions

Symbol	Description	Min.	Typ.	Max.	Units
Transmitter					
External Termination					
R_L	1% external resistor with V_{CCIO} = 2.5 V	—	50	—	Ω
	1% external resistor with V_{CCIO} = 3.3 V	—	50	—	
R_H	1% external resistor with performance up to 800 Mbps or with performance up 900 Mbps when V_{CCIO} = 2.5 V	—	330	—	Ω
	1% external resistor with performance between 800 Mbps to 900 Mbps when V_{CCIO} = 3.3 V	—	464	—	Ω
High Speed					
V_{CCIO}	V_{CCIO} of the Bank with LVDS Emulated output buffer	—	2.5	—	V
	V_{CCIO} of the Bank with LVDS Emulated output buffer	—	3.3	—	V
V_{CMTX}	HS transmit static common mode voltage	150	200	250	mV
V_{OD}	HS transmit differential voltage	140	200	270	mV
V_{OHHS}	HS output high voltage	—	—	360	V
ZOS	Single ended output impedance	—	50	—	Ω
ΔZOS	Single ended output impedance mismatch	—	—	10	%
Low Power					
V_{CCIO}	V_{CCIO} of the Bank with LVCMOS12D 6 mA drive bidirectional I/O buffer	—	1.2	—	V
V_{OH}	Output high level	1.1	1.2	1.3	V
V_{OL}	Output low level	–50	0	50	mV
ZOLP	Output impedance of LP transmitter	110	—	—	Ω

3.14. Typical Building Block Function Performance

3.14.1. Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Table 3.18. Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	–6 Timing	–3 Timing	Units
Basic Functions			
16-bit decoder	7.9	13.0	ns
4:1 MUX	6.6	9.9	ns
16:1 MUX	7.8	13.3	ns

3.14.2. Register-to-Register Performance

Table 3.19. Register-to-Register Performance

Function	–6 Timing	–3 Timing	Units
Basic Functions			
16:1 MUX	423	191	MHz
16-bit adder	277	125	MHz
16-bit counter	325	149	MHz
64-bit counter	161	77	MHz
Embedded Memory Functions			
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	182	90	MHz
Distributed Memory Functions			
16x4 Pseudo-Dual Port RAM (one PFU)	500	400	MHz

Note: The above timing numbers in Table 3.18 and Table 3.19 are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.

3.15. Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

3.16. Maximum sysI/O Buffer Performance

Table 3.20. Maximum sysI/O Buffer Performance

I/O Standard	Maximum Speed	Units
MIPI	450	MHz
LVDS25	400	MHz
LVDS25E	150	MHz
BLVDS25	150	MHz
BLVDS25E	150	MHz
MLVDS25	150	MHz
MLVDS25E	150	MHz
LVPECL33	150	MHz
LVPECL33E	150	MHz
LVTTL33	150	MHz
LVTTL33D	150	MHz
LVCMOS33	150	MHz
LVCMOS33D	150	MHz
LVCMOS25	150	MHz
LVCMOS25D	150	MHz
LVCMOS18	150	MHz
LVCMOS18D	150	MHz
LVCMOS15	150	MHz
LVCMOS15D	150	MHz
LVCMOS12	91	MHz
LVCMOS12D	91	MHz
I3C33	12.5	MHz
I3C18	12.5	MHz
I3C12	12.5	MHz

3.17. MachXO3D External Switching Characteristics – HC Devices

Over Recommended Operating Conditions.

Table 3.21. MachXO3D External Switching Characteristics – HC Devices[1, 2, 3, 4, 5, 6, 10]

Parameter	Description	Device	–6		–5		Units
			Min.	Max.	Min.	Max.	
Clocks							
Primary Clocks							
f_{MAX_PRI}[7]	Frequency for Primary Clock Tree	All MachXO3D devices	—	390	—	320	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	All MachXO3D devices	0.5	—	0.6	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	MachXO3D-4300	—	—	—	—	ps
		MachXO3D-9400	—	1648	—	1657	ps
Edge Clock							
f_{MAX_EDGE}[7]	Frequency for Edge Clock	MachXO3D	—	400	—	333	MHz
Pin-LUT-Pin Propagation Delay							
t_{PD}	Best case propagation delay through one LUT-4	All MachXO3D devices	—	6.70	—	7.00	ns
General I/O Pin Parameters (Using Primary Clock without PLL)							
t_{CO}	Clock to Output – PIO Output Register	MachXO3D-4300	—	—	—	—	ns
		MachXO3D-9400	—	7.53	—	7.83	ns
t_{SU}	Clock to Data Setup – PIO Input Register	MachXO3D-4300	—	—	—	—	ns
		MachXO3D-9400	–0.24	—	–0.24	—	ns
t_{H}	Clock to Data Hold – PIO Input Register	MachXO3D-4300	—	—	—	—	ns
		MachXO3D-9400	1.99	—	2.24	—	ns
t_{SU_DEL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO3D-4300	—	—	—	—	ns
		MachXO3D-9400	1.65	—	1.80	—	ns
t_{H_DEL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO3D-4300	—	—	—	—	ns
		MachXO3D-9400	–0.24	—	–0.24	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	All MachXO3D devices	—	390	—	320	MHz
General I/O Pin Parameters (Using Edge Clock without PLL)							
T_{COE}	Clock to Output – PIO Output Register	MachXO3D-4300	—	—	—	—	ns
		MachXO3D-9400	—	8.93	—	9.35	ns
t_{SUE}	Clock to Data Setup – PIO Input Register	MachXO3D-4300	—	—	—	—	ns
		MachXO3D-9400	–0.20	—	–0.20	—	ns
t_{HE}	Clock to Data Hold – PIO Input Register	MachXO3D-4300	—	—	—	—	ns
		MachXO3D-9400	1.98	—	2.25	—	ns
t_{SU_DELE}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO3D-4300	—	—	—	—	ns
		MachXO3D-9400	1.71	—	1.85	—	ns
t_{H_DELE}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO3D-4300	—	—	—	—	ns
		MachXO3D-9400	–0.30	—	–0.30	—	ns
General I/O Pin Parameters (Using Primary Clock with PLL)							
t_{COPLL}	Clock to Output – PIO Output Register	MachXO3D-4300	—	—	—	—	ns
		MachXO3D-9400	—	5.55	—	6.13	ns
t_{SUPLL}	Clock to Data Setup – PIO Input Register	MachXO3D-4300	—	—	—	—	ns
		MachXO3D-9400	0.33	—	0.33	—	ns

Parameter	Description	Device	–6		–5		Units
			Min.	Max.	Min.	Max.	
t_{HPLL}	Clock to Data Hold – PIO Input Register	MachXO3D-4300	—	—	—	—	ns
		MachXO3D-9400	0.47	—	0.55	—	ns
t_{SU_DELPLL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO3D-4300	—	—	—	—	ns
		MachXO3D-9400	3.06	—	3.37	—	ns
t_{H_DELPLL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO3D-4300	—	—	—	—	ns
		MachXO3D-9400	–0.93	—	–0.93	—	ns
Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Aligned[8,9,13]							
t_{DVA}	Input Data Valid After CLK	All MachXO3D devices, all sides	—	0.317	—	0.344	UI
t_{DVE}	Input Data Hold After CLK		0.742	—	0.702	—	UI
f_{DATA}	DDRX1 Input Data Speed		—	300	—	250	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	150	—	125	MHz
Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Centered[8,9,13]							
t_{SU}	Input Data Setup Before CLK	All MachXO3D devices, all sides	0.566	—	0.560	—	ns
t_{HO}	Input Data Hold After CLK		0.778	—	0.879	—	ns
f_{DATA}	DDRX1 Input Data Speed		—	300	—	250	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	150	—	125	MHz
Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Aligned[8,9]							
t_{DVA}	Input Data Valid After CLK	MachXO3D devices, bottom side only	—	0.316	—	0.342	UI
t_{DVE}	Input Data Hold After CLK		0.710	—	0.675	—	UI
f_{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	332	—	277	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	MHz
Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Centered[8,9]							
t_{SU}	Input Data Setup Before CLK	MachXO3D devices, bottom side only	0.233	—	0.219	—	ns
t_{HO}	Input Data Hold After CLK		0.287	—	0.287	—	ns
f_{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	332	—	277	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	MHz
Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Aligned[8]							
t_{DVA}	Input Data Valid After ECLK	MachXO3D devices, bottom side only	—	0.307	—	0.320	UI
t_{DVE}	Input Data Hold After ECLK		0.782	—	0.699	—	UI
f_{DATA}	DDRX4 Serial Input Data Speed		—	800	—	630	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	400	—	315	MHz
f_{SCLK}	SCLK Frequency		—	100	—	79	MHz
Generic DDR4 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Centered[8]							
t_{SU}	Input Data Setup Before ECLK	MachXO3D devices, bottom side only	0.233	—	0.219	—	ns
t_{HO}	Input Data Hold After ECLK		0.287	—	0.287	—	ns
f_{DATA}	DDRX4 Serial Input Data Speed		—	800	—	630	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	400	—	315	MHz
f_{SCLK}	SCLK Frequency		—	100	—	79	MHz
7:1 LVDS Inputs (GDDR71_RX.ECLK.7:1)[9]							
t_{DVA}	Input Data Valid After ECLK (See Figure 3.6)	MachXO3D devices, bottom side only	—	0.290	—	0.320	UI
t_{DVE}	Input Data Hold After ECLK (See Figure 3.6)		0.739	—	0.699	—	UI
f_{DATA}	DDR71 Serial Input Data Speed		—	756	—	630	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	378	—	315	MHz

Parameter	Description	Device	–6		–5		Units
			Min.	Max.	Min.	Max.	
f_{CLKIN}	7:1 Input Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	MHz
MIPI D-PHY Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input - GDDRX4_RX.ECLK.Centered[10,11,12]							
t_{SU}[16]	Input Data Setup Before ECLK	All MachXO3D devices, bottom side only	0.200	—	0.200	—	UI
t_{HO}[16]	Input Data Hold After ECLK		0.200	—	0.200	—	UI
f_{DATA}[15]	MIPI D-PHY Input Data Speed		—	900	—	900	Mbps
f_{DDRX4}[15]	MIPI D-PHY ECLK Frequency		—	450	—	450	MHz
f_{SCLK}[15]	SCLK Frequency		—	112.5	—	112.5	MHz
Generic DDR Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Aligned[8,13]							
t_{DIA}	Output Data Invalid After CLK Output	All MachXO3D devices, all sides	—	0.52	—	0.55	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.52	—	0.55	ns
f_{DATA}	DDRX1 Output Data Speed		—	300	—	250	Mbps
f_{DDRX1}	DDRX1 SCLK frequency		—	150	—	125	MHz
Generic DDR Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Centered[8,13]							
t_{DVB}	Output Data Valid Before CLK Output	All MachXO3D devices, all sides	1.210	—	1.510	—	ns
t_{DVA}	Output Data Valid After CLK Output		1.210	—	1.510	—	ns
f_{DATA}	DDRX1 Output Data Speed		—	300	—	250	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency (minimum limited by PLL)		—	150	—	125	MHz
Generic DDRX2 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Aligned[8]							
t_{DIA}	Output Data Invalid After CLK Output	MachXO3D devices, top side only	—	0.200	—	0.215	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.200	—	0.215	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	664	—	554	Mbps
f_{DDRX2}	DDRX2 ECLK frequency		—	332	—	277	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	MHz
Generic DDRX2 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Centered[8,9]							
t_{DVB}	Output Data Valid Before CLK Output	MachXO3D devices, top side only	0.535	—	0.670	—	ns
t_{DVA}	Output Data Valid After CLK Output		0.535	—	0.670	—	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	664	—	554	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency (minimum limited by PLL)		—	332	—	277	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	MHz
Generic DDRX4 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Aligned[8,9]							
t_{DIA}	Output Data Invalid After CLK Output	MachXO3D devices, top side only	—	0.200	—	0.215	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.200	—	0.215	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	800	—	630	Mbps

Parameter	Description	Device	–6		–5		Units
			Min.	Max.	Min.	Max.	
f_{DDRX4}	DDRX4 ECLK Frequency		—	400	—	315	MHz
f_{SCLK}	SCLK Frequency		—	100	—	79	MHz
Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered[8,9]							
t_{DVB}	Output Data Valid Before CLK Output	MachXO3D devices, top side only	0.455	—	0.570	—	ns
t_{DVA}	Output Data Valid After CLK Output		0.455	—	0.570	—	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	800	—	630	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency (minimum limited by PLL)		—	400	—	315	MHz
f_{SCLK}	SCLK Frequency		—	100	—	79	MHz
7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1[8,9]							
t_{DIB}	Output Data Invalid Before CLK Output (See Figure 3.7)	MachXO3D devices, top side only	—	0.160	—	0.180	ns
t_{DIA}	Output Data Invalid After CLK Output (See Figure 3.7)		—	0.160	—	0.180	ns
f_{DATA}	DDR71 Serial Output Data Speed		—	756	—	630	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	378	—	315	MHz
f_{CLKOUT}	7:1 Output Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	MHz
MIPI D-PHY Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered[10,11,12]							
t_{DVB}	Output Data Valid Before CLK Output	All MachXO3D devices, top side only	0.200	—	0.200	—	UI
t_{DVA}	Output Data Valid After CLK Output		0.200	—	0.200	—	UI
f_{DATA}	MIPI D-PHY Output Data Speed		—	900	—	900	Mbps
F_{DDRX4}	MIPI D-PHY ECLK Frequency (minimum limited by PLL)		—	450	—	450	MHz
f_{SCLK}	SCLK Frequency		—	112.5	—	112.5	MHz

Notes:

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85°C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Lattice Diamond software.
2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0pf load, fast slew rate.
3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
4. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
5. For Generic DDRX1 mode tSU = tHO = (tDVE - tDVA - 0.03 ns)/2.
6. The tSU_DEL and tH_DEL values use the SCLK_ZERHOLD default step size. Each step is 105 ps (–6), 113 ps (–5).
7. This number for general purpose usage. Duty cycle tolerance is +/–10%.
8. Duty cycle is +/– 5% for system usage.
9. Performance is calculated with 0.225 UI.
10. Performance is calculated with 0.20 UI.
11. Performance for Industrial devices are only supported with VCC between 1.16 V to 1.24 V.
12. Performance for Industrial devices and –5 devices are not modeled in the Diamond design tool.
13. GDDRX1 is not recommended to mix top banks with other banks in applications. Or, the related clock skew is increased significantly.
14. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
15. Above 800 Mbps is only supported with WLCSP and csfBGA packages.
16. Between 800 Mbps to 900 Mbps:

- VIDTH exceeds the MIPI D-PHY Input DC Conditions (Over recommended operating conditions. Table 3.16) and can be calculated with the equation tSU or tH = –0.0005*VIDTH + 0.3284
- Example calculations
  - t_{SU} and t_{HO} = 0.28 with VIDTH = 100 mV
  - t_{SU} and t_{HO} = 0.25 with VIDTH = 170 mV
  - t_{SU} and t_{HO} = 0.20 with VIDTH = 270 mV

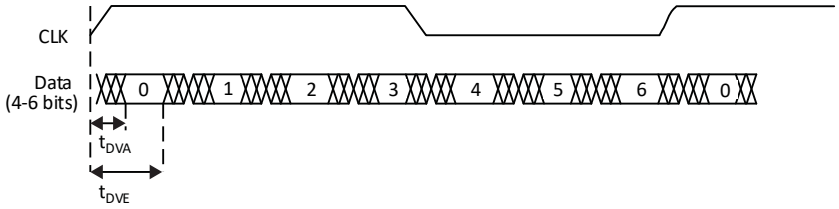


Figure 3.6. Receiver GDDR71_RX. Waveforms

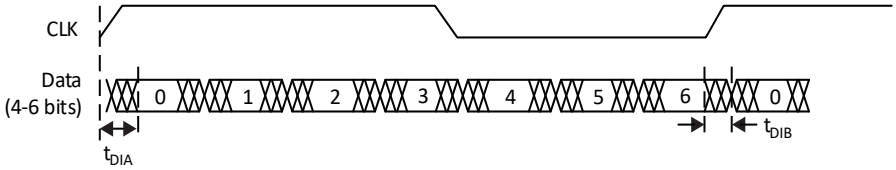


Figure 3.7. Transmitter GDDR71_TX. Waveforms

3.18. MachXO3D External Switching Characteristics – ZC Devices

Over Recommended Operating Conditions

Table 3.22. MachXO3D External Switching Characteristics – ZC Devices[1,2,3,4,5,6]

Parameter	Description	Device	–3		–2		Units
			Min.	Max.	Min.	Max.	
Clocks							
Primary Clocks							
f_{MAX_PRI}[7]	Frequency for Primary Clock Tree	All MachXO3D devices	—	150	—	125	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	All MachXO3D devices	1.0	—	1.2	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	MachXO3D-4300	—	—	—	—	ps
		MachXO3D-9400	—	1898	—	1907	ps
Edge Clock							
f_{MAX_EDGE}[7]	Frequency for Edge Clock	MachXO3D	—	210	—	175	MHz
Pin-LUT-Pin Propagation Delay							
t_{PD}	Best case propagation delay through one LUT-4	All MachXO3D devices	—	6.70	—	7.00	ns
General I/O Pin Parameters (Using Primary Clock without PLL)							
t_{CO}	Clock to Output – PIO Output Register	MachXO3D-4300	—	—	—	—	ns
		MachXO3D-9400	—	11.22	—	11.76	ns
t_{SU}	Clock to Data Setup – PIO Input Register	MachXO3D-4300	—	—	—	—	ns
		MachXO3D-9400	–0.33	—	–0.33	—	ns
t_{H}	Clock to Data Hold – PIO Input Register	MachXO3D-4300	—	—	—	—	ns
		MachXO3D-9400	5.57	—	5.83	—	ns
t_{SU_DEL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO3D-4300	—	—	—	—	ns
		MachXO3D-9400	2.17	—	2.33	—	ns
t_{H_DEL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO3D-4300	—	—	—	—	ns
		MachXO3D-9400	–0.21	—	–0.21	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	All MachXO3D devices	—	150	—	125	MHz
General I/O Pin Parameters (Using Primary Clock with PLL)							
t_{COPLL}	Clock to Output – PIO Output Register	MachXO3D-4300	—	—	—	—	ns
		MachXO3D-9400	—	8.02	—	8.14	ns
t_{SUPLL}	Clock to Data Setup – PIO Input Register	MachXO3D-4300	—	—	—	—	ns
		MachXO3D-9400	0.83	—	0.83	—	ns
t_{HPLL}	Clock to Data Hold – PIO Input Register	MachXO3D-4300	—	—	—	—	ns
		MachXO3D-9400	0.73	—	0.74	—	ns
t_{SU_DELPLL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO3D-4300	—	—	—	—	ns
		MachXO3D-9400	5.15	—	5.71	—	ns
t_{H_DELPLL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO3D-4300	—	—	—	—	ns
		MachXO3D-9400	–1.41	—	–1.41	—	ns
Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Aligned[8,9,10]							
t_{DVA}	Input Data Valid After CLK	All MachXO3D devices, all sides	—	0.382	—	0.401	UI
t_{DVE}	Input Data Hold After CLK		0.670	—	0.684	—	UI
f_{DATA}	DDRX1 Input Data Speed		—	140	—	116	Mbps

Parameter	Description	Device	–3		–2		Units
			Min.	Max.	Min.	Max.	
f_{DDRX1}	DDRX1 SCLK Frequency		—	70	—	58	MHz
Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Centered[8,9,10]							
t_{SU}	Input Data Setup Before CLK	All MachXO3D devices, all sides	1.319	—	1.412	—	ns
t_{HO}	Input Data Hold After CLK		0.717	—	1.010	—	ns
f_{DATA}	DDRX1 Input Data Speed		—	140	—	116	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	70	—	58	MHz
Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Aligned[8,9]							
t_{DVA}	Input Data Valid After CLK	MachXO3D devices, bottom side only	—	0.361	—	0.346	UI
t_{DVE}	Input Data Hold After CLK		0.602	—	0.625	—	UI
f_{DATA}	DDRX2 Serial Input Data Speed		—	280	—	234	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	140	—	117	MHz
f_{SCLK}	SCLK Frequency		—	70	—	59	MHz
Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Centered[8,9]							
t_{SU}	Input Data Setup Before CLK	MachXO3D devices, bottom side only	0.472	—	0.672	—	ns
t_{HO}	Input Data Hold After CLK		0.363	—	0.501	—	ns
f_{DATA}	DDRX2 Serial Input Data Speed		—	280	—	234	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	140	—	117	MHz
f_{SCLK}	SCLK Frequency		—	70	—	59	MHz
Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Aligned[8]							
t_{DVA}	Input Data Valid After ECLK	MachXO3D devices, bottom side only	—	0.307	—	0.316	UI
t_{DVE}	Input Data Hold After ECLK		0.662	—	0.650	—	UI
f_{DATA}	DDRX4 Serial Input Data Speed		—	420	—	352	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	210	—	176	MHz
f_{SCLK}	SCLK Frequency		—	53	—	44	MHz
Generic DDR4 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Centered[8]							
t_{SU}	Input Data Setup Before ECLK	MachXO3D devices, bottom side only	0.434	—	0.535	—	ns
t_{HO}	Input Data Hold After ECLK		0.385	—	0.395	—	ns
f_{DATA}	DDRX4 Serial Input Data Speed		—	420	—	352	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	210	—	176	MHz
f_{SCLK}	SCLK Frequency		—	53	—	44	MHz
7:1 LVDS Inputs (GDDR71_RX.ECLK.7:1)[9]							
t_{DVA}	Input Data Valid After ECLK	MachXO3D devices, bottom side only	—	0.307	—	0.316	UI
t_{DVE}	Input Data Hold After ECLK		0.662	—	0.650	—	UI
f_{DATA}	DDR71 Serial Input Data Speed		—	420	—	352	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	210	—	176	MHz
f_{CLKIN}	7:1 Input Clock Frequency (SCLK) (minimum limited by PLL)		—	60	—	50	MHz
Generic DDR Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Aligned[8,10]							
t_{DIA}	Output Data Invalid After CLK Output	All MachXO3D devices, all sides	—	0.850	—	0.910	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.850	—	0.910	ns

Parameter	Description	Device	–3		–2		Units
			Min.	Max.	Min.	Max.	
f_{DATA}	DDRX1 Output Data Speed		—	140	—	117	Mbps
f_{DDRX1}	DDRX1 SCLK frequency		—	70	—	58	MHz
Generic DDR Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Centered[8,10]							
t_{DVB}	Output Data Valid Before CLK Output	All MachXO3D devices, all sides	2.720	—	3.380	—	ns
t_{DVA}	Output Data Valid After CLK Output		2.720	—	3.380	—	ns
f_{DATA}	DDRX1 Output Data Speed		—	140	—	117	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency (minimum limited by PLL)		—	70	—	58	MHz
Generic DDRX2 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Aligned[8]							
t_{DIA}	Output Data Invalid After CLK Output	MachXO3D devices, top side only	—	0.270	—	0.300	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.270	—	0.300	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	280	—	224	Mbps
f_{DDRX2}	DDRX2 ECLK frequency		—	140	—	112	MHz
f_{SCLK}	SCLK Frequency		—	70	—	56	MHz
Generic DDRX2 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Centered[8,9]							
t_{DVB}	Output Data Valid Before CLK Output	MachXO3D devices, top side only	1.445	—	1.760	—	ns
t_{DVA}	Output Data Valid After CLK Output		1.445	—	1.760	—	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	280	—	224	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency (minimum limited by PLL)		—	140	—	112	MHz
f_{SCLK}	SCLK Frequency		—	70	—	56	MHz
Generic DDRX4 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Aligned[8,9]							
t_{DIA}	Output Data Invalid After CLK Output	MachXO3D devices, top side only	—	0.270	—	0.300	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.270	—	0.300	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	420	—	350	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	210	—	175	MHz
f_{SCLK}	SCLK Frequency		—	53	—	44	MHz
Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered[8,9]							
t_{DVB}	Output Data Valid Before CLK Output	MachXO3D devices, top side only	0.873	—	1.067	—	ns
t_{DVA}	Output Data Valid After CLK Output		0.873	—	1.067	—	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	420	—	350	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency (minimum limited by PLL)		—	210	—	175	MHz
f_{SCLK}	SCLK Frequency		—	53	—	44	MHz
7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1[8,9]							

Parameter	Description	Device	–3		–2		Units
			Min.	Max.	Min.	Max.	
t_{DIB}	Output Data Invalid Before CLK Output	MachXO3D devices, top side only	—	0.240	—	0.270	ns
t_{DIA}	Output Data Invalid After CLK Output		—	0.240	—	0.270	ns
f_{DATA}	DDR71 Serial Output Data Speed		—	420	—	350	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	210	—	175	MHz
f_{CLKOUT}	7:1 Output Clock Frequency (SCLK) (minimum limited by PLL)		—	60	—	50	MHz

Notes:

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0pf load, fast slew rate.
3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
4. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
5. For Generic DDRX1 mode tSU = tHO = (tDVE - tDVA - 0.03 ns)/2.
6. The tSU_DEL and tH_DEL values use the SCLK_ZERHOLD default step size.
7. This number for general purpose usage. Duty cycle tolerance is +/–10%.
8. Duty cycle is +/– 5% for system usage.
9. Performance is calculated with 0.225 UI.
10. GDDRX1 is not recommended to mix top banks with other banks in applications. Or, the related clock skew is increased significantly.

3.19. sysCLOCK PLL Timing

Over Recommended Operating Conditions.

Table 3.23. sysCLOCK PLL Timing

Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)	—	7	400	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS, CLKOS2)	—	1.5625	400	MHz
f_{OUT2}	Output Frequency (CLKOS3 cascaded from CLKOS2)	—	0.0122	400	MHz
f_{VCO}	PLL VCO Frequency	—	200	800	MHz
f_{PFD}	Phase Detector Input Frequency	—	7	400	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	Without duty trim selected[3]	40	60	%
t_{DT_TRIM}[7]	Edge Duty Trim Accuracy	—	–75	75	%
t_{PH}[4]	Output Phase Accuracy	—	–6	6	%
t_{OPJIT}[1,8]	Output Clock Period Jitter	f_{OUT} > 100 MHz	—	210	ps p-p
		f_{OUT} < 100 MHz	—	0.008	UIPP
	Output Clock Cycle-to-cycle Jitter	f_{OUT} > 100 MHz	—	390	ps p-p
		f_{OUT} < 100 MHz	—	0.01	UIPP
	Output Clock Phase Jitter	f_{PFD} > 100 MHz	—	160	ps p-p
		f_{PFD} < 100 MHz	—	0.011	UIPP
	Output Clock Period Jitter (Fractional-N)	f_{OUT} > 100 MHz	—	270	ps p-p
		f_{OUT} < 100 MHz	—	0.38	UIPP
	Output Clock Cycle-to-cycle Jitter (Fractional-N)	f_{OUT} > 100 MHz	—	320	ps p-p
		f_{OUT} < 100 MHz	—	0.44	UIPP
t_{SPO}	Static Phase Offset	Divider ratio = integer	–120	120	ps
t_W	Output Clock Pulse Width	At 90% or 10%[3]	0.9	—	ns
t_{LOCK}[2,5]	PLL Lock-in Time	—	—	15	ms
t_{UNLOCK}	PLL Unlock Time	—	—	50	ns
t_{IPJIT}[6]	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1,000	ps p-p
		f_{PFD} < 20 MHz	—	0.02	UIPP
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t_{STABLE}[5]	STANDBY High to PLL Stable	—	—	15	ms
t_{RST}	RST/RESETM Pulse Width	—	1	—	ns
t_{RSTREC}	RST Recovery Time	—	1	—	ns
t_{RST_DIV}	RESETC/D Pulse Width	—	10	—	ns
t_{RSTREC_DIV}	RESETC/D Recovery Time	—	1	—	ns
$t_{ROTATE-SETUP}$	PHASESTEP Setup Time	—	10	—	ns
t_{ROTATE_WD}	PHASESTEP Pulse Width	—	4	—	VCO Cycles

Notes:

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after tLOCK for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. CLKOS as compared to CLKOP output for one phase step at the maximum VCO frequency. See MachXO3D sysCLOCK PLL Design and Usage Guide (FPGA-TN-02070) for more details.

5. At minimum fPFD. As the fPFD increases, the time decreases to approximately 60% the value listed.
6. Maximum allowed jitter on an input clock. PLL unlock may occur if the input jitter exceeds this specification. Jitter on the input clock may be transferred to the output clocks, resulting in jitter measurements outside the output specifications listed in this table.
7. Edge Duty Trim Accuracy is a percentage of the setting value. Settings available are 70 ps, 140 ps, and 280 ps in addition to the default value of none.
8. Jitter values measured with the internal oscillator operating. The jitter values increase with loading of the PLD fabric and in the presence of SSO noise.

3.20. Flash Download Time

Table 3.24. Flash Download Time

Symbol	Parameter	Device	Typ.	Units
$t_{REFRESH}$	POR to Device I/O Active	MACHXO3D-4300	—	ms
		MACHXO3D-9400	5.2	ms

Notes:
- Assumes sysMEM EBR initialized to an all zero pattern if they are used.
- The NVCM/Flash download time is measured starting from the maximum voltage of POR trip point.
- The worst case can be up to 1.75 times the Typ value.

3.21. JTAG Port Timing Specifications

Table 3.25. JTAG Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	TCK clock frequency	—	25	MHz
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	10	—	ns
t_{BTH}	TCK [BSCAN] hold time	10	—	ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	11	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	11	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	20	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

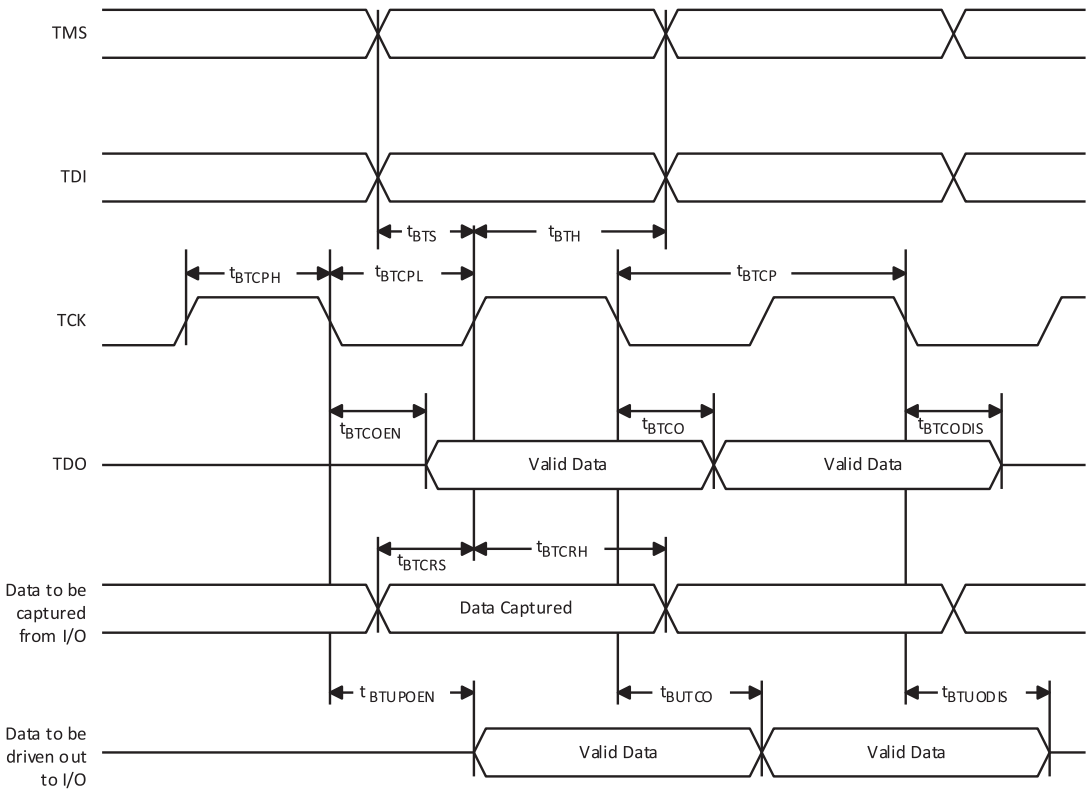


Figure 3.8. JTAG Port Timing Waveforms

3.22. sysCONFIG Port Timing Specifications

Table 3.26. sysCONFIG Port Timing Specifications

Symbol	Parameter		Min.	Max.	Units
All Configuration Modes					
t_{PRGM}	PROGRAMN low pulse accept		99	—	ns
t_{PRGMJ}	PROGRAMN low pulse rejection		—	69	ns
t_{INITL}	INITN low time	MACHXO3D-4300	—	—	us
		MACHXO3D-9400	—	175	us
$t_{DPPINIT}$	PROGRAMN low to INITN low		—	150	ns
$t_{DPPDONE}$	PROGRAMN low to DONE low		—	165	ns
t_{IODISS}	PROGRAMN low to I/O disable		—	185	ns
Slave SPI					
f_{MAX}	CCLK clock frequency		—	66	MHz
t_{CCLKH}	CCLK clock pulse width high		7.5	—	ns
t_{CCLKL}	CCLK clock pulse width low		7.5	—	ns
t_{STSU}	CCLK setup time		2	—	ns
t_{STH}	CCLK hold time		0	—	ns
t_{STCO}	CCLK falling edge to valid output		—	14	ns
t_{STOZ}	CCLK falling edge to valid disable		—	12	ns
t_{STOV}	CCLK falling edge to valid enable		—	14	ns
t_{SCS}	Chip select high time		25	—	ns
t_{SCSS}	Chip select setup time		3	—	ns
t_{SCSH}	Chip select hold time		3	—	ns
Master SPI					
f_{MAX}	MCLK clock frequency		—	66	MHz
t_{MCLKH}	MCLK clock pulse width high		7.5	—	ns
t_{MCLKL}	MCLK clock pulse width low		7.5	—	ns
t_{STSU}	MCLK setup time		6	—	ns
t_{STH}	MCLK hold time		2	—	ns
t_{CSSPI}	INITN high to chip select low		100	200	ns
t_{MCLK}	INITN high to first MCLK edge		0.75	1	us

3.23. I²C Port Timing Specifications

Table 3.27. I²C Port Timing Specification[1,2]

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	Maximum SCL clock frequency	—	400	kHz

Notes:

1. MachXO3D device supports the following modes:
   - Standard-mode (Sm), with a bit rate up to 100 kb/s (user and configuration mode)
   - Fast-mode (Fm), with a bit rate up to 400 kb/s (user and configuration mode)
2. Refer to the I²C specification for timing requirements.

3.24. SPI Port Timing Specifications

Table 3.28. SPI Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	Maximum SCK clock frequency	—	45	MHz

Note: Applies to user mode only. For configuration mode timing specifications, refer to sysCONFIG Port Timing Specifications table in this data sheet.

3.25. Switching Test Conditions

Figure 3.9 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3.29.

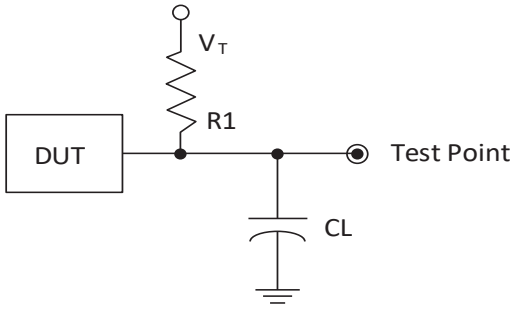


Figure 3.9. Output Test Load, LVTTL and LVCMOS Standards

Table 3.29. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R1	CL	Timing Ref.	VT
LVTTL and LVCMOS settings (L -> H, H -> L)	∞	0 pF	LVTTL, LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
			LVCMOS 1.5 = $V_{CCIO}/2$	—
			LVCMOS 1.2 = $V_{CCIO}/2$	—
LVTTL and LVCMOS 3.3 (Z -> H)	188	0 pF	1.5	V_{OL}
LVTTL and LVCMOS 3.3 (Z -> L)			1.5	V_{OH}
Other LVCMOS (Z -> H)			$V_{CCIO}/2$	V_{OL}
Other LVCMOS (Z -> L)			$V_{CCIO}/2$	V_{OH}
LVTTL + LVCMOS (H -> Z)			$V_{OH} - 0.15$	V_{OL}
LVTTL + LVCMOS (L -> Z)			$V_{OL} - 0.15$	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

4. Signal Descriptions

Table 4.1. Signal Descriptions

Signal Name	I/O	Descriptions
General Purpose		
P[Edge] [Row/Column Number]_[A/B/C/D]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PFU row or the column of the device on which the PIO Group exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B/C/D] indicates the PIO within the group to which the pad is connected. Some of these user-programmable pins are shared with special function pins. When not used as special function pins, these pins can be programmed as I/O for user logic. During configuration of the user-programmable I/O, you have an option to tri-state the I/O and enable an internal pull-up, pull-down or buskeeper resistor. This option also applies to unused pins (or those not bonded to a package pin). The default during configuration is for user-programmable I/O to be tri-stated with an internal pull-down resistor enabled. When the device is erased, I/O is tri-stated with an internal pull-down resistor enabled. Some pins, such as PROGRAMN and JTAG pins, default to tri-stated I/O with pull-up resistors enabled when the device is erased.
NC	—	No connect.
GND	—	GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together.
V_{CC}	—	V_{CC} – The power supply pins for core logic. Dedicated pins. It is recommended that all V_{CC}s are tied to the same supply.
V_{CCIO}x	—	V_{CCIO} – The power supply pins for I/O Bank x. Dedicated pins. It is recommended that all V_{CCIO}s located in the same bank are tied to the same supply.
PLL and Clock Functions (Used as user-programmable I/O pins when not used for PLL or clock pins)		
[LOC]_GPLL[T, C]_IN	—	Reference Clock (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
[LOC]_GPLL[T, C]_FB	—	Optional Feedback (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
PCLK [n]_[2:0]	—	Primary Clock pads. One to three clock pads per side.
Test and Programming (Dual function pins used for test access port and during sysCONFIG™)		
TMS	I	Test Mode Select input pin, used to control the 1149.1 state machine.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine.
TDI	I	Test Data input pin, used to load data into the device using an 1149.1 state machine.
TDO	O	Output pin – Test Data output pin used to shift data out of the device using 1149.1.
JTAGENB	I	Optionally controls behavior of TDI, TDO, TMS, TCK. If the device is configured to use the JTAG pins (TDI, TDO, TMS, TCK) as general purpose I/O, then: If JTAGENB is low: TDI, TDO, TMS and TCK can function a general purpose I/O. If JTAGENB is high: TDI, TDO, TMS and TCK function as JTAG pins.
Configuration (Dual function pins used during sysCONFIG)		
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the start-up sequence is in progress.
MCLK/CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA in SPI and SPIm configuration modes.
SN	I	Slave SPI active low chip select input.
CSSPIN	I/O	Master SPI active low chip select output.
SI/SPISI	I/O	Slave SPI serial data input and master SPI serial data output.
SO/SPISO	I/O	Slave SPI serial data output and master SPI serial data input.

Signal Name	I/O	Descriptions
SCL	I/O	Slave I^2C clock input and master I^2C clock output.
SDA	I/O	Slave I^2C data input and master I^2C data output.

4.1. Pin Information Summary

Table 4.1. MachXO3D-4300

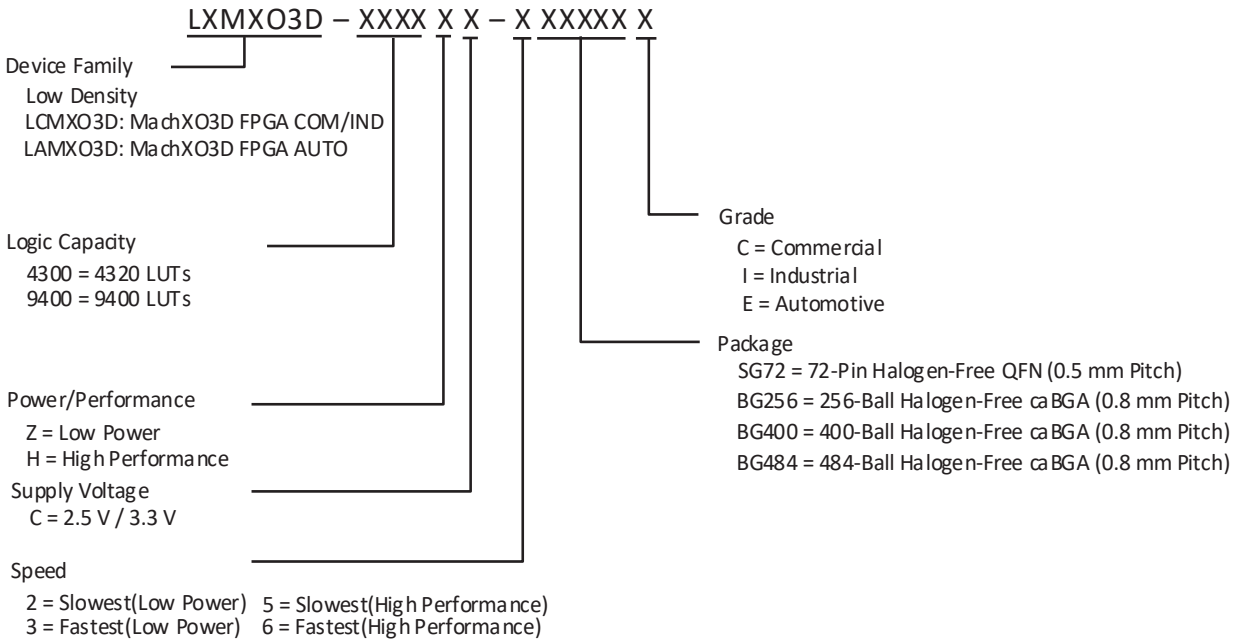
	MachXO3D-4300	
	QFN72	CABGA256
General Purpose I/O per Bank		
Bank 0	19	50
Bank 1	13	52
Bank 2	17	52
Bank 3	9	16
Bank 4	0	16
Bank 5	0	20
Total General Purpose Single Ended I/O	58	206
Differential I/O per Bank		
Bank 0	10	25
Bank 1	5	26
Bank 2	8	26
Bank 3	4	8
Bank 4	0	8
Bank 5	0	10
Total General Purpose Differential I/O	27	103
Dual Function I/O	33	33
Number 7:1 or 8:1 Gearboxes		
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	5	14
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	9	14
High-speed Differential Outputs		
Bank 0	5	14
VCCIO Pins		
Bank 0	3	4
Bank 1	3	4
Bank 2	3	4
Bank 3	1	1
Bank 4	0	2
Bank 5	0	1
VCC	3	8
GND	0 (ePAD)	24
NC	0	1
Reserved for Configuration	1	1
Total Count of Bonded Pins	72	256

Table 4.2. MachXO3D-9400

	MachXO3D-9400			
	QFN72	**CABGA256**	**CABGA400**	**CABGA484**
General Purpose I/O per Bank				
Bank 0	19	50	83	95
Bank 1	13	52	84	96
Bank 2	17	52	84	96
Bank 3	9	16	28	36
Bank 4	0	16	24	24
Bank 5	0	20	32	36
Total General Purpose Single Ended I/O	58	206	335	383
Differential I/O per Bank				
Bank 0	10	25	42	48
Bank 1	5	26	42	48
Bank 2	8	26	42	48
Bank 3	4	8	14	18
Bank 4	0	8	12	12
Bank 5	0	10	16	18
Total General Purpose Differential I/O	27	103	168	192
Dual Function I/O	33	37	37	45
Number 7:1 or 8:1 Gearboxes				
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	5	20	22	24
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	9	20	22	24
High-speed Differential Outputs				
Bank 0	5	20	21	24
V_{CCIO} Pins				
Bank 0	3	4	5	9
Bank 1	3	4	5	9
Bank 2	3	4	5	9
Bank 3	1	1	2	3
Bank 4	0	2	2	3
Bank 5	0	1	2	3
VCC	3	8	10	12
GND	0 (ePAD)	24	33	52
NC	0	1	0	0
Reserved for Configuration	1	1	1	1
Total Count of Bonded Pins	72	256	400	484

5. Ordering Information

5.1. MachXO3D Part Number Description



5.2. Ordering Information

MachXO3D devices have top-side markings as shown in the examples below, on the 484-Ball caBGA package with MachXO3D-9400 device in Commercial Temperature in Speed Grade 5.

Figure 5.1. Top Marking Diagram

Note: Markings are abbreviated for small packages.

5.3. MachXO3D Low Power Commercial, Industrial and Automotive Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3D-4300HC-5SG72C	4300	2.5 V / 3.3 V	5	Halogen-Free QFN	72	COM
LCMXO3D-4300HC-6SG72C	4300	2.5 V / 3.3 V	6	Halogen-Free QFN	72	COM
LCMXO3D-4300HC-5SG72I	4300	2.5 V / 3.3 V	5	Halogen-Free QFN	72	IND
LCMXO3D-4300HC-6SG72I	4300	2.5 V / 3.3 V	6	Halogen-Free QFN	72	IND
LCMXO3D-4300HC-5BG256C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3D-4300HC-6BG256C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3D-4300HC-5BG256I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3D-4300HC-6BG256I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3D-4300ZC-2SG72C	4300	2.5 V / 3.3 V	2	Halogen-Free QFN	72	COM
LCMXO3D-4300ZC-3SG72C	4300	2.5 V / 3.3 V	3	Halogen-Free QFN	72	COM
LCMXO3D-4300ZC-2SG72I	4300	2.5 V / 3.3 V	2	Halogen-Free QFN	72	IND
LCMXO3D-4300ZC-3SG72I	4300	2.5 V / 3.3 V	3	Halogen-Free QFN	72	IND
LCMXO3D-4300ZC-2BG256C	4300	2.5 V / 3.3 V	2	Halogen-Free caBGA	256	COM
LCMXO3D-4300ZC-3BG256C	4300	2.5 V / 3.3 V	3	Halogen-Free caBGA	256	COM
LCMXO3D-4300ZC-2BG256I	4300	2.5 V / 3.3 V	2	Halogen-Free caBGA	256	IND
LCMXO3D-4300ZC-3BG256I	4300	2.5 V / 3.3 V	3	Halogen-Free caBGA	256	IND
LAMXO3D-4300ZC-2SG72E	4300	2.5 V / 3.3 V	2	Halogen-Free QFN	72	AUTO
LAMXO3D-4300ZC-2BG256E	4300	2.5 V / 3.3 V	2	Halogen-Free caBGA	256	AUTO
Part Number	**LUTs**	**Supply Voltage**	**Speed**	**Package**	**Leads**	**Temp.**
LCMXO3D-9400HC-5SG72C	9400	2.5 V / 3.3 V	5	Halogen-Free QFN	72	COM
LCMXO3D-9400HC-6SG72C	9400	2.5 V / 3.3 V	6	Halogen-Free QFN	72	COM
LCMXO3D-9400HC-5SG72I	9400	2.5 V / 3.3 V	5	Halogen-Free QFN	72	IND
LCMXO3D-9400HC-6SG72I	9400	2.5 V / 3.3 V	6	Halogen-Free QFN	72	IND
LCMXO3D-9400HC-5BG256C	9400	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3D-9400HC-6BG256C	9400	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3D-9400HC-5BG256I	9400	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3D-9400HC-6BG256I	9400	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3D-9400HC-5BG400C	9400	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3D-9400HC-6BG400C	9400	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3D-9400HC-5BG400I	9400	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3D-9400HC-6BG400I	9400	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	IND
LCMXO3D-9400HC-5BG484C	9400	2.5 V / 3.3 V	5	Halogen-Free caBGA	484	COM
LCMXO3D-9400HC-6BG484C	9400	2.5 V / 3.3 V	6	Halogen-Free caBGA	484	COM
LCMXO3D-9400HC-5BG484I	9400	2.5 V / 3.3 V	5	Halogen-Free caBGA	484	IND
LCMXO3D-9400HC-6BG484I	9400	2.5 V / 3.3 V	6	Halogen-Free caBGA	484	IND
LCMXO3D-9400ZC-2SG72C	9400	2.5 V / 3.3 V	2	Halogen-Free QFN	72	COM
LCMXO3D-9400ZC-3SG72C	9400	2.5 V / 3.3 V	3	Halogen-Free QFN	72	COM
LCMXO3D-9400ZC-2SG72I	9400	2.5 V / 3.3 V	2	Halogen-Free QFN	72	IND
LCMXO3D-9400ZC-3SG72I	9400	2.5 V / 3.3 V	3	Halogen-Free QFN	72	IND
LCMXO3D-9400ZC-2BG256C	9400	2.5 V / 3.3 V	2	Halogen-Free caBGA	256	COM
LCMXO3D-9400ZC-3BG256C	9400	2.5 V / 3.3 V	3	Halogen-Free caBGA	256	COM
LCMXO3D-9400ZC-2BG256I	9400	2.5 V / 3.3 V	2	Halogen-Free caBGA	256	IND
LCMXO3D-9400ZC-3BG256I	9400	2.5 V / 3.3 V	3	Halogen-Free caBGA	256	IND
LCMXO3D-9400ZC-2BG400C	9400	2.5 V / 3.3 V	2	Halogen-Free caBGA	400	COM
LCMXO3D-9400ZC-3BG400C	9400	2.5 V / 3.3 V	3	Halogen-Free caBGA	400	COM

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3D-9400ZC-2BG400I	9400	2.5 V / 3.3 V	2	Halogen-Free caBGA	400	IND
LCMXO3D-9400ZC-3BG400I	9400	2.5 V / 3.3 V	3	Halogen-Free caBGA	400	IND

References

A variety of technical notes for the MachXO3D family are available on the Lattice web site.

- MachXO3D sysCLOCK PLL Design and Usage Guide (FPGA-TN-02070)
- Implementing High-Speed Interfaces with MachXO3D Devices Usage Guide (FPGA-TN-02065)
- MachXO3D sysI/O Usage Guide (FPGA-TN-02068)
- MachXO3D Programming and Configuration Usage Guide (FPGA-TN-02069)
- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- Minimizing System Interruption During Configuration Using TransFR Technology (TN1087)
- Boundary Scan Testability with Lattice sysI/O Capability (AN8066)
- Thermal Management document (FPGA-TN-02044)
- Lattice Design Tools

Revision History

Revision 1.0, November 2019

Section	Change Summary
All	Production release.

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