

User's Guide

Using the UCC27624EVM



ABSTRACT

This user's guide describes the characteristics, operation, and use of the UCC27624EVM Evaluation Module (EVM). A complete schematic diagram, PCB layouts, and BOM are included in this document.

Table of Contents

1 Introduction.....	2
2 Description.....	2
2.1 Features.....	2
2.2 I/O Description.....	3
3 Electrical Specifications.....	3
4 Test Summary.....	4
4.1 Definitions.....	4
4.2 Equipment.....	4
4.3 Equipment Setup.....	4
5 Power Up and Power Down Procedure.....	6
5.1 Power Up.....	6
5.2 Power Down.....	6
6 Typical Performance Waveforms ($C_L = 1800 \text{ pF}$).....	7
6.1 Propagation Delays.....	7
7 Schematic.....	8
8 Layout Diagrams.....	9
9 List of Materials.....	13

List of Figures

Figure 4-1. Bench Setup Diagram and Configuration.....	5
Figure 5-1. Example Input and Output Waveforms.....	6
Figure 6-1. IN+ to OUT Propagation Delay Waveforms	7
Figure 7-1. UCC27624EVM Schematic.....	8
Figure 8-1. Top Overlay.....	9
Figure 8-2. Top Layer.....	9
Figure 8-3. Bottom Layer.....	10
Figure 8-4. Bottom Overlay.....	10
Figure 8-5. Top Image.....	11
Figure 8-6. Bottom Image.....	12

List of Tables

Table 2-1. Connection Descriptions.....	3
Table 4-1. Two-Channel Function Generator Settings.....	4
Table 4-2. Oscilloscope Settings.....	5
Table 9-1. UCC27624EVM List of Materials.....	13

Trademarks

All trademarks are the property of their respective owners.

1 Introduction

The UCC27624EVM is designed to primarily evaluate the UCC27624 performance. The UCC27624 is a 30-V dual channel low-side driver with 5-A peak source and 5-A peak sink current for driving Si/IGBTs/SiC and GaN FETs. The UCC27624EVM board can be used to evaluate other pin-to-pin compatible parts in the supported package. The UCC27624 has low propagation delay and low propagation delay matching between the respective channels rising and falling edges of the driver outputs for reliable timing of the gate-drive signals. The UCC27624 inputs can tolerate signals as high as 26 V regardless of the VDD voltage which enhances device robustness.

The UCC27624 driver includes EN pins which enable the driver's outputs when pulled high, and disables the driver into a low standby current mode when low.

2 Description

The UCC27624EVM is designed to primarily evaluate the UCC27624 functionality. The driver's performances can be evaluated for capacitive loads and/or power devices with provisions for TO-220 footprints. The UCC27624EVM evaluation boards use surface-mount test points allowing connections to INA, INB, ENA, ENB, VDD, OUTA and OUTB UCC27624. For detailed device information, see the *UCC27624 Datasheet UCC27624 30-V, 5-A dual channel low-side driver Data Sheet*.

2.1 Features

The EVM supports the following features:

- EVM for the low-voltage features of the UCC27624 gate driver
- 4.5-V to 26-V VCC power supply range
- 5-A source, 5-A sink current
- -10V input voltage capability
- TTL-compatible inputs
- PCB layout optimized for bias supply bypassing cap, gate-drive resistance selection
- Capacitive load, external gate drive resistor and TO-220 footprint for N-ch MOSFETs gate drive network evaluation
- Ability to parallel both OUTA and OUTB channels for higher pulsed output current
- Allows quick verification of most of the data sheet parameters
- Test points allow probing all the key pins of the UCC27624

2.2 I/O Description

Table 2-1 details the connection descriptions.

Table 2-1. Connection Descriptions

Pins	Description
VCC	V_{CC} positive input test point. Powers IC VDD pin, use 4.5-V to 26-V range.
VDD	V_{DD} positive input of UCC27624 IC
GND	Multiple test points. VCC negative input, HI_IN, LI_IN, and ENA_IN negative inputs, and ground at UCC27624 IC
INA_IN+	Channel-A PWM signal
INB_IN-	Channel-B PWM signal
INA	INA input pin
INB	INB input pin.
ENA_IN	Enable A input. Connect to GND to disable ch-A
ENB_IN	Enable B input. Connect to GND to disable ch-B
Gate_A	OUTA output at capacitive load and gate
Gate_B	OUTB output at capacitive load and gate
OUTA	OUTA output at driver's pin of UCC27624
OUTB	OUTB output at driver's pin of UCC27624

3 Electrical Specifications

For the full range of recommended operating specifications and design guidelines for driving loads, see the *UCC27624 Datasheet UCC27624 30-V, 5-A dual channel low-side driver Data Sheet*.

CAUTION

The UCC27624EVM is designed for low-voltage evaluation only, and is not certified for evaluation with voltages beyond the absolute maximums listed in the electrical specifications. Do **not** evaluate high-voltage parameters with this board.

4 Test Summary

4.1 Definitions

This procedure details how to configure the UCC27624EVM evaluation board. Within this test procedure, the following naming conventions are applied. See the *UCC27624EVM Bench Setup Diagram and Configuration, Figure 4-1*, for details.

DMM: Digital multimeter

EVM: Evaluation module

4.2 Equipment

4.2.1 Power Supply

DC power supply with voltage and current above 26-V and 1-A, for example: Agilent E3634A

4.2.2 Function Generator

Two-channel function generator over 10 MHz, for example: Tektronics AFG3252

4.2.3 DMM

DMM with voltage and current above 26 V and 1 A, for example: Fluke 187

4.2.4 Oscilloscope

Four channel oscilloscope with 500 MHz or greater bandwidth, for example: DPO 7054

4.3 Equipment Setup

4.3.1 DC Power Supply Settings

- DC power supply #1
 - Voltage setting: 12 V
 - Current limit: 0.05 A

4.3.2 Digital Multi-Meter Settings

- DMM #1
 - DC current measurement, auto-range. Expected current is within 1 mA to 15 mA.

4.3.3 Two-Channel Function Generator Settings

Table 4-1 displays the two-channel function generator settings.

Table 4-1. Two-Channel Function Generator Settings

	Mode	Frequency	Width	Delay	High	Low	Output Impedance
Channel A	Pulse	100 kHz	5 µs	0 us	5 V	0 V	High Z
Channel B			5 µs	5 µs			

4.3.4 Oscilloscope Settings

Table 4-2 details the oscilloscope settings.

Table 4-2. Oscilloscope Settings

	Bandwidth	Coupling	Termination	Scale Settings	Inverting
Channel A	500 MHz or above	DC	1 MΩ or automatic	10 × or automatic	OFF
Channel B					

4.3.5 Bench Setup Diagram

The bench setup diagram includes the function generator and oscilloscope connections.

Use the following connection procedure, refer to [Figure 4-1](#).

- Make sure all the output of the function generator, voltage source are disabled before connection.
- Function generator Ch-A channel applied on INA_IN+, see in [Figure 4-1](#).
- Function generator Ch-B channel applied on INB_IN-, see in [Figure 4-1](#).
- Power supply #1: positive node connected to input of DMM #1 and DMM #1 output connected to test point marked as VCC, negative node of Power Supply #1 connected directly to test point marked as GND; see in [Figure 4-1](#).
- Connect oscilloscope Ch-1 probes to test points marked as Gate_A, smaller measurement loop is preferred; see in [Figure 4-1](#).
- Connect oscilloscope Ch-2 probes to test points marked as Gate_B, smaller measurement loop is preferred; see in [Figure 4-1](#).

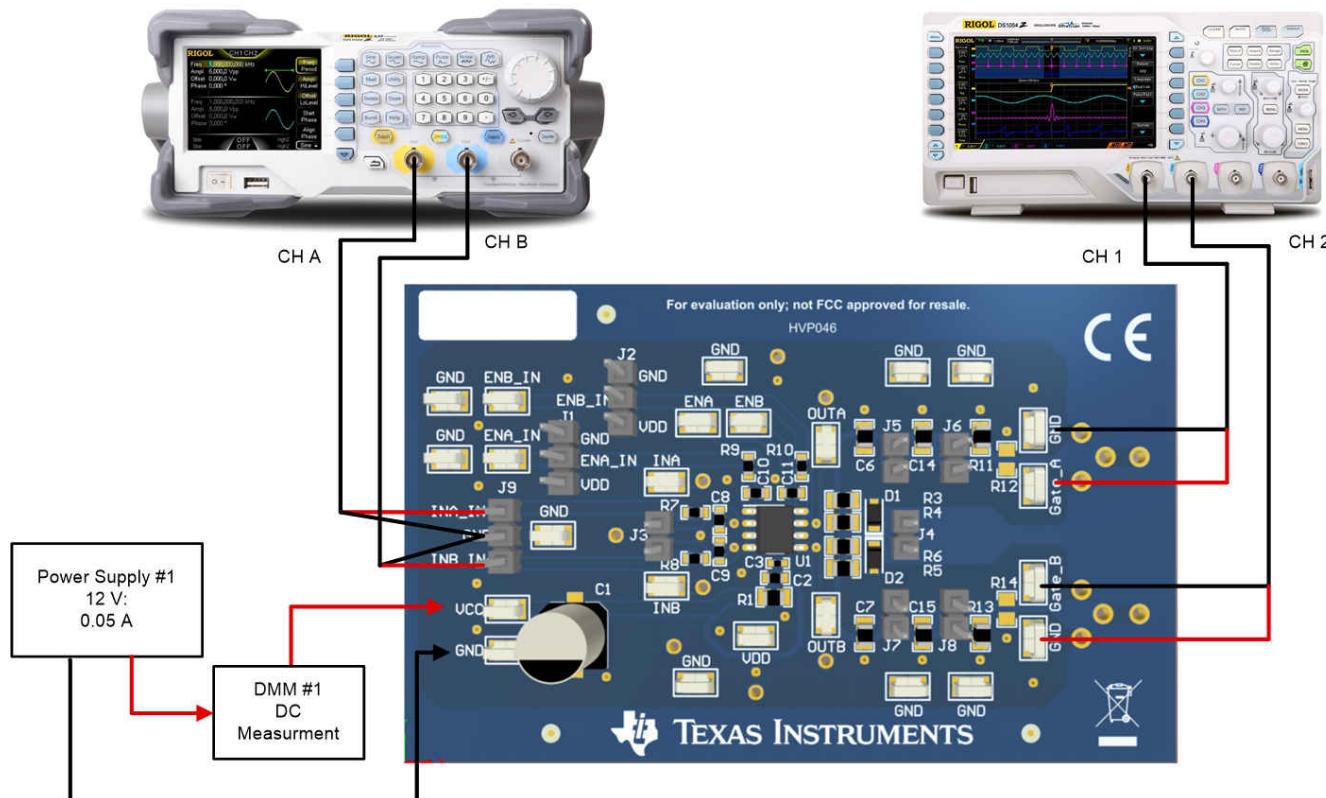


Figure 4-1. Bench Setup Diagram and Configuration

5 Power Up and Power Down Procedure

5.1 Power Up

1. Before beginning the power up test procedure, verify the connections with [Figure 4-1](#).
2. Enable supply #1, if the current on DMM1 is more than 0.25 mA and less than 0.8 mA, everything is set correctly.
3. Enable function generator outputs channel-A and channel-B.
4. The following conditions should be present:
 - a. Stable pulse output on channel-1 and channel-2 in the oscilloscope, refer to
 - b. Frequency measurement should be 100 kHz, ± 5 kHz or equal to the programmed function generator frequency
 - c. DMM #1 should display around 4.6 mA, ± 2 mA with the default load capacitance of 1.0 nF. For more information about operating current, see the [UCC27624 Datasheet UCC27624 30-V 5-A dual channel low-side driver Data Sheet](#).
5. Connect ENA_IN and ENB_IN test points to GND test point with jumpers. The pulse outputs on channel-1 and channel-2 will cease operation and the voltage level should be near ground.

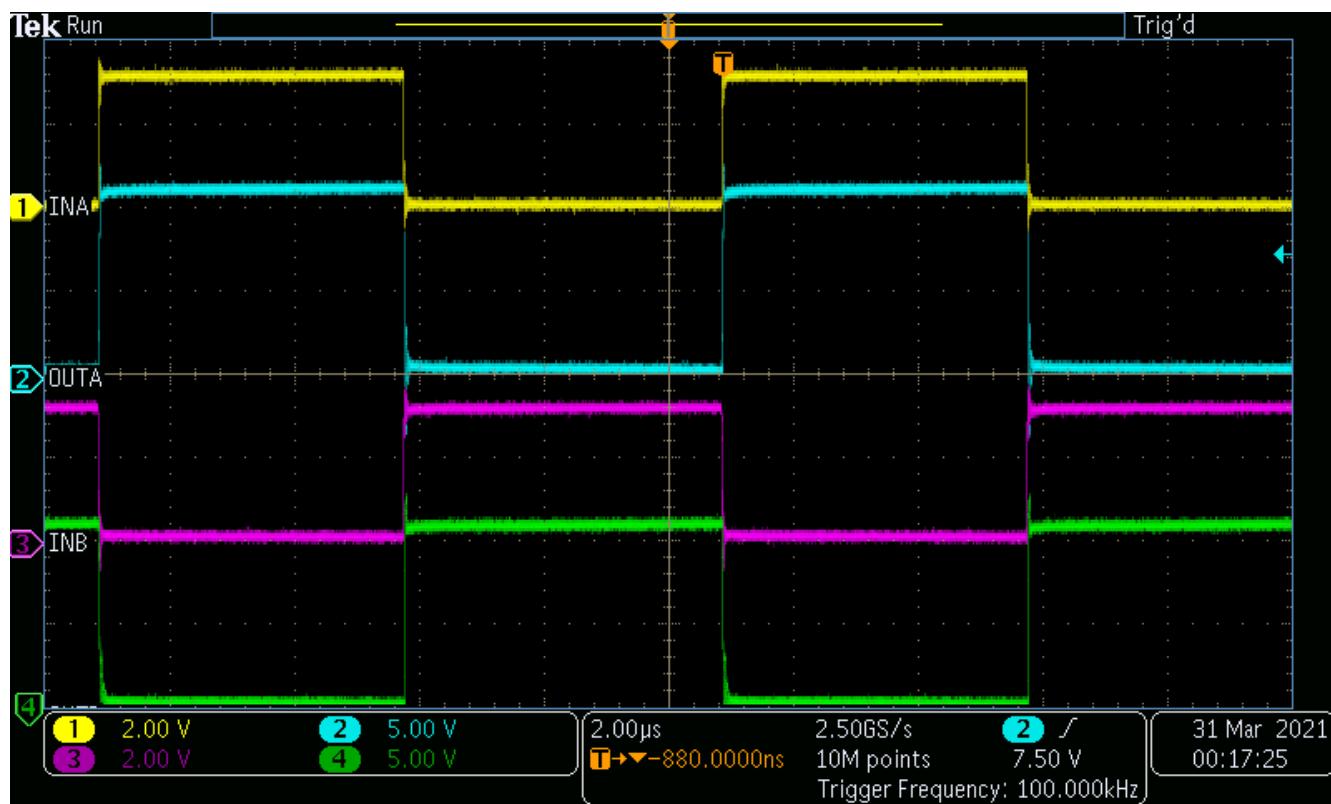


Figure 5-1. Example Input and Output Waveforms

5.2 Power Down

Use the following steps to power down the EVM:

1. Disable function generator
2. Disable power supply #1
3. Disconnect cables and probes

6 Typical Performance Waveforms ($C_L = 1800 \text{ pF}$)

6.1 Propagation Delays

The following waveforms illustrate the INx inputs and OUTx output.

To evaluate propagation delays and rising and falling details, it is recommended to have scope probe connections with short ground leads.

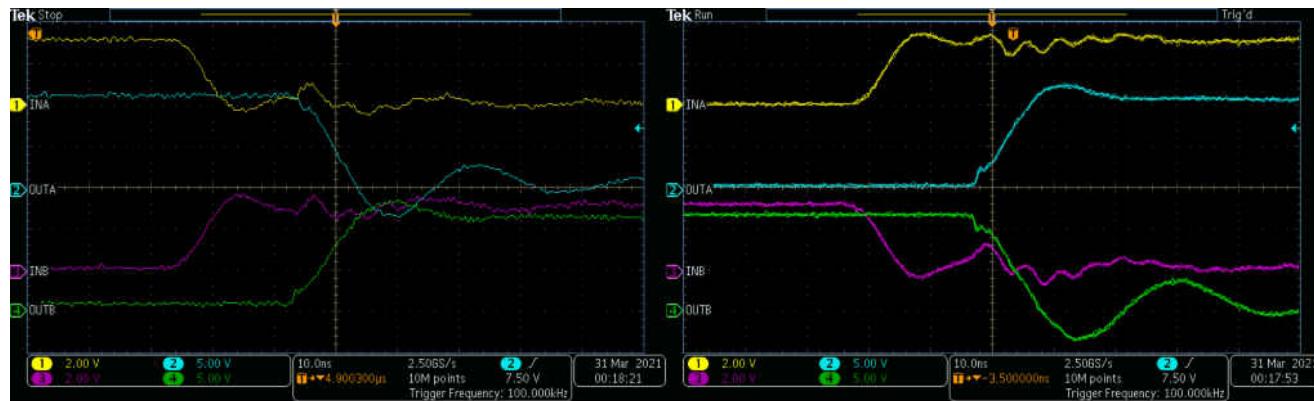


Figure 6-1. IN+ to OUT Propagation Delay Waveforms

7 Schematic

Figure 7-1 shows the UCC27624EVM schematic diagram.

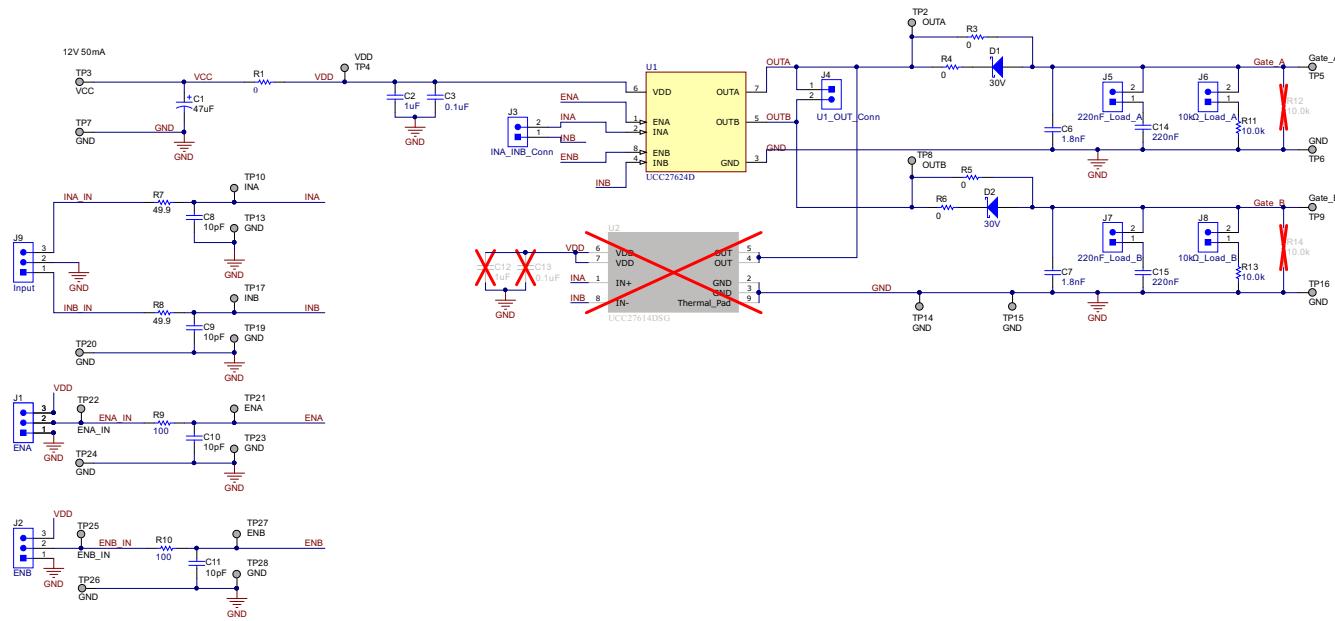


Figure 7-1. UCC27624EVM Schematic

U2 is not installed since it is an alternate driver IC used on a different board assembly variation.

8 Layout Diagrams

Figure 8-1 through Figure 8-6 show the PCB layout information for the UCC27624EVM.

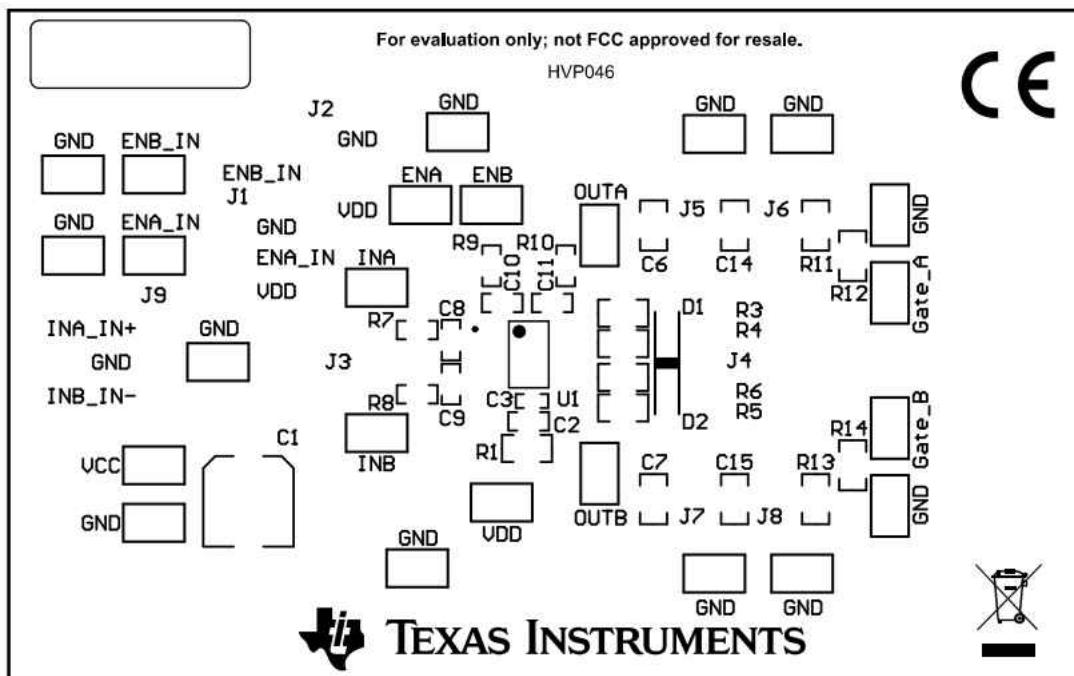


Figure 8-1. Top Overlay

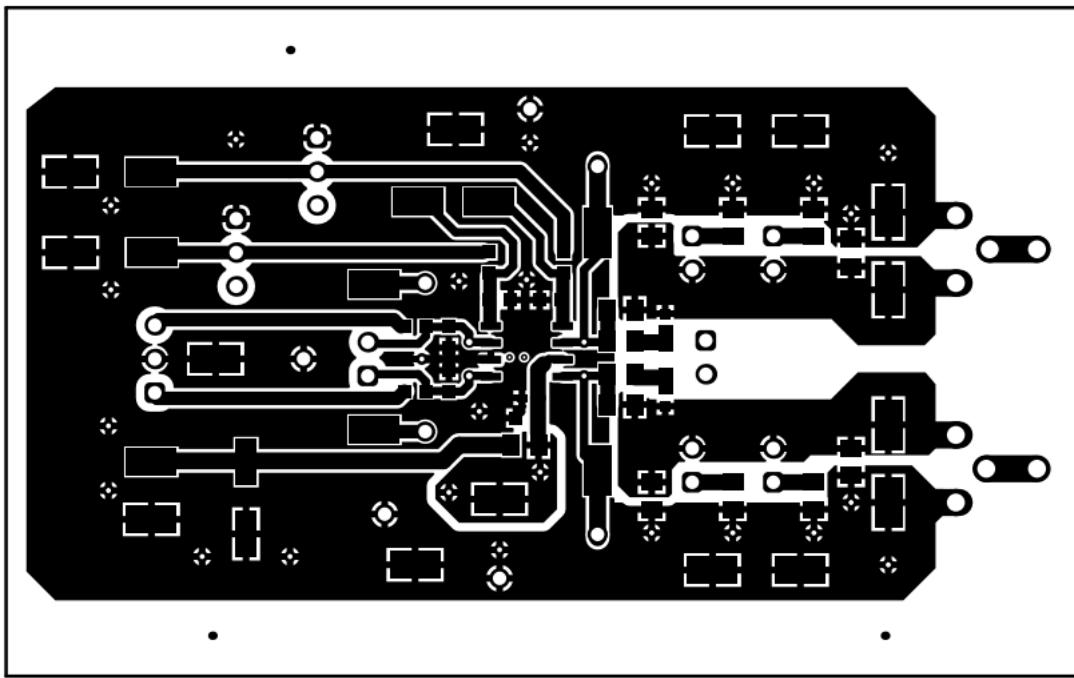


Figure 8-2. Top Layer

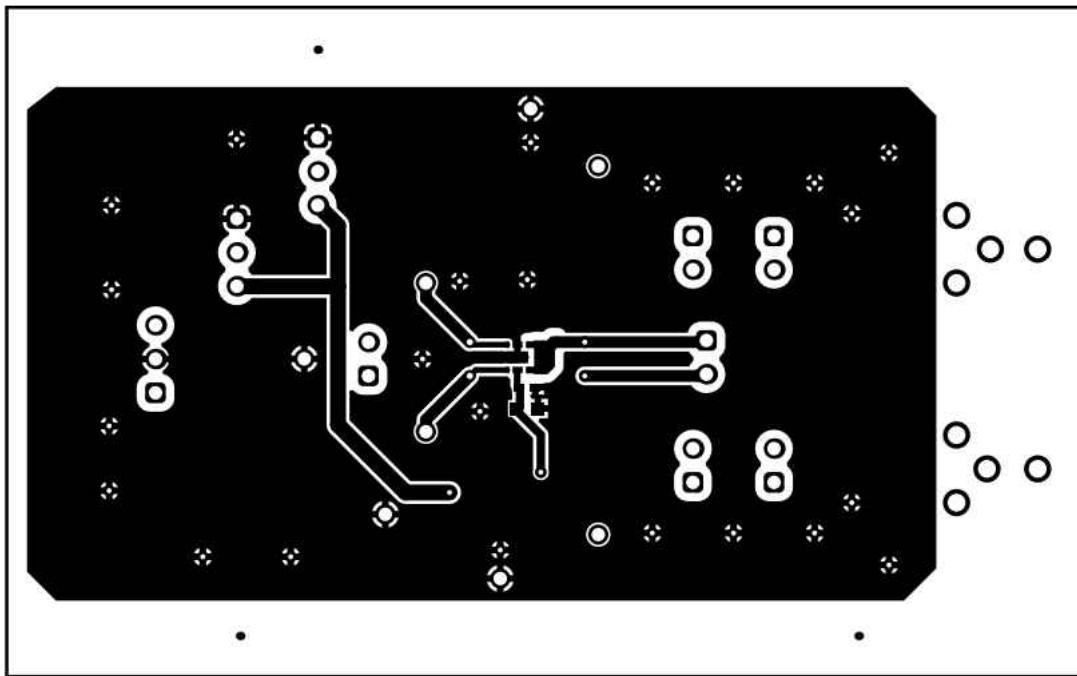


Figure 8-3. Bottom Layer

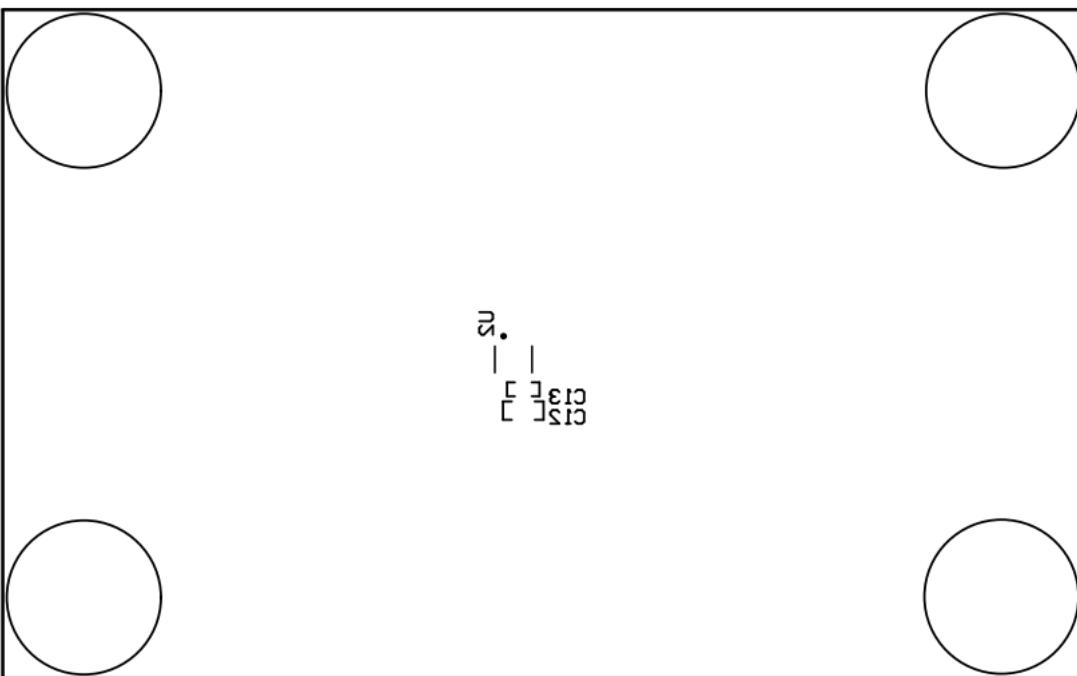


Figure 8-4. Bottom Overlay

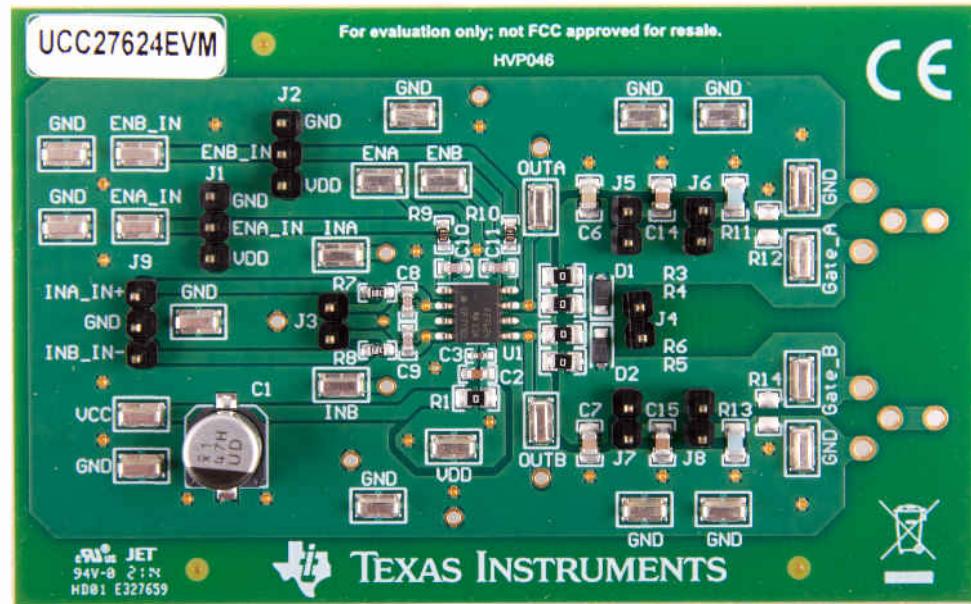


Figure 8-5. Top Image

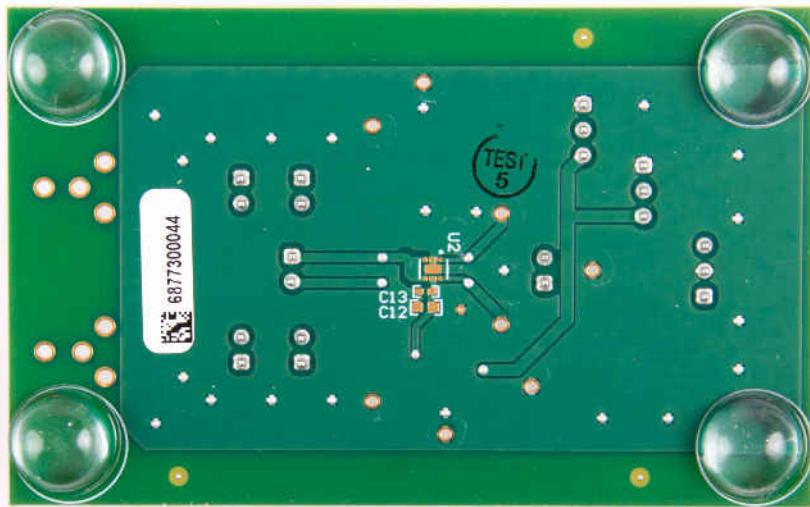


Figure 8-6. Bottom Image

9 List of Materials

Table 9-1. UCC27624EVM List of Materials

QUANTITY	DESCRIPTION	DESCRIPTION
1	C1	CAP, AL, 47 uF, 50 V, +/- 20%, 0.68 ohm, SMD
2	C2, C12	CAP, CERM, 1 uF, 50 V, +/- 10%, X6S, 0603
2	C3, C13	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0402
2	C6, C7	CAP, CERM, 1800 pF, 50 V, +/- 10%, X7R, 0805
4	C8, C9, C10, C11	CAP, CERM, 10 pF, 50 V, +/- 5%, COG/NP0, 0603
2	C14, C15	CAP, CERM, 0.22 uF, 50 V, +/- 10%, X7R, 0805
2	D1, D2	Diode, Schottky, 30 V, 1 A, AEC-Q101, MicroSMP
6	FID1, FID2, FID3, FID4, FID5, FID6	Fiducial mark. There is nothing to buy or mount.
4	H1, H2, H3, H4	Bumpon, Hemisphere, 0.44 X 0.20, Clear
1	J1	Header, 2.54 mm, 3x1, Tin, TH
1	J2	Header, 2.54 mm, 3x1, Tin, TH
1	J3	Header, 2.54 mm, 2x1, Tin, TH
1	J4	Header, 2.54 mm, 2x1, Tin, TH
1	J5	Header, 2.54 mm, 2x1, Tin, TH
1	J6	Header, 2.54 mm, 2x1, Tin, TH
1	J8	Header, 2.54 mm, 2x1, Tin, TH
1	J9	Header, 2.54 mm, 3x1, Tin, TH
1	LBL1	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll
1	R1	RES, 0, 5%, 0.125 W, AEC-Q200 Grade 0, 0805
4	R3, R4, R5, R6	RES, 0, 5%, 0.125 W, 0805
2	R7, R8	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
2	R9, R10	RES, 100, 0.01%, 0.1 W, AEC-Q200 Grade 0, 0603
4	R11, R12, R13, R14	RES, 10.0 k, 1%, 0.2 W, 0805
1	TP2	Test Point, Miniature, SMT
1	TP3	Test Point, Miniature, SMT
1	TP4	Test Point, Miniature, SMT
1	TP5	Test Point, Miniature, SMT
12	TP6, TP7, TP13, TP14, TP15, TP16, TP19, TP20, TP23, TP24, TP26, TP28	Test Point, Miniature, SMT
1	TP8	Test Point, Miniature, SMT
1	TP9	Test Point, Miniature, SMT
1	TP10	Test Point, Miniature, SMT
1	TP17	Test Point, Miniature, SMT
1	TP21	Test Point, Miniature, SMT
1	TP22	Test Point, Miniature, SMT
1	TP25	Test Point, Miniature, SMT
1	TP27	Test Point, Miniature, SMT

Table 9-1. UCC27624EVM List of Materials (continued)

1	U1	UCC27624 Dual, 5A, High-Speed Low-Side Power MOSFET Driver, with Negative Input Voltage Ability, D0008A (SOIC-8)
---	----	--

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated