

## General Description

The Sanrise SRT10N043H is a low voltage power MOSFET, fabricated using advanced split gate trench technology. The resulting device has extremely low on resistance, low gate charge and fast switching time, making it especially suitable for applications which require superior power density and synchronous rectification.

The SRT10N043H break down voltage is 100V and it has a high rugged avalanche characteristics. The SRT10N043H is available in PDFN5\*6 and TO-220C and TO-263-2 packages.

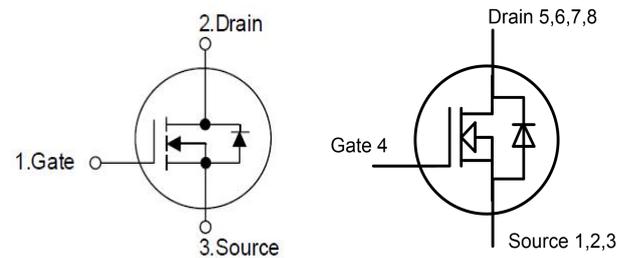
## Features

- Ultra Low  
 $R_{DS(ON\_TYP)} = 3.7m\Omega$ , PDFN5\*6 @ $V_{GS} = 10V$ .  
 $R_{DS(ON\_TYP)} = 4.1m\Omega$ , TO-220C @ $V_{GS} = 10V$ .  
 $R_{DS(ON\_TYP)} = 3.9m\Omega$ , TO-263-2 @ $V_{GS} = 10V$ .
- Ultra Low Gate Charge,  $Q_g = 57nC$  typ.
- Fast switching capability
- Robust design with better EAS performance

## Application

- Server/Telecom
- High Power Supply
- E-Tools
- BMS

## Symbol

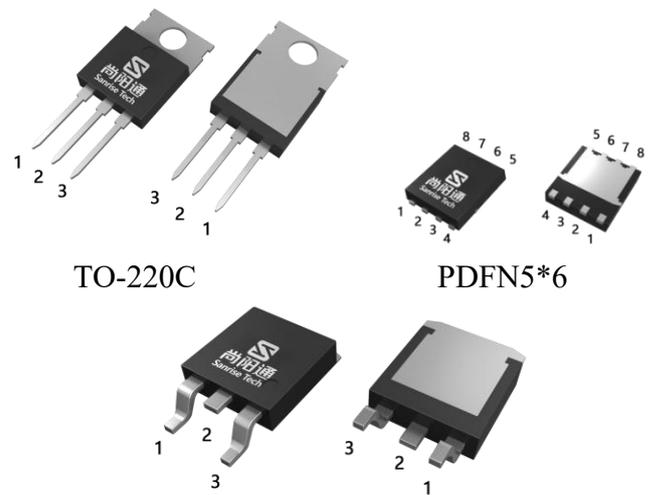


TO-220C, TO-263-2

PDFN5\*6

Figure 1 Symbol of SRT10N043H

## Package Type

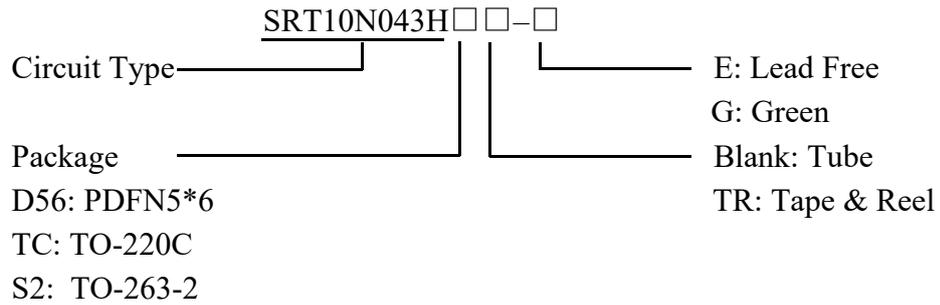


TO-220C

PDFN5\*6

TO-263-2

Figure 2 Package Type of SRT10N043H

**Ordering Information**


Package	Part Number	Marking ID	Packing Type
PDFN5*6	SRT10N043HD56TR-G	SRT10N043HD56G	Tape & Reel
TO-220C	SRT10N043HTC-E	SRT10N043HTCE	Tube
TO-263-2	SRT10N043HS2TR-E	SRT10N043HS2E	Tape & Reel

**Absolute Maximum Ratings**

Parameter		Symbol	Rating	Unit	
Drain-Source Voltage		$V_{DSS}$	100	V	
Gate-Source Voltage		$V_{GSS}$	±20	V	
Continuous Drain Current	$T_C=25^{\circ}\text{C}$	$I_D$	PDFN5*6	125	A
			TO-220C	125	
			TO-263-2	125	
	$T_C=100^{\circ}\text{C}$		PDFN5*6	77	
			TO-220C	79	
			TO-263-2	81	
Pulsed Drain Current (Note 2)		$I_{DM}$	PDFN5*6	500	A
			TO-220C	500	
			TO-263-2	500	
Max Power Dissipation		$P_D$	119	W	
Avalanche Destructive Energy, Single Pulse (Note 4)		$E_{AS\_Limit}$	625	mJ	
Avalanche Energy, Single Pulse (Note 3)		$E_{AS}$	110	mJ	
Avalanche Energy, Repetitive (Note 2)		$E_{AR}$	0.2	mJ	
Avalanche Current, Repetitive (Note 2)		$I_{AR}$	40.0	A	
Continuous Diode Forward Current		$I_S$	100	A	
Diode Pulse Current		$I_{S,PULSE}$	300	A	
Operating Junction Temperature		$T_J$	150	°C	
Storage Temperature		$T_{STG}$	-55 to 150	°C	
Lead Temperature (Soldering, 10 sec)		$T_{LEAD}$	260	°C	

Note:

1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature
3.  $I_{AS}=21.0\text{A}$ ,  $V_{DD}=50\text{V}$ ,  $R_G=25\Omega$ , Starting  $T_J=25^{\circ}\text{C}$
4.  $I_{AS\_Limit}=50\text{A}$ ,  $V_{DD}=50\text{V}$ ,  $R_G=25\Omega$ , Starting  $T_J=25^{\circ}\text{C}$

**Thermal Resistance**

Parameter		Symbol	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	PDFN5*6	$R_{thJC}$			1.05	°C/W
	TO-220C				0.94	
	TO-263-2				0.94	
Thermal Resistance, Junction-to-Ambient	PDFN5*6	$R_{thJA}$			50	
	TO-220C				60	
	TO-263-2				60	

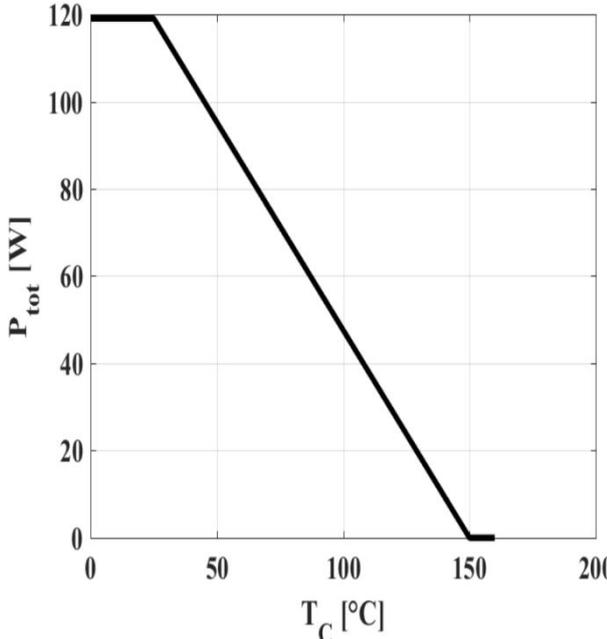
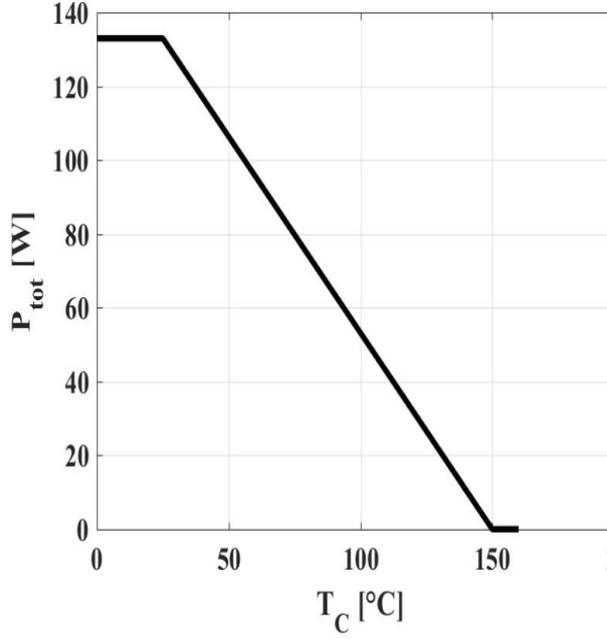
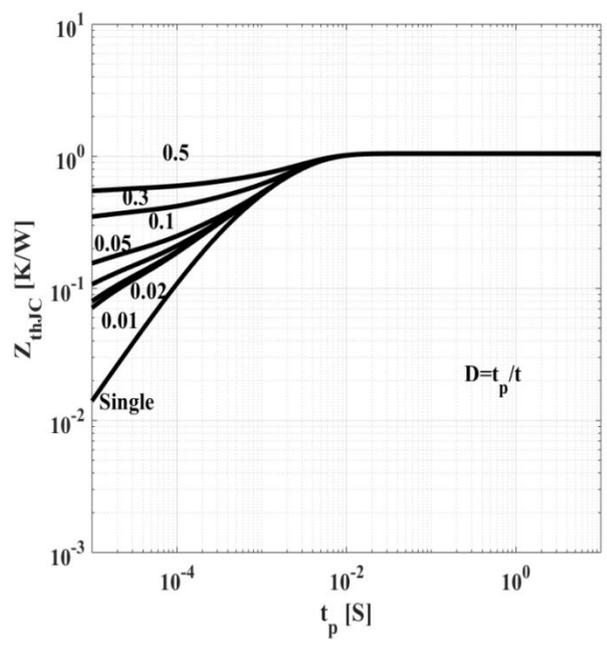
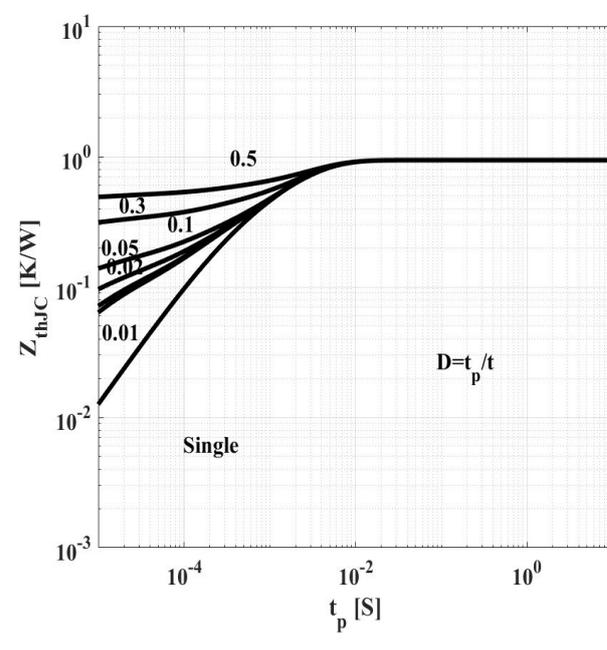
**Electrical Characteristics**
 $T_J = 25^\circ\text{C}$ , unless otherwise specified.

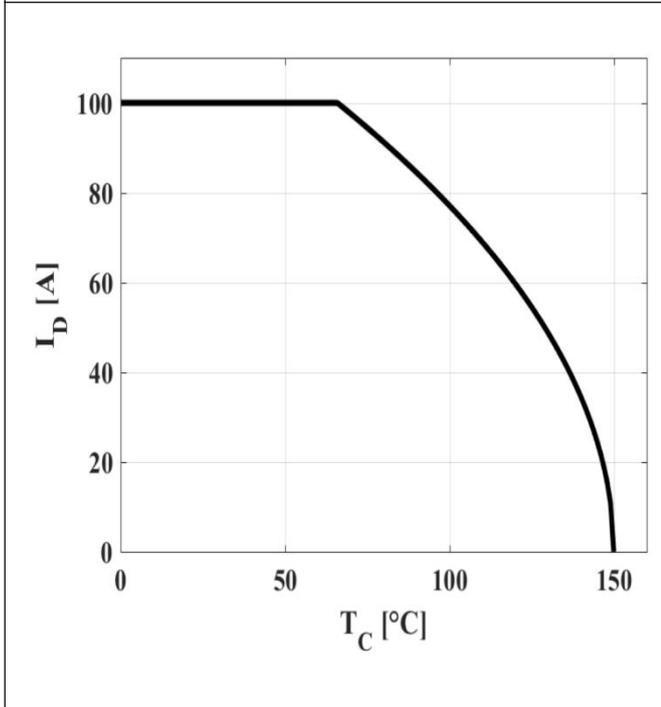
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Statistic Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	100			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=100V, V_{GS}=0V$			1	$\mu A$
Gate-Body Leakage Current	Forward	$I_{GSSF}, V_{GS}=20V, V_{DS}=0V$			100	nA
	Reverse	$I_{GSSR}, V_{GS}=-20V, V_{DS}=0V$			-100	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=0.25mA$	2.0	3.0	4.0	V
Static Drain-Source On-Resistance	PDFN5*6	$R_{DS(ON)}, V_{GS}=10V, I_D=20A$		3.7	4.3	mΩ
	TO-220C			4.1	4.5	
	TO-263-2			3.9	4.3	
Gate Resistance	$R_G$	$f=1MHz, \text{Open Drain}$		1.0		Ω
<b>Dynamic Characteristics</b>						
Input Capacitance	$C_{ISS}$	$V_{DS}=50V, V_{GS}=0V, f=1MHz$		3.9		nF
Output Capacitance	$C_{OSS}$			1.3		nF
Reverse Transfer Capacitance	$C_{RSS}$			24		pF
Effective output capacitance, energy related NOTE5	$C_{O(er)}$	$V_{GS}=0V, V_{DS}=0\dots 60V$		1.7		nF
Effective output capacitance, time related NOTE6	$C_{O(tr)}$			2.1		
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=50V, I_D=20A, R_G=3.0\Omega, V_{GS}=10V$		14		nS
Rise Time	$t_r$			7		
Turn-off Delay Time	$t_{d(off)}$			32		
Fall Time	$t_f$			11		
<b>Gate Charge Characteristics</b>						
Gate to Source Charge	$Q_{gs}$	$V_{DD}=50V, I_D=20A, V_{GS}=0 \text{ to } 10V$		16		nC
Gate to Drain Charge	$Q_{gd}$			11		
Gate Charge Total	$Q_g$			57		
Gate Plateau Voltage	$V_{plateau}$			4.2		V
Gate Charge Total, sync FET	$Q_g$	$V_{DD}=0.1V, V_{GS}=0 \text{ to } 10V$		49		nC
<b>Reverse Diode Characteristics</b>						
Drain-Source Diode Forward Voltage	$V_{SD}$	$V_{GS}=0V, I_{SD}=20A$		0.81	1.0	V
Reverse Recovery Time	$t_{rr}$	$V_R=50V, I_F=20A, dI_F/dt=100A/\mu s$		50		nS
Reverse Recovery Charge	$Q_{rr}$			75		nC
Peak Reverse Recovery Current	$I_{rrm}$			3		A

Note:

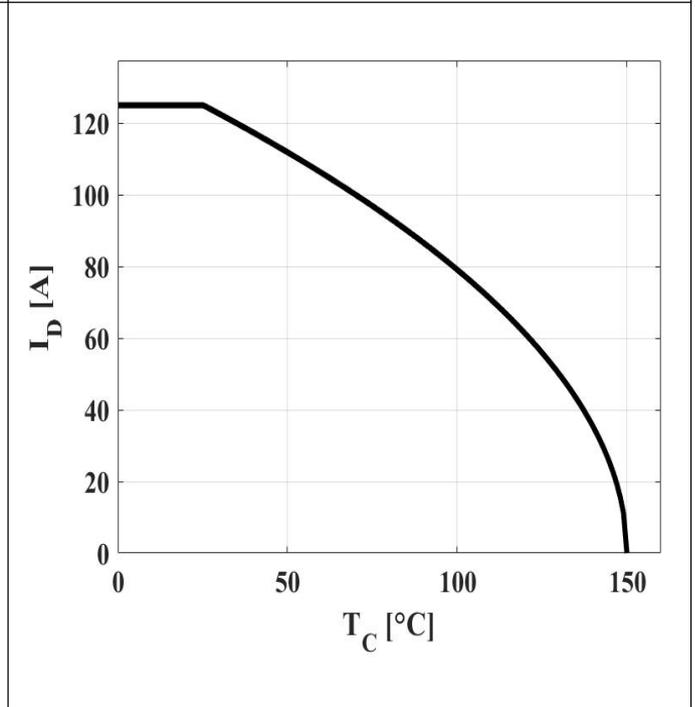
- $C_{O(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 60V
- $C_{O(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 60V

**Typical Performance Characteristics**

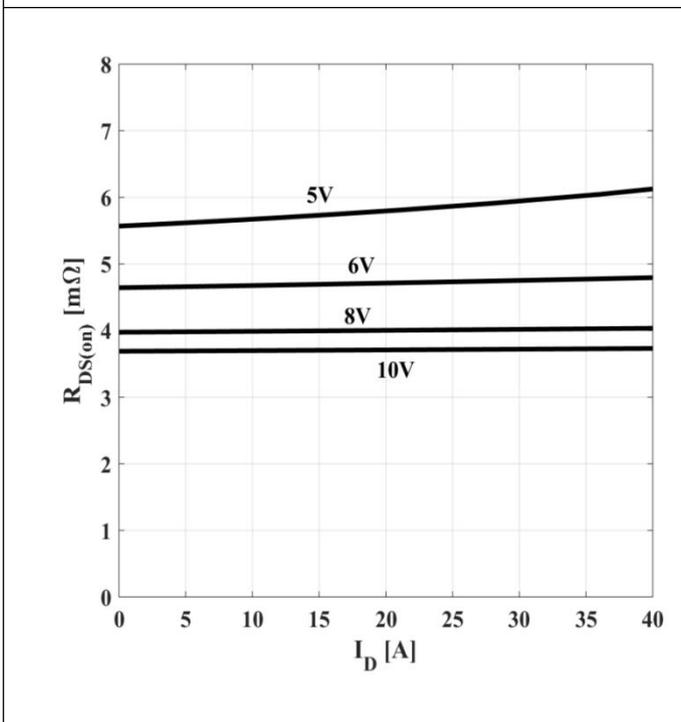
Figure 3A: Power Dissipation (PDFN5*6)	Figure 3B: Power Dissipation (TO-220C&TO-263)
	
$P_{tot}=f(T_c)$	$P_{tot}=f(T_c)$
Figure 4A: Max. Transient Thermal Impedance (PDFN5*6)	Figure 4B: Max. Transient Thermal Impedance (TO-220C&TO-263)
	
$Z_{(th)JC}=f(t_p)$ ;parameter: $D=t_p/T$	$Z_{(th)JC}=f(t_p)$ ;parameter: $D=t_p/T$

**Figure5A: Drain Current**  
 (PDFN5\*6)


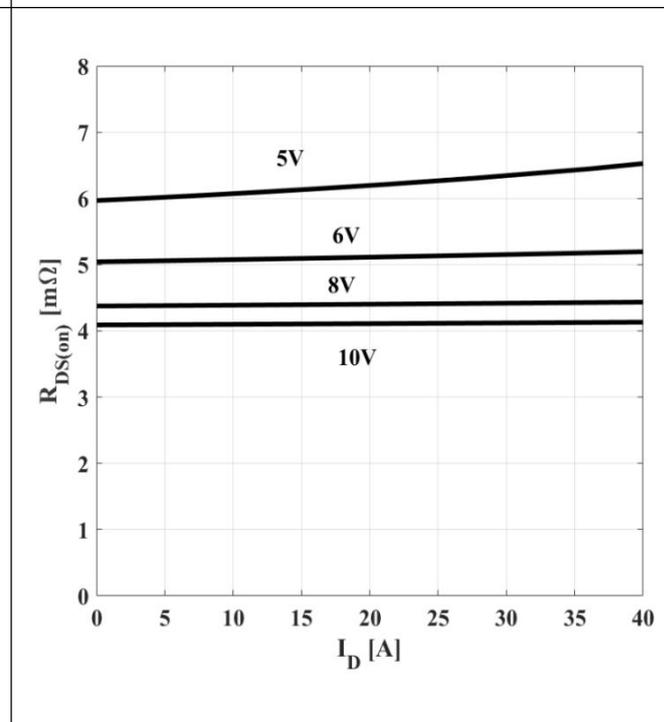
$$I_D = f(T_C); V_{GS} \geq 10V$$

**Figure5B: Typ. Drain Current**  
 (TO-220C&TO-263)


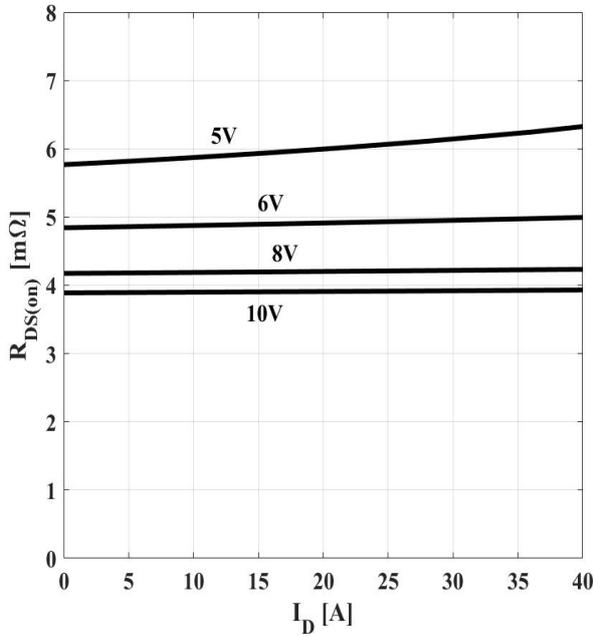
$$I_D = f(T_C); V_{GS} \geq 10V$$

**Figure6A: Typ. Drain-Source On-State Resistance**  
 (PDFN5\*6)


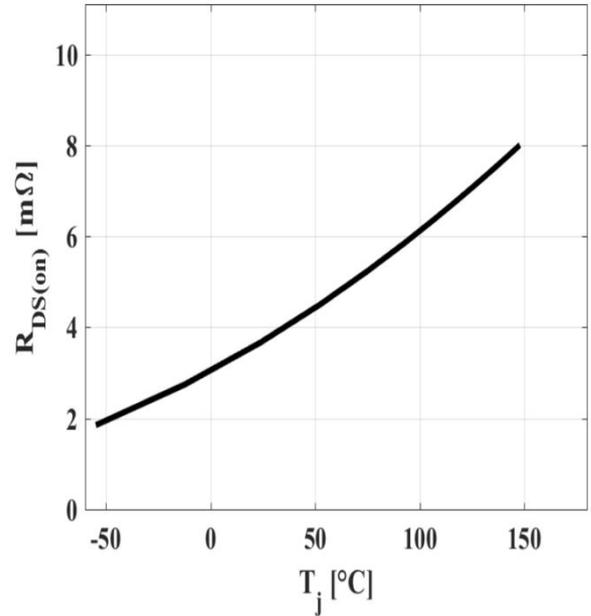
$$R_{DS(ON)} = f(I_D); T_j = 25^\circ C; \text{parameter: } V_{GS}$$

**Figure6B: Typ. Drain-Source On-State Resistance**  
 (TO-220C)


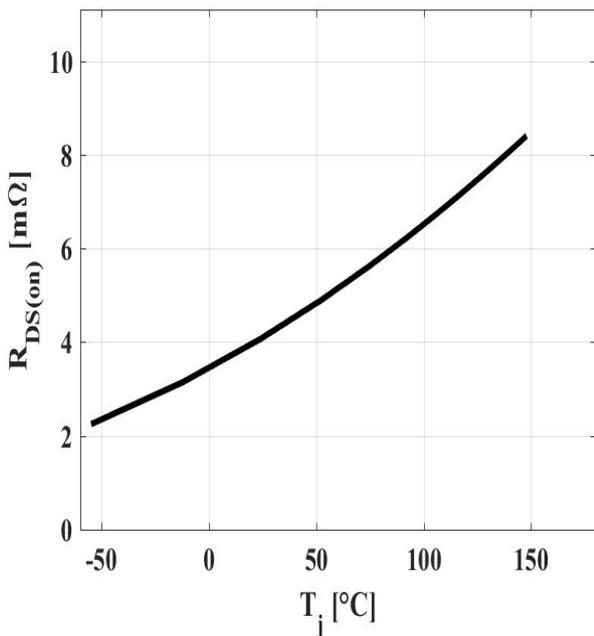
$$R_{DS(ON)} = f(I_D); T_j = 25^\circ C; \text{parameter: } V_{GS}$$

**Figure6C: Typ. Drain-Source On-State Resistance (TO-263)**


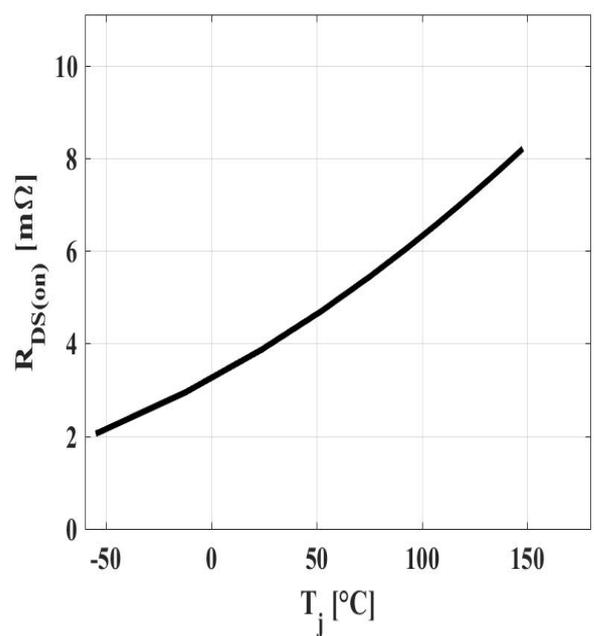
$$R_{DS(ON)}=f(I_D); T_j=25^{\circ}\text{C}; \text{parameter: } V_{GS}$$

**Figure7A: Typ. Drain-Source On-State Resistance(PDFN5\*6)**


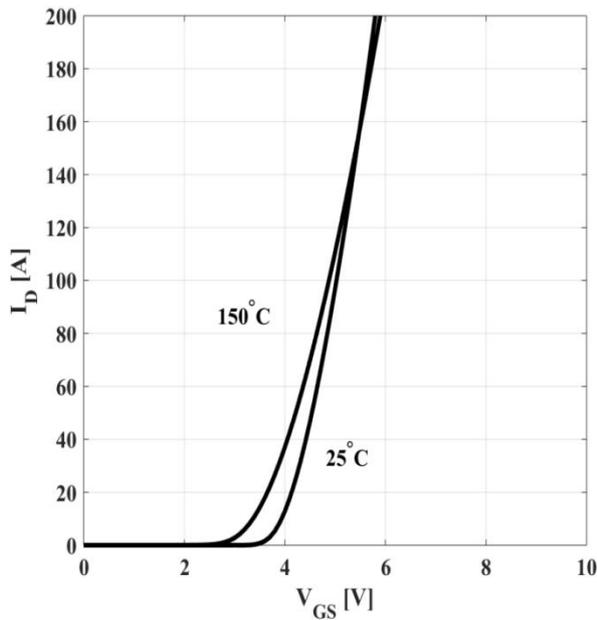
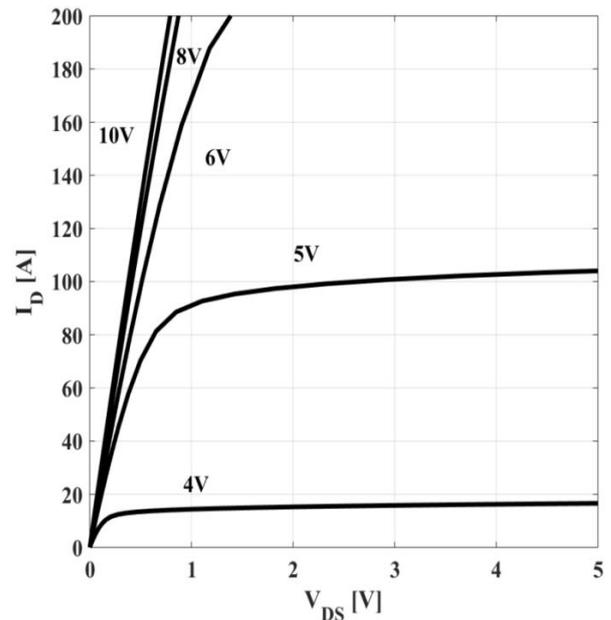
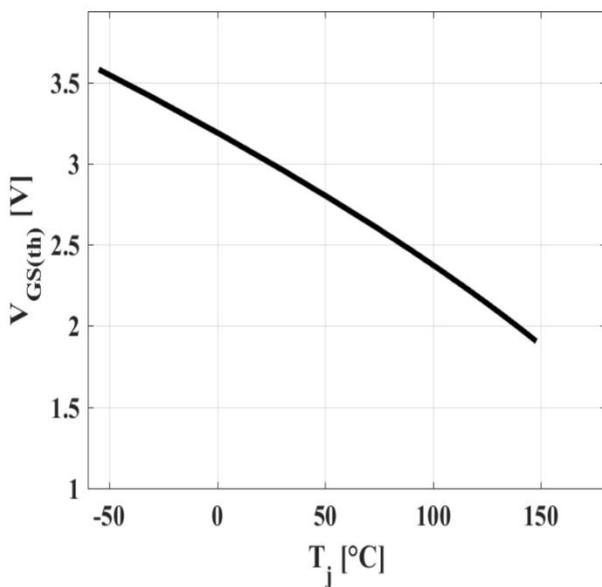
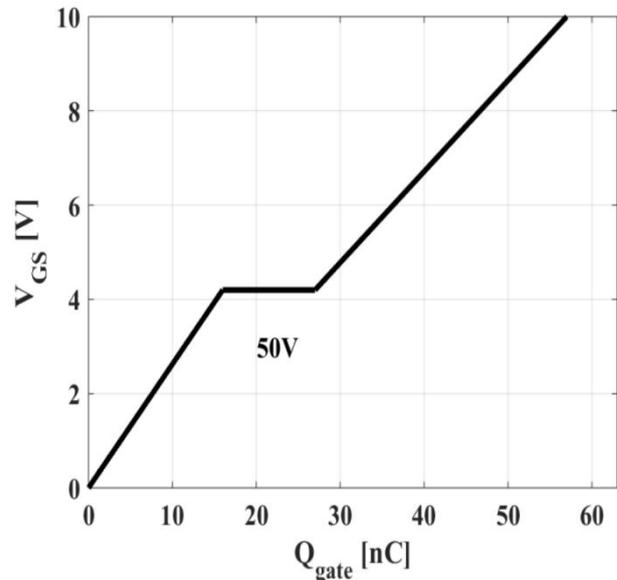
$$R_{DS(ON)}=f(T_j); I_D=20\text{A}; V_{GS}=10\text{V}$$

**Figure7B: Typ. Drain-Source On-State Resistance (TO-220C)**


$$R_{DS(ON)}=f(T_j); I_D=20\text{A}; V_{GS}=10\text{V}$$

**Figure7C: Typ. Drain-Source On-State Resistance (TO-263)**


$$R_{DS(ON)}=f(T_j); I_D=20\text{A}; V_{GS}=10\text{V}$$

**Figure8: Typ. Transfer Characteristics**

 $I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}; \text{parameter: } T_j$ 
**Figure9: Typ. Output Characteristics**

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$ 
**Figure10: Typ. Gate Threshold Voltage**

 $V_{GS(th)} = f(T_j); V_{GS} = V_{DS}; I_{DS} = 250\mu\text{A}$ 
**Figure 11: Typ. Gate Charge**

 $V_{GS} = f(Q_{gate}), I_D = 20\text{A pulsed}$

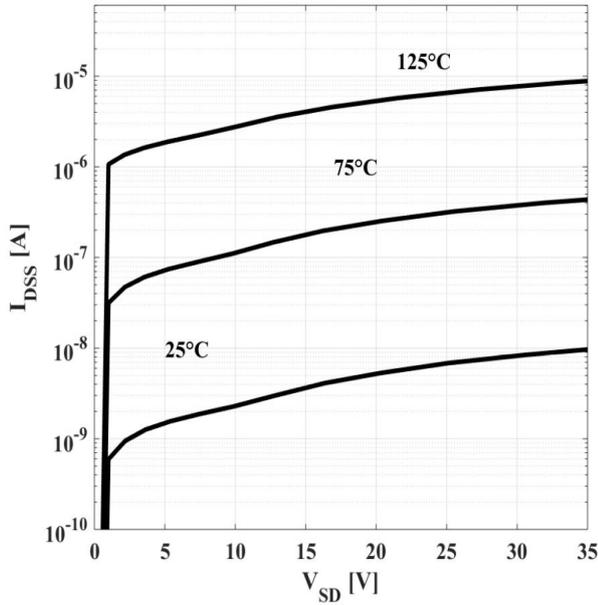
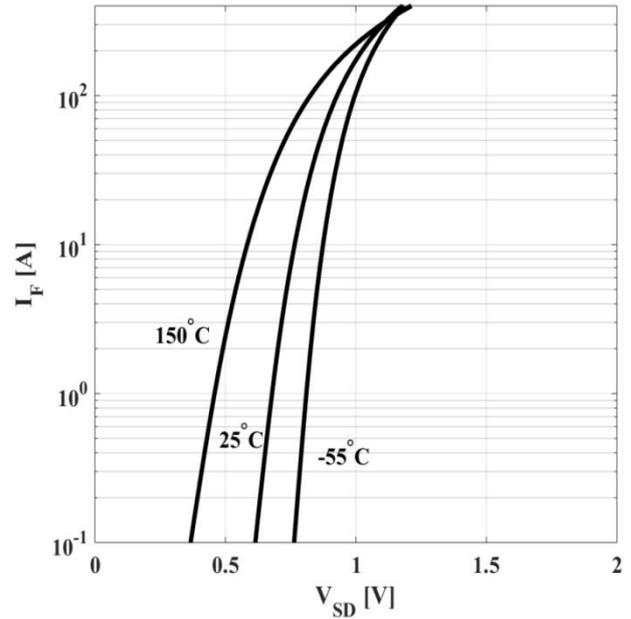
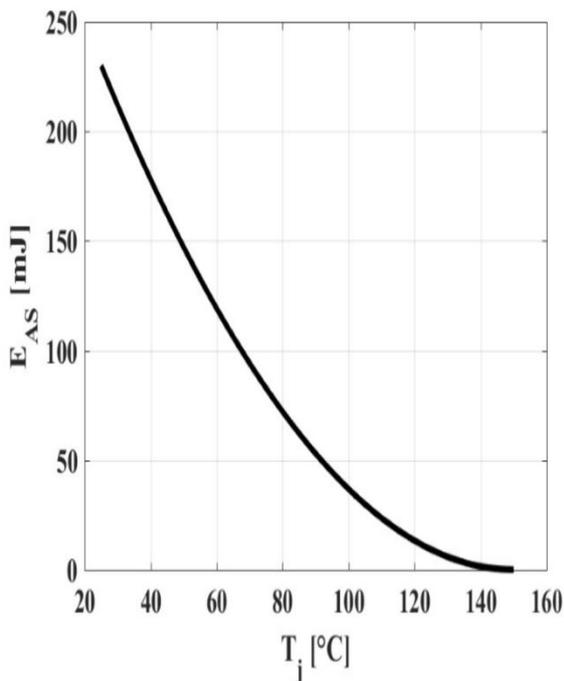
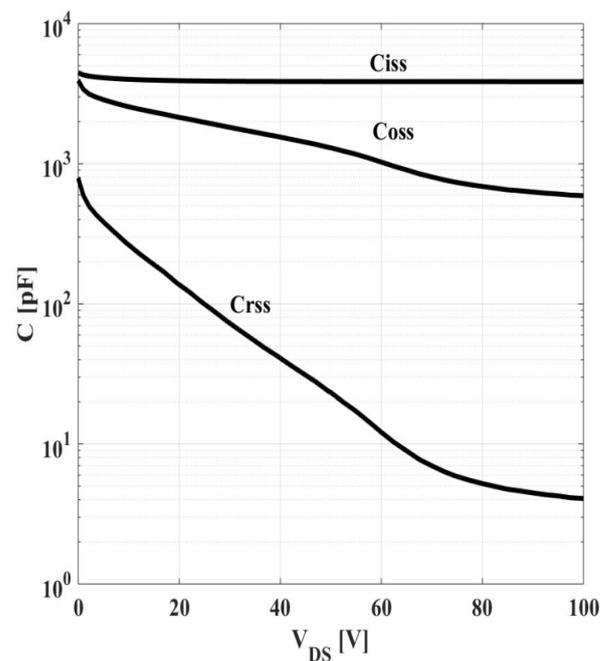
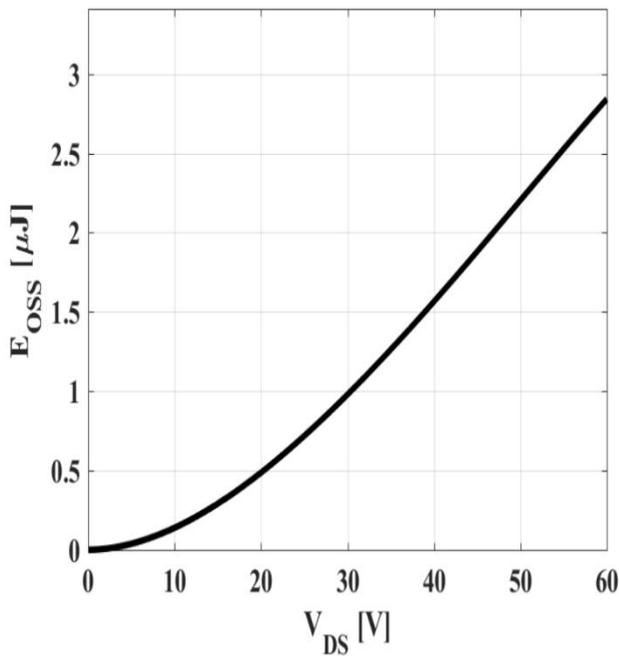
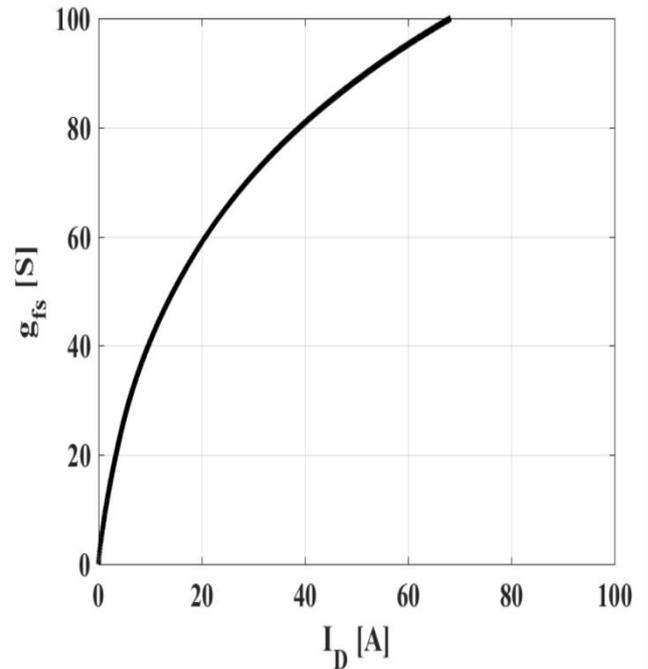
**Figure 12: Drain-Source Leakage Current**

 $I_{DSS}=f(V_{DS}); V_{GS}=0V; \text{parameter: } T_j$ 
**Figure 13: Forward Characteristics of Reverse Diode**

 $I_F=f(V_{SD}); \text{parameter: } T_j$ 
**Figure 14: Avalanche Energy**

 $E_{AS}=f(T_j); I_D=20.0A; V_{DD}=20V$ 
**Figure 15: Typ. Capacitances**

 $C=f(V_{DS}); V_{GS}=0; f=1MHz$

Figure 16:  $C_{OSS}$  Stored Energy


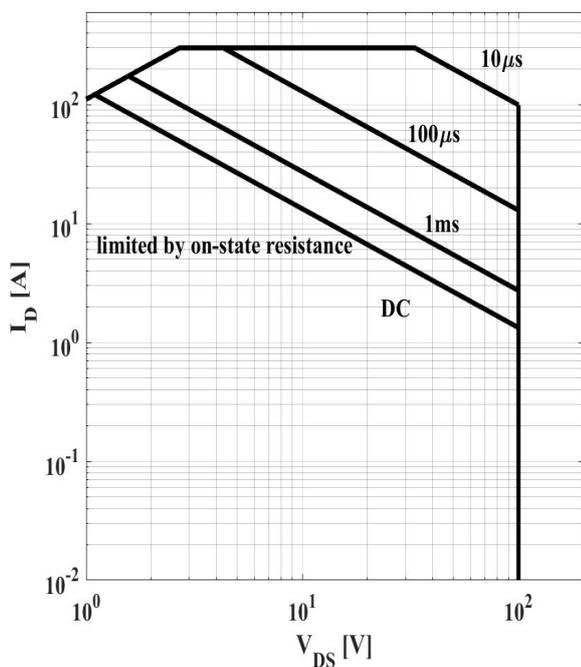
$$E_{OSS} = f(V_{DS})$$

Figure 17: Typ. Forward Transconductance



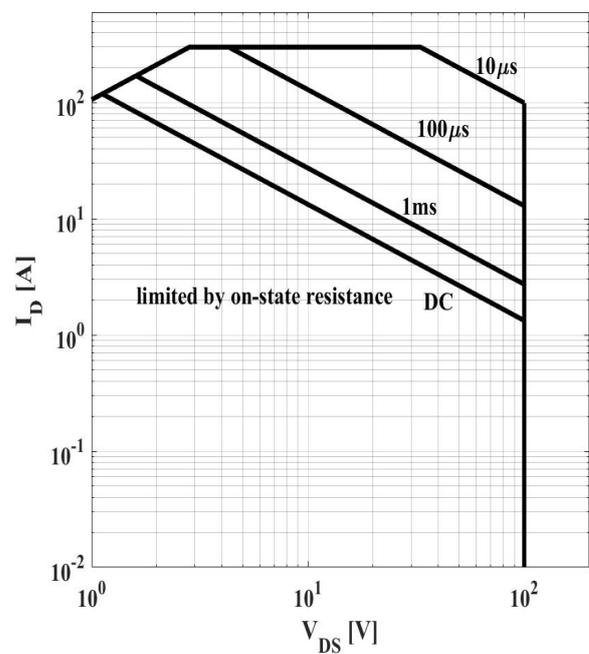
$$g_{fs} = f(I_D); T_j = 25^\circ\text{C}$$

Figure 18A: Safe Operating Area (PDFN5\*6)



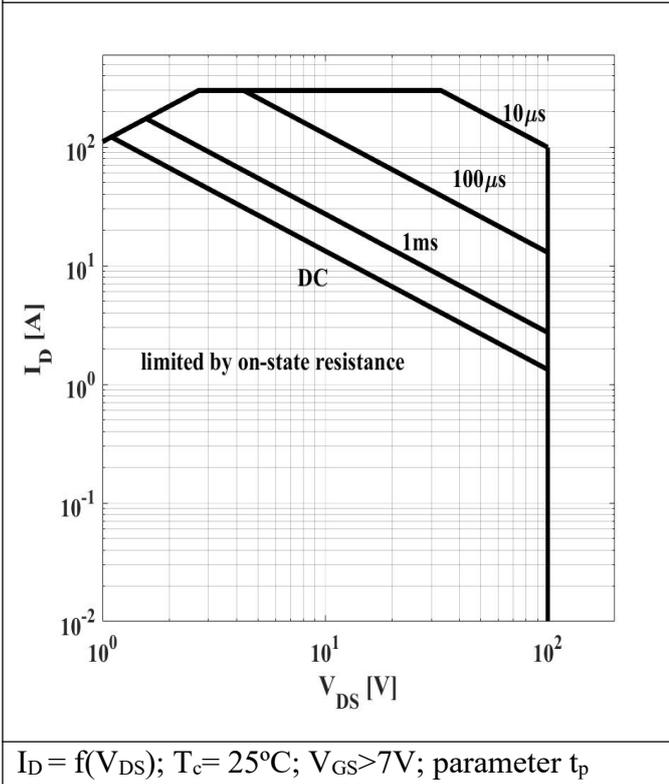
$$I_D = f(V_{DS}); T_c = 25^\circ\text{C}; V_{GS} > 7\text{V}; \text{parameter } t_p$$

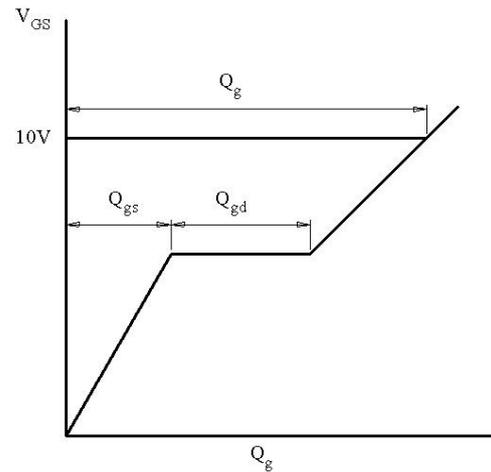
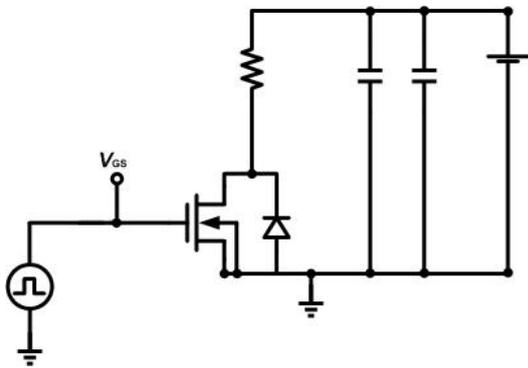
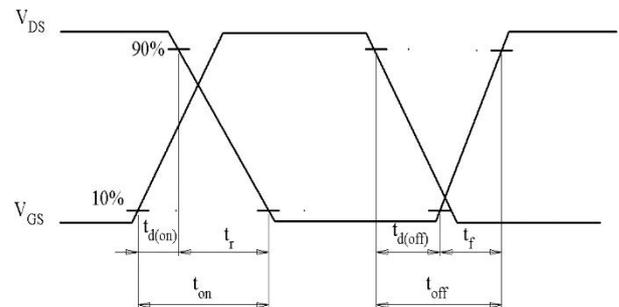
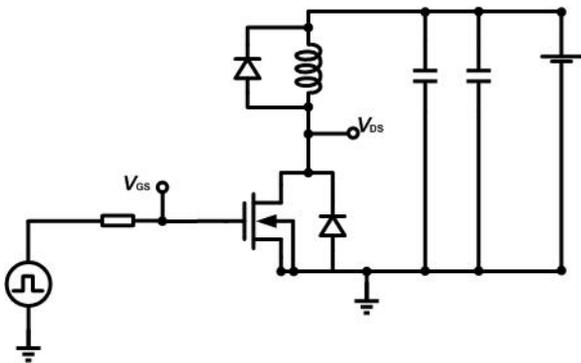
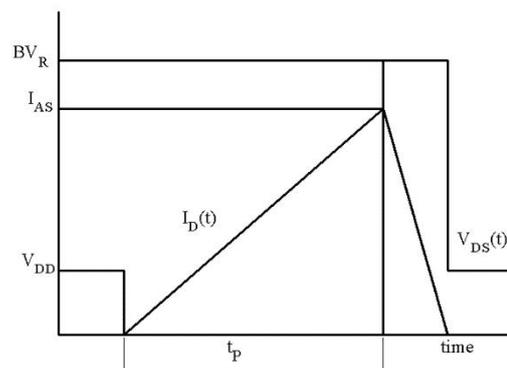
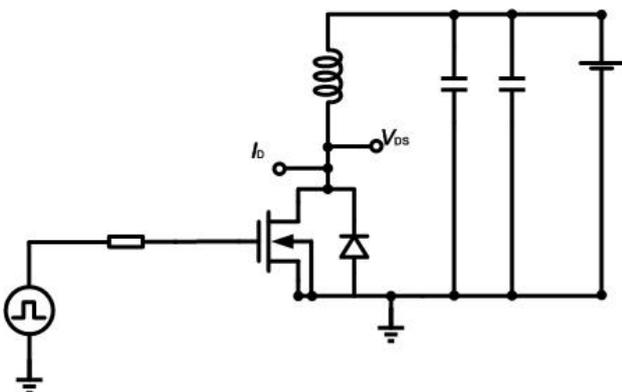
Figure 18B: Safe Operating Area (TO-220C)



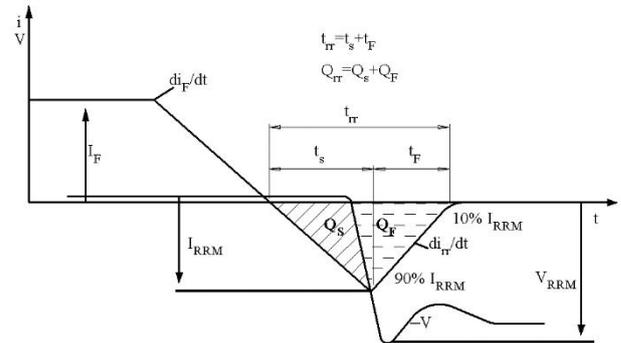
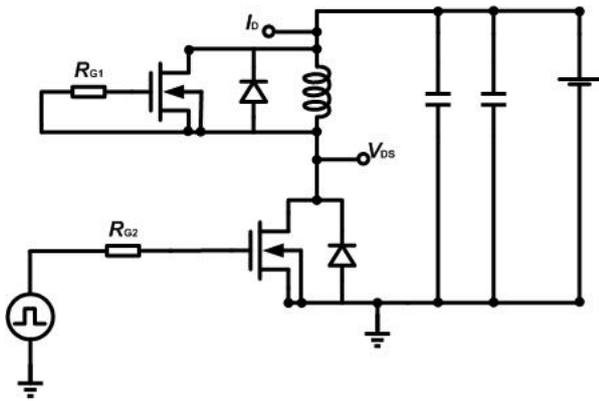
$$I_D = f(V_{DS}); T_c = 25^\circ\text{C}; V_{GS} > 7\text{V}; \text{parameter } t_p$$

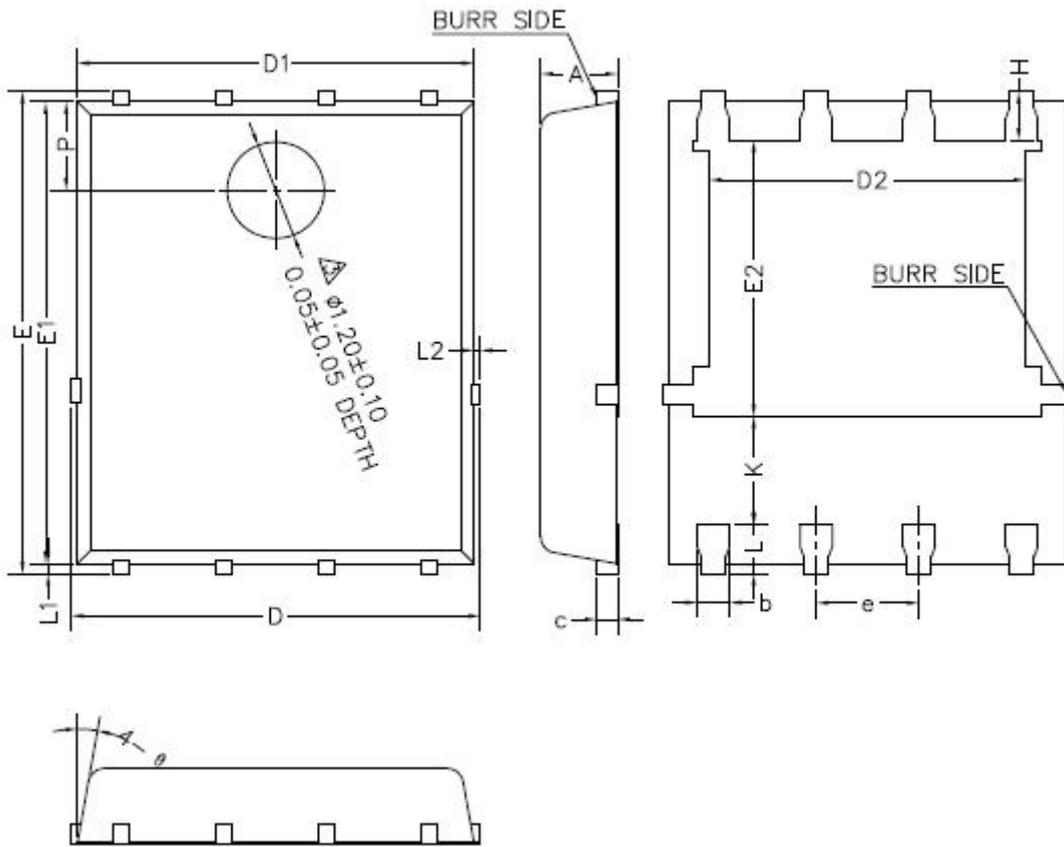
Figure 18C: Safe Operating Area(TO-263)



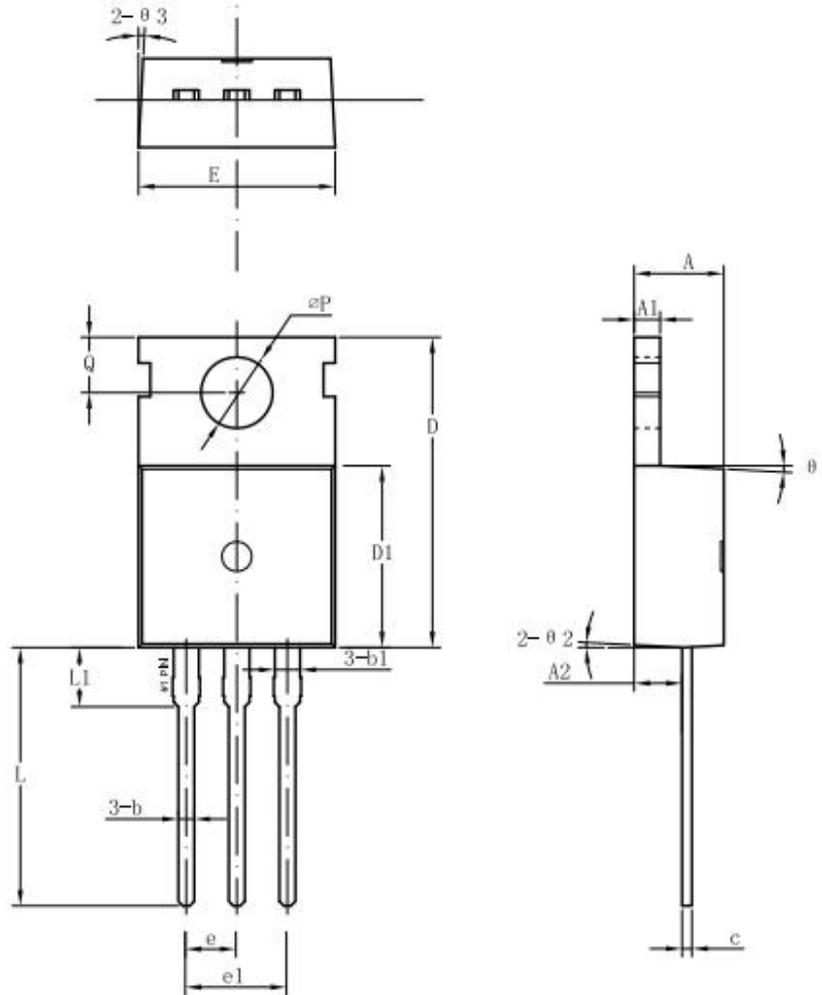
**Test Circuits**
**1. Gate Charge Test Circuit & Waveform**

**2. Switch Time Test Circuit**

**3. Unclamped Inductive Switching Test Circuit & Waveforms**


4. Test Circuit and Waveform for Diode Characteristics

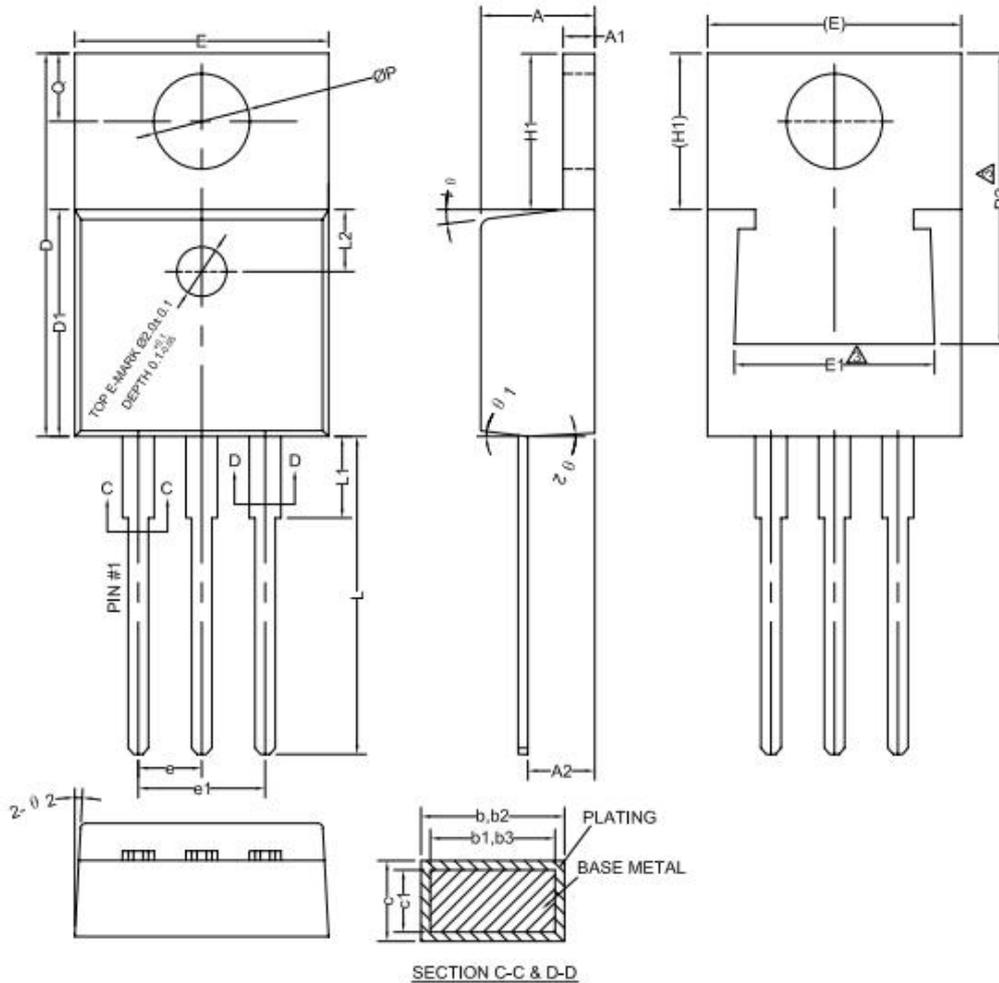


**Mechanical Dimensions**
**PDFN5\*6 Unit: mm**


Symbol	Dimensions(mm)		
	Min.	Typ.	Max.
A	0.90	1.10	1.20
b	0.35	0.40	0.45
c	0.21	0.25	0.34
D			5.10
D1	4.80	4.90	5.00
D2	3.91	4.01	4.11
e	1.17	1.27	1.37
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.34	3.44	3.54
H	0.51	0.61	0.71
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
L2			0.10
P	1.00	1.10	1.20
θ	8°	10°	12°

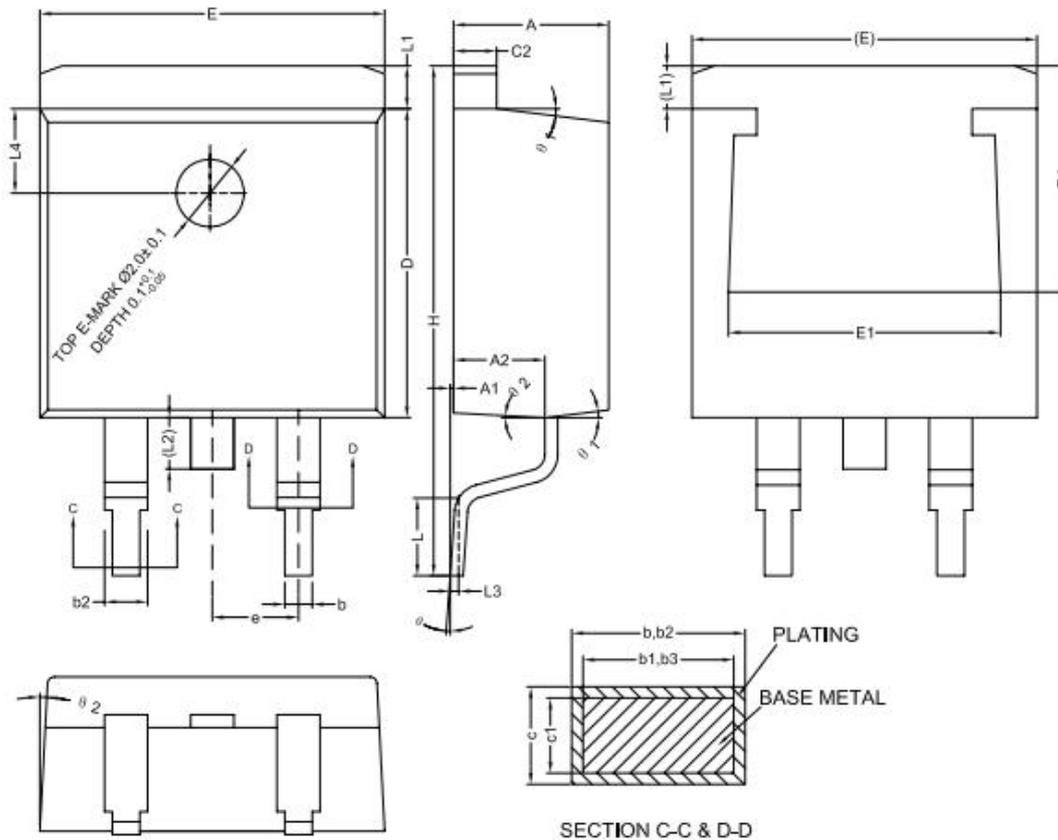
**Mechanical Dimensions**
**TO-220C(Package1)**
**Unit: mm**


Symbol	Dimensions (mm)			Symbol	Dimensions (mm)		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	4.30	4.50	4.70	e	-	2.54	-
A1	1.25	1.30	1.40	e1	-	5.08	-
A2	2.20	2.40	2.60	L	12.60	13.08	13.60
b	0.70	0.80	0.95	L1	-	3.00	-
b1	-	1.27	-	$\Phi P$	3.50	3.60	3.80
c	0.40	0.50	0.65	Q	2.60	2.80	3.00
D	15.20	15.70	16.20	$\theta 1$	-	3°	-
D1	9.00	9.20	9.40	$\theta 2$	-	3°	-
E	9.70	10.00	10.10	$\theta 3$	-	3°	-

**Mechanical Dimensions**
**TO-220C(Package2)**
**Unit: mm**


Symbol	Dimensions (mm)			Symbol	Dimensions (mm)		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	4.40	4.57	4.70	E	9.96	10.16	10.36
A1	1.22	-	1.32	E1	6.86	-	8.89
A2	2.59	2.69	2.79	e	2.44	2.54	2.64
b	0.77	-	0.90	e1	4.98	5.08	5.18
b1	0.76	0.81	0.86	H1	6.10	6.30	6.50
b2	1.23	-	1.36	L	12.70	-	13.12
b3	1.22	1.27	1.32	L1	-	-	3.90
c	0.34	-	0.47	L2	-	2.50REF	-
c1	0.33	0.38	0.43	ΦP	3.80	3.84	3.88
D	15.15	15.45	15.75	Q	2.60	-	2.90
D1	9.05	9.15	9.25	θ 1	5°	7°	9°
D2	11.40	-	12.88	θ 2	1°	3°	5°



**Mechanical Dimensions (Continued)**
**TO-263-2(Package2)**
**Unit: mm**


Symbol	Dimensions (mm)			Symbol	Dimensions (mm)		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	4.40	4.57	4.70	E	10.06	10.16	10.26
A1	0.00	0.10	0.25	E1	7.80	-	8.20
A2	2.59	2.69	2.79	e	-	2.54BSC	-
b	0.77	-	0.90	H	14.70	15.10	15.50
b1	0.76	0.81	0.86	L	2.00	2.30	2.60
b2	1.23	-	1.36	L1	1.17	1.27	1.40
b3	1.22	1.27	1.32	L2	-	-	1.75
c	0.34	-	0.47	L3	-	0.25BSC	-
c1	0.33	0.38	0.43	L4	-	2.00REF	-
c2	1.22	-	1.32	⊙	0°	-	8°
D	9.05	9.15	9.25	⊙1	5°	7°	9°
D1	6.60	-	-	⊙2	1°	3°	5°



Sanrise Technology Limited Company

<http://www.sanrise-tech.com>

#### IMPORTANT NOTICE

Shenzhen Sanrise Technology Co., LTD. reserves the right to make changes without further notice to any products or specifications herein. Shenzhen Sanrise Technology Co., LTD. does not assume any responsibility for use of any its products for any particular purpose, nor does Shenzhen Sanrise Technology Co., LTD. assume any liability arising out of the application or use of any its products or circuits. Shenzhen Sanrise Technology Co., LTD. does not convey any license under its patent rights or other rights nor the rights of others.

---

#### Main Site:

##### - Headquarter

Shenzhen Sanrise Technology Co., LTD.

A1206, Skyworth building, No. 008, gaoxinnan 1st Road,  
Gaoxin District, Yuehai street,, Nanshan District, ShenZhen,  
P.R.China

Tel: +86-755-22953335

Fax: +86-755-22916878

##### - Shanghai Office

Sanrise Technology Limited Company

Rm.401, Building B, No. 666, Zhangheng Road,  
Zhangjiang Hi-Tech Park, Shanghai, P.R.China

Tel: +86-21-68825918