DS90UB934-Q1 12-bit 100-MHz FPD-Link III Deserializer for 1MP/60fps and 2MP/30fps Cameras

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified for Automotive Applications With the Following Results:
  - Device Temperature Grade 2: –40°C to +105°C Ambient Operating Temperature
  - Device HBM ESD Classification Level ±2 kV
  - Device CDM ESD Classification Level C4
- Operates up to 100 MHz in 12-bit Mode to Support 1MP/60fps and 2MP/30fps Imagers as well as Satellite RADAR
- Configurable 12-bit Parallel CMOS Compatible with DS90UB913A/933 Serializers
- Adaptive Equalization Compensates for Cable Aging and Degradation Effects
- Ultra-low Latency Bi-directional Control Data Channel with Data Protection
- Cable Link Detect Diagnostics
- Supports Power-over-Coax Operation (PoC)
- ISO 10605 and IEC 61000-4-2 ESD Compliant
- Low Radiated and Conductive Emissions
- BIST (Built in Self-Test)

2 Applications

- Automotive
  - Rear-View Cameras (RVC)
  - Surround View Systems (SVS)
  - Camera Monitor Systems (CMS)
  - Forward Vision Cameras (FC)
  - Driver Monitoring Systems (DMS)
  - Satellite RADAR Modules
- Security and Surveillance Cameras
- Industrial and Medical Imaging

3 Description

The DS90UB934-Q1 FPD-Link III deserializer, in conjunction with the DS90UB913A/933-Q1 serializers, supports the video transport needs with an ultra-high-speed forward channel and an embedded bidirectional control channel. The DS90UB934-Q1 converts the FPD-Link III stream into a parallel CMOS output interface designed to support automotive image sensors up to 12 bits at 100 MHz with resolutions including 1MP/60fps and 2MP/30fps.

The DS90UB933/934 chipset is fully AEC-Q100 qualified and designed to receive data across either 50-Ω single-ended coaxial or 100-Ω shielded-twisted pair (STP) cable assemblies. The DS90UB934-Q1 uses an advanced adaptive equalizer to allow support of various cable lengths and types with no additional programming required.

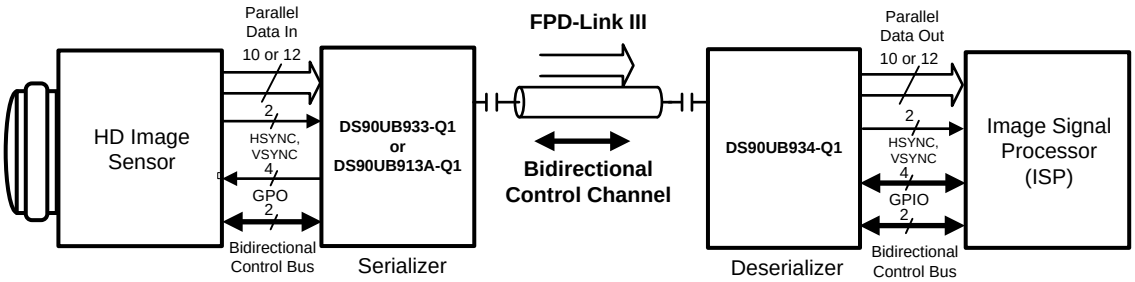
The DS90UB934-Q1 is improved over prior generations of ADAS FPD-Link III deserializer devices (such as DS90UB914A-Q1) offering higher bandwidth support with additional enhancements.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS90UB934-Q1	VQFN (48)	7.00 mm × 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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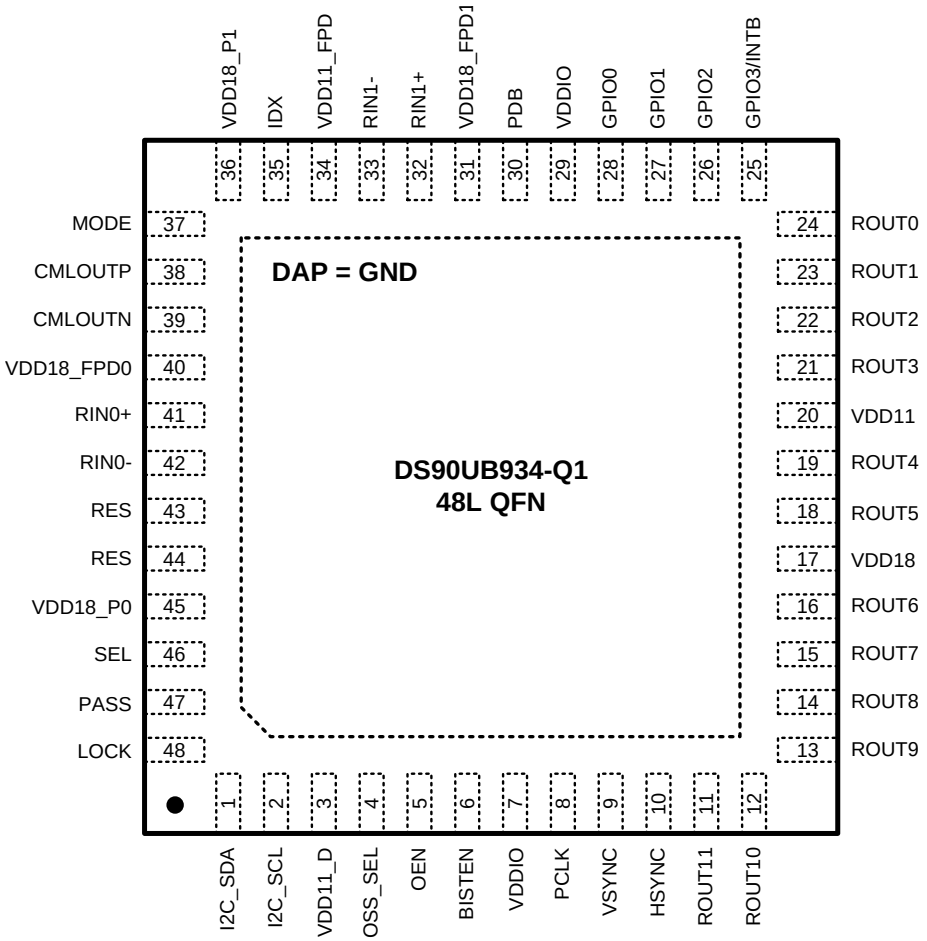
4 Revision History

Changes from Original (September 2016) to Revision A **Page**

- Changed product preview to production data ... 1

5 Pin Configuration and Functions

RGZ Package
48-Pin VQFN With Thermal Pad
Top View



Pin Functions

PIN		I/O TYPE	DESCRIPTION
NAME	NO.		
RECEIVE DATA PARALLEL OUTPUT			
ROUT0	24	O	RECEIVE DATA OUTPUT: This signal carries data from the FPD-LINK III deserializer to the processor. Output is parallel, configurable for up to 12 bits (ROUT0 – ROUT11) single ended outputs. VDDIO logic levels. For unused outputs leave as No Connect.
ROUT1	23		
ROUT2	22		
ROUT3	21		
ROUT4	19		
ROUT5	18		
ROUT6	16		
ROUT7	15		
ROUT8	14		
ROUT9	13		
ROUT10	12		
ROUT11	11		
HSYNC	10	O	Horizontal SYNC output. VDDIO logic levels.

Pin Functions (continued)

PIN		I/O TYPE	DESCRIPTION
NAME	NO.		
VSYNC	9	O	Vertical SYNC output. VDDIO logic levels.
PCLK	8	O	Pixel clock (PCLK) output. VDDIO logic levels.
GPIO			
GPIO0	28	I/O, PD	General purpose input/output: Pins can be used to control and respond to various commands. They may be configured to be the input signals for the corresponding GPOs on the serializer or they may be configured to be outputs to follow local register settings. At power up the GPIO are disabled and by default include a 25-kΩ (typical) pulldown resistor. VDDIO logic levels.
GPIO1	27		
GPIO2	26		
GPIO3/INTB	25	I/O, Open Drain	General purpose input/output: Pin GPIO3 can be configured to be an input signal for GPOs on the serializer. Pin 25 is shared with INTB. Pull up with 4.7 kΩ to VDDIO. Programmable input/output pin is an active-low open drain and controlled by the status registers.
FPD-LINK III INTERFACE			
RIN0+	41	I/O	Receive input channel 0: Differential FPD-Link receiver and bidirectional control back channel output. The IO must be AC coupled. There is internal 100Ω differential termination between RIN0+ and RIN0-. For applications using single-ended coaxial channel connect RIN0+ with 100-nF, AC-coupling capacitor and terminate RIN0– to GND with a 47-nF capacitor and 50-Ω resistor. For STP applications connect both RIN0+ and RIN0- with 100-nF, AC-coupling capacitor.
RIN0–	42		
RIN1+	32	I/O	Receive input channel 1: Differential FPD-Link receiver and bidirectional control back channel output. The IO must be AC coupled. There is internal 100Ω differential termination between RIN1+ and RIN1–. For applications using single-ended coaxial channel connect RIN0+ with 100nF AC coupling capacitor and terminate RIN1- to Ground with a 47 nF capacitor and 50 ohm resistor. For STP applications connect both RIN1+ and RIN1– with 100 nF AC coupling capacitor.
RIN1–	33		
I2C PINS			
I2C_SCL	2	I/O, Open Drain	I2C serial clock: Clock line for the bidirectional control bus communication. External 2-kΩ to 4.7-kΩ pullup resistor to VDDIO recommended per I2C interface standards.
I2C_SDA	1	I/O, Open Drain	I2C serial data: Data line for bidirectional control bus communication. External 2-kΩ to 4.7-kΩ pullup resistor to VDDIO recommended per I2C interface standards.
CONFIGURATION and CONTROL PINS			
IDX	35	S	Input. I2C serial control bus device ID address Connect to external pullup to VDD18 (pin 17) and pull down to GND to create a voltage divider. See Table 7.
MODE	37	S	Mode select configuration input to set operating mode based on input voltage level. Typically connected to voltage divider via external pullup to VDD18 (pin 17) and pulldown to GND See Table 2.
PDB	30	S, PD	Power-down inverted Input Pin. When PDB input is brought HIGH, the device is enabled. Asserting PDB signal low powers down the device and consume minimum power. The default function of this pin is PDB = LOW; POWER DOWN. This pin has a 50-kΩ (typical) internal pulldown resistor. *INPUT IS 3.3 V TOLERANT.* PDB = 1.8 V, device is enabled (normal operation) PDB = 0, device is powered down.
SEL	46	S,PD	MUX select: Digital input for selecting FPD Link input channel 0 (A) or channel 1 (B). The default state of SEL = L, selects RIN0, input A, as the active channel on the deserializer. Asserting SEL = H selects RIN1 input B as the active channel on the deserializer. This pin has a 25-kΩ (typical) internal pulldown resistor. VDDIO logic levels.
OSS_SEL	4	S, PD	Output sleep state select pin for enabling output sleep state. This pin has a 25-kΩ (typical) internal pulldown resistor. VDDIO logic levels. See *DVP Output Control*.
OEN	5	S, PD	Output enable. This pin has a 1-MΩ (typical) internal pulldown resistor. VDDIO logic levels. See *DVP Output Control*.

Pin Functions (continued)

PIN		I/O TYPE	DESCRIPTION
NAME	NO.		
DIAGNOSTIC PINS			
CMLOUTP	38	O	Channel monitor loop-through (CML) driver differential output. Typically routed to test points and not connected. For monitoring terminate CMLOUT with a 100-Ω differential load.
CMLOUTN	39		
BISTEN	6	S, PD	BIST enable: BISTEN = H, BIST mode is enabled BISTEN = L, BIST mode is disabled. See *Built-In Self Test (BIST)* for more information. This pin has a 25-kΩ (typ) internal pulldown resistor. VDDIO logic levels.
PASS	47	O	PASS Output: PASS = H, ERROR FREE transmission in forward channel operation. PASS = L, one or more errors were detected in the received payload. See *Built-In Self Test (BIST)* for more information. Leave No Connect if unused. Typically route to test point for monitoring. VDDIO logic levels.
LOCK	48	O	LOCK Status: Output pin for monitoring lock status of FPD-Link III channel. LOCK = H, PLL is Locked, outputs are active. LOCK = L, PLL is unlocked, may be used as link status. VDDIO logic levels.
RES	44	S, PD	Reserved: Input for selecting digital test mode. Must be NC or tied to GND for normal operation.
RES	43	S,PD	Reserved: Input for selecting digital test mode. Must be NC or tied to GND for normal operation.
POWER AND GROUND			
VDDIO	7,29	P	VDDIO voltage supply input: The single-ended outputs and control input are powered from VDDIO. VDDIO can be connected to a 1.8-V, ±5% or 3-V to 3.6-V power rail. Each pin requires a minimum 10-nF capacitor to GND.
VDD18	17	P	1.8-V (±5%) power supply. Requires 1-μF, 0.1-μF, and 0.01-μF capacitors to GND at each VDD pin.
VDD18_P0 VDD18_P1	45 36	P	1.8-V (±5%) PLL power supplies. Requires 1-μF, 0.1-μF, and 0.01-μF capacitors to GND at each VDD pin.
VDD18_FPD0 VDD18_FPD1	40 31	P	1.8-V (±5%) high-speed transceiver (HSTRX) analog power supplies. Requires 10-μF, 0.1-μF, and 0.01-μF capacitors to GND at each VDD pin.
VDD11_FPD	34	D	Decoupling capacitor connection for internal analog regulator. Requires a minimum 4.7-μF capacitor to GND and must not be connected to other 1.1-V supply rails.
VDD11_DVP	20	D	Decoupling capacitor connection for internal mixed signal regulator. Requires a minimum 4.7-μF capacitor to GND and must not be connected to other 1.1-V supply rails.
VDD11_D	3	D	Decoupling capacitor connection for internal digital regulator. Requires a minimum 4.7-μF capacitor to GND and must not be connected to other 1.1-V supply rails.
GND	DAP	G	DAP is the large metal contact at the bottom side, located at the center of the QFN package. Connect to the ground plane (GND).

These definitions define the functionality of the I/O cells for each pin:

TYPE:

- I = Input
- O = Output
- I/O = Input/Output
- S = Configuration pin (All strap pins have internal pulldowns. If the default strap value is needed to be changed then use an external resistor.)
- PD = Internal pulldown
- P, G = Power supply, ground
- D = Decoupling pin for internal voltage rail

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Supply voltage	VDD18 (VDD18, VDD18_P1 , VDD18_P0 , VDD18_FPD0, VDD18_FPD1)	–0.3	2.16	V
	VDDIO	–0.3	3.96	V
FPD-Link III input voltage	RIN0+, RIN0–, RIN1+, RIN1– Device powered up (VDD18 and VDDIO within recommended operating conditions)	–0.3	2.75	V
	RIN0+, RIN0–, RIN1+, RIN1– Device powered down (VDD18 and VDDIO below recommended operating conditions) Transient Voltage	–0.3	1.45	V
	RIN0+, RIN0–, RIN1+, RIN1– Device powered down (VDD18 and VDDIO below recommended operating conditions) DC Voltage	–0.3	1.35	V
LVCMOS IO voltage	ROUT[11:0], PCLK, VSYNC, HSYNC, GPIO0, GPIO1, GPIO2, PDB, SEL, OSS_SEL, OEN, BISTEN, PASS, LOCK	–0.3	$V_{(VDDIO)}$ + 0.3	V
Configuration input voltage	MODE, IDX	–0.3	$V_{(VDD18)}$ + 0.3	V
Open-drain voltage	GPIO3/INTB, I2C_SDA, I2C_SCL	–0.3	3.96	V
Junction temperature			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office or Distributors for availability and specifications.
(2) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings – JEDEC

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	RIN0+, RIN0–, RIN1+, RIN1–	±2000	V
			Other pins	±2000	
		Charged device model (CDM), per AEC Q100-011		±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 ESD Ratings – IEC and ISO

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	ESD Rating (IEC 61000-4-2) R_D= 330 Ω, C_S = 150 pF	Contact Discharge (RIN0+, RIN0–, RIN1+, RIN1–)	±8000	V
			Air Discharge (RIN0+, RIN0–, RIN1+, RIN1–)	±15000	
		ESD Rating (ISO 10605) R_D= 330 Ω, C_S = 150 pF and 330 pF R_D= 2 kΩ, C_S = 150 pF and 330 pF	Contact Discharge (RIN0+, RIN0–, RIN1+, RIN1–)	±8000	V
			Air Discharge (RIN0+, RIN0–, RIN1+, RIN1–)	±15000	

6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage	$V_{(VDD18)}$	1.71	1.8	1.89	V
LVCMOS supply voltage	$V_{(VDDIO)}$ = 1.8	1.71	1.8	1.89	V
	OR $V_{(VDDIO)}$ = 3.3	3.0	3.3	3.6	V
Operating free-air temperature, T_A		–40	25	105	°C
Data rate		0.7		1.87	Gbps
PCLK frequency		25		100	MHz
Local I^2C frequency, f_{I2C}				1	MHz
Supply Noise (1) (2)	$V_{(VDD18)}$			50	mV_{P-P}
	$V_{(VDDIO)}$			50	
Power-over-Coax noise (3)	RIN0+, RIN0–, RIN1+, RIN1–		20		

(1) DC-50 MHz
(2) Specification is ensured by design and/or characterization and is not tested in production.
(3) Measured across RIN[1:0]+ and RIN[1:0]− terminals

6.5 Thermal Information

THERMAL METRIC (1)		DS90UB934-Q1 RGZ (VQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.3	°C/W
$R_{\theta JC(TOP)}$	Junction-to-case (top) thermal resistance	12.3	°C/W
$R_{\theta JC(BOT)}$	Junction-to-case (bottom) thermal resistance	1.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics*.

6.6 DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
TOTAL POWER CONSUMPTION							
P_T	Total Power Consumption normal operation See Figure 5	Worst Case pattern Default registers	$V_{(VDD18)}$ = $V_{(VDDIO)}$ = 1.89 V		500	685	mW
			$V_{(VDD18)}$ = 1.89 V, $V_{(VDDIO)}$ = 3.6 V		900	1125	

DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS		PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
SUPPLY CURRENT								
I_{DD}	Deserializer Supply Current (includes load current). See Figure 5.	f = 100 MHz, 10-bit mode $V_{(VDD18)}$ = 1.89 V Worst Case Pattern, Default Registers C_L = 8 pF	$V_{(VDDIO)}$ = 1.89 V OR 3.6 V	VDD18			250	mA
			$V_{(VDDIO)}$ = 1.89 V	VDDIO			60	
			$V_{(VDDIO)}$ = 3.6 V	VDDIO			145	
		f = 100 MHz, 12-bit HF mode $V_{(VDD18)}$ = 1.89 V Worst Case Pattern, Default Registers C_L = 8 pF	$V_{(VDDIO)}$ = 1.89 V OR 3.6 V	VDD18			270	mA
			$V_{(VDDIO)}$ = 1.89 V	VDDIO			90	
			$V_{(VDDIO)}$ = 3.6 V	VDDIO			170	
		f = 50 MHz, 12-bit LF mode $V_{(VDD18)}$ = 1.89 V Worst Case Pattern, Default Registers C_L = 8 pF	$V_{(VDDIO)}$ = 1.89 V OR 3.6 V	VDD18			240	mA
			$V_{(VDDIO)}$ = 1.89 V	VDDIO			80	
			$V_{(VDDIO)}$ = 3.6 V	VDDIO			155	
I_{DDZ}	Deserializer Power Down Supply Current	$V_{(VDD18)}$ = 1.89 V, $V_{(VDDIO)}$ = 3.6V PDB = L, All other LVCMOS inputs = 0V, Default Registers		VDD18			30	mA
				VDDIO			10	
1.8V LVCMOS I/O (1)								
V_{OH}	High Level Output Voltage	I_{OH} = –2 mA	$V_{(VDDIO)}$ = 1.71 V to 1.89 V	ROUT[11:0], HSYNC, VSYNC, LOCK, PASS	$V_{(VDDIO)}$ – 0.45		$V_{(VDDIO)}$	V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA	$V_{(VDDIO)}$ = 1.71 V to 1.89 V		GND		0.45	V
V_{IH}	High Level Input Voltage	$V_{(VDDIO)}$ = 1.71 V to 1.89 V		GPIO[3:0], PDB, OEN, SEL, OSS_SEL, BISTEN	0.65 × $V_{(VDDIO)}$		$V_{(VDDIO)}$	V
V_{IL}	Low Level Input Voltage	$V_{(VDDIO)}$ = 1.71 V to 1.89 V			GND		0.35 × $V_{(VDDIO)}$	V
I_{IH}	Input High Current	V_{IN} = 1.71 V to 1.89 V		GPIO[3:0] (2), OEN	–20		20	µA
				GPIO[2:0] (3), SEL, PDB, OSS_SEL, BISTEN	–100		100	µA
I_{IL}	Input Low Current	V_{IN} = 0 V		GPIO[3:0], PDB, OEN, SEL, OSS_SEL, BISTEN	–20		20	µA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0 V				–17		mA
I_{OZ}	TRI-STATE Output Current	V_{OUT} = 0 V or $V_{(VDDIO)}$, PDB = L			–20		20	µA
3.3V LVCMOS I/O (4)								
V_{OH}	High Level Output Voltage	I_{OH} = –4 mA	$V_{(VDDIO)}$ = 3.0 V to 3.6 V	GPIO[3:0], ROUT[11:0], HSYNC, VSYNC, LOCK, PASS	2.4		$V_{(VDDIO)}$	V
V_{OL}	Low Level Output Voltage	I_{OL} = 4 mA	$V_{(VDDIO)}$ = 3.0 V to 3.6 V		GND		0.4	V

(1) $V_{(VDDIO)}$ = 1.8 V ± 5%
(2) GPIO[2:0] Pull-down disabled; Register 0xBE = 0x03
(3) GPIO[2:0] Pull-down enabled; Register 0xBE = 0x00
(4) $V_{(VDDIO)}$ = 3.0 V to 3.6 V

DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
V_{IH}	High Level Input Voltage	$V_{(VDDIO)}$ = 3.0 V to 3.6 V	GPIO[3:0], OEN, SEL, OSS_SEL, BISTEN	2		$V_{(VDDIO)}$	V
			PDB	1.17		$V_{(VDDIO)}$	V
V_{IL}	Low Level Input Voltage	$V_{(VDDIO)}$ = 3.0 V to 3.6 V	GPIO[3:0], OEN, SEL, OSS_SEL, BISTEN	GND		0.8	V
			PDB	GND		0.63	V
I_{IH}	Input High Current	V_{IN} = 3.0 V to 3.6 V	GPIO[3:0](2), OEN, PDB	-20		20	µA
			GPIO[2:0](3), SEL, OSS_SEL, BISTEN	–190		190	µA
I_{IL}	Input Low Current	V_{IN} = 0 V	GPIO[3:0], OEN, SEL, OSS_SEL, BISTEN, PDB	–20		20	µA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0 V			–40		mA
I_{OZ}	TRI-STATE Output Current	V_{OUT} = 0 V or $V_{(VDDIO)}$, PDB = LOW		–60		60	µA
I2C SERIAL CONTROL BUS(5)							
V_{IH}	Input High Level		I2C_SDA, I2C_SCL	0.7 × $V_{(VDDIO)}$		$V_{(VDDIO)}$	V
V_{IL}	Input Low Level			GND		0.3 × $V_{(VDDIO)}$	V
V_{HY}	Input Hysteresis			50			mV
V_{OL}	Output Low Level	Standard/Fast Mode - I_{OL} = 4 mA; Fast Plus Mode - I_{OL} = 20 mA		0		0.4	V
I_{IH}	Input High Current	V_{IN} = $V_{(VDDIO)}$		–10		10	µA
I_{IL}	Input Low Current	V_{IN} = 0V		–10		10	µA
C_{IN}	Input Capacitance(6)				5	10	pF
FPD-LINK III INPUT							
V_{CM}	Common Mode Voltage See Figure 2.				1.2		V
R_T	Internal Termination Resistor	Single Ended		40	50	60	Ω
		Differential		80	100	120	Ω
FPD-LINK III BI-DIRECTIONAL CONTROL CHANNEL							
V_{OUT-BC}	Back Channel Single-Ended Output Voltage	RL = 50 Ω, Coaxial configuration, forward channel disabled	RIN0+, RIN1+	190		260	mV
V_{OD-BC}	Back Channel Differential Output Voltage	RL = 100 Ω, STP configuration, forward channel disabled	RIN0+, RIN0- RIN1+, RIN1-	380		520	mV

(5) $V_{(VDDIO)}$ = 1.8 V ± 5% **OR** 3.0 V to 3.6 V
(6) Specification is ensured by design and/or characterization and is not tested in production.

6.7 AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
LVCMOS I/O							
t_{RCP}	Receiver Output Clock Period. See Figure 7.	10-bit Mode	PCLK, 50 - 100 MHz	10		20	ns
		12-bit HF Mode	PCLK, 37.5 - 100 MHz	10		26.7	ns
		12-bit LF Mode	PCLK, 25 - 50 MHz	20		40	ns
t_{PDC}	PCLK Duty Cycle(1)	10-bit Mode	PCLK	45	50	55	%
		12-bit HF or LF Mode		40	50	60	%
t_{CLH}	LVCMOS Low-to-High Transition Time(1) See Figure 1.	$V_{(VDDIO)}$ = 1.71 V to 1.89 V OR $V_{(VDDIO)}$ = 3.0 V to 3.6 V CL = 8 pF (lumped load) Default Registers	PCLK		2	2.8	ns
t_{CHL}	LVCMOS High-to-Low Transition Time(1) See Figure 1.		PCLK		2	2.8	ns
t_{CLH}	LVCMOS Low-to-High Transition Time(1) See Figure 1.		ROUT[11:0], HSYNC, VSYNC, GPIO[2:0]		2.5	4	ns
t_{CHL}	LVCMOS High-to-Low Transition Time(1) See Figure 1.		ROUT[11:0], HSYNC, VSYNC, GPIO[2:0]		2.5	4	ns
t_{ROS}	ROUT Setup Data to PCLK(1) See Figure 7.		PCLK, ROUT[11:0], HSYNC, VSYNC	0.38T	0.5T		ns
t_{ROH}	ROUT Hold Data to PCLK(1) See Figure 7.		PCLK, ROUT[11:0], HSYNC, VSYNC	0.38T	0.5T		ns
t_{DD}	Deserializer Delay(1) See Figure 6.	Default Registers (RRFB = 1)	10-bit mode	175T		185T	ns
			12-bit HF mode	100T		115T	ns
			12-bit LF mode	65T		80T	ns
t_{DDLT}	Deserializer Data Lock Time See Figure 3.	Digital Reset, or PDB = HIGH to LOCK = HIGH	10-bit mode			22	ms
			12-bit HF mode			22	ms
			12-bit LF mode			22	ms
t_{RCJ}	Receiver Clock Jitter(1)	PCLK, SSCG[3:0] = OFF	10-bit mode		40	70	ps
			12-bit HF mode		52	90	ps
			12-bit LF mode		45	85	ps
t_{DPJ}	Deserializer Period Jitter(1)	PCLK, SSCG[3:0] = OFF	10-bit mode		885	1020	ps
			12-bit HF mode		420	880	ps
			12-bit LF mode		400	515	ps
t_{DCCJ}	Deserializer Cycle-to-Cycle Clock Jitter(2)	PCLK, SSCG[3:0] = OFF	10-bit mode		1360	1800	ps
			12-bit HF mode		1280	1500	ps
			12-bit LF mode		890	1150	ps
f_{dev}	Spread Spectrum Clocking Deviation Frequency See Figure 9.	LVCMOS Output Bus, SSCG[3:0] = ON	25 - 100 MHz		±0.5% to ±2.5%		
f_{mod}	Spread Spectrum Clocking Modulation Frequency See Figure 9.	LVCMOS Output Bus, SSCG[3:0] = ON	25 - 100 MHz		5 to 50		kHz

(1) Specification is ensured by design and/or characterization and is not tested in production.
(2) Specification is ensured by characterization.

AC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
FPD-Link III							
V_{IN}	Single Ended Input Voltage See Figure 2.	Coaxial configuration. 1010 pattern applied to the far end of a 15 meter cable. V_{IN} measured after the cable, at the deserializer input pins.	RIN0+, RIN0- RIN1+, RIN1-		50		mV
V_{ID}	Differential Input Voltage See Figure 2.	STP Configuration. 1010 pattern applied to the far end of a 15 meter cable. V_{ID} measured after the cable, at the deserializer input pins.			100		mV
f_{BC}	Back Channel Frequency			3.5		5.5	MHz
T_J	Back Channel Jitter(1)				7	15	ns
TOL_{JIT}	Input Jitter	10MHz Sinusoidal Jitter applied to FPD-Link III input				0.4	UI

6.8 Recommended Timing for the Serial Control Bus

Over I^2C supply and temperature ranges unless otherwise specified.

PARAMETER		STANDARD-MODE		FAST-MODE		FAST-MODE PLUS		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
I^2C SERIAL CONTROL BUS (Figure 4)								
f_{SCL}	SCL Clock Frequency	>0	100	>0	400	>0	1000	kHz
t_{LOW}	SCL Low Period	4.7		1.3		0.5		µs
t_{HIGH}	SCL High Period	4.0		0.6		0.26		µs
$t_{HD;STA}$	Hold time for a start or a repeated start condition	4.0		0.6		0.26		µs
$t_{SU;STA}$	Set Up time for a start or a repeated start condition	4.7		0.6		0.26		µs
$t_{HD;DAT}$	Data Hold Time	0		0		0		µs
$t_{SU;DAT}$	Data Set Up Time	250		100		50		ns
$t_{SU;STO}$	Set Up Time for STOP Condition	4.0		0.6		0.26		µs
t_{BUF}	Bus Free Time Between STOP and START	4.7		1.3		0.5		µs
t_r	SCL and SDA Rise Time		1000		300		120	ns
t_f	SCL and SDA Fall Time		300		300		120	ns
C_b	Capacitive Load for Each Bus Line(1)		400		400		550	pF
t_{SP}	Input Filter(1)		-		50		50	ns

(1) Specification is ensured by design and/or characterization and is not tested in production.

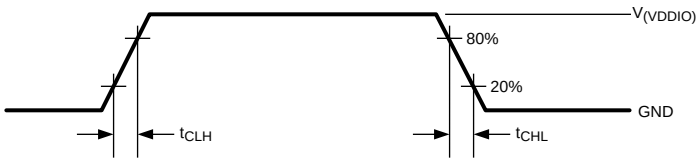


Figure 1. LVCMOS Transition Times

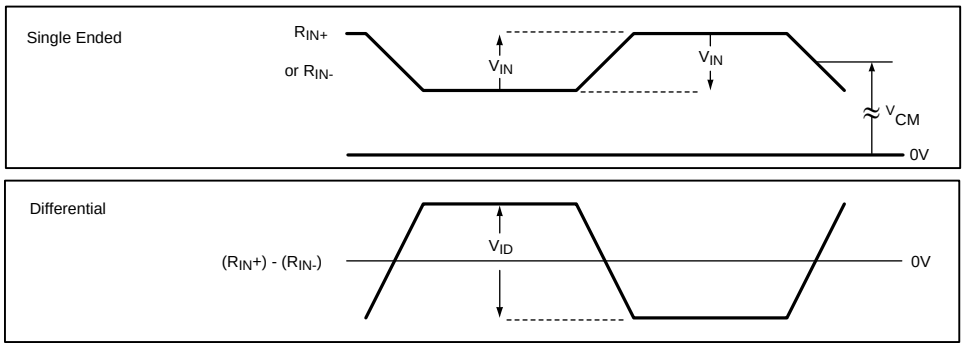


Figure 2. FPD-Link III Receiver V_{ID}, V_{IN}, V_{CM}

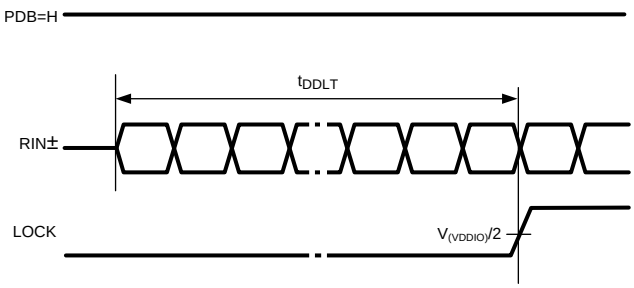


Figure 3. Deserializer Data Lock Time

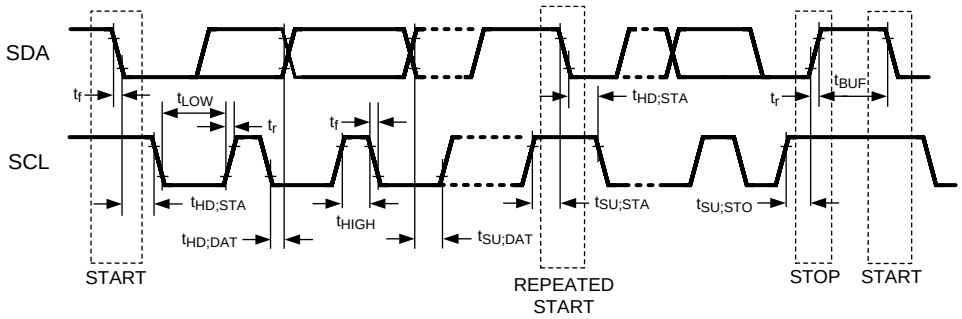


Figure 4. I2C Serial Control Bus Timing

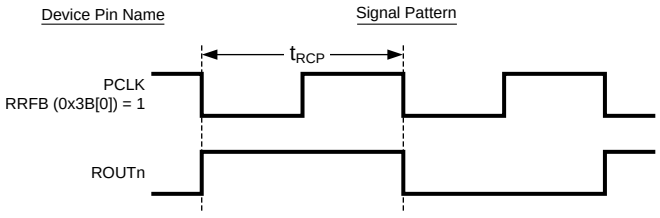


Figure 5. SSO Test Pattern for Power Consumption

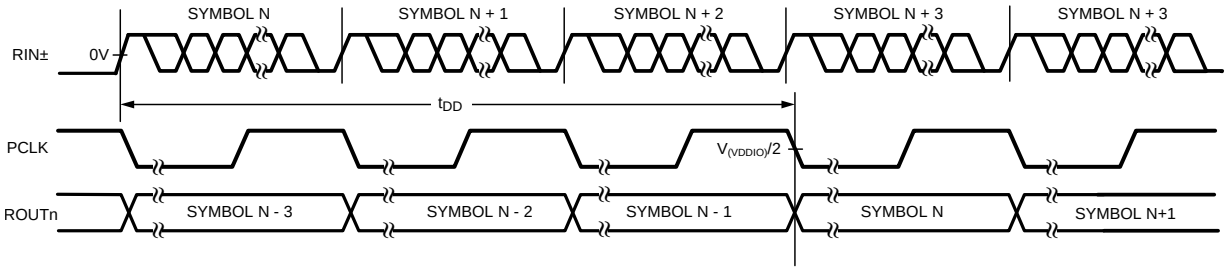


Figure 6. Deserializer Delay

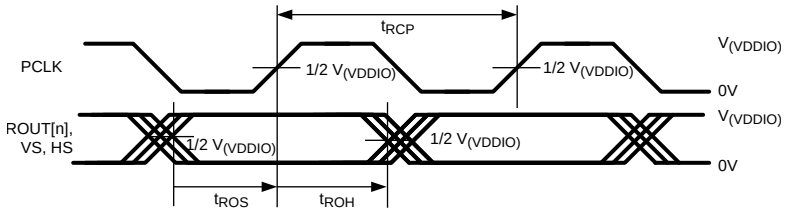


Figure 7. Deserializer Output Setup/Hold Times

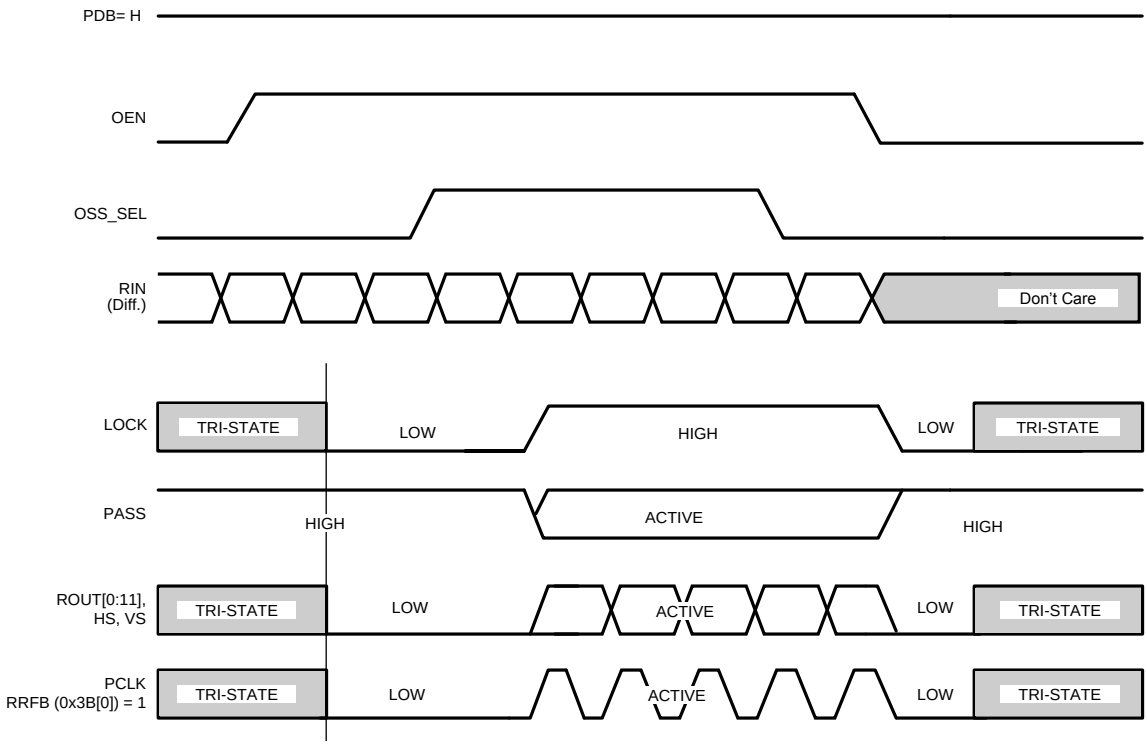


Figure 8. Output State (Setup and Hold) Times

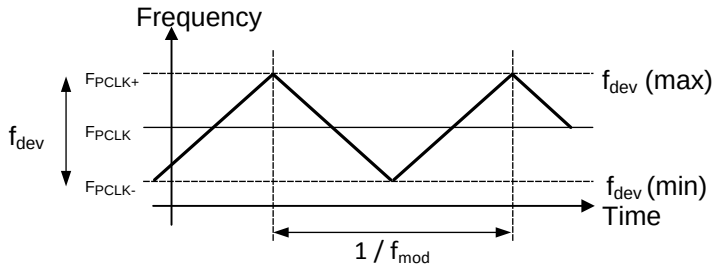


Figure 9. Spread Spectrum Clock Output Profile

6.9 Typical Characteristics

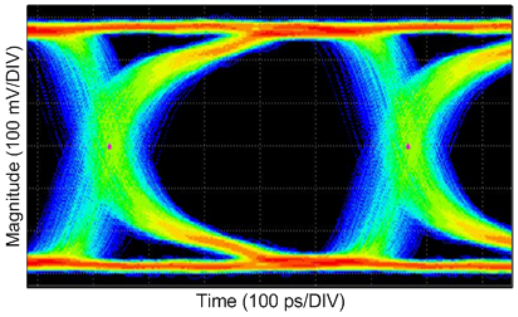


Figure 10. CMLOUTP/N Loop-through Eye Diagram at 1.867 Gbps

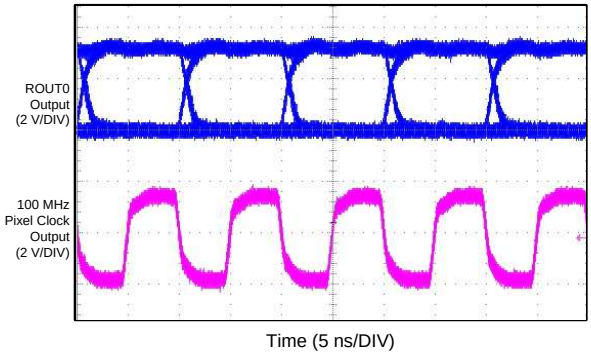


Figure 11. ROUT0 Data Sampled by 100-MHz PCLK RRFB (0x3B[0]) = 1

7 Detailed Description

7.1 Overview

The DS90UB934-Q1 FPD-Link III deserializer, in conjunction with the DS90UB913A/933-Q1 serializers, supports the video transport needs with a ultra-high-speed forward channel and an embedded bidirectional control channel. The DS90UB934-Q1 deserializer selects data streams from dual camera sources and outputs the recovered data onto a parallel LVCMOS output data bus. The DS90UB934-Q1 is designed to interface with the DS90UB933-Q1 device and is backwards compatible with the DS90UB913A-Q1 device using a 50-Ω coax interface. The DS90UB934-Q1 also works with the DS90UB933-Q1 or DS90UB913A-Q1 using an STP interface. The DS90UB933/934 FPD-link III chipsets are intended to link mega-pixel camera imagers and video processors in ECUs. The serializer/deserializer chipset can operate from 25-MHz to 100-MHz pixel clock frequency.

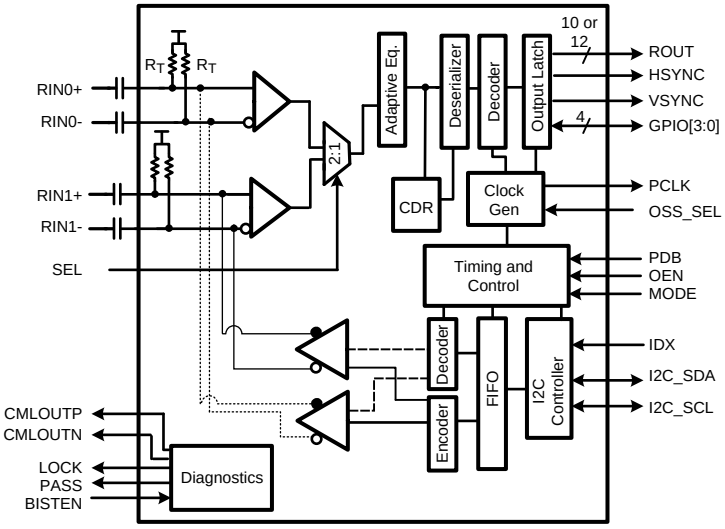
7.1.1 Functional Description

The DS90UB934-Q1 converts the FPD-Link III stream into a parallel CMOS output interface designed to support automotive image sensors up to 12 bits at 100 MHz with resolutions including 1MP/60fps and 2MP/30fps. The DS90UB934-Q1 device recovers a high-speed FPD-Link III forward channel signal and outputs a 10- or 12-bit wide parallel LVCMOS data bus along with generating a bidirectional control channel control signal in the reverse channel direction. The high-speed, serial-bit stream contains an embedded clock and DC-balanced information which enhances signal quality to support AC coupling. The DS90UB934 deserializer can accept up to:

- 12 bits of DATA + 2 SYNC bits for an input PCLK range of 37.5 MHz to 100 MHz in the 12-bit high frequency mode. Note: No HS/VS restrictions (raw).
- 10 bits of DATA + 2 SYNC bits for an input PCLK range of 50 MHz to 100 MHz in the 10-bit mode. Note: HS/VS restricted to no more than one transition per 10 PCLK cycles.
- 12 bits of DATA + 2 bits SYNC for an input PCLK range of 25 MHz to 50 MHz in the 12-bit low frequency mode. Note: No HS/VS restrictions (raw).

The DS90UB934-Q1 device has a 2:1 multiplexer, which allows customers to select between two serializer inputs. The control channel function of the DS90UB933/DS90UB934-Q1 chipset provides bidirectional communication between the image sensor and ECUs. The integrated bidirectional control channel transfers data bidirectionally over the same channel used for video data interface. This interface offers advantages over other chipsets by eliminating the need for additional wires for programming and control. The bidirectional control channel bus is controlled via an I2C port. The bidirectional control channel offers asymmetrical communication and is not dependent on video blanking intervals. The DS90UB933/934 chipset offer customers the choice to work with different clocking schemes. The DS90UB933/934 chipsets can use an external oscillator as the reference clock source for the PLL or PCLK from the imager as primary reference clock to the PLL (see the *DS90UB933-Q1 data sheet*).

7.2 Functional Block Diagram



7.3 Feature Description

The DS90UB934-Q1 device has a 2:1 multiplexer that allows customers to select between two serializer inputs for camera applications. Frequency range operates up to 100 MHz in 12-bit mode or in 10-bit mode to support 1MP/60fps and 2MP/30fps imagers. The device accepts FPD-Link III inputs compatible to DS90UB933/913A serializers. The received camera data stream from the selected input port is output onto the parallel interface.

7.3.1 Serial Frame Format

The high-speed forward channel is composed of 28 bits of data containing video data, sync signals, I2C, and parity bits. This data payload is optimized for signal transmission over an AC-coupled link. Data is randomized, DC-balanced, and scrambled. The 28-bit frame structure changes in the 12-bit, low-frequency mode, 12-bit, high-frequency mode and the 10-bit mode internally and is seamless to the customer. The bidirectional control channel data is transferred over the single serial link along with the high-speed forward data. This architecture provides a full duplex low-speed forward and backward path across the serial link together with a high-speed forward channel without the dependence on the video blanking phase.

7.3.2 Line Rate Calculations for the DS90UB933/934

The DS90UB933-Q1 device divides the clock internally by divide-by-1 in the 12-bit low-frequency mode, by divide-by-2 in the 10-bit mode, and by divide-by-1.5 in the 12-bit high-frequency mode. Conversely, the DS90UB934-Q1 multiplies the recovered serial clock to generate the proper pixel clock output frequency. Thus the maximum line rate in the three different modes remains 1.867 Gbps. The following are the formulae used to calculate the maximum line rate in the different modes:

- For the 12-bit mode: Line rate = f_{PCLK} × (2/3) × 28; for example, fPCLK = 100 MHz, line rate = (100 MHz) × (2/3) × 28 = 1.87 Gbps
- For the 10-bit mode: Line rate = f_{PCLK} / 2 × 28; for example, fPCLK = 100 MHz, line rate = (100 MHz/2) × 28 = 1.4 Gbps

7.3.3 Deserializer Multiplexer Input

The DS90UB934-Q1 offers a 2:1 multiplexer that can be used to select which camera is used as the input. Figure 12 shows the operation of the 2:1 multiplexer in the deserializer. The selection of the camera can be pin controlled as well as register controlled. Only one deserializer input can be selected at a time. If the serializer A is selected as the active serializer, the back-channel for deserializer A turns ON and vice versa. To switch between the two cameras, first the serializer B must be selected using the SEL pin/register on the deserializer. After that the back channel driver for deserializer B has to be enabled using the register in the deserializer.

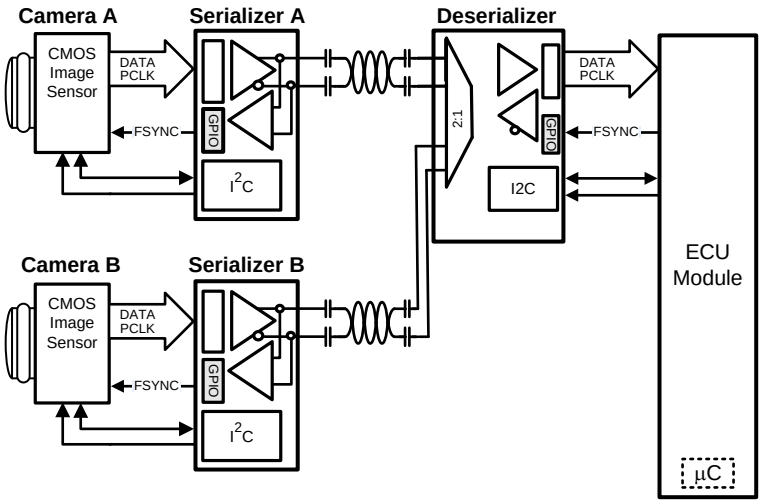


Figure 12. Using the Multiplexer on the Deserializer to Enable a Two-Camera System

7.4 Device Functional Modes

DS90UB934-Q1 supports the use cases shown in Table 1:

Table 1. PCLK Frequency Modes

DS90UB934-Q1 DEVICE MODE	PCLK FREQUENCY RANGE	
	DS90UB913A-Q1 PARTNER	DS90UB933-Q1 PARTNER
RAW12 High-Frequency (HF)	37.5 MHz - 75 MHz	37.5 MHz - 100 MHz
RAW12 Low-Frequency (LF)	25 MHz - 50 MHz	N/A
RAW10	50 MHz - 100 MHz	50 MHz - 100 MHz

The modes control the FPD-Link III receiver operation of the device. In each of the cases, the output format for the device is parallel.

The input mode of operation is controlled by the FPD3_MODE (Register 0x6D[1:0]) setting in the Port Configuration register. The input mode may also be controlled by the MODE strap pin.

7.4.1 RX MODE Pin

Configuration of the device may be done via the MODE input strap pin, or via the configuration register bits. A pullup resistor and a pulldown resistor of suggested values may be used to set the voltage ratio of the MODE input (V_{TARGET}) and $V_{(VDD18)}$ (pin 17) to select one of the 6 possible selected modes. Possible configurations are:

- FPD-Link III coax or STP
- 12-bit HF / 12-bit LF / 10-bit DVP modes

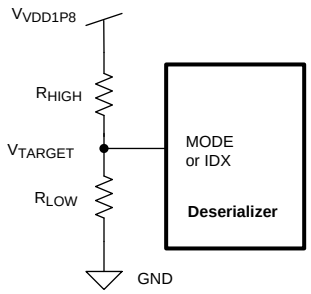


Figure 13. Strap Pin Connection Diagram

Table 2. Strap Configuration Mode Select

MODE NO.	V_{TARGET} VOLTAGE RANGE			V_{TARGET} STRAP VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		COAX /STP	RX MODE
	V_{MIN}	V_{TYP}	V_{MAX}	(V); $V_{(VDD18)}$ = 1.8 V	R_{HIGH} (kΩ)	R_{LOW} (kΩ)		
0	RESERVED							
1	0.179 × $V_{(VDD18)}$	0.213 × $V_{(VDD18)}$	0.247 × $V_{(VDD18)}$	0.374	88.7	23.2	STP	RAW12 LF
2	0.296 × $V_{(VDD18)}$	0.330 × $V_{(VDD18)}$	0.362 × $V_{(VDD18)}$	0.582	75	35.7	STP	RAW12 HF
3	0.412 × $V_{(VDD18)}$	0.443 × $V_{(VDD18)}$	0.474 × $V_{(VDD18)}$	0.792	71.5	56.2	STP	RAW10
4	RESERVED							
5	0.642 × $V_{(VDD18)}$	0.673 × $V_{(VDD18)}$	0.704 × $V_{(VDD18)}$	1.202	39.2	78.7	COAX	RAW12 LF
6	0.761 × $V_{(VDD18)}$	0.792 × $V_{(VDD18)}$	0.823 × $V_{(VDD18)}$	1.42	25.5	95.3	COAX	RAW12 HF
7	0.876 × $V_{(VDD18)}$	$V_{(VDD18)}$	$V_{(VDD18)}$	1.8	10	OPEN	COAX	RAW10

The strapped values can be viewed and/or modified in the following locations:

- Coax – Port configuration COAX_MODE (Register 0x6D[2])
- RX mode – Port configuration FPD3_MODE (Register 0x6D[1:0])

7.4.2 DVP Output Control

The LVCMOS outputs are controlled via the OEN and OSS_SEL pins or via register override of these values. Register override is controlled by bits in the General Configuration register (0x02).

Table 3. Output States

INPUTS				OUTPUTS			
SERIAL INPUTS	PDB	OEN	OSS_SEL	LOCK	PASS	DATA	PCLK
X	0	X	X	Z	Z	Z	Z
X	1	0	0	L	L	L	L
X	1	0	1	Z	Z	Z	Z
static	1	1	0	L	L	L	L
static	1	1	1	L	previous state	L	L
active	1	1	0	H	L	L	L
active	1	1	1	H	valid	valid	valid

7.4.2.1 LOCK Status

In 12-bit HF mode, the LOCK pin is only high if there is a link with a serializer that has an active PCLK input. LOCK is low if there is a serializer connected and there is a link established using the internal oscillator of the serializer. Therefore, when using this mode, it is preferred to use the port specific LOCK_STS register (0x4D[0]), which is high when linked to a serializer with internal oscillator. This LOCK_STS signal can also be output to a GPIO pin for monitoring in real time. Once LOCK_STS is high for a specific port, remote I2C is available to that serializer.

In 12-bit LF or 10-bit modes, the LOCK pin is high when there is a link with a serializer regardless of whether there is an active PCLK input. The port specific LOCK_STS register is also valid in either of these modes.

7.4.3 Input Jitter Tolerance

Input jitter tolerance is the ability of the CDR PLL of the receiver to track and recover the incoming serial data stream. Jitter tolerance at a specific frequency is the maximum jitter permissible before data errors occur. Figure 14 and Table 4 show the allowable total jitter of the receiver inputs and must be less than the values in Table 4.

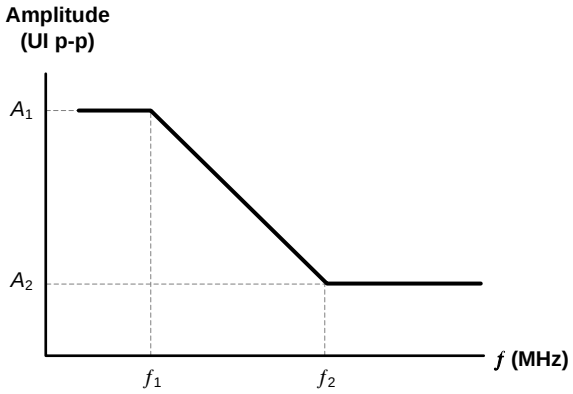


Figure 14. Input Jitter Tolerance Plot

Table 4. Input Jitter Tolerance Limit

INTERFACE	JITTER AMPLITUDE (UI p-p)		FREQUENCY (MHz) (1)	
FPD3	A1	A2	*f*1	*f*2
	1	0.4	FPD3_PCLK / 80	FPD3_PCLK / 15

(1) FPD3_PCLK is equivalent to PCLK frequency based on the operating MODE:
10-bit mode: PCLK_Freq. /2
12-bit HF mode: PCLK_Freq. x 2/3
12-bit LF mode: PCLK_Freq.

7.4.4 Adaptive Equalizer

The receiver inputs provide an adaptive equalization filter in order to compensate for signal degradation from the interconnect components. In order to determine the maximum cable reach, factors that affect signal integrity such as jitter, skew, ISI, crosstalk, etc. must be taken into consideration. The receiver incorporates an adaptive equalizer (AEQ), which continuously monitors cable characteristics for long-term cable aging and temperature changes. The AEQ attempts to optimize the equalization setting of the RX receiver.

If the deserializer loses LOCK, the adaptive equalizer resets and performs the LOCK algorithm again to reacquire the serial data stream being sent by the serializer.

7.4.5 Channel Monitor Loop-Through Output Driver

The DS90UB934-Q1 includes an internal *c*hannel *m*onitor *l*oop-through output on the CMLOUTP/N pins. A buffered loop-through output driver is provided on the CMLOUTP/N for observing jitter after equalization for each of the two RX receive channels. The CMLOUT monitors the post EQ stage, thus providing the recovered input of the deserializer signal. The measured serial data width on the CMLOUT loop-through is the total jitter including the internal driver, AEQ, back channel echo, etc. Each channel also has its own CMLOUT monitor and can be used for debug purposes. This CMLOUT is useful in identifying gross signal conditioning issues. The intrinsic jitter, J_{CML}, represents the amount of jitter seen with a clean serial stream applied to the FPD-Link III input pins. When the total jitter is measured on CMLOUTP and CMLOUTN, the typical intrinsic jitter value can be subtracted to get an approximation of how much jitter is seen at the RIN[1:0]± input pins.

Table 6 includes details on selecting the corresponding RX receiver of CMLOUTP/N configuration.

Table 5. CML Monitor Output Driver

PARAMETER		TEST CONDITIONS	PIN	MIN	TYP	MAX	UNIT
J_{CML}	CMLOUT Differential Output Intrinsic Jitter	Clean clock fed into FPD-Link III input R_L = 100 Ω (Figure 15)	CMLOUTP, CMLOUTN		0.15		UI(1)

(1) UI – Unit interval is equivalent to one ideal serialized data bit width. The UI scales with serializer input PCLK frequency.
10-bit mode: 1 UI = 1 / (PCLK_Freq. /2 x 28)
12-bit HF mode: 1 UI = 1 / (PCLK_Freq. x 2/3 x 28)
12-bit LF mode: 1 UI = 1 / (PCLK_Freq. x 28)

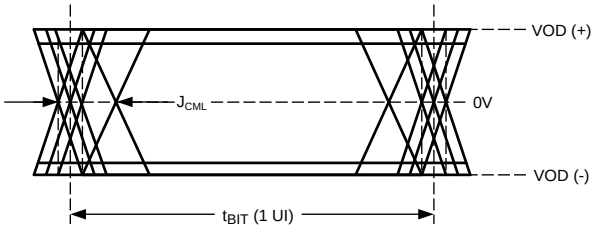


Figure 15. CMLOUT Output Driver

Table 6. Channel Monitor Loop-Through Output Configuration

	FPD3 RX Port 0	FPD3 RX Port 1
ENABLE MAIN LOOPTHRU DRIVER	0xB0 = 0x14 0xB1 = 0x00 0xB2 = 0x80	0xB0 = 0x14 0xB1 = 0x00 0xB2 = 0x80
SELECT CHANNEL MUX	0xB1 = 0x02 0xB2 = 0x20 0xB1 = 0x03 0xB2 = 0x28 0xB1 = 0x04 0xB2 = 0x28	0xB1 = 0x02 0xB2 = 0xA0 0xB1 = 0x03 0xB2 = 0x28 0xB1 = 0x04 0xB2 = 0x28
SELECT RX PORT	0xB0 = 0x18 0xB1 = 0x0F 0xB2 = 0x01 0xB1 = 0x10 0xB2 = 0x02	0xB0 = 0x18 0xB1 = 0x0F 0xB2 = 0x01 0xB1 = 0x10 0xB2 = 0x02

7.4.5.1 Code Example for CMLOUT FPD3 RX Port 0:

```
board.WriteReg(0xB0,0x14)
board.WriteReg(0xB1,0x00)
board.WriteReg(0xB2,0x80)
board.WriteReg(0xB1,0x02)
board.WriteReg(0xB2,0x20)
board.WriteReg(0xB1,0x03)
board.WriteReg(0xB2,0x28)
board.WriteReg(0xB1,0x04)
board.WriteReg(0xB2,0x28)
board.WriteReg(0xB0,0x18)
board.WriteReg(0xB1,0x0F)
board.WriteReg(0xB2,0x01)
board.WriteReg(0xB1,0x10)
board.WriteReg(0xB2,0x02)
```

7.4.6 GPIO Support

The DS90UB934-Q1 supports 4 pins programmable for use in multiple options through the GPIOx_PIN_CTL registers.

7.4.6.1 Back Channel GPIO

The DS90UB934-Q1 can input data on the GPIO pins to send on the back channel to remote serializers. Each GPIO pin can be programmed for input mode. In addition, the back channel for each FPD3 port can be programmed to send any of the 4 GPIO pins data. The same GPIO pin can be connected to multiple back channel GPIO signals.

In addition to sending GPIO from pins, an internally generated frame synchronization signal (FrameSync) signal may be sent on any of the back-channel GPIOs.

For each port, the following GPIO control is available through the BC_GPIO_CTL0 register 0x6E and BC_GPIO_CTL1 register 0x6F.

7.4.6.2 GPIO Pin Status

GPIO pin status may be read through the GPIO_PIN_STS register 0x0E. This register provides the status of the GPIO pin independent of whether the GPIO pin is configured as an input or output.

7.4.6.3 Other GPIO Pin Controls

Each GPIO pin has a input disable and a pulldown disable. By default, the GPIO pin input paths are enabled and the internal pulldown circuit in the GPIO is enabled. The GPIO_INPUT_CTL register 0x0F and GPIO_PD_CTL register 0xBE allow control of the input enable and the pulldown respectively. For most applications, there is no need to modify the default register settings.

7.4.6.4 FrameSync Operation

A FrameSync signal can be sent via the back channel using any of the back channel GPIOs. The signal can be generated in two different methods. The first option offers sending the external FrameSync using one of the available GPIO pins on the DS90UB934-Q1 and mapping that GPIO to a back channel GPIO on one of the FPD-Link III ports.

The second option is to have the DS90UB934-Q1 internally generate a FrameSync signal to send via GPIO to one of the attached serializers.

7.4.6.4.1 External FrameSync Control

In external FrameSync mode, an external signal is input to the DS90UB934-Q1 via one of the GPIO pins on the device. The external FrameSync signal may be propagated to either of the attached FPD3 serializers via a GPIO signal in the back channel.

Enabling the external FrameSync mode is done by setting the FS_MODE control in the FS_CTL (0x18) register to a value between 0x8 (GPIO0 pin) to 0xB (GPIO3 pin). Set FS_GEN_ENABLE to 0 for this mode.

To send the FrameSync signal on the BC_GPIOx signal of a port, the BC_GPIO_CTL0 or BC_GPIO_CTL1 register must be programmed for that port to select the FrameSync signal.

7.4.6.4.2 Internally Generated FrameSync

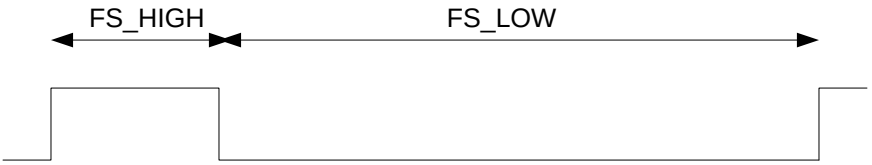
In internal FrameSync mode, an internally generated FrameSync signal is sent to one or more of the attached FPD3 serializers via a GPIO signal in the back channel.

FrameSync operation is controlled by the FS_CTL 0x18, FS_HIGH_TIME_x, and FS_LOW_TIME_x 0x19–0x1A registers. The resolution of the FrameSync generator clock (FS_CLK_PD) is derived from the back channel frame period (BC_FREQ_SELECT register). For 2.5-Mbps back-channel operation, the frame period is 12 µs (30 bits × 400 ns/bit).

Once enabled, the FrameSync signal is sent continuously based on the programmed conditions.

Enabling the internal FrameSync mode is done by setting the FS_GEN_ENABLE control in the FS_CTL (0x18) register to a value of 1. The FS_MODE field controls the clock source used for the FrameSync generation. The FS_GEN_MODE field configures whether the duty cycle of the FrameSync is 50/50 or whether the high and low periods are controlled separately. The FrameSync high and low periods are controlled by the FS_HIGH_TIME and FS_LOW_TIME registers.

The accuracy of the internally generated FrameSync is directly dependent on the accuracy of the internal oscillator used to generate the back-channel reference clock. The internal oscillator has ±5% variation over process, voltage, and temperature.



FS_LOW = FS_LOW_TIME * FS_CLK_PD
FS_HIGH = FS_HIGH_TIME * FS_CLK_PD
where FS_CLK_PD is the resolution of the FrameSync generator clock

Figure 16. Internal FrameSync Signal

The following example shows generation of a FrameSync signal at 60 pulses per second. Mode settings:

- Programmable high/low periods: FS_GEN_MODE 0x18[1]=0
- Use port 0 back channel frame period: FS_MODE 0x18[7:4]=0x0
- Back channel rate of 2.5 Mbps: BC_FREQ_SELECT for port 0 0x58[2:0]=0x0
- Initial FS state of 0: FS_INIT_STATE 0x18[2]=0

Based on mode settings, the FrameSync is generated based upon FS_CLK_PD of 12 μs.

The total period of the FrameSync is (1 sec / 60 Hz) / 12 μs or approximately 1,389 counts.

For a 10% duty cycle, set the high time to 139 (0x008A) cycles, and the low time to 1,250 (0x04E1) cycles:

- FS_HIGH_TIME_1: 0x19 = 0x00
- FS_HIGH_TIME_0: 0x1A = 0x8A
- FS_LOW_TIME_1: 0x1B = 0x04
- FS_LOW_TIME_0: 0x1C = 0xE1

7.4.6.4.2.1 Code Example for Internally Generated FrameSync

```
WriteI2C(0x4C,0x01) # RX0
WriteI2C(0x6E,0xAA) # BC_GPIO_CTL0: FrameSync signal to GPIO0/1
WriteI2C(0x4C,0x12) # RX1
WriteI2C(0x6E,0xAA) # BC_GPIO_CTL0: FrameSync signal to GPIO0/1
WriteI2C(0x10,0x91) # FrameSync signal; Device Status; Enabled
WriteI2C(0x58,0x58) # BC FREQ SELECT: 2.5 Mbps
WriteI2C(0x19,0x00) # FS_HIGH_TIME_1
WriteI2C(0x1A,0x8A) # FS_HIGH_TIME_0
WriteI2C(0x1B,0x04) # FS_LOW_TIME_1
WriteI2C(0x1C,0xE1) # FS_LOW_TIME_0
WriteI2C(0x18,0x01) # Enable FrameSync
```

7.5 Programming

7.5.1 Serial Control Bus

The DS90UB934-Q1 implements an I2C-compatible serial control bus. The I2C is for local device configuration and incorporates a bidirectional control channel (BCC) that allows communication with a remote serializers as well as remote I2C slave devices.

The device address is set via a resistor divider (R_{HIGH} and R_{LOW} — see Figure 17) connected to the IDX pin.

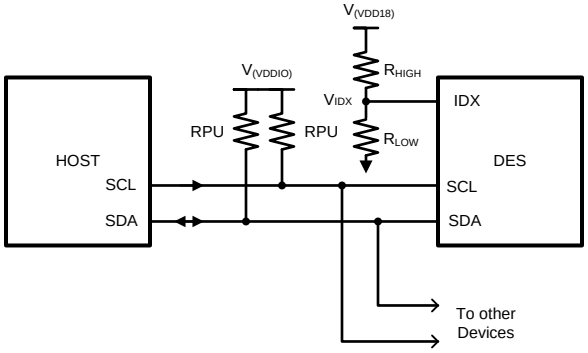


Figure 17. Serial Control Bus Connection

The serial control bus consists of two signals, SCL and SDA. SCL is a serial bus clock input. SDA is the serial bus data input/output signal. Both SCL and SDA signals require an external pullup resistor to 1.8-V or 3.3-V $V_{(VDDIO)}$. For most applications, TI recommends a 4.7-kΩ pullup resistor to $V_{(VDDIO)}$. However, the pullup resistor value may be adjusted for capacitive loading and data rate requirements. The signals are either pulled high or driven low.

The IDX pin configures the control interface to one of 8 possible device addresses. A pullup resistor and a pulldown resistor may be used to set the appropriate voltage ratio between the IDX input pin ($V_{(IDX)}$) and $V_{(VDDIO)}$, each ratio corresponding to a specific device address (see Table 7).

Table 7. Serial Control Bus Addresses for IDX

	V_{IDX} VOLTAGE RANGE			V_{IDX} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		ASSIGNED I2C ADDRESS	
NO.	V_{MIN}	V_{TYP}	V_{MAX}	(V); $V_{(VDD18)}$ = 1.8 V	R_{HIGH} (kΩ)	R_{LOW} (kΩ)	7-BIT	8-BIT
0	0	0	0.131 × $V_{(VDD18)}$	0	OPEN	10.0	0x30	0x60
1	0.179 × $V_{(VDD18)}$	0.213 × $V_{(VDD18)}$	0.247 × $V_{(VDD18)}$	0.374	88.7	23.2	0x32	0x64
2	0.296 × $V_{(VDD18)}$	0.330 × $V_{(VDD18)}$	0.362 × $V_{(VDD18)}$	0.582	75.0	35.7	0x34	0x68
3	0.412 × $V_{(VDD18)}$	0.443 × $V_{(VDD18)}$	0.474 × $V_{(VDD18)}$	0.792	71.5	56.2	0x36	0x6C
4	0.525 × $V_{(VDD18)}$	0.559 × $V_{(VDD18)}$	0.592 × $V_{(VDD18)}$	0.995	78.7	97.6	0x38	0x70
5	0.642 × $V_{(VDD18)}$	0.673 × $V_{(VDD18)}$	0.704 × $V_{(VDD18)}$	1.202	39.2	78.7	0x3A	0x74
6	0.761 × $V_{(VDD18)}$	0.792 × $V_{(VDD18)}$	0.823 × $V_{(VDD18)}$	1.420	25.5	95.3	0x3C	0x78
7	0.876 × $V_{(VDD18)}$	$V_{(VDD18)}$	$V_{(VDD18)}$	1.8	10	OPEN	0x3D	0x7A

The serial bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SDA transitions low while SCL is high. A STOP occurs when SDA transitions high while SCL is also high. See Figure 18.

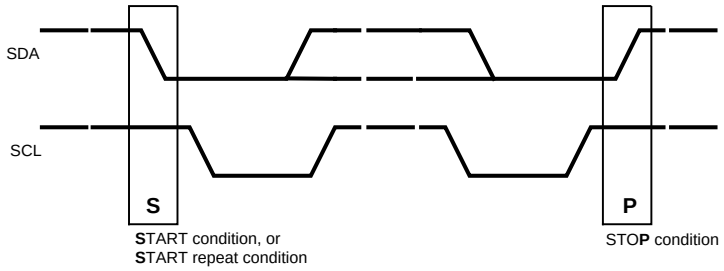


Figure 18. START and STOP Conditions

To communicate with a remote device, the host controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit (ACK). If a slave on the bus is addressed correctly, it acknowledges (ACKs) the master by driving the SDA bus low. If the address does not match the slave address of a device, it not-acknowledges (NACKs) the master by letting SDA be pulled High. ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know it wants to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a START condition or a REPEATED-START condition. All communication on the bus ends with a STOP condition. A READ is shown in Figure 19 and a WRITE is shown in Figure 20.

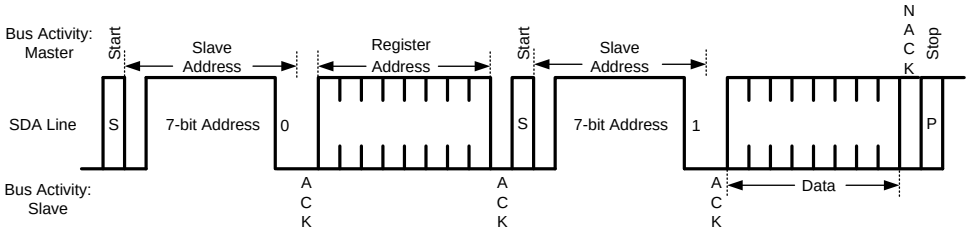


Figure 19. Serial Control Bus — READ

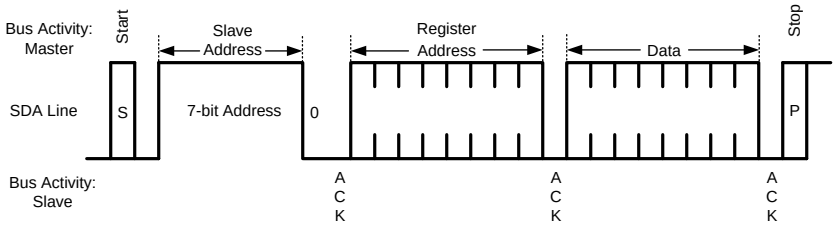


Figure 20. Serial Control Bus — WRITE

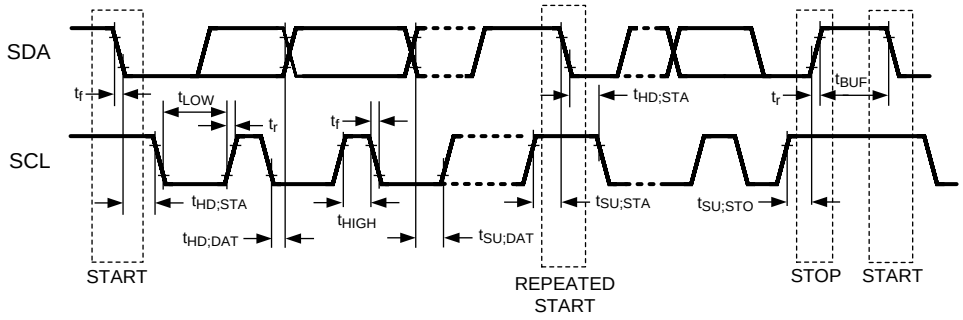


Figure 21. Basic Operation

The I2C master located at the deserializer must support I2C clock stretching. For more information on I2C interface requirements and throughput considerations, refer to *AN-2173 I2C Communication Over FPD-Link III with Bidirectional Control Channel*.

7.5.2 Interrupt Support

Interrupts can be brought out on the INTB pin as controlled by the INTERRUPT_CTL 0x23 and INTERRUPT_STS 0x24 registers. The main interrupt control registers provide control and status for interrupts from each of the two FPD3 receive ports. Clearing interrupt conditions requires reading the associated status register for the source. The setting of the individual interrupt status bits is not dependent on the related interrupt enable controls. The interrupt enable controls whether an interrupt is generated based on the condition, but does not prevent the interrupt status assertion.

For an interrupt to be generated based on one of the interrupt status assertions, both the individual interrupt enable and the INT_EN control must be set in the INTERRUPT_CTL 0x23 register. For example, to generate an interrupt if IS_RX0 is set, both the IE_RX0 and INT_EN bits must be set. If IE_RX0 is set but INT_EN is not, the INT status is indicated in the INTERRUPT_STS register, and the INTB pin does not indicate the interrupt condition.

See INTERRUPT_CTL 0x23 and INTERRUPT_STS 0x24 in Table 9 for details.

7.5.2.1 Code Example to Enable Interrupts

```
# RX0/1 INTERRUPT_CTL enable
# "RX0 INTERRUPT_CTL enable"
WriteI2C(0x4C,0x01) # RX0
WriteI2C(0x23,0x81) # RX0 & INTB PIN EN

# "RX1 INTERRUPT_CTL enable"
WriteI2C(0x4C,0x12) # RX1
WriteI2C(0x23,0x82) # RX1 & INTB PIN EN
```

7.5.2.2 FPD-Link III Receive Port Interrupts

For each FPD-Link III receive port, multiple options are available for generating interrupts. Interrupt generation is controlled via the PORT_ICR_HI 0xD8 and PORT_ICR_LO 0xD9 registers. In addition, the PORT_ISR_HI 0xDA and PORT_ISR_LO 0xDB registers provide read-only status for the interrupts. Clearing of interrupt conditions is handled by reading the RX_PORT_STS and RX_PORT_STS2 registers. The status bits in the PORT_ISR_HI/LO registers are copies of the associated bits in the main status registers.

To enable interrupts from one of the receive port interrupt sources:

1. Enable the interrupt source by setting the appropriate interrupt enable bit in the PORT_ICR_HI or PORT_ICR_LO register
2. Set the RX port X Interrupt control bit (IE_RXx) in the INTERRUPT_CTL register
3. Set the INT_EN bit in the INTERRUPT_CTL register to allow the interrupt to assert the INTB pin low

To clear interrupts from one of the receive port interrupt sources:

1. (optional) Read the INTERRUPT_STS register to determine which RX port caused the interrupt
2. (optional) Read the PORT_ISR_HI and PORT_ISR_LO registers to determine source of interrupt
3. Read the appropriate RX_PORT_STS1, RX_PORT_STS2 register to clear the interrupt.

The first two steps are optional. The interrupt could be determined and cleared by just reading the status registers.

7.5.2.3 Code Example to Readback Interrupts

```
INTERRUPT_STS = ReadI2C(0x24) # 0x24 INTERRUPT_STS


if ((INTERRUPT_STS & 0x80) >> 7):
    print "# GLOBAL INTERRUPT DETECTED "
if ((INTERRUPT_STS & 0x02) >> 1):
    print "# IS_RX1 DETECTED "
if ((INTERRUPT_STS & 0x01) ):
    print "# IS_RX0 DETECTED "

# "################################################"
#  "RX0 status"
# "################################################"

WriteReg(0x4C,0x01) # RX0
PORT_ISR_LO = ReadI2C(0xDB)

print "0xDB PORT_ISR_LO : ", hex(PORT_ISR_LO) # readout; cleared by RX_PORT_STS2

if ((PORT_ISR_LO & 0x04) >> 2):
    print "# IS_FPD3_PAR_ERR DETECTED "
if ((PORT_ISR_LO & 0x02) >> 1):
    print "# IS_PORT_PASS DETECTED "
if ((PORT_ISR_LO & 0x01) ) :
    print "# IS_LOCK_STS DETECTED "

################################################

PORT_ISR_HI = ReadI2C(0xDA)

print "0xDA PORT_ISR_HI : ", hex(PORT_ISR_HI) # readout; cleared by RX_PORT_STS2

if ((PORT_ISR_HI & 0x04) >> 2):
    print "# IS_FPD3_ENC_ERR DETECTED "
if ((PORT_ISR_HI & 0x02) >> 1):
    print "# IS_BCC_SEQ_ERR DETECTED "
if ((PORT_ISR_HI & 0x01) ) :
    print "# IS_BCC_CRC_ERR DETECTED "

################################################

RX_PORT_STS1 = ReadI2C(0x4D) # R/COR

elif ((RX_PORT_STS1 & 0xc0) >> 6) == 1:
    print "# RX_PORT_NUM = RX1"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 0:
    print "# RX_PORT_NUM = RX0"

if ((RX_PORT_STS1 & 0x20) >> 5):
    print "# BCC_CRC_ERR DETECTED "
if ((RX_PORT_STS1 & 0x10) >> 4):
    print "# LOCK_STS_CHG DETECTED "
if ((RX_PORT_STS1 & 0x08) >> 3):
    print "# BCC_SEQ_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x04) >> 2):
    print "# PARITY_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x02) >> 1):
    print "# PORT_PASS=1 "
if ((RX_PORT_STS1 & 0x01) ):
    print "# LOCK_STS=1 "

################################################
```

```
RX_PORT_STS2 = ReadI2C(0x4E)

if ((RX_PORT_STS2 & 0x20) >> 5):
    print "# FPD3_ENCODE_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x04) >> 2):
    print "# FREQ_STABLE DETECTED "
if ((RX_PORT_STS2 & 0x02) >> 1):
    print "# NO_FPD3_CLK DETECTED "

################################################

# "################################################"
#  "RX1 status"
# "################################################"


WriteReg(0x4C,0x12) # RX1
PORT_ISR_LO = ReadI2C(0xDB) # PORT_ISR_LO readout; cleared by RX_PORT_STS2

if ((PORT_ISR_LO & 0x04) >> 2):
    print "# IS_FPD3_PAR_ERR DETECTED "
if ((PORT_ISR_LO & 0x02) >> 1):
    print "# IS_PORT_PASS DETECTED "
if ((PORT_ISR_LO & 0x01) ) :
    print "# IS_LOCK_STS DETECTED "

################################################

PORT_ISR_HI = ReadI2C(0xDA) # readout; cleared by RX_PORT_STS2

if ((PORT_ISR_HI & 0x04) >> 2):
    print "# IS_FPD3_ENC_ERR DETECTED "
if ((PORT_ISR_HI & 0x02) >> 1):
    print "# IS_BCC_SEQ_ERR DETECTED "
if ((PORT_ISR_HI & 0x01) ) :
    print "# IS_BCC_CRC_ERR DETECTED "

################################################

RX_PORT_STS1 = ReadI2C(0x4D) # R/COR

elif ((RX_PORT_STS1 & 0xc0) >> 6) == 1:
    print "# RX_PORT_NUM = RX1"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 0:
    print "# RX_PORT_NUM = RX0"

if ((RX_PORT_STS1 & 0x20) >> 5):
    print "# BCC_CRC_ERR DETECTED "
if ((RX_PORT_STS1 & 0x10) >> 4):
    print "# LOCK_STS_CHG DETECTED "
if ((RX_PORT_STS1 & 0x08) >> 3):
    print "# BCC_SEQ_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x04) >> 2):
    print "# PARITY_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x02) >> 1):
    print "# PORT_PASS=1 "
if ((RX_PORT_STS1 & 0x01) ):
    print "# LOCK_STS=1 "

################################################

RX_PORT_STS2 = ReadI2C(0x4E)

if ((RX_PORT_STS2 & 0x20) >> 5):
    print "# FPD3_ENCODE_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x04) >> 2):
    print "# FREQ_STABLE DETECTED "
if ((RX_PORT_STS2 & 0x02) >> 1):
    print "# NO_FPD3_CLK DETECTED "


################################################
```

7.5.2.4 Built-In Self Test (BIST)

An optional at-speed BIST feature supports testing of the high-speed serial link and the back channel without external data connections. This is useful in the prototype stage, equipment production, in-system test, and system diagnostics.

7.5.2.4.1 BIST Configuration and Status

The BIST mode is enabled by BIST configuration register 0xB3. The test may select either an external PCLK or the internal oscillator clock (OSC) frequency in the serializer. In the absence of PCLK, the user can select the internal OSC frequency at the deserializer through the BIST configuration register. When BIST is activated at the deserializer, a BIST enable signal is sent to the serializer through the back channel. The serializer outputs a continuous stream of a pseudo-random sequence and drives the link at speed. The deserializer detects the test pattern and monitors it for errors. The serializer also tracks errors indicated by the CRC fields in each back channel frame. While the lock indications are required to identify the beginning of proper data reception, for any link failures or data corruption, the best indication is the contents of the error counter in the BIST_ERR_COUNT register 0x57 for each RX port.

The clock frequency that is output onto the PCLK pin during BIST mode is based on an internal FPD-Link III clock, and may not match the expected PCLK coming from the serializer.

7.6 Register Maps

7.6.1 Register Description

The DS90UB934-Q1 implements the following register blocks, accessible via I2C as well as the bi-directional control channel:

- Main registers
- FPD3 RX port registers (separate register block for each of the two RX ports)
- DVP port registers

Table 8. Main Register Map Descriptions

ADDRESS RANGE	DESCRIPTION	ADDRESS MAP	
0x00-0x31	Digital Shared registers	Shared	
0x32-0x3A	Reserved	Reserved	
0x3B-0x3F	Digital DVP registers	Shared	
0x4C-0x7F	Digital RX Port registers (paged)	FPD3 RX Port 0 *R: 0x4C[5:4]=00* *W: 0x4C[0]=1*	FPD3 RX Port 1 *R: 0x4C[5:4]=01* *W: 0x4C[1]=1*
0x80-0xAF	Reserved	Reserved	
0xB0-0xB2	Indirect Access registers	Shared	
0xB0-0xBF	Digital Share registers	Shared	
0xC0-0xCF	Reserved	Reserved	
0xD0-0xDF	Digital RX Port Debug registers	FPD3 RX Port 0	FPD3 RX Port 1
0xE0-0xEF	Reserved	Reserved	
0xF0-0xF5	FPD3 RX ID	Shared	
0xF6-0xF7	Reserved	Reserved	
0xF8-0xFB	Port I2C Addressing	Shared	
0xFC-0xFF	Reserved	Reserved	

In the register definitions under the “TYPE” heading, the following definitions apply::

- RW = Read Write access
- RO = Read Only access
- S = Register set by configuration pin
- SC = Register sets on event occurrence and Self-Clears when event ends
- RO/P = Read Only, permanently set to a default value
- LL = Latched low and held until read, based upon the occurrence of the corresponding event
- LH = Latched high and held until read, based upon the occurrence of the corresponding event

Table 9. Serial Control Bus Registers

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
Share	0x00	I2C Device ID	7:1	DEVICE ID	S, RW	0x3D	7-bit I2C ID of deserializer Defaults to address configured by IDX strap pin. This field always indicates the current value of the I2C ID. When bit 0 of this register is 0, this field is read-only and shows the strapped ID. When bit 1 of this register is 1, this field is read/write and can be used to assign any valid I2C ID.
			0	DES ID	RW	0	0: Device ID is from IDX strap pin 1: Register I2C device ID overrides strapped value
Share	0x01	Reset	7:3	RESERVED	RW	0	Reserved
			2	RESTART_AUTOLOAD	RW,SC	0	Restart ROM auto-load Setting this bit to 1 causes a re-load of the ROM. This bit is self-clearing. Software may check for auto-load complete by checking the CFG_INIT_DONE bit in the DEVICE_STS register.
			1	DIGITAL RESET1	RW,SC	0	Digital reset Resets the entire digital block including registers. This bit is self-clearing. 1: Reset 0: Normal operation
			0	DIGITAL RESET0	RW,SC	0	Digital reset Resets the entire digital block except registers. This bit is self-clearing. 1: Reset 0: Normal operation
Share	0x02	General Configuration	7	INPUT_PORT_OVERRIDE	RW	0	Input port override bit allows control of the input port selection via the INPUT_PORT_SEL bit in this register.
			6	INPUT_PORT_SEL	RW	0	Input port select. This bit either controls the input mode (if INPUT_PORT_OVERRIDE is set) or indicates the status of the SEL pin.
			5	OUTPUT_OVERRIDE	RW	0	Output Control Override bit. The OUTPUT_ENABLE and OUTPUT_SLEEP_STATE_SEL values typically come from the device input pins. If this bit is set, the register values in this register will be used instead.
			4	RESERVED	RW	1	Reserved
			3	OUTPUT_ENABLE	RW	1	Output enable control (in conjunction with output sleep state select) If OUTPUT_SLEEP_STATE_SEL is set to 1 and this bit is set to 0, the TX outputs will be forced into a high impedance state. If OUTPUT_OVERRIDE is 0, this register indicates the value on the OEN pin. See Table 3.
			2	OUTPUT_SLEEP_STATE_SEL	RW	1	OSS Select controls the output state when LOCK is low (used in conjunction with Output Enable) When this bit is set to 0, the TX outputs is forced into a HS-0 state. If OUTPUT_OVERRIDE is 0, this register indicates the value on the OSS_SEL pin. See Table 3.

Table 9. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			1	RX_PARITY_CHECKER_EN	RW	1	FPD3 Receiver Parity Checker Enable When enabled, the parity check function is enabled for the FPD3 receiver. This allows detection of errors on the FPD3 receiver data bits. 0: Disable 1: Enable
			0	Reserved	RW	0	Reserved
Share	0x03	Revision/Mask ID	7:4	REVISION_ID	RO/P	0	Revision ID 0000: Production release
			3:0	RESERVED	RO/P	0	Reserved
Share	0x04	DEVICE_STS	7	CFG_CKSUM_STS	RO	1	Config Checksum passed This bit is set following initialization if the configuration data in the eFuse ROM had a valid checksum
			6	CFG_INIT_DONE	RO	1	Power-up initialization complete This bit is set after Initialization is complete. Configuration from eFuse ROM has completed.
			5:4	RESERVED	RO	0x0	Reserved
			3	PASS	RO, LH	0	Device PASS status This bit indicates the PASS status for the device. The value in this register matches the indication on the PASS pin.
			2	LOCK	RO, LH	0	Device LOCK status This bit indicates the LOCK status for the device. The value in this register matches the indication on the LOCK pin.
			1:0	RESERVED	RO	0x0	Reserved
Share	0x05	PAR_ERR_THOLD_HI	7:0	PAR_ERR_THOLD_HI	RW	0x01	FPD3 parity error threshold high byte This register provides the 8 most significant bits of the parity error threshold value. For each port, if the FPD-Link III receiver detects a number of parity errors greater than or equal to this value, the PARITY_ERROR flag is set in the RX_PORT_STS1 register.
Share	0x06	PAR_ERR_THOLD_LO	7:0	PAR_ERR_THOLD_LO	RW	0	FPD3 parity error threshold low byte This register provides the 8 least significant bits of the parity error threshold value. For each port, if the FPD-Link III receiver detects a number of parity errors greater than or equal to this value, the PARITY_ERROR flag is set in the RX_PORT_STS1 register.
Share	0x07	BCC Watchdog Control	7:1	BCC WATCHDOG TIMER	RW	0x7f	The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the bidirectional control channel watchdog timeout value in units of 2 milliseconds. Do not set his field to 0.
			0	BCC WATCHDOG TIMER DISABLE	RW	0	Disable bidirectional control channel watchdog timer 1: Disables BCC watchdog timer operation 0: Enables BCC watchdog timer operation
Share	0x08	I2C Control 1	7	LOCAL WRITE DISABLE	RW	0	Disable remote writes to local registers Setting this bit to a 1 prevents remote writes to local device registers from across the control channel. This prevents writes to the deserializer registers from an I2C master attached to the serializer. Setting this bit does not affect remote access to I2C slaves at the deserializer.

Table 9. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			6:4	I2C SDA HOLD	RW	0x1	Internal SDA hold time This field configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 50 nanoseconds.
			3:0	I2C FILTER DEPTH	RW	0xC	I2C glitch filter depth This field configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 5 nanoseconds.
Share	0x09	I2C Control 2	7:4	SDA Output Setup	RW	1	Remote Ack SDA output setup When a control channel (remote) access is active, this field configures setup time from the SDA output relative to the rising edge of SCL during ACK cycles. Setting this value will increase setup time in units of 640ns. The nominal output setup time value for SDA to SCL when this field is 0 is 80 ns.
			3:2	SDA Output Delay	RW	0	SDA output delay This field configures additional delay on the SDA output relative to the falling edge of SCL. Setting this value increases output delay in units of 40 ns. Nominal output delay values for SCL to SDA are: 00: 240 ns 01: 280 ns 10: 320 ns 11: 360 ns
			1	I2C BUS TIMER SPEEDUP	RW	0	Speed up I2C bus watchdog timer 1: Watchdog Timer expires after approximately 50 microseconds 0: Watchdog Timer expires after approximately 1 second.
			0	I2C BUS TIMER DISABLE	RW	0	Disable I2C bus watchdog timer When the I2C Watchdog Timer may be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signaling occurs for approximately 1 second, the I2C bus is assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL.
Share	0x0A	SCL High Time	7:0	SCL HIGH TIME	RW	0x7A	I2C Master SCL high time This field configures the high pulse width of the SCL output when the Serializer is the Master on the local I2C bus. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to approximately 100 kHz with the internal oscillator clock running at nominal 25 MHz. Delay includes 4 additional oscillator clock periods. Nominal High Time = 40 ns × (TX_SCL_HIGH + 4) The internal oscillator has ±10% variation which must be taken into account when setting the SCL High and Low Time registers.

Table 9. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
Share	0x0B	SCL Low Time	7:0	SCL LOW TIME	RW	0x7A	I2C SCL low time This field configures the low pulse width of the SCL output when the serializer is the master on the local I2C bus. This value is also used as the SDA setup time by the I2C Slave for providing data prior to releasing SCL during accesses over the Bidirectional control channel. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to approximately 100 kHz with the internal oscillator clock running at nominal 25 MHz. Delay includes 4 additional clock periods. Nominal low time = 40 ns × (TX_SCL_LOW + 4) The internal oscillator has ±10% variation which must be taken into account when setting the SCL High and Low Time registers.
Share	0x0C	RESERVED	7:0	RESERVED	RW	0x0	Reserved
Share	0x0D	IO_CTL	7	SEL3P3V	RW	0	3.3-V I/O Select on pins INTB, I2C 0: 1.8-V I/O Supply 1: 3.3-V I/O Supply If IO_SUPPLY_MODE_OV is 0, a read of this register returns the detected I/O voltage level.
			6	IO_SUPPLY_MODE_OV	RW	0	Override I/O Supply Mode bit If set to 0, the detected voltage level is used for both SEL3P3V and IO_SUPPLY_MODE controls. If set to 1, the values written to the SEL3P3V and IO_SUPPLY_MODE fields is used.
			5:4	IO_SUPPLY_MODE	RW	0x0	I/O supply mode 00: 1.8 V 11: 3.3 V If IO_SUPPLY_MODE_OV is 0, a read of this register returns the detected I/O voltage level.
			3:0	RESERVED	RW	0x9	Reserved
Share	0x0E	GPIO_PIN_STS	7:4	RESERVED	RW	0x0	Reserved
			3:0	GPIO_STS	RO	0x0	GPIO pin status This register reads the current values on each of the 4 GPIO pins. Bit 4 reads GPIO3 and bit 0 reads GPIO0.
Share	0x0F	GPIO_INPUT_CTL	7:4	RESERVED	RW	0x7	Reserved
			3	GPIO3_INPUT_EN	RW	1	GPIO3 input enable 0: Disabled 1: Enabled
			2	GPIO2_INPUT_EN	RW	1	GPIO2 input enable 0: Disabled 1: Enabled
			1	GPIO1_INPUT_EN	RW	1	GPIO1 input enable 0: Disabled 1: Enabled
			0	GPIO0_INPUT_EN	RW	1	GPIO0 input enable 0: Disabled 1: Enabled

Table 9. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
Share	0x10	GPIO0_PIN_CTL	7:5	GPIO0_OUT_SEL	RW	0x0	GPIO0 output select Determines the output data for the selected source. If GPIO0_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000 : Received GPIO0 001 : Received GPIO1 010 : Received GPIO2 011 : Received GPIO3 100 : RX port lock indication 101 : RX port pass indication 110- 111 : Reserved If GPIO0_OUT_SRC is set to 100 (Device Status), the following selections apply: 000 : Value in GPIO0_OUT_VAL 001 : Logical OR of Lock indication from enabled RX ports 010 : Logical AND of Lock indication from enabled RX ports 011 : Logical AND of Pass indication from enabled RX ports 100 : FrameSync signal 101 - 111 : Reserved
			4:2	GPIO0_OUT_SRC	RW	0x0	GPIO0 Output source select Selects output source for GPIO0 data: 000 : RX Port 0 001 : RX Port 1 01x : Reserved 100 : Device status 101 - 111 : Reserved
			1	GPIO0_OUT_VAL	RW	0	GPIO0 output value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
			0	GPIO0_OUT_EN	RW	0	GPIO0 Output Enable 0: Disabled 1: Enabled
Share	0x11	GPIO1_PIN_CTL	7:5	GPIO1_OUT_SEL	RW	0x0	GPIO1 Output Select Determines the output data for the selected source. If GPIO1_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000 : Received GPIO0 001 : Received GPIO1 010 : Received GPIO2 011 : Received GPIO3 100 : RX Port Lock indication 101 : RX Port Pass indication 110- 111 : Reserved If GPIO1_OUT_SRC is set to 100 (Device Status), the following selections apply: 000 : Value in GPIO1_OUT_VAL 001 : Logical OR of Lock indication from enabled RX ports 010 : Logical AND of Lock indication from enabled RX ports 011 : Logical AND of Pass indication from enabled RX ports 100 : FrameSync signal 101 - 111 : Reserved

Table 9. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			4:2	GPIO1_OUT_SRC	RW	0x0	GPIO1 Output Source Select Selects output source for GPIO1 data: 000 : RX port 0 001 : RX port 1 01x : Reserved 100 : Device dtatus 101 - 111 : Reserved
			1	GPIO1_OUT_VAL	RW	0	GPIO1 output value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
			0	GPIO1_OUT_EN	RW	0	GPIO1 output enable 0: Disabled 1: Enabled
Share	0x12	GPIO2_PIN_CTL	7:5	GPIO2_OUT_SEL	RW	0x0	GPIO2 output select Determines the output data for the selected source. If GPIO2_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000 : Received GPIO0 001 : Received GPIO1 010 : Received GPIO2 011 : Received GPIO3 100 : RX port lock indication 101 : RX port pass indication 110- 111 : Reserved If GPIO2_OUT_SRC is set to 100 (Device Status), the following selections apply: 000 : Value in GPIO2_OUT_VAL 001 : Logical OR of Lock indication from enabled RX ports 010 : Logical AND of Lock indication from enabled RX ports 011 : Logical AND of Pass indication from enabled RX ports 100 : FrameSync signal 101 - 111 : Reserved
			4:2	GPIO2_OUT_SRC	RW	0x0	GPIO2 output source select Selects output source for GPIO2 data: 000 : RX port 0 001 : RX port 1 01x : Reserved 100 : Device status 101 - 111 : Reserved
			1	GPIO2_OUT_VAL	RW	0	GPIO2 output value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
			0	GPIO2_OUT_EN	RW	0	GPIO2 output enable 0: Disabled 1: Enabled

Table 9. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
Share	0x13	GPIO3_PIN_CTL	7:5	GPIO3_OUT_SEL	RW	0x0	GPIO3 output select Determines the output data for the selected source. If GPIO3_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000 : Received GPIO0 001 : Received GPIO1 010 : Received GPIO2 011 : Received GPIO3 100 : RX port lock indication 101 : RX port pass indication 110- 111 : Reserved If GPIO2_OUT_SRC is set to 100 (Device Status), the following selections apply: 000 : Value in GPIO3_OUT_VAL 001 : Logical OR of lock indication from enabled RX ports 010 : Logical AND of lock indication from enabled RX ports 011 : Logical AND of pass indication from enabled RX ports 100 : FrameSync signal 101 - 111 : Reserved
			4:2	GPIO3_OUT_SRC	RW	0x0	GPIO3 output source select Selects output source for GPIO3 data: 000 : RX port 0 001 : RX port 1 01x : Reserved 100 : Device Status 101 - 111 : Reserved
			1	GPIO3_OUT_VAL	RW	0	GPIO3 output value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
			0	GPIO3_OUT_EN	RW	0	GPIO3 output enable 0: Disabled 1: Enabled
Share	0x14 - 0x17	RESERVED	7:0	RESERVED	RW	0x0	Reserved
Share	0x18	FS_CTL	7:4	FS_MODE	RW	0	FrameSync mode 0000: Internal generated FrameSync, use back-channel frame clock from port 0 0001: Internal generated FrameSync, use back-channel frame clock from port 1 0010 : Reserved 0011: Reserved 01xx: Internal generated FrameSync, use 25-MHz (typical) clock 1000: External FrameSync from GPIO0 1001: External FrameSync from GPIO1 1010: External FrameSync from GPIO2 1011: External FrameSync from GPIO3 1100 - 1111: Reserved
			3	FS_SINGLE	RW, SC	0	Generate single FrameSync pulse When this bit is set, a single FrameSync pulse is generated. The system waits for the full duration of the desired pulse before generating another pulse. When using this feature, the FS_GEN_ENABLE bit remains set to 0. This bit is self-clearing and always returns to 0.
			2	FS_INIT_STATE	RW	0	Initial State This register controls the initial state of the FrameSync signal. 0: FrameSync initial state is 0 1: FrameSync initial state is 1

Table 9. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			1	FS_GEN_MODE	RW	0	FrameSync Generation Mode This control selects between Hi/Lo and 50/50 modes. In High/Lo mode, the FrameSync generator uses the FS_HIGH_TIME and FS_LOW_TIME register values to separately control the high and low periods for the generated FrameSync signal. In 50/50 mode, the FrameSync generator uses the values in the FS_HIGH_TIME_0, FS_LOW_TIME_1 and FS_LOW_TIME_0 registers as a 24-bit value for both the high and low periods of the generated FrameSync signal. 0: Hi/Lo 1: 50/50
			0	FS_GEN_ENABLE	RW	0	FrameSync generation enable 0: Disabled 1: Enabled
Share	0x19	FS_HIGH_TIME_1	7:0	FRAMESYNC_HIGH_TIME_1	RW	0	FrameSync high time bits 15:8 The value programmed to the FS_HIGH_TIME register should be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_HIGH_TIME field results in a 1 cycle high pulse on the FrameSync signal.
Share	0x1A	FS_HIGH_TIME_0	7:0	FRAMESYNC_HIGH_TIME_0	RW	0	FrameSync High Time bits 7:0 The value programmed to the FS_HIGH_TIME register should be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_HIGH_TIME field results in a 1 cycle high pulse on the FrameSync signal.
Share	0x1B	FS_LOW_TIME_1	7:0	FRAMESYNC_LOW_TIME_1	RW	0	FrameSync Low Time bits 15:8 The value programmed to the FS_HIGH_TIME register should be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_HIGH_TIME field results in a 1 cycle high pulse on the FrameSync signal.
Share	0x1C	FS_LOW_TIME_0	7:0	FRAMESYNC_LOW_TIME_0	RW	0	FrameSync Low Time bits 7:0 The value programmed to the FS_HIGH_TIME register should be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_HIGH_TIME field results in a 1 cycle high pulse on the FrameSync signal.
Share	0x1D - 0x22	RESERVED	7:0	RESERVED	RO	0x00	Reserved
Share	0x23	INTERRUPT_CTL	7	INT_EN	RW	0	Global interrupt enable Enables interrupt on the interrupt signal to the controller.
			6	RESERVED	RW	0	Reserved
			5	RESERVED	RW	0	Reserved
			4	RESERVED	RW	0	Reserved
			3	RESERVED	RW	0	Reserved
			2	RESERVED	RW	0	Reserved
			1	IE_RX1	RW	0	RX port 1 Interrupt: Enable interrupt from receiver port 1.
			0	IE_RX0	RW	0	RX Port 0 Interrupt: Enable interrupt from receiver port 0.

Table 9. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
Share	0x24	INTERRUPT_STS	7	INT	RO	0	Global Interrupt: Set if any enabled interrupt is indicated in the individual status bits in this register. The setting of this bit is not dependent on the INT_EN bit in the INTERRUPT_CTL register but does depend on the IE_xxx bits. For example, if IE_RX0 and IS_RX0 are both asserted, the INT bit is set to 1.
			6	RESERVED	RO	0	Reserved
			5	RESERVED	RO	0	Reserved
			4	RESERVED	RO	0	Reserved
			3	RESERVED	RO	0	Reserved
			2	RESERVED	RO	0	Reserved
			1	IS_RX1	RO	0	RX port 1 interrupt: An interrupt has occurred for receive port 1. This interrupt is cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are RX_PORT_STS1 and RX_PORT_STS2.
			0	IS_RX0	RO	0	RX Port 0 Interrupt: An interrupt has occurred for receive port 0. This interrupt is cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are RX_PORT_STS1 and RX_PORT_STS2.
Share	0x25	FS_CONFIG	7	RESERVED	RW	0	Reserved
			6	FS_POLARITY	RW	0	Framesync Polarity Indicates active edge of FrameSync signal 0: Rising edge 1: Falling edge
			5:0	RESERVED	RW	0x00	Reserved
Share	0x26 - 0x3A	RESERVED	7:0	RESERVED	RW	0x00	Reserved
DVP	0x3B	DVP_CLK_CTL	7:1	RESERVED	RW	0x00	Reserved
			0	RRFB	RW	1	Pixel clock edge select (relative to the sink) 1: Parallel interface data is driven on the falling clock edge and sampled on the rising clock edge 0: Parallel interface data is driven on the rising clock edge and sampled on the falling clock edge
DVP	0x3C	DVP_FREQ_DET0	7:5	RESERVED	RW	0x0	Reserved
			4:0	FPD3_FREQ_LO_THR	RW	0x14	Frequency low threshold Sets the low threshold for the CDR Clock frequency detect circuit in MHz. This value is used to determine if the clock frequency is too low for proper operation.

Table 9. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
DVP	0x3E	DVP_SSCG_CTL	7:6	RESERVED	RO	0x0	Reserved
			5	RESERVED	RW	0	Reserved
			4	SSCG_ENABLE	RW	0	Enable SSCG modulation 0 : SSCG modulation is disabled 1 : SSCG modulation is enabled Prior to enabling SSCG, the SSCG_MOD_RATE must be set. This requires a separate write to set the SSCG_MOD_RATE with SSCG disabled, then a write to set the SSCG_ENABLE with the same SSCG_MOD_RATE setting. In addition, when changing the SSCG_MOD_RATE, disable the SSCG first.
			3:1	RESERVED	RW	0x0	Reserved
			0	SSCG_MOD_RATE	RW	0	SSCG modulation frequency with its deviation 0: Reserved 1: frequency modulation PCLK/3168 ±1%
Share	0x44 - 0x4B	RESERVED	7:0	RESERVED	RW	0x00	Reserved
Share	0x4C	FPD3_PORT_SEL	7:6	PHYS_PORT_NUM	RO	0	Physical port number This field provides the physical port connection when reading from a remote device via the bidirectional control channel. When accessed via local I2C interfaces, the value returned is always 0. When accessed via bidirectional control channel, the value returned is the port number of the receive port connection.
			5	RESERVED			Reserved
			4	RX_READ_PORT	RW	0	Select RX port for register read This bit selects one of the two RX port register blocks for readback. This applies to all paged FPD3 receiver port registers. 0: Port 0 registers 1: Port 1 registers When accessed via local I2C interfaces, the default setting is 0. When accessed via bidirectional control channel, the default value is the port number of the receive port connection.
			3:2	RESERVED	RW	0x0	Reserved
			1	RX_WRITE_PORT_1	RW	0	Write Enable for RX port 1 registers This bit enables writes to RX port 1 registers. Any combination of RX port registers can be written simultaneously. This applies to all paged FPD3 Receiver port registers. 0: Writes disabled 1: Writes enabled When accessed via bidirectional control channel, the default value is 1 if accessed over RX port 1.
			0	RX_WRITE_PORT_0	RW	0	Write Enable for RX port 0 registers This bit enables writes to RX port 0 registers. Any combination of RX port registers can be written simultaneously. This applies to all paged FPD3 receiver port registers. 0: Writes disabled 1: Writes enabled When accessed via Bidirectional Control Channel, the default value is 1 if accessed over RX port 0.
RX	0x4D	RX_PORT_STS1	7	RESERVED	RO	0	Reserved

Table 9. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			6	RX_PORT_NUM	RO	0	RX port number This read-only field indicates the number of the currently selected RX read port.
			5	BCC_CRC_ERROR	RO, LH	0	Bidirectional control channel CRC error detected This bit indicates a CRC error has been detected in the forward control channel. If this bit is set, an error may have occurred in the control channel operation. This bit is cleared on read.
			4	LOCK_STS_CHG	RO, LH	0	Lock status changed This bit is set if a change in receiver lock status has been detected since the last read of this register. Current lock status is available in the LOCK_STS bit of this register This bit is cleared on read.
			3	BCC_SEQ_ERROR	RO, LH	0	Bidirectional control channel sequence error detected This bit indicates a sequence error has been detected in the forward control channel. If this bit is set, an error may have occurred in the control channel operation. This bit is cleared on read.
			2	PARITY_ERROR	RO, LH	0	FPD3 parity errors detected This flag is set when the number of parity errors detected is greater than the threshold programmed in the PAR_ERR_THOLD registers. 1: Number of FPD3 parity errors detected is greater than the threshold 0: Number of FPD3 parity errors is below the threshold. This bit is cleared when the RX_PAR_ERR_HI/LO registers are cleared.
			1	PORT_PASS	RO	0	Receiver PASS indication This bit indicates the current status of the Receiver PASS indication. The requirements for setting the Receiver PASS indication are controlled by the PORT_PASS_CTL register. 1: Receive input has met PASS criteria 0: Receive input does not meet PASS criteria
			0	LOCK_STS	RO	0	FPD-Link III receiver is locked to incoming data 1: Receiver is locked to incoming data 0: Receiver is not locked
RX	0x4E	RX_PORT_STS2	7:6	RESERVED	RO	0x0	Reserved
			5	FPD3_ENCODE_ERROR	RO, LH	0	FPD3 encoder error detected If set, this flag indicates an error in the FPD-Link III encoding has been detected by the FPD-Link III receiver. This bit is cleared on read.
			4:3	RESERVED	RO	0x0	Reserved
			2	FREQ_STABLE	RO	0	Frequency measurement stable
			1	NO_FPD3_CLK	RO	0	No FPD-Link III input clock detected
			0	RESERVED	RO	0	Reserved
RX	0x4F	RX_FREQ_HIGH	7:0	FREQ_CNT_HIGH	RO	0	FPD Link-III frequency measurement high byte (MHz) The frequency counter reports the measured frequency for the FPD3 receiver. This portion of the field is the integer value in MHz. frequency measurements scales with reference clock frequency.

Table 9. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
RX	0x50	RX_FREQ_LOW	7:0	FREQ_CNT_LOW	RO	0	FPD Link-III frequency measurement low byte (1/256 MHz) The Frequency counter reports the measured frequency for the FPD3 Receiver. This portion of the field is the fractional value in 1/256 MHz. Values scales with reference clock frequency.
RX	0x51	RESERVED	7:0	RESERVED	RO	0	Reserved
RX	0x52	RESERVED	7:0	RESERVED	RO	0	Reserved
RX	0x53	RESERVED	7:0	RESERVED	RO	0	Reserved
RX	0x54	RESERVED	7:0	RESERVED	RO	0	Reserved
RX	0x55	RX_PAR_ERR_HI	7:0	PAR ERROR BYTE 1	RO	0	Number of FPD3 parity errors – 8 most significant bits. The parity error counter registers return the number of data parity errors that have been detected on the FPD3 Receiver data since the last detection of valid lock or last read of the RX_PAR_ERR_LO register. For accurate reading of the parity error count, disable the RX PARITY CHECKER ENABLE bit in register 0x2 prior to reading the parity error count registers. This register is cleared upon reading the RX_PAR_ERR_LO register.
RX	0x56	RX_PAR_ERR_LO	7:0	PAR ERROR BYTE 0	RO	0	Number of FPD3 parity errors – 8 least significant bits. The parity error counter registers return the number of data parity errors that have been detected on the FPD3 Receiver data since the last detection of valid lock or last read of the RX_PAR_ERR_LO register. For accurate reading of the parity error count, disable the RX PARITY CHECKER ENABLE bit in register 0x2 prior to reading the parity error count registers. This register will be cleared on read.
RX	0x57	BIST_ERR_COUNT	7:0	BIST ERROR COUNT	RO	0	BIST error count Returns BIST error count
RX	0x58	BCC_CONFIG	7	I2C PASS THROUGH ALL	RW	0	I2C pass-through all transactions 0: Disabled 1: Enabled
			6	I2C PASS THROUGH	RW	0	I2C pass-through to serializer if decode matches 0: Pass-through disabled 1: Pass-through enabled
			5	AUTO ACK ALL	RW	0	Automatically acknowledge all I2C writes independent of the forward channel lock state or status of the remote acknowledge 1: Enable 0: Disable
			4	BACK CHANNEL ENABLE FOR CAMERA MODE	RW	1	Back channel enable for camera mode (display mode BC is always enabled) 1: Enable 0: Disable
			3	BC CRC GENERATOR ENABLE	RW	1	Back Channel CRC Generator Enable 0: Disable 1: Enable
			2	RESERVED	RW	0	Reserved

Table 9. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			1:0	BC FREQ SELECT	RW, S	0	Back channel frequency select 00: 2.5 Mbps (default for DS90UB913/A and DS90UB933 compatibility) 01: 1.5625 Mbps 10 - 11 : Reserved Note that changing this setting results in some errors on the back channel for a short period of time. If set over the control channel, first program the deserializer to Auto-Ack operation to avoid a control channel timeout due to lack of response from the serializer.
RX	0x59	RESERVED	7:0	RESERVED	RW	0	Reserved
RX	0x5A	RESERVED	7:0	RESERVED	RW	0	Reserved
RX	0x5B	SER_ID	7:1	SER ID	RW	0x00	Remote serializer ID This field is normally loaded automatically from the remote serializer.
			0	FREEZE DEVICE ID	RW	0	Freeze serializer device ID Prevent auto-loading of the serializer device ID from the forward channel. The ID is frozen at the value written.
RX	0x5C	SER_ALIAS_ID	7:1	SER ALIAS ID	RW	0	7-bit remote serializer alias ID Configures the decoder for detecting transactions designated for an I2C slave device attached to the remote deserializer. The transaction will be remapped to the address specified in the slave ID register. A value of 0 in this field disables access to the remote I2C slave.
			0	SER AUTO ACK	RW	0	Automatically acknowledge all I2C writes to the remote serializer independent of the forward channel lock state or status of the remote serializer acknowledge 1: Enable 0: Disable
RX	0x5D	SlaveID[0]	7:1	SLAVE ID0	RW	0	7-bit remote slave device ID 0 Configures the physical I2C address of the remote I2C slave device attached to the remote serializer. If an I2C transaction is addressed to the slave alias ID0, the transaction is remapped to this address before passing the transaction across the bidirectional control channel to the serializer.
			0	RESERVED	RO	0	Reserved
RX	0x5E	SlaveID[1]	7:1	SLAVE ID1	RW	0	7-bit remote slave device ID 1 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the slave alias ID1, the transaction is remapped to this address before passing the transaction across the bidirectional control channel to the serializer.
			0	RESERVED	RO	0	Reserved
RX	0x5F	SlaveID[2]	7:1	SLAVE ID2	RW	0	7-bit remote slave device ID 2 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID2, the transaction is remapped to this address before passing the transaction across the bidirectional control channel to the serializer.
			0	RESERVED	RO	0	Reserved

Table 9. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
RX	0x60	SlaveID[3]	7:1	SLAVE ID3	RW	0	7-bit remote slave device ID 3 Configures the physical I2C address of the remote I2C slave device attached to the remote serializer. If an I2C transaction is addressed to the slave alias ID3, the transaction is remapped to this address before passing the transaction across the bidirectional control channel to the serializer.
			0	RESERVED	RO	0	Reserved
RX	0x61	SlaveID[4]	7:1	SLAVE ID4	RW	0	7-bit remote slave device ID 4 Configures the physical I2C address of the remote I2C slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID4, the transaction is remapped to this address before passing the transaction across the bidirectional control channel to the serializer.
			0	RESERVED	RO	0	Reserved
RX	0x62	SlaveID[5]	7:1	SLAVE ID5	RW	0	7-bit remote slave device ID 5 Configures the physical I2C address of the remote I2C slave device attached to the remote serializer. If an I2C transaction is addressed to the slave alias ID5, the transaction is remapped to this address before passing the transaction across the bidirectional control channel to the serializer.
			0	RESERVED	RO	0	Reserved
RX	0x63	SlaveID[6]	7:1	SLAVE ID6	RW	0	7-bit remote slave device ID 6 Configures the physical I2C address of the remote I2C slave device attached to the remote serializer. If an I2C transaction is addressed to the slave alias ID6, the transaction is remapped to this address before passing the transaction across the bidirectional control channel to the serializer.
			0	RESERVED	RO	0	Reserved
RX	0x64	SlaveID[7]	7:1	SLAVE ID7	RW	0	7-bit remote slave device ID 7 Configures the physical I2C address of the remote I2C slave device attached to the remote serializer. If an I2C transaction is addressed to the slave alias ID7, the transaction is remapped to this address before passing the transaction across the bidirectional control channel to the serializer.
			0	RESERVED	RO	0	Reserved
RX	0x65	SlaveAlias[0]	7:1	SLAVE ALIAS ID0	RW	0	7-bit remote slave device alias ID 0 Configures the decoder for detecting transactions designated for an I2C slave device attached to the remote serializer. The transaction is remapped to the address specified in the slave ID0 register. A value of 0 in this field disables access to the remote I2C slave.
			0	SLAVE AUTO ACK 0	RW	0	Automatically acknowledge all I2C writes to the remote slave 0 independent of the forward channel lock state or status of the remote serializer acknowledge. 1: Enable 0: Disable

Table 9. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
RX	0x66	SlaveAlias[1]	7:1	SLAVE ALIAS ID1	RW	0	7-bit remote slave device alias ID 1 Configures the decoder for detecting transactions designated for an I2C slave device attached to the remote serializer. The transaction is remapped to the address specified in the slave ID1 register. A value of 0 in this field disables access to the remote I2C slave.
			0	SLAVE AUTO ACK 1	RW	0	Automatically acknowledge all I2C writes to the remote slave 1 independent of the forward channel lock state or status of the remote serializer acknowledge 1: Enable 0: Disable
RX	0x67	SlaveAlias[2]	7:1	SLAVE ALIAS ID2	RW	0	7-bit remote slave device alias ID 2 Configures the decoder for detecting transactions designated for an I2C slave device attached to the remote serializer. The transaction is remapped to the address specified in the slave ID2 register. A value of 0 in this field disables access to the remote I2C slave.
			0	SLAVE AUTO ACK 2	RW	0	Automatically acknowledge all I2C writes to the remote slave 2 independent of the forward channel lock state or status of the remote serializer acknowledge 1: Enable 0: Disable
RX	0x68	SlaveAlias[3]	7:1	SLAVE ALIAS ID3	RW	0	7-bit remote slave device alias ID 3 Configures the decoder for detecting transactions designated for an I2C slave device attached to the remote serializer. The transaction is remapped to the address specified in the slave ID3 register. A value of 0 in this field disables access to the remote I2C slave.
			0	SLAVE AUTO ACK 3	RW	0	Automatically acknowledge all I2C writes to the remote slave 3 independent of the forward channel lock state or status of the remote serializer acknowledge. 1: Enable 0: Disable
RX	0x69	SlaveAlias[4]	7:1	SLAVE ALIAS ID4	RW	0	7-bit remote slave device alias ID 4 Configures the decoder for detecting transactions designated for an I2C slave device attached to the remote serializer. The transaction is remapped to the address specified in the slave ID4 register. A value of 0 in this field disables access to the remote I2C slave.
			0	SLAVE AUTO ACK 4	RW	0	Automatically acknowledge all I2C writes to the remote slave 4 independent of the forward channel lock state or status of the remote serializer acknowledge. 1: Enable 0: Disable
RX	0x6A	SlaveAlias[5]	7:1	SLAVE ALIAS ID5	RW	0	7-bit remote slave device alias ID 5 Configures the decoder for detecting transactions designated for an I2C slave device attached to the remote serializer. The transaction is remapped to the address specified in the slave ID5 register. A value of 0 in this field disables access to the remote I2C slave.

Table 9. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			0	SLAVE AUTO ACK 5	RW	0	Automatically acknowledge all I2C writes to the remote slave 5 independent of the forward channel lock state or status of the remote serializer acknowledge. 1: Enable 0: Disable
RX	0x6B	SlaveAlias[6]	7:1	SLAVE ALIAS ID6	RW	0	7-bit remote slave device alias ID 6 Configures the decoder for detecting transactions designated for an I2C slave device attached to the remote serializer. The transaction is remapped to the address specified in the slave ID6 register. A value of 0 in this field disables access to the remote I2C slave.
			0	SLAVE AUTO ACK 6	RW	0	Automatically acknowledge all I2C writes to the remote slave 6 independent of the forward channel lock state or status of the remote serializer acknowledge. 1: Enable 0: Disable
RX	0x6C	SlaveAlias[7]	7:1	SLAVE ALIAS ID7	RW	0	7-bit remote slave device alias ID 7 Configures the decoder for detecting transactions designated for an I2C slave device attached to the remote serializer. The transaction is remapped to the address specified in the slave ID7 register. A value of 0 in this field disables access to the remote I2C slave.
			0	SLAVE AUTO ACK 7	RW	0	Automatically acknowledge all I2C writes to the remote slave 7 independent of the forward channel lock state or status of the remote serializer acknowledge. 1: Enable 0: Disable
RX	0x6D	PORT_CONFIG	7:3	RESERVED	RW	0x0F	Reserved
			2	COAX_MODE	RW, S	0	Enable coax cable mode 0: Shielded twisted pair (STP) mode 1: Coax mode This bit is loaded from the MODE pin strap at power-up.
			1:0	FPD3_MODE	RW, S	0	FPD3 input mode 00: Reserved 01: RAW12 LF mode 10: RAW12 HF mode 11: RAW10 mode This field is loaded from the MODE pin strap at power-up.
RX	0x6E	BC_GPIO_CTL0	7:4	BC_GPIO1_SEL	RW	0x8	Back channel GPIO1 select: Determines the data sent on GPIO1 for the port back channel. 0xxx : Pin GPIOx where x is BC_GPIO1_SEL[2:0] 1000 : Constant value of 0 1001 : Constant value of 1 1010 : FrameSync signal 1011 - 1111 : Reserved

Table 9. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			3:0	BC_GPIO0_SEL	RW	0x8	Back channel GPIO0 Select: Determines the data sent on GPIO0 for the port back channel. 0xxx : Pin GPIOx where x is BC_GPIO1_SEL[2:0] 1000 : Constant value of 0 1001 : Constant value of 1 1010 : FrameSync signal 1011 - 1111 : Reserved
RX	0x6F	BC_GPIO_CTL1	7:4	BC_GPIO3_SEL	RW	0x8	Back channel GPIO3 select: Determines the data sent on GPIO3 for the port back channel. 0xxx : Pin GPIOx where x is BC_GPIO1_SEL[2:0] 1000 : Constant value of 0 1001 : Constant value of 1 1010 : FrameSync signal 1011 - 1111 : Reserved
			3:0	BC_GPIO2_SEL	RW	0x8	Back channel GPIO2 select: Determines the data sent on GPIO2 for the port back channel. 0xxx : Pin GPIOx where x is BC_GPIO1_SEL[2:0] 1000 : Constant value of 0 1001 : Constant value of 1 1010 : FrameSync signal 1011 - 1111 : Reserved
RX	0x70 - 0x76	RESERVED	7:0	RESERVED	RW		Reserved
RX	0x77	FREQ_DET_CTL	7:6	FREQ_HYST	RW	0x3	Frequency detect hysteresis: The frequency detect hysteresis controls reporting of the FPD3 Clock frequency stability via the FREQ_STABLE status in the RX_PORT_STS2 register. The frequency is considered stable when the frequency remains within a range of +/- the FREQ_HYST value from the previous measurement. The FREQ_HYST setting is in MHz.
			5:4	FREQ_STABLE_THR	RW	0	Frequency stability threshold: The frequency detect circuit can be used to detect a stable clock frequency. The stability threshold determines the amount of time required for the clock frequency to stay within the FREQ_HYST range to be considered stable: 00 : 40 µs 01 : 80 µs 10 : 320 µs 11 : 1.28 ms
			3:0	FREQ_LO_THR	RW	0x5	Frequency low threshold: Sets the low threshold for the clock frequency detect circuit in MHz. If the input clock is below this threshold, the NO_FPD3_CLK status is set to 1.
RX	0x78	MAILBOX_1	7:0	MAILBOX_0	RW	0	Mailbox register This register is an unused read/write register that can be used for any purpose such as passing messages between I2C masters on opposite ends of the link.

Table 9. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
RX	0x79	MAILBOX_2	7:0	MAILBOX_1	RW	0x01	Mailbox register This register is an unused read/write register that can be used for any purpose such as passing messages between I2C masters on opposite ends of the link.
RX	0x7A - 0x7F	RESERVED	7:0	RESERVED	RO	0	Reserved
Share	0xB0	IND_ACC_CTL	7:6	RESERVED	R	0	Reserved
			5:2	IA_SEL	RW	0	Indirect Access register select: Selects target for register access 0000 : Pattern Generator registers 0001 : FPD3 RX Port 0 registers 0010 : FPD3 RX Port 1 registers 0011 : Reserved 0100 : Reserved 0101 : FPD3 RX Shared registers 0110 : Simultaneous write to FPD3 RX Port 0-1 registers 0111 : Reserved
			1	IA_AUTO_INC	RW	0	Indirect access auto increment: Enables auto-increment mode. Upon completion of a read or write, the register address automatically increments by 1
			0	IA_READ	RW	0	Indirect access read: Setting this allows generation of a read strobe to the selected register block upon setting of the IND_ACC_ADDR register. In auto-increment mode, read strobes is also asserted following a read of the IND_ACC_DATA register. This function is only required for blocks that need to pre-fetch register data.
Share	0xB1	IND_ACC_ADDR	7:0	IA_ADDR	RW	0	Indirect access register offset: This register contains the 8-bit register offset for the indirect access.
Share	0xB2	IND_ACC_DATA	7:0	IA_DATA	RW	0	Indirect access data: Writing this register causes an indirect write of the IND_ACC_DATA value to the selected analog block register. Reading this register returns the value of the selected block register
Share	0xB3	BIST Control	7:6	BIST_OUT_MODE	RW	0	BIST output mode 00 : No toggling 01 : Alternating 1/0 toggling 1x : Toggle based on BIST data
			5:4	RESERVED	RW	0	Reserved
			3	BIST PIN CONFIG	RW	1	BIST Configured through pin 1: BIST configured through pin 0: BISTconfigured through bits 2:0 in this register
			2:1	BIST CLOCK SOURCE	RW	0	BIST Clock Source This register field selects the BIST clock source at the Serializer. These register bits are automatically written to the CLOCK SOURCE bits (register offset 0x14) in the serializer after BIST is enabled. See the appropriate serializer register descriptions for details. Note: When connected to a DS90UB913A or DS90UB933, a setting of 0x3 may result in a clock frequency that is too slow for proper recovery.
			0	BIST_EN	RW	0	BIST Control 1: Enabled 0: Disabled

Table 9. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
Share	0xB8	MODE_IDX_STS	7	IDX_DONE	R	1	IDX Done: If set, indicates the IDX decode has completed and latched into the IDX status bits.
			6:4	IDX	R	0	IDX Decode 3-bit decode from IDX pin
			3	MODE_DONE	R	1	MODE Done: If set, indicates the MODE decode has completed and latched into the MODE status bits.
			2:0	MODE	R	0	MODE Decode 3-bit decode from MODE pin
Share	0xBE	GPIO_PD_CTL	7	RESERVED	RW	0	Reserved
			6	RESERVED	RW	0	Reserved
			5	RESERVED	RW	0	Reserved
			4	RESERVED	RW	0	Reserved
			3	RESERVED	RW	0	Reserved
			2	GPIO2_PD_DIS	RW	0	GPIO2 pulldown resistor disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor is also disabled when the GPIO pin is in an input only mode. 1 : Disable GPIO pulldown resistor 0 : Enable GPIO pulldown resistor
			1	GPIO1_PD_DIS	RW	0	GPIO1 pulldown resistor disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor is also disabled when the GPIO pin is in an input only mode. 1 : Disable GPIO pulldown resistor 0 : Enable GPIO pulldown resistor
			0	GPIO0_PD_DIS	RW	0	GPIO0 pulldown resistor disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor is also disabled when the GPIO pin is in an input only mode. 1 : Disable GPIO pulldown resistor 0 : Enable GPIO pulldown resistor
RX	0xD0	PORT DEBUG	7:6	RESERVED	RW	0	Reserved
			5	SER BIST ACT	R	0	Serializer BIST Active This register indicates whether the serializer is in BIST mode. 0: BIST mode not active 1: BIST mode active If the deserializer is not in BIST mode, this bit being 1 could indicate an error condition.
			4:2	RESERVED	RW	0	Reserved
			1	FORCE BC ERRORS	RW	0	This bit introduces continuous errors into the back channel frame.
			0	FORCE 1 BC ERROR	RW, SC	0	This bit introduces typically one, worst case two, errors into the back channel frame. Self clearing bit.
RX	0xD8	PORT_ICR_HI	7:2	Reserved	R	0	Reserved

Table 9. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			2	IE_FPD3_ENC_ERR	RW	0	Interrupt on FPD-Link III receiver encoding error When enabled, an interrupt is generated on detection of an encoding error on the FPD-Link III interface for the receive port as reported in the FPD3_ENC_ERROR bit in the RX_PORT_STS2 register
			1	IE_BCC_SEQ_ERR	RW	0	Interrupt on BCC SEQ sequence error When enabled, an interrupt is generated if a sequence error is detected for the bidirectional control channel forward channel receiver as reported in the BCC_SEQ_ERROR bit in the RX_PORT_STS1 register.
			0	IE_BCC_CRC_ERR	RW	0	Interrupt on BCC CRC error detect When enabled, an interrupt is generated if a CRC error is detected on a bidirectional control channel frame received over the FPD-Link III forward channel as reported in the BCC_CRC_ERROR bit in the RX_PORT_STS1 register.
RX	0xD9	PORT_ICR_LO	7:3	RESERVED	RW	0	Reserved
			2	IE_FPD3_PAR_ERR	RW	0	Interrupt on FPD-Link III receiver parity error When enabled, an interrupt is generated on detection of parity errors on the FPD-Link III interface for the receive port. Parity error status is reported in the PARITY_ERROR bit in the RX_PORT_STS1 register.
			1	IE_PORT_PASS	RW	0	Interrupt on change in port PASS status When enabled, an interrupt is generated on a change in receiver port valid status as reported in the PORT_PASS bit in the PORT_STS1 register.
			0	IE_LOCK_STS	RW	0	Interrupt on change in lock status When enabled, an interrupt is generated on a change in lock status. Status is reported in the LOCK_STS_CHG bit in the RX_PORT_STS1 register.
RX	0xDA	PORT_ISR_HI	7:3	Reserved	R	0	Reserved
			2	IS_FPD3_ENC_ERR	R	0	FPD-Link III receiver encode error interrupt status An encoding error on the FPD-Link III interface for the receive port has been detected. Status is reported in the FPD3_ENC_ERROR bit in the RX_PORT_STS2 register. This interrupt condition is cleared by reading the RX_PORT_STS2 register.
			1	IS_BCC_SEQ_ERR	R	0	BCC CRC sequence error interrupt status A sequence error has been detected for the bidirectional control channel forward channel receiver. Status is reported in the BCC_SEQ_ERROR bit in the RX_PORT_STS1 register. This interrupt condition is cleared by reading the RX_PORT_STS1 register.
			0	IS_BCC_CRC_ERR	R	0	BCC CRC error detect interrupt status A CRC error has been detected on a bidirectional control channel frame received over the FPD-Link III forward channel. Status is reported in the BCC_CRC_ERROR bit in the RX_PORT_STS1 register. This interrupt condition is cleared by reading the RX_PORT_STS1 register.
RX	0xDB	PORT_ISR_LO	7:3	Reserved	R	0	Reserved

Table 9. Serial Control Bus Registers (continued)

Page	Addr (hex)	Register Name	Bit(s)	Field	Type	Default	Description
			2	IS_FPD3_PAR_ERR	R	0	FPD-Link III receiver parity error interrupt status A parity error on the FPD-Link III interface for the receive port has been detected. Parity error status is reported in the PARITY_ERROR bit in the RX_PORT_STS1 register. This interrupt condition is cleared by reading the RX_PORT_STS1 register.
			1	IS_PORT_PASS	R	0	Port valid interrupt status A change in receiver port valid status as reported in the PORT_PASS bit in the PORT_STS1 register. This interrupt condition is cleared by reading the RX_PORT_STS1 register.
			0	IS_LOCK_STS	R	0	Lock interrupt status A change in lock status has been detected. Status is reported in the LOCK_STS_CHG bit in the RX_PORT_STS1 register. This interrupt condition is cleared by reading the RX_PORT_STS1 register.
Share	0xF0	FPD3_RX_ID0	7:0	FPD3_RX_ID0	R	0x5F	FPD3_RX_ID0: First byte ID code: '_'
Share	0xF1	FPD3_RX_ID1	7:0	FPD3_RX_ID1	R	0x55	FPD3_RX_ID1: 2nd byte of ID code: 'U'
Share	0xF2	FPD3_RX_ID2	7:0	FPD3_RX_ID2	R	0x42	FPD3_RX_ID2: 3rd byte of ID code: 'B'
Share	0xF3	FPD3_RX_ID3	7:0	FPD3_RX_ID3	R	0x39	FPD3_RX_ID3: 4th byte of ID code: '9'
Share	0xF4	FPD3_RX_ID4	7:0	FPD3_RX_ID4	R	0x33	FPD3_RX_ID4: 5th byte of ID code: '3'
Share	0xF5	FPD3_RX_ID5	7:0	FPD3_RX_ID5	R	0x34	FPD3_RX_ID5: 6th byte of ID code: '4'
Share	0xF8	I2C_RX0_ID	7:1	RX_PORT0_ID	RW	0x00	7-bit Receive Port 0 I2C ID Configures the decoder for detecting transactions designated for Receiver port 0 registers. This provides a simpler method of accessing device registers specifically for port 0 without having to use the paging function to select the register page. A value of 0 in this field disables the Port0 decoder.
			0	RESERVED	R	0	Reserved
Share	0xF9	I2C_RX1_ID	7:1	RX_PORT1_ID	RW	0x00	7-bit Receive Port 1 I2C ID Configures the decoder for detecting transactions designated for Receiver port 1 registers. This provides a simpler method of accessing device registers specifically for port 1 without having to use the paging function to select the register page. A value of 0 in this field disables the Port1 decoder.
			0	RESERVED	R	0	Reserved

LEGEND:
- RW = Read Write access
- RO = Read Only access
- S = Register set by configuration pin
- SC = Register sets on event occurrence and self-clears when event ends
- RO/P = Read Only, Permanently set to a default value
- LL = Latched Low and held until read, based upon the occurrence of the corresponding event
- LH = Latched High and held until read, based upon the occurrence of the corresponding event

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DS90UB933/934 chipset supports video transport and bidirectional control over a single coaxial or STP cable targeted at ADAS applications, such as front, rear, and surround-view cameras, camera monitoring systems, and sensor fusion.

8.2 Typical Application

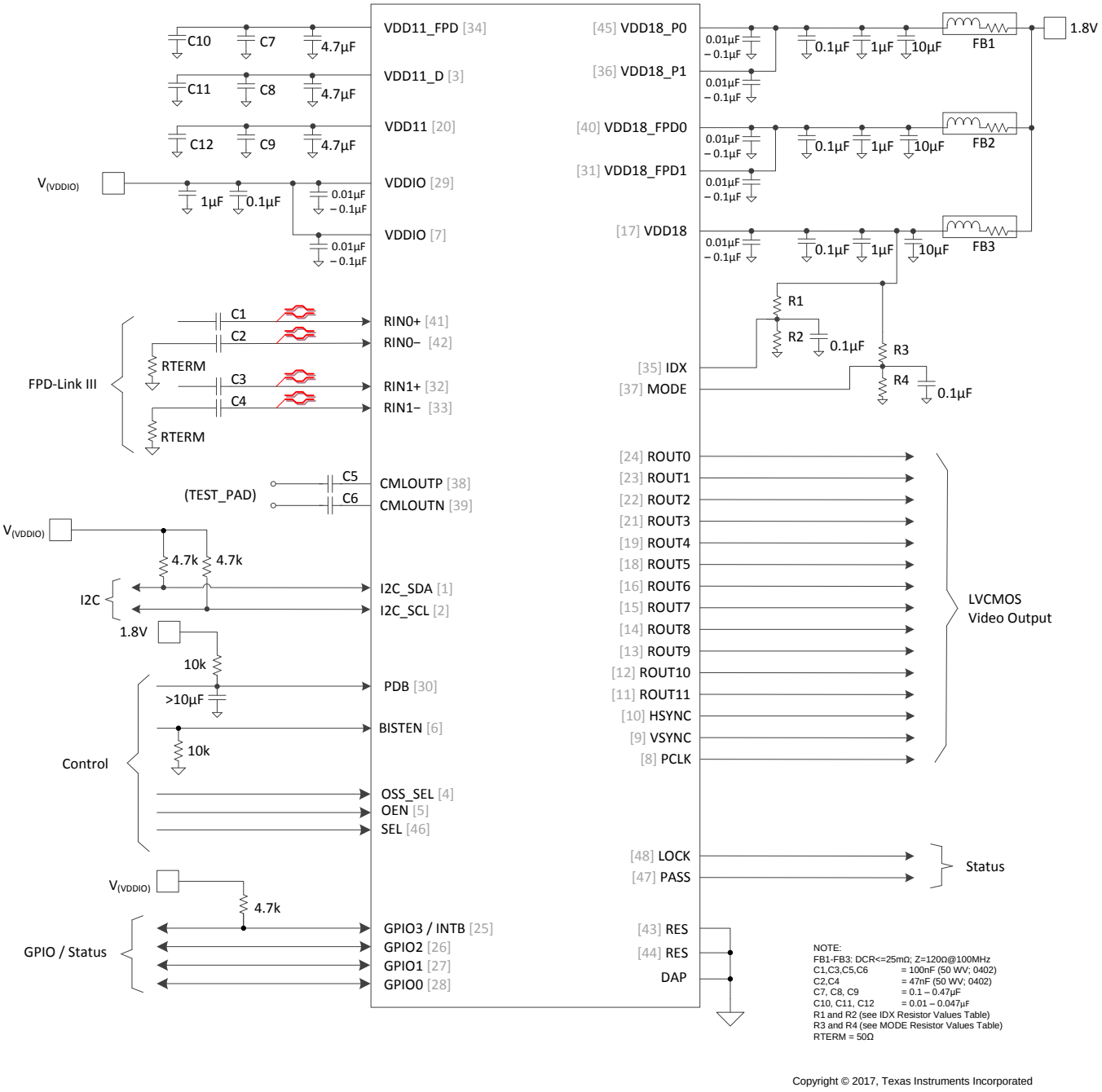


Figure 22. Typical Connection Diagram (Coax)

Typical Application (continued)

8.2.1 Design Requirements

For the typical FPD-Link III serializer and deserializer applications, use the input parameters in Table 10.

Table 10. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
$V_{(VDDIO)}$	1.8 V or 3.3 V
$V_{(VDD18)}$	1.8 V
AC-coupling capacitor for STP with 913/A or 933: RIN[1:0]±	100 nF (50 WV 0402)
AC-coupling capacitor for coaxial with 913A or 933: RIN[1:0]+	100 nF (50 WV 0402)
AC-coupling capacitor for coaxial with 913A or 933: RIN[1:0]-	47 nF (50 WV 0402)

8.2.2 Detailed Design Procedure

The serializer and deserializer support only AC-coupled interconnects through an integrated DC-balanced decoding scheme. External AC-coupling capacitors must be placed in series in the FPD-Link III signal path as shown in Figure 23. For applications utilizing single-ended 50-Ω coaxial cable, terminate the unused data pins (RIN0–, RIN1–, RIN2–, RIN3–) with AC coupling capacitor and a 50-Ω resistor.

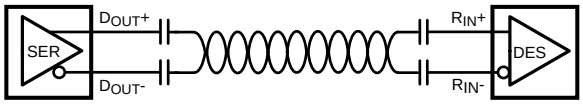


Figure 23. AC-Coupled Connection (STP)

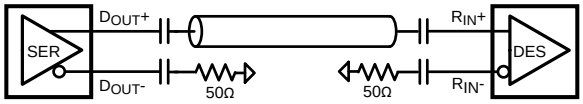


Figure 24. AC-Coupled Connection (Coaxial)

For high-speed FPD–Link III transmissions, use the smallest available package for the AC-coupling capacitor. This helps minimize degradation of signal quality due to package parasitics.

8.2.3 Application Curves

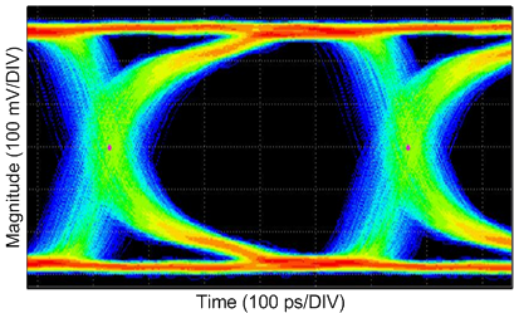


Figure 25. CMLOUTP/N Loop-through Eye Diagram at 1.867 Gbps
15 Meters of DACAR 462 Cable

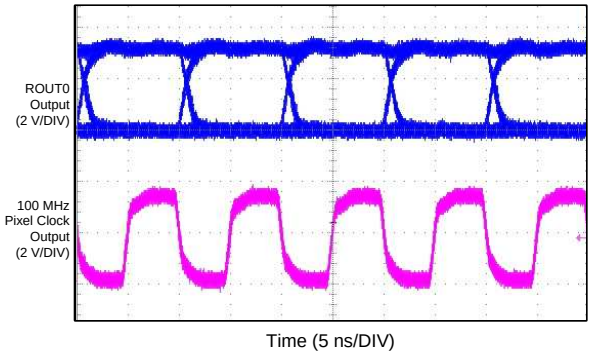


Figure 26. ROUT0 Data Sampled by 100-MHz PCLK
RRFB (0x3B[0]) = 1

8.3 System Examples

The DS90UB934-Q1 has two input ports that operate as a multiplexer controlled by the SEL pin. A single camera can be connected to either Rx input port 0 or Rx input port 1 (Figure 27).

Two cameras can be connected simultaneously, but only one is active at a time (Figure 28). The SEL pin can be toggled on-the-fly to select which camera is forwarded to the DVP output.

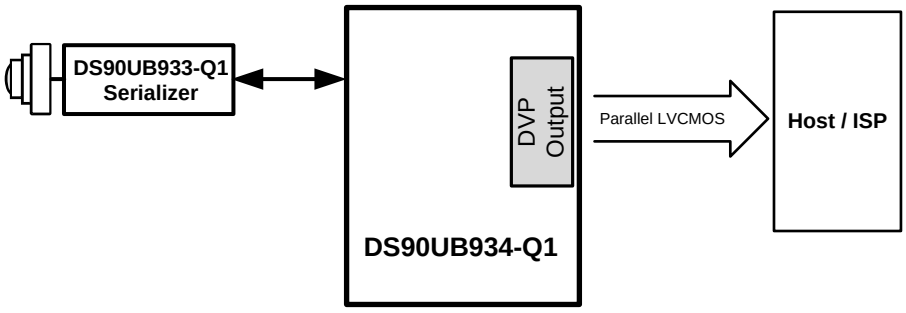


Figure 27. DS90UB933-Q1 Camera Data to 1 Rx Port

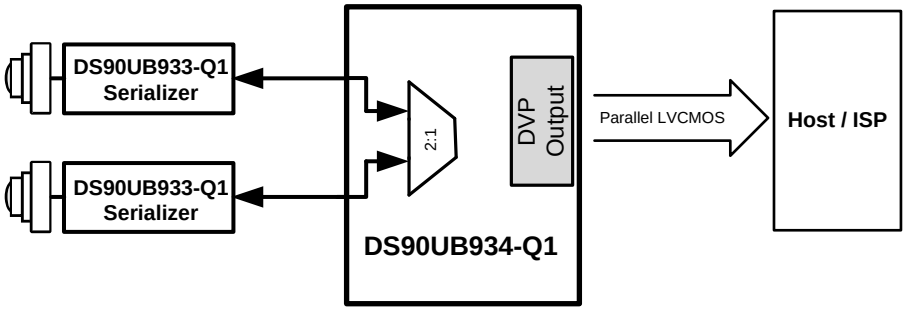


Figure 28. Two DS90UB933-Q1 Camera Data to 2 Rx Ports

9 Power Supply Recommendations

This device provides separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs.

9.1 VDD Power Supply

Each VDD power supply pin must have a 10-nF capacitor to ground connected as close as possible to the DS90UB934-Q1 device. TI recommends having additional decoupling capacitors (0.1 µF, 1 µF, and 10 µF) on it. It is also recommended to have the pins connected to a solid power plane.

9.2 Power-Up Sequencing

All inputs must not be driven until both power supplies have reached steady state. The power-up sequence for the DS90UB934-Q1 is as follows:

Table 11. Timing Diagram for the Power-Up Sequence

PARAMETER		MIN	TYP	MAX	UNIT	NOTES
T0	$V_{(VDDIO)}$ to $V_{(VDD18)}$	0			ms	$V_{(VDDIO)}$ must come before (or at the same time as) $V_{(VDD18)}$
T1	$V_{(VDDIO)}$ rise time	1			ms	rise time = 10/90%
T2	$V_{(VDD18)}$ rise time	1			ms	rise time = 10/90%
T3	$V_{(VDDIO)}$ / $V_{(VDD18)}$ stable to PDB	0			ms	PDB = H must come after supplies are stable
T4	PDB pulse width	2			ms	Hard reset

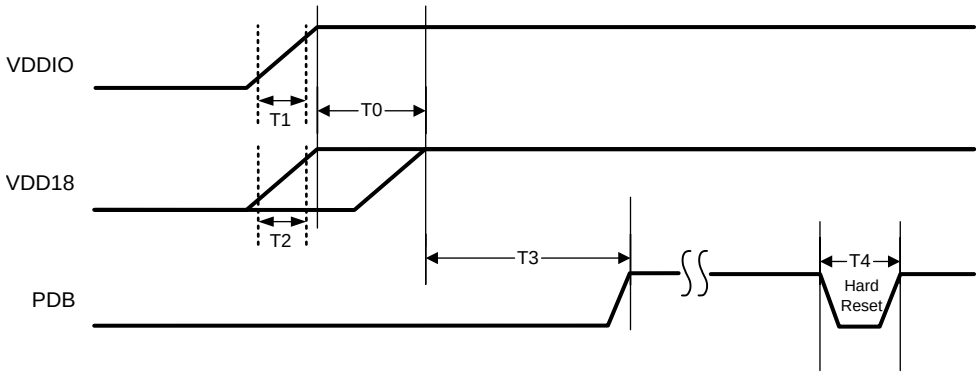


Figure 29. Power-Up Sequencing

9.3 PDB Pin

The PDB pin is active HIGH and must remain LOW until the power supplies are within the recommended operating conditions. An external RC network on the PDB pin may be connected to ensure PDB arrives after all the supply pins have settled to the recommended operating voltage. When PDB pin is pulled up to VDD18, a 10-kΩ pullup and a >10-µF capacitor to GND are required to delay the PDB input signal rise.

9.4 Ground

TI recommends that only one board ground plane be used in the design. This provides the best image plane for signal traces running above the plane. Connect the thermal pad of the DS90UB934-Q1 to this plane with vias.

10 Layout

10.1 Layout Guidelines

Circuit board layout and stack-up for the FPD-Link III devices must be designed to provide low-noise power feed to the device. Good layout practice also separates high-frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback, and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power/ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies and makes the value and placement of external bypass capacitors less critical. Include both RF-ceramic and tantalum-electrolytic type external bypass capacitors in the layout. RF capacitors may use values in the range of 0.01 µF to 0.1 µF. Tantalum capacitors may be in the 2.2-µF to 10-µF range. Voltage rating of the tantalum capacitors must be at least 5× the power supply voltage being used

TI recommends surface mount capacitors due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50-µF to 100-µF range and smooths low frequency switching noise. TI recommends connecting power and ground pins directly to the power and connecting ground planes with bypass capacitors to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor increases the inductance of the path.

A small body size X7R chip capacitor, such as 0603 or 0402, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin function tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four-layer board with a power and ground plane. Locate LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines. Differential impedance of 100 Ω are typically recommended for STP interconnect and single-ended impedance of 50 Ω for coax interconnect. The closely coupled lines help to ensure that coupled noise appears as common-mode and thus is rejected by the receivers. The tightly coupled lines also radiate less.

10.1.1 DVP Interface Guidelines

1. Route R_{OUT}[11:0] with controlled 50-Ω single-ended impedance (±15%).
2. Keep away from other high speed signals.
3. Keep lengths to within 5 mils of each other.
4. Length matching must be near the location of mismatch.
5. Separate each signal by at least by 3 times the signal trace width.
6. Keep the use of bends in traces to a minimum. When bends are used, the number of left and right bends must be as equal as possible, and the angle of the bends must be ≥ 135 degrees. This arrangement minimizes any length mismatch caused by the bends, and therefore minimizes the impact that bends have on EMI.
7. Route all signals on the same layer
8. The number of vias should be kept to a minimum. TI recommends keeping the via count to 2 or fewer.
9. Keep traces on layers adjacent to ground plane.
10. Do NOT route signals over any GND plane split.
11. Adding test points causes impedance discontinuity and therefore negatively impacts signal performance. If test points are used, place them in series and symmetrically. They must not be placed in a manner that causes a stub.

10.2 Layout Example

Stencil parameters such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the VQFN package is highly recommended to improve board assembly yields. If the via and aperture openings are not carefully monitored, the solder may flow unevenly through the DAP.

Figure 30 shows a PCB layout example derived from the layout design of the DS90UB934-Q1EVM Evaluation Board. The graphic and layout description are used to determine proper routing when designing the board. The FPD-Link III traces leading to RIN0+, RIN0−, RIN1+, RIN1− carry critical high-speed signals, and have highest priority in routing.

For STP applications, the positive and negative traces are tightly coupled with differential 100-Ω characteristic impedance.

For coaxial applications, the FPD-Link III traces must have 50-Ω characteristic impedance. As a secondary priority, loosely couple the traces with differential 100-Ω characteristic impedance.

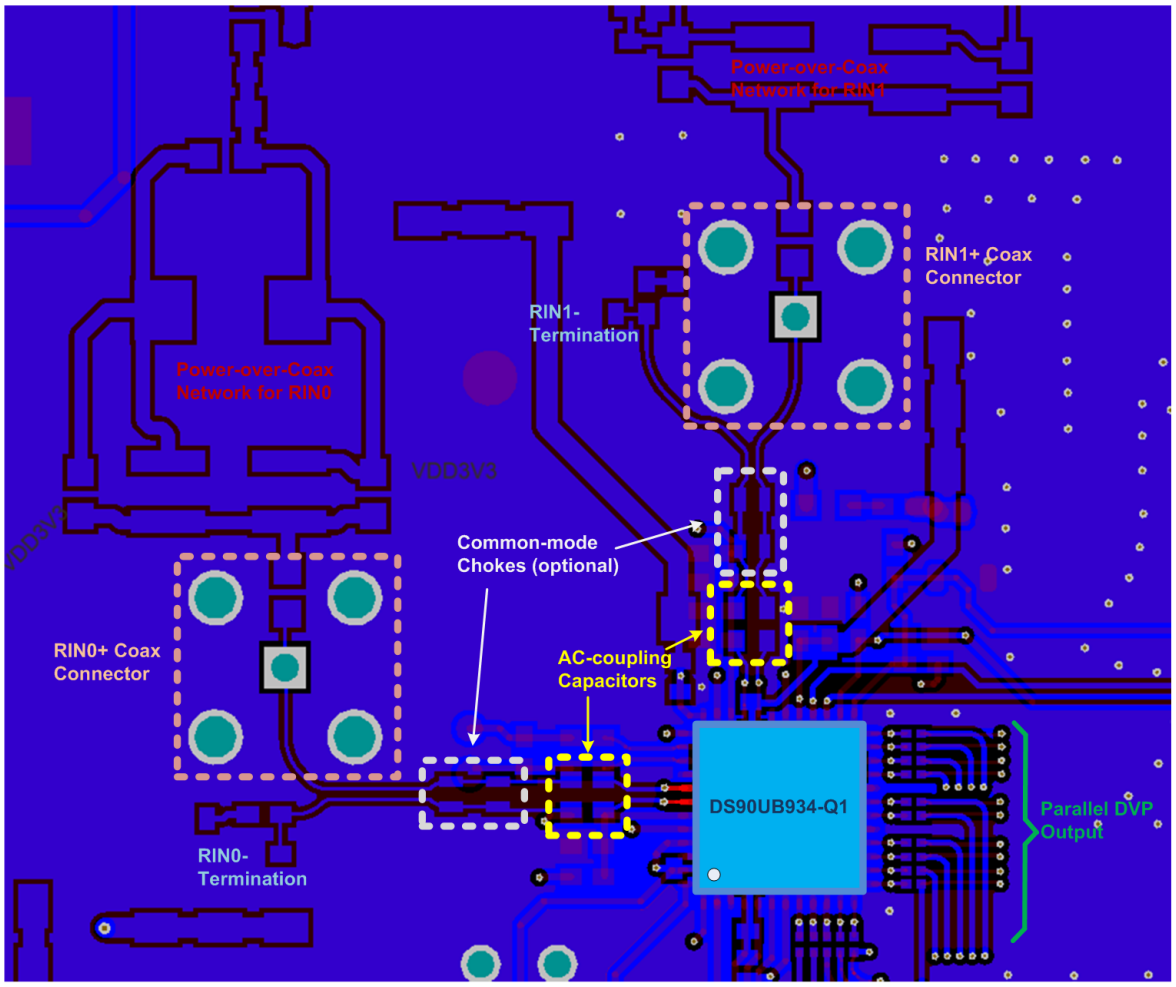


Figure 30. DS90UB934-Q1 Example PCB Layout

1. Place vias, AC-coupling capacitors, and common-mode chokes (if used) on the FPD-Link III traces closely together so that the impedance discontinuity appears as tightly grouped as possible.
2. If PoC is used, place a ferrite bead placed as close as possible to the FPD-Link III trace to minimize the stub seen due to the filter network.
3. The high-speed FPD-Link III traces are routed differentially up to the connector. For the layout of a coaxial interconnects, use coupled traces with the RINx– termination near to the connector.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *DS90UB913A-CXEVM & DS90UB914A-CXEVM REV A User's Guide*
- *I2C over DS90UB913/4 FPD-Link III with Bidirectional Control Channel*
- *Sending Power Over Coax in DS90UB913A Designs*
- *I2C Communication Over FPD-Link III with Bidirectional Control Channel*
- *Soldering Specifications Application Report*
- *Semiconductor and IC Package Thermal Metrics Application Report*
- *Leadless Leadframe Package (LLP) Application Report*
- *LVDS Owner's Manual*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90UB934TRGZRQ1	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	UB934Q	Samples
DS90UB934TRGZTQ1	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	UB934Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

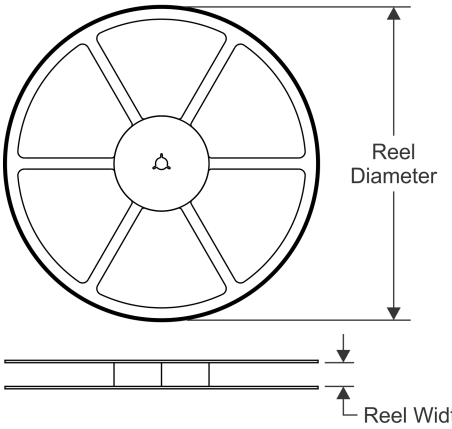
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

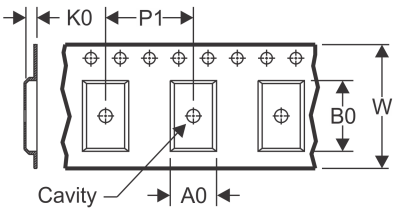
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

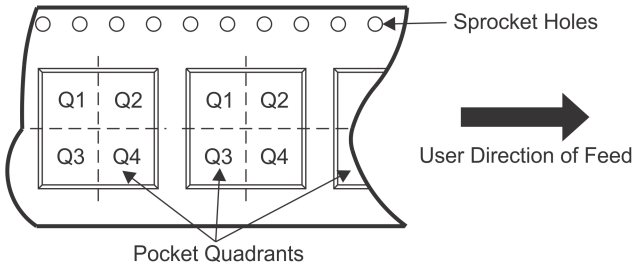


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

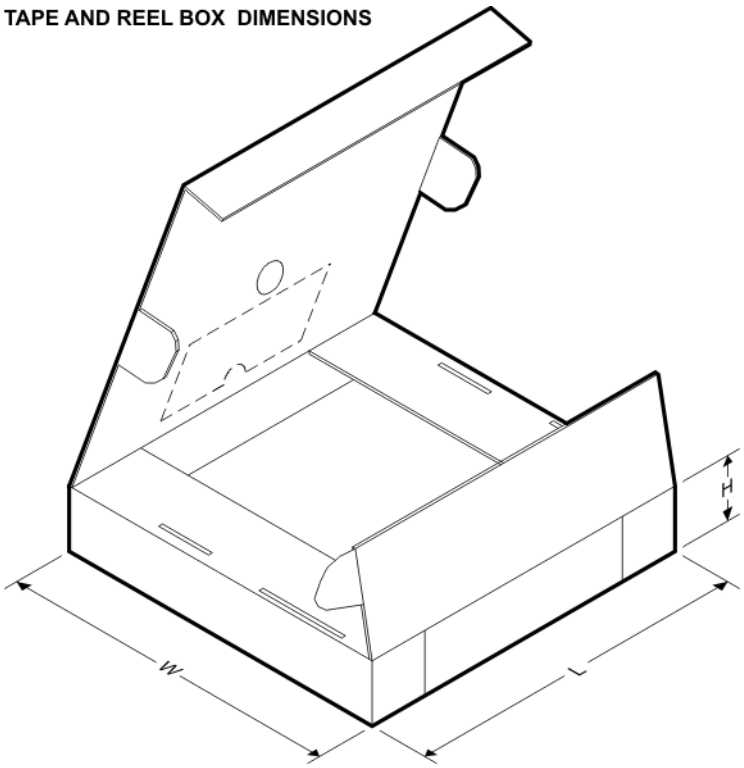
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UB934TRGZRQ1	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
DS90UB934TRGZTQ1	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

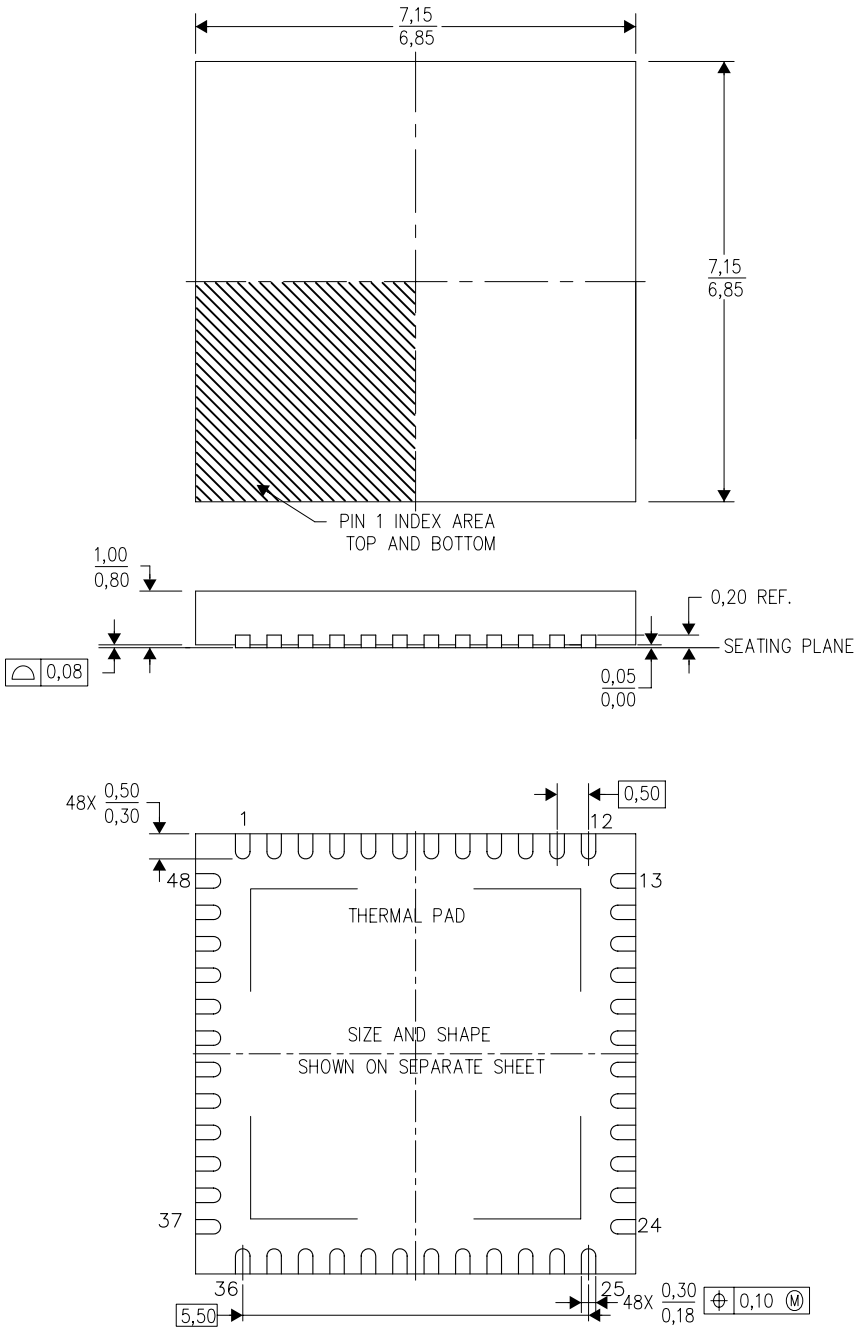
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UB934TRGZRQ1	VQFN	RGZ	48	2500	367.0	367.0	38.0
DS90UB934TRGZTQ1	VQFN	RGZ	48	250	210.0	185.0	35.0

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

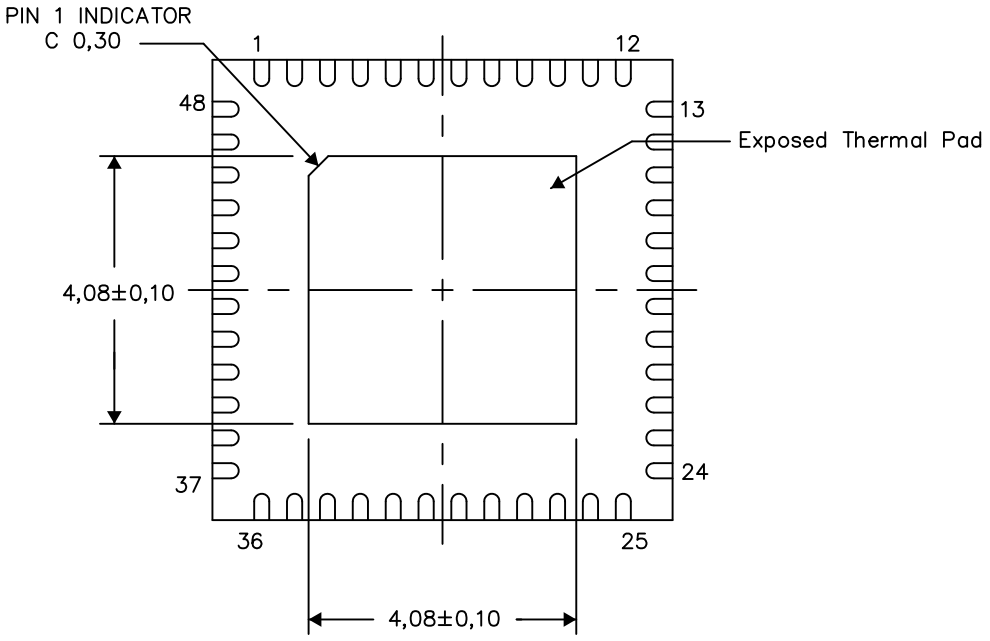
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206354–8/Z 03/15

NOTE: All linear dimensions are in millimeters

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